Advanced Computer Architecture (COMSM0109)

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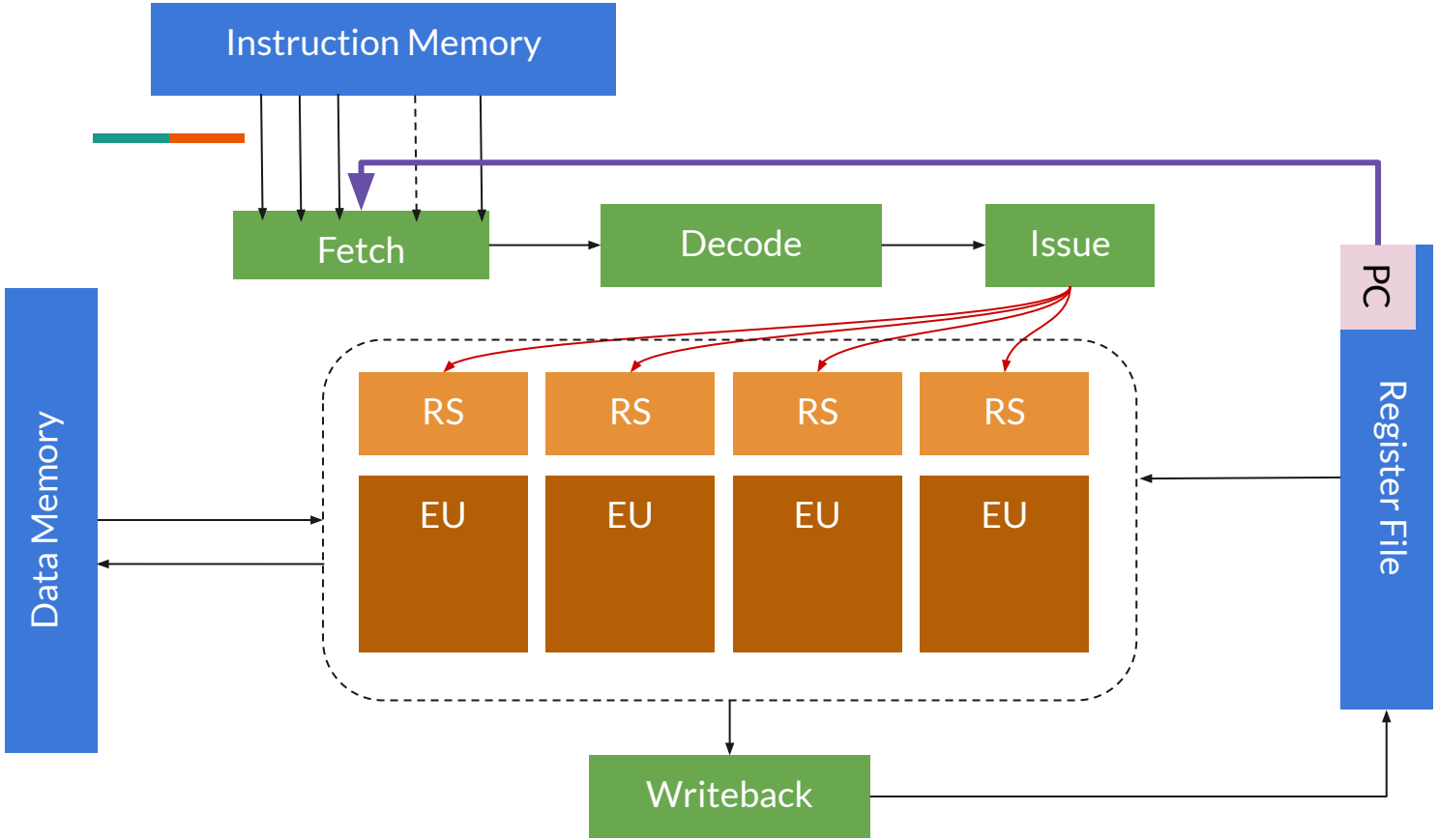
Instruction Memory
Fetch
Decode
Issue
PC
Register File
Data Memory
RS
RS
RS
RS
EU
EU
EU
EU
Writeback

Features

- Pipelined 5 stages (Fetch, Decode, Issue, Execute, Writeback)
- 4 - way super-scalar with 2-way issue
- Out of order without re-order buffer
- MIPS style inspired instructions
- Arithmetic(add, sub, mul, mov ,divd,)
- Branch (bgt, blt, beq, j, br)
- Memory (ld, sto)
- Out of order without re-order buffer

Super-scaler increases instructions per cycle

Vector addition (5 elements)		
Configuration	Clock Cycles	Useful Instructions Executed
Pipelined	44	28
Super Scalar	41	40

Hypothesis: Super Scaler processor will increase the number of instructions per cycle

Result:
The instructions per cycle has increased but also the the instructions have increased, this is due the processor re executing instructions that it has run previously.

Super Scalar Performance

Fibonacci (Up to 5000)		
Configuration	Clock Cycles	Useful Instructions Executed
Pipelined	174	116
Super Scalar	116	116

Hypothesis: Super Scalar processor will increase the number of instructions per cycle

Result:
For this example the Fibonacci instruction was greatly improved by the super scalar performance.
From 0.667 instructions per cycle to 1 instruction per cycle.