CPE201
Digital Design

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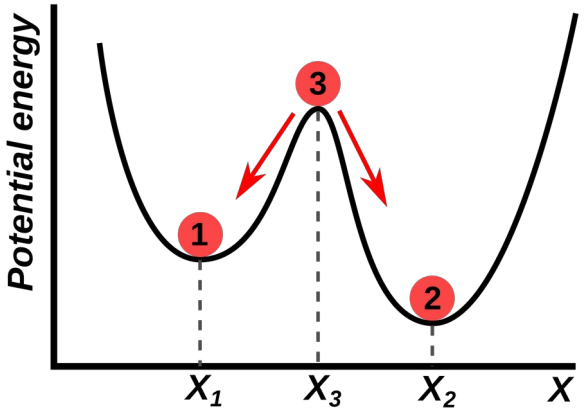
Class 17: Latches and Troubleshooting 2

University of Nevada, Reno

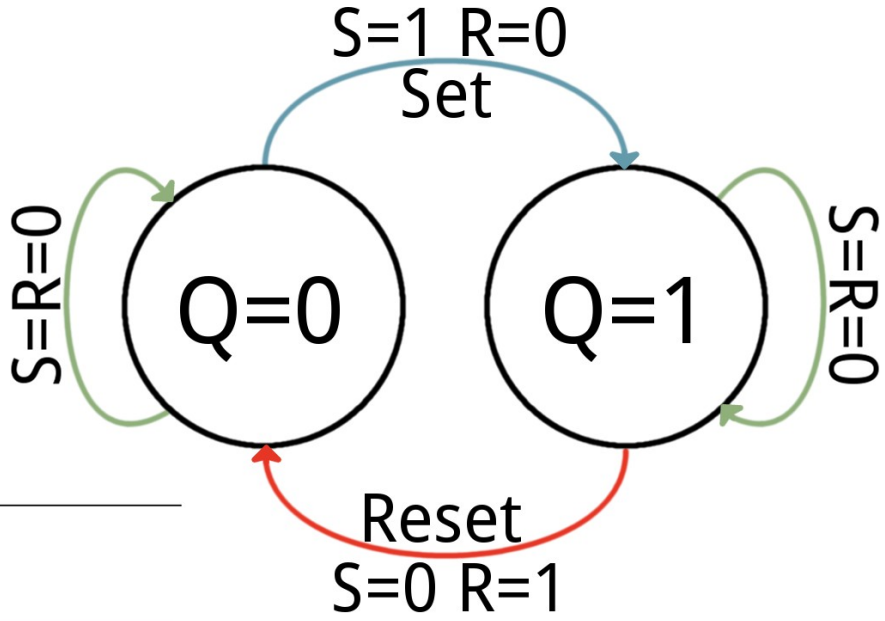
Latches

- Stores a state
  - Memory (1-bit)!
- Bistable Multivibrator
  - 2 stable states
- Feedback



SR (Set-Reset) Latch

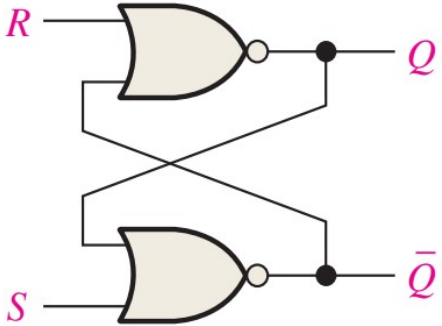
- State machine
- S = Set
- R = Reset
- Q = Output



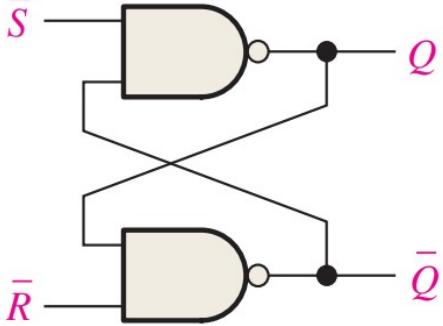
Truth table for an active-LOW input $\overline{S}$-$\overline{R}$ latch.

Inputs		Outputs		
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

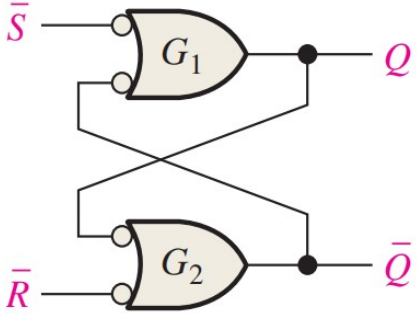
SR Latch



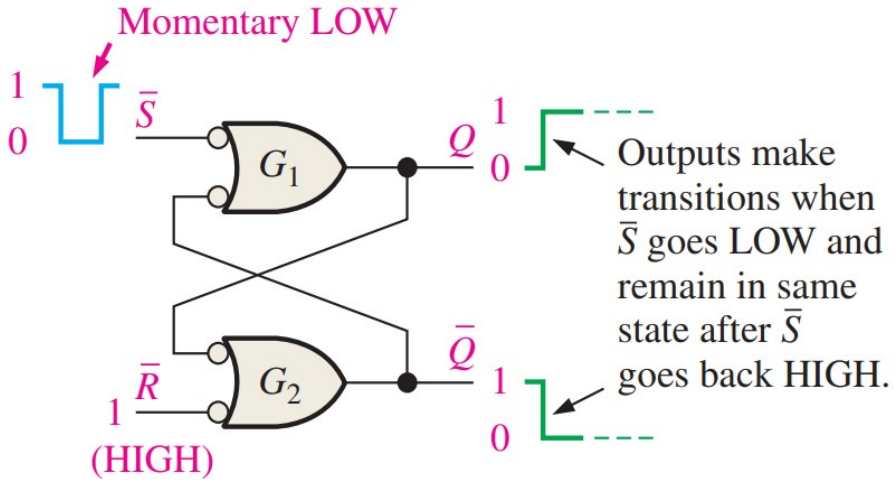
Active-HIGH input S-R latch



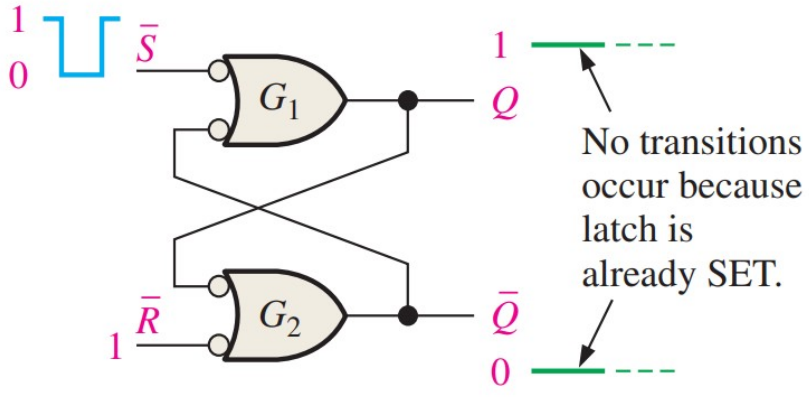
Active-LOW input $\bar{S}$-$\bar{R}$ latch



Set



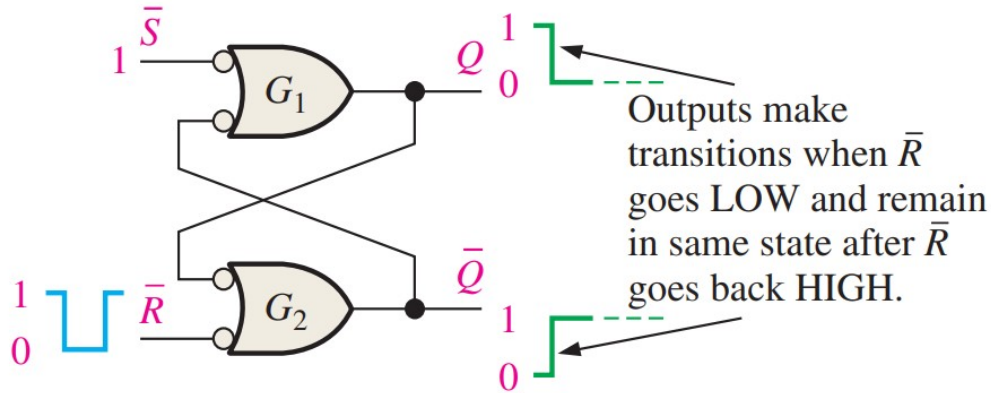
Latch starts out RESET ($Q = 0$).



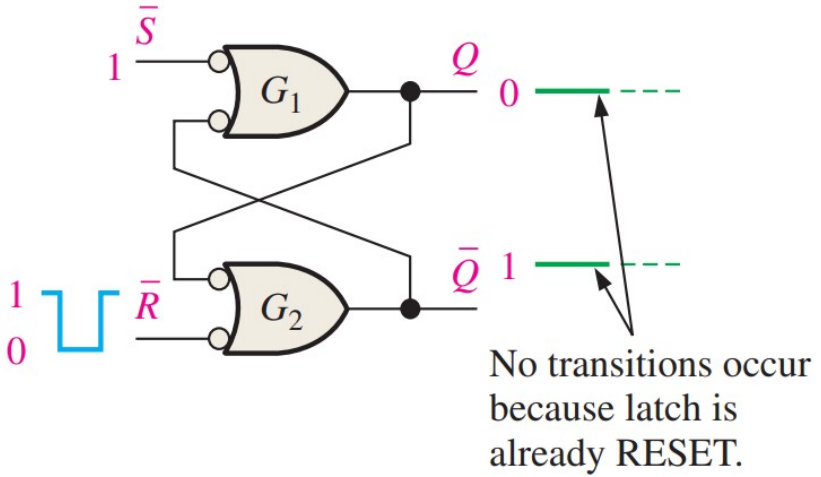
Latch starts out SET ($Q = 1$).

Two possibilities for the SET operation

Reset



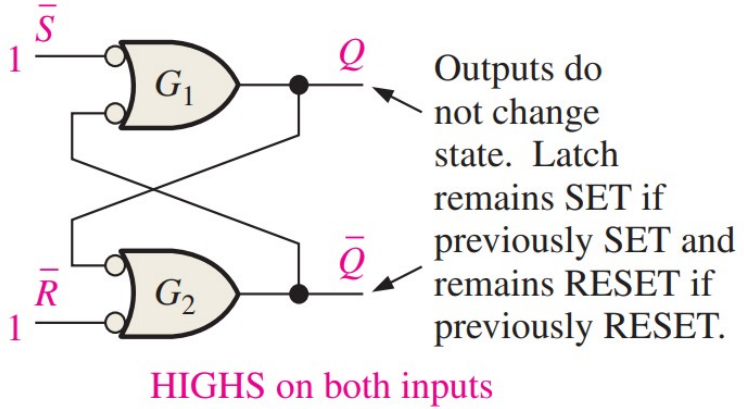
Latch starts out SET ($Q = 1$).



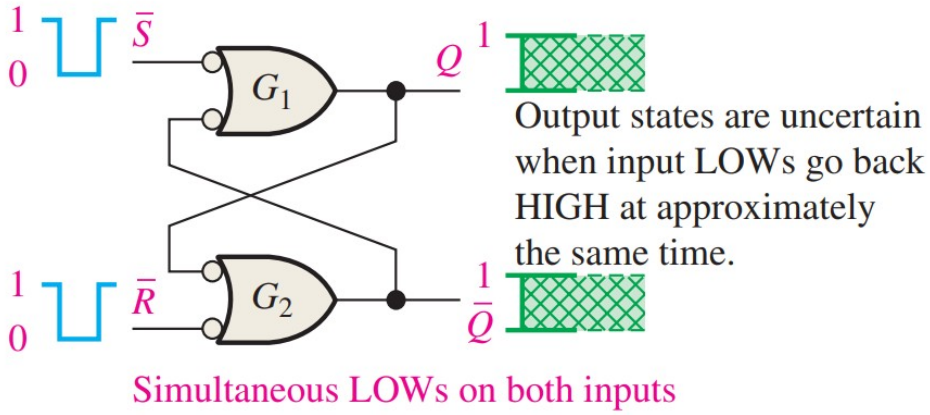
Latch starts out RESET ($Q = 0$).

Two possibilities for the RESET operation

No Change & Invalid

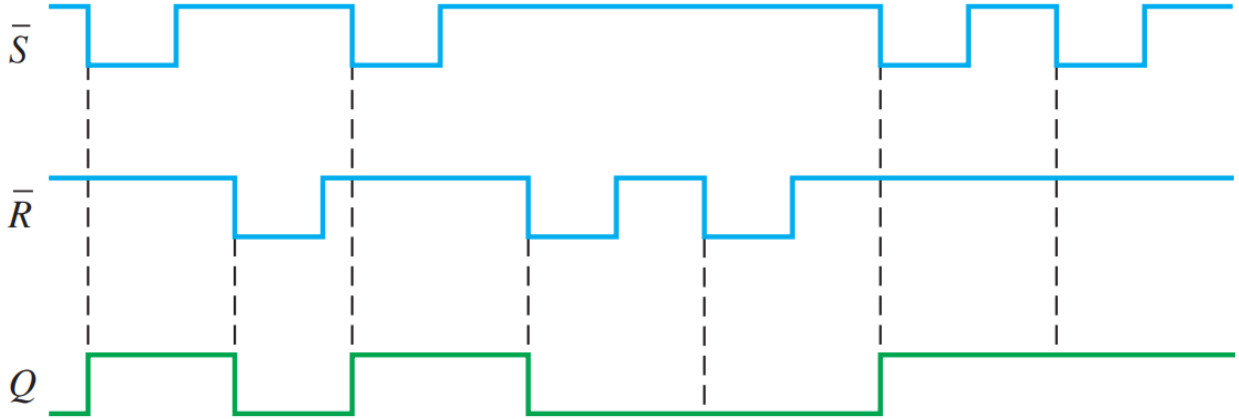


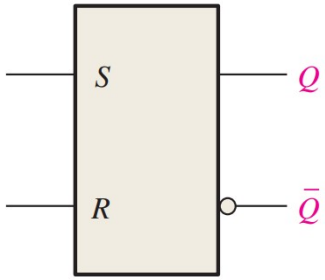
No-change condition



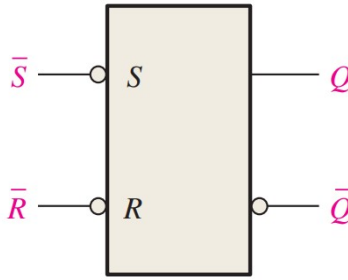
Invalid condition

Symbol & Example





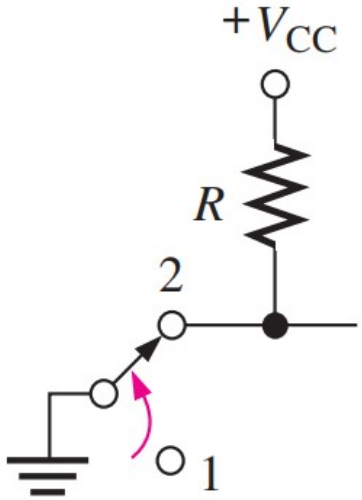
(a) Active-HIGH input S-R latch

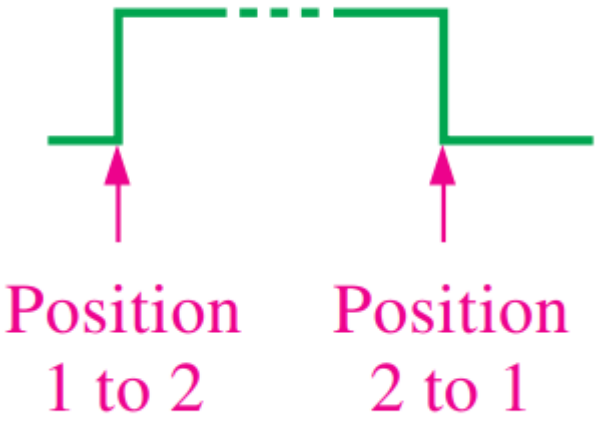


(b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

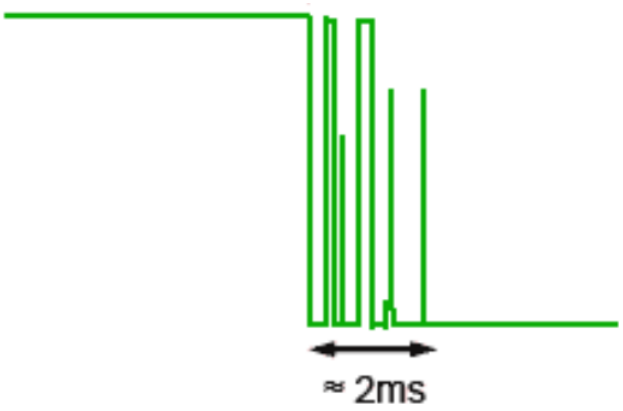
Logic symbols for the S-R and $\overline{S}$-$\overline{R}$ latch.

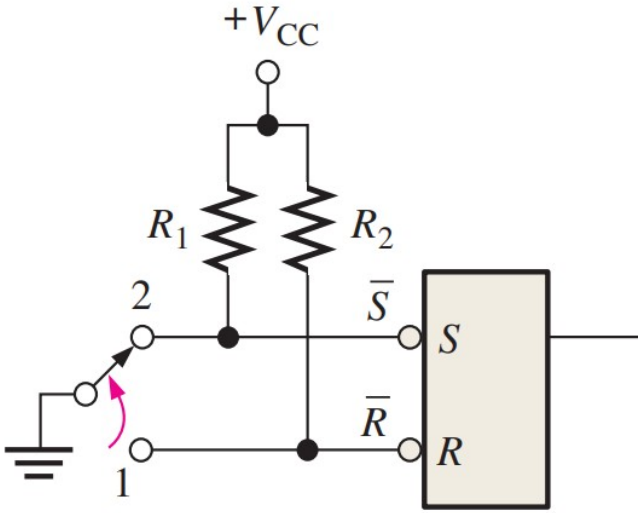
Debouncing Switches

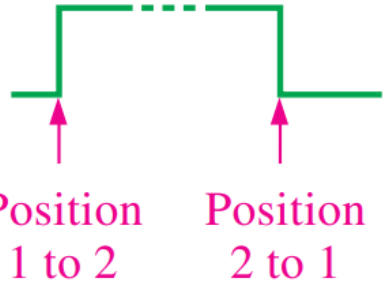




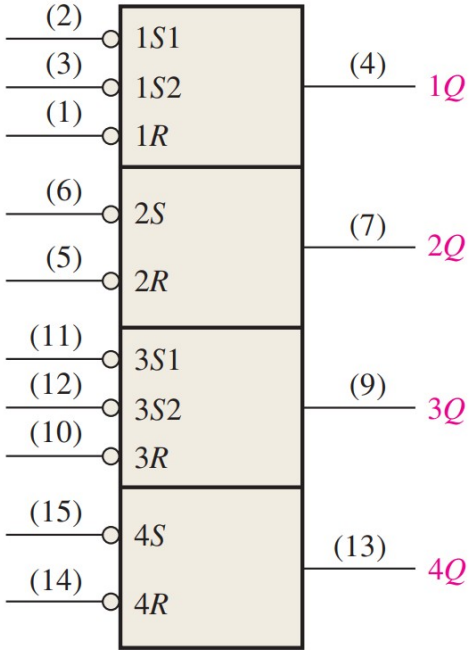
Debouncing Switches

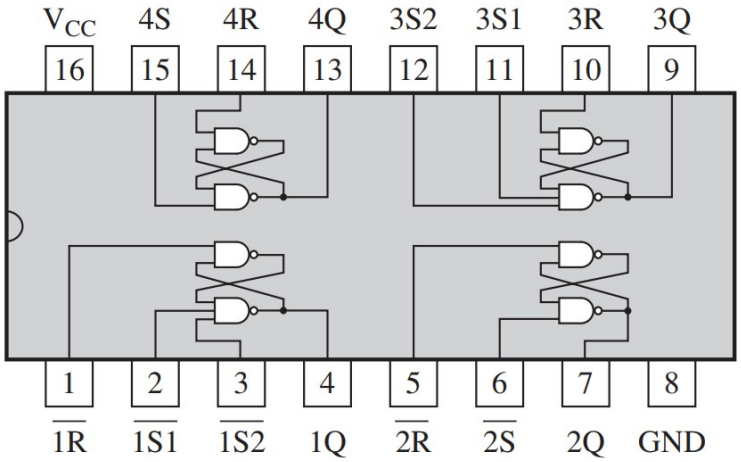






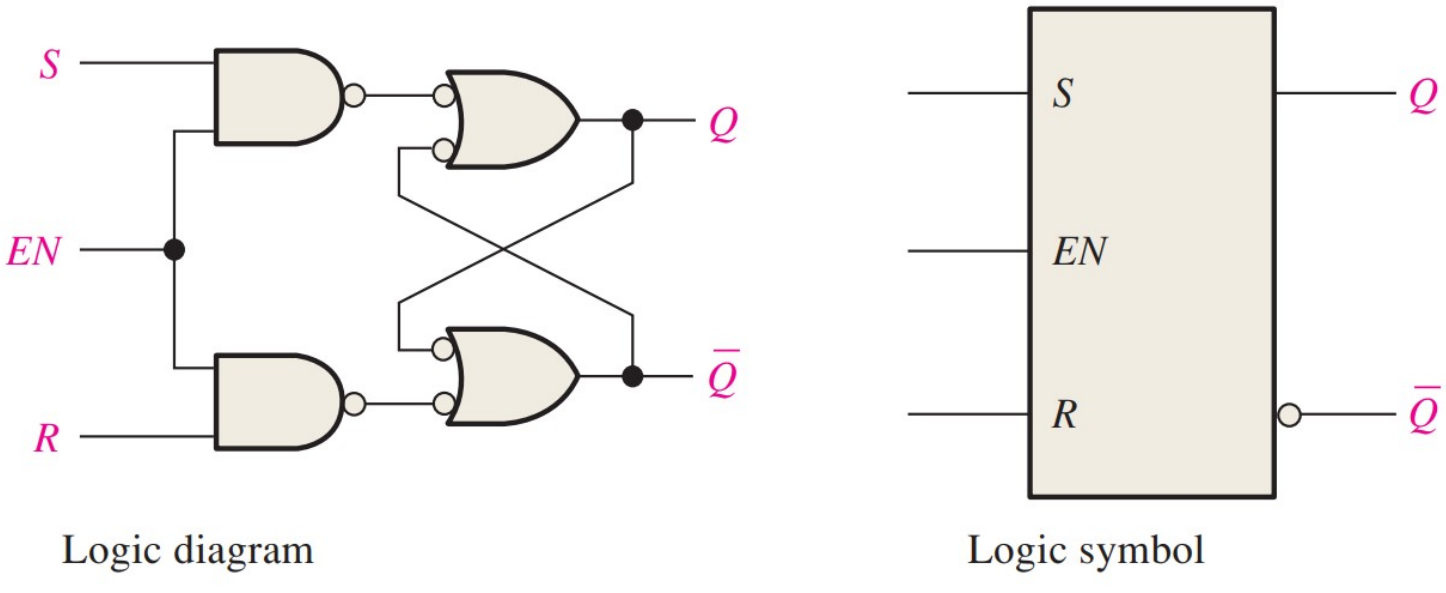
Real Chip – 74HC279A





Gated SR Latch

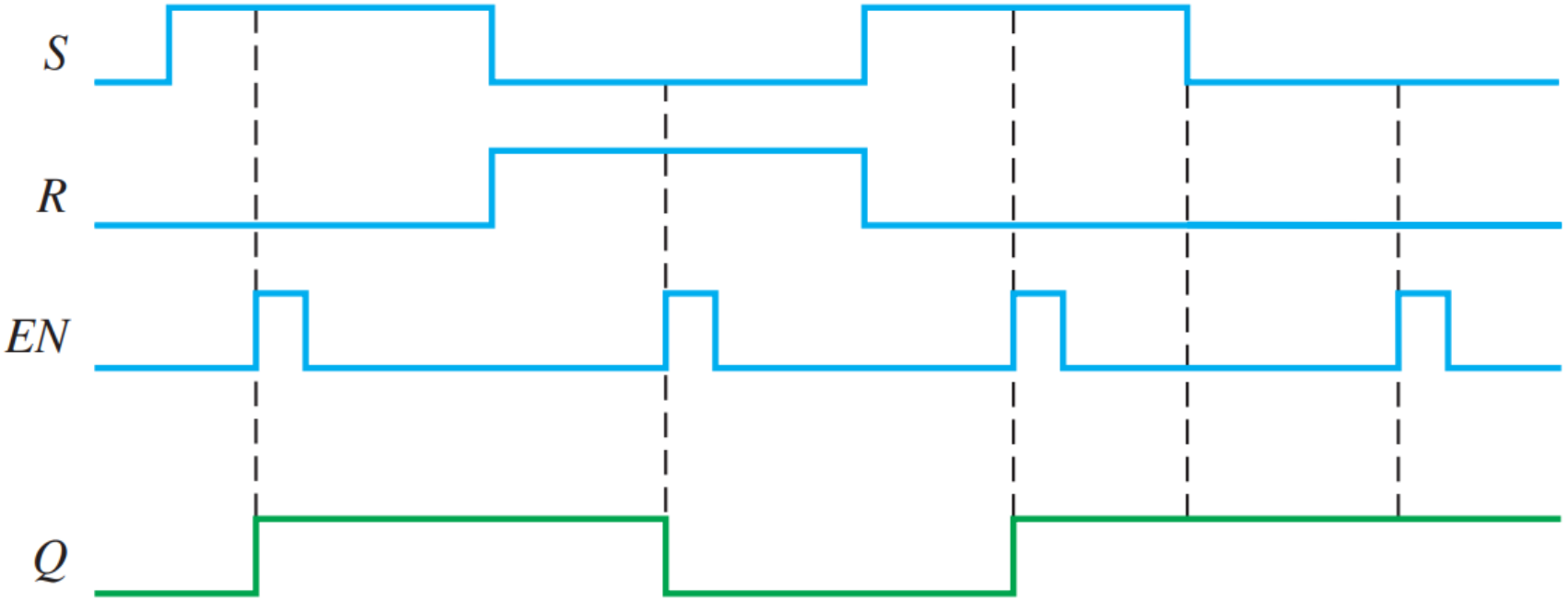
- Now with Enable!



Logic diagram

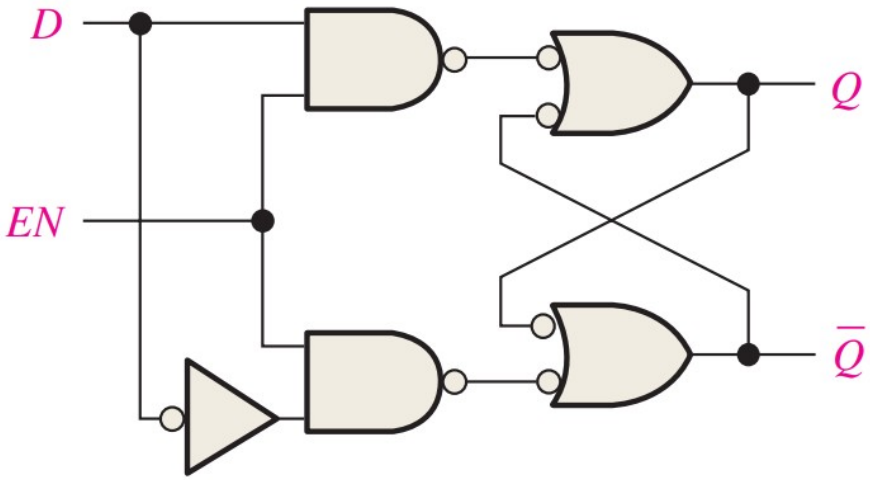
Logic symbol

Example

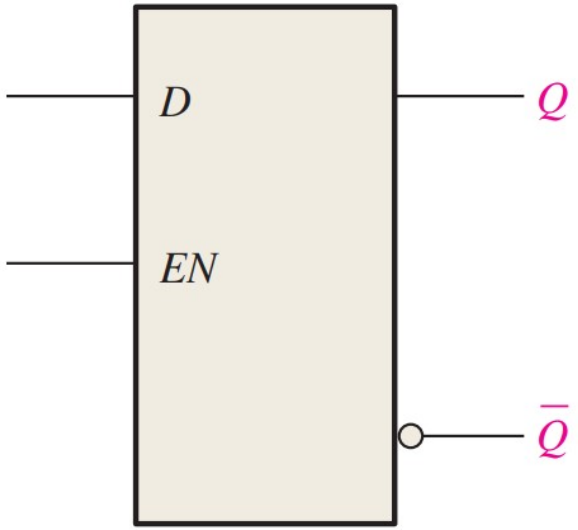


D Latch

- Data Latch – saves D state when Enable

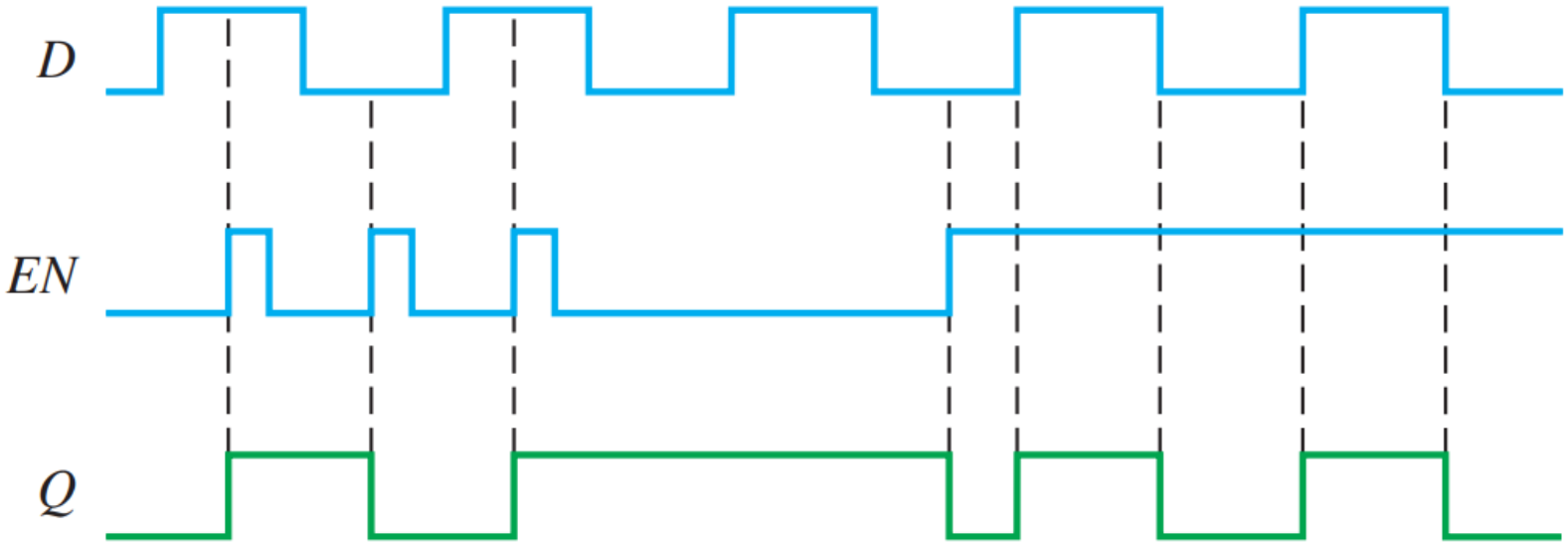


Logic diagram



Logic symbol

Example

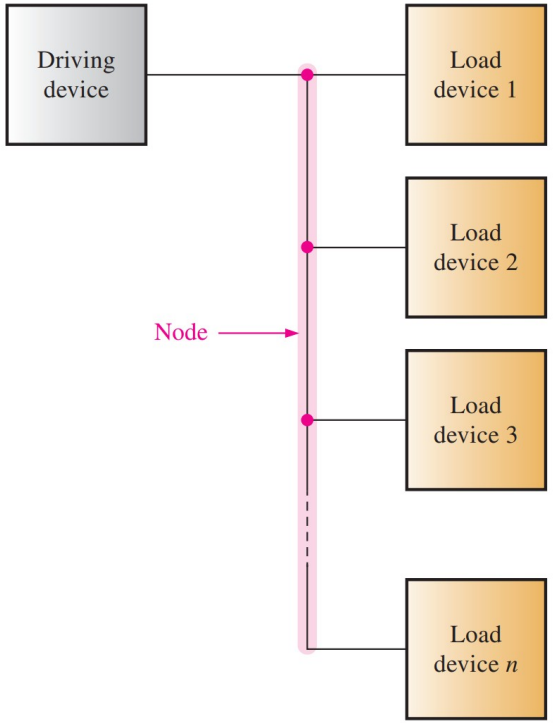


A Node

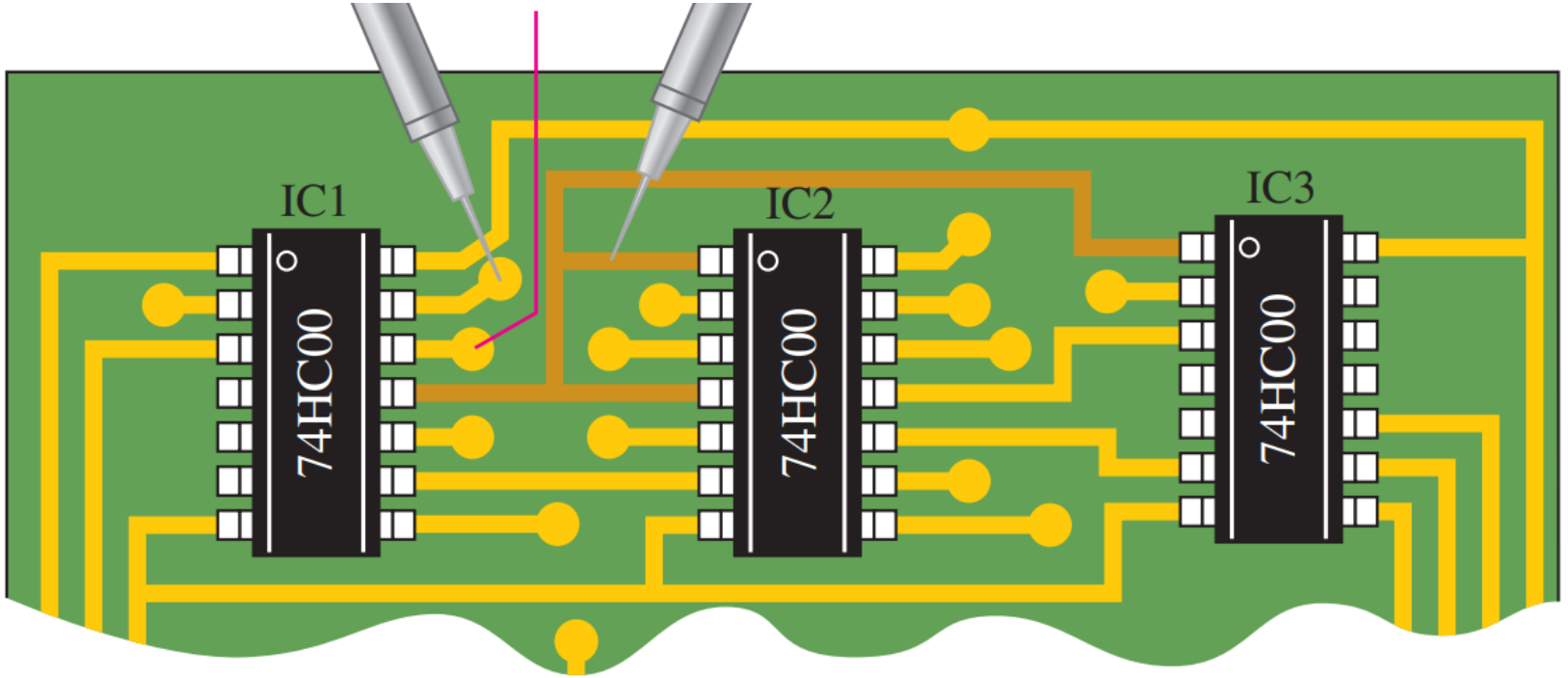
- Electrically the same

on all points of the wire

- Shorts vs Opens



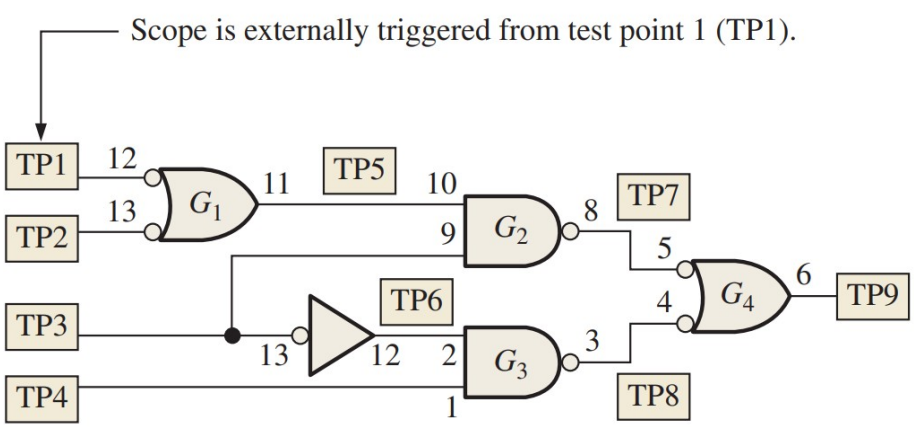
Checking Interconnects

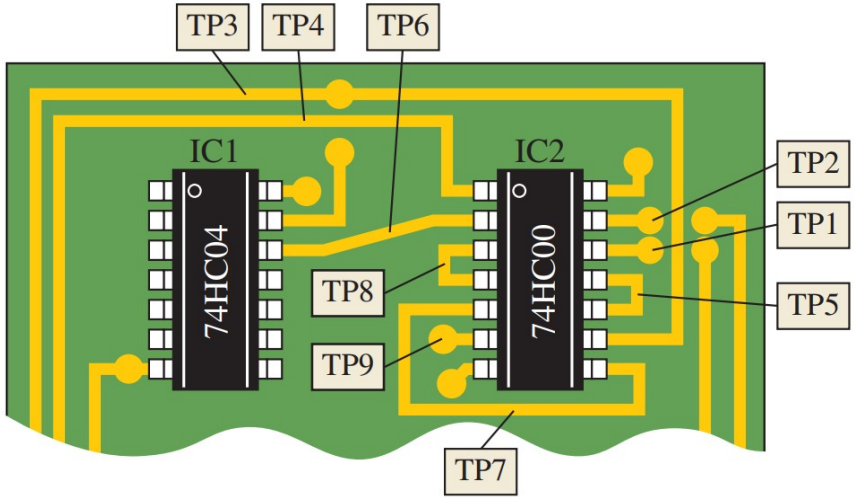


Other Checks

- Power
- Ground
- Inputs
- Outputs
- Wires?

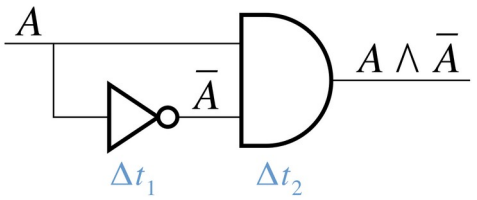
Signal Tracing

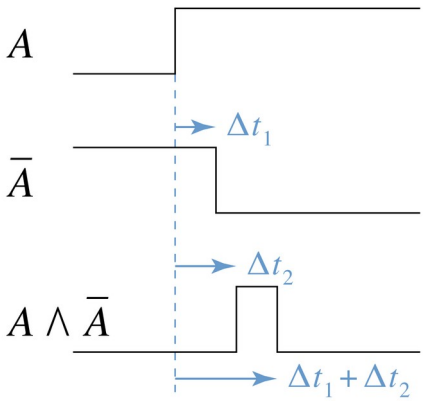




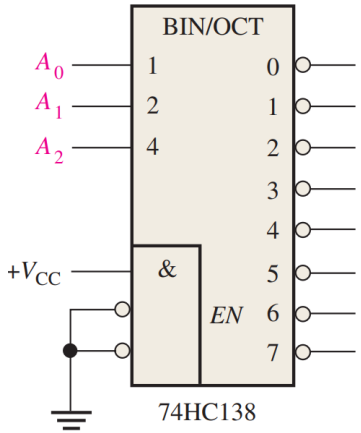
Glitches

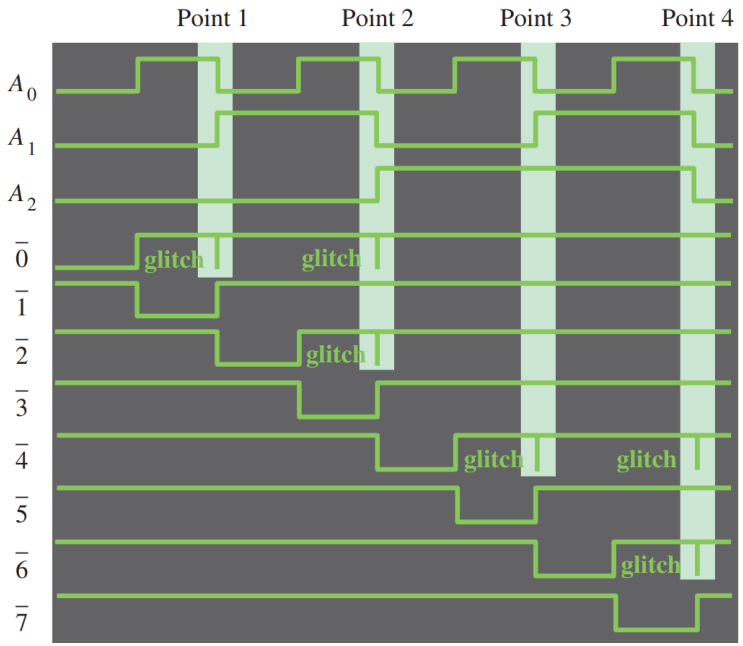
- Any undesired short duration voltage or current spike
- Also called a race conditio
- Most common at signal changes



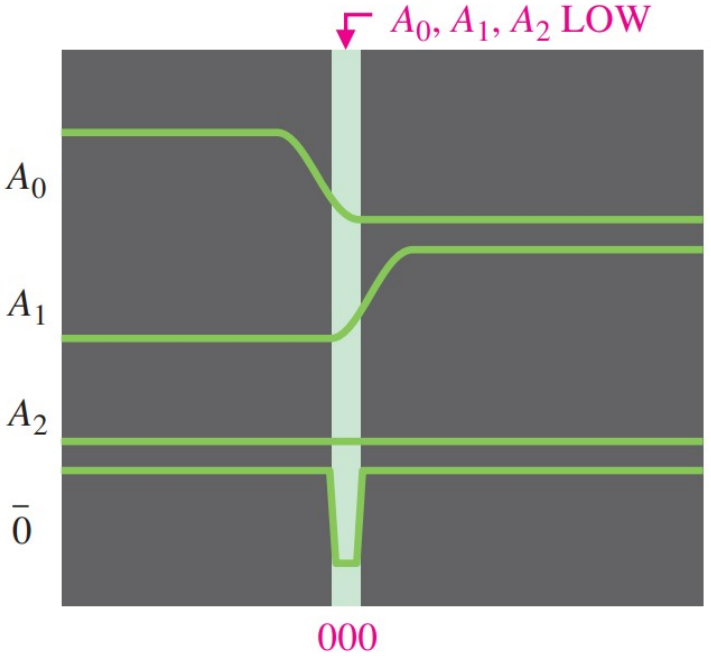


Example



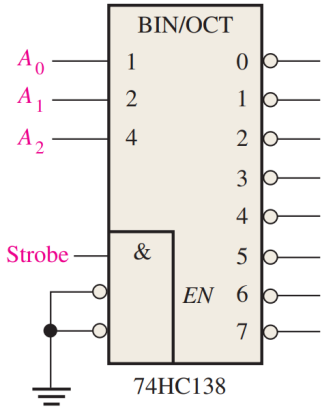


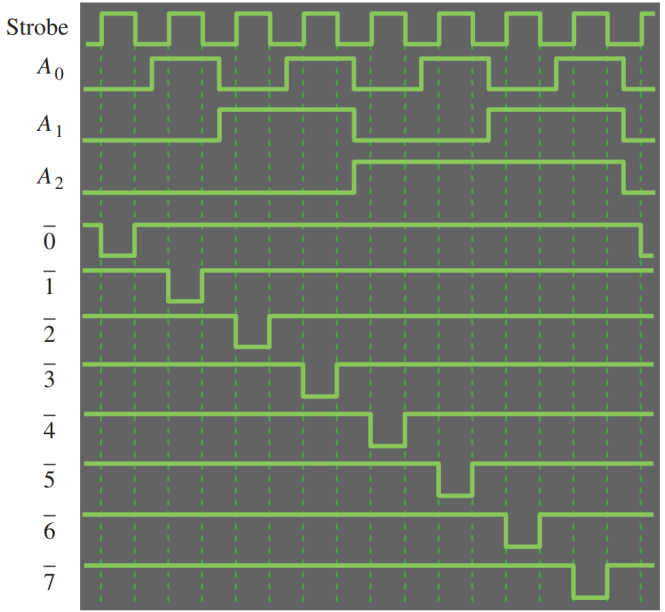
Point 1: waveforms on expanded time base



Strobing

- Use the Enabl





Reading

- This lecture
  - Sections 5.7, 6.11, 7.1
- Next lecture
  - Sections 7.2-7.4