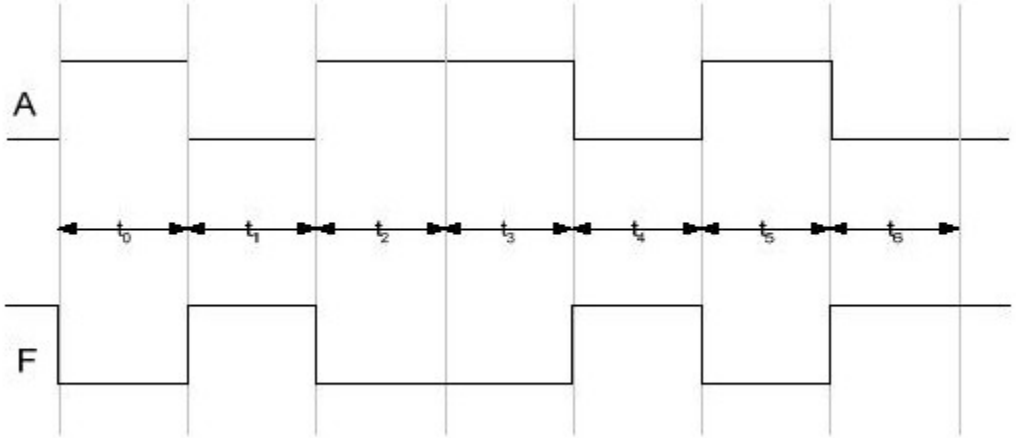
CPE201
Digital Design

By Benjamin Haas

Class 6: More Gates, Timing, and Chips

University of Nevada, Reno

NOT Timing



Truth tables:

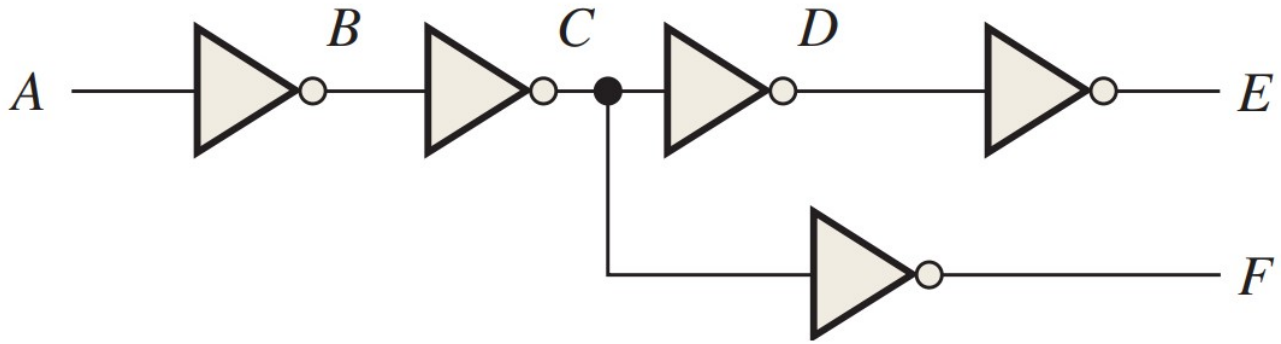
a	b	AND
0	0	0
0	1	0
1	0	0
1	1	1

a	b	OR
0	0	0
0	1	1
1	0	1
1	1	1

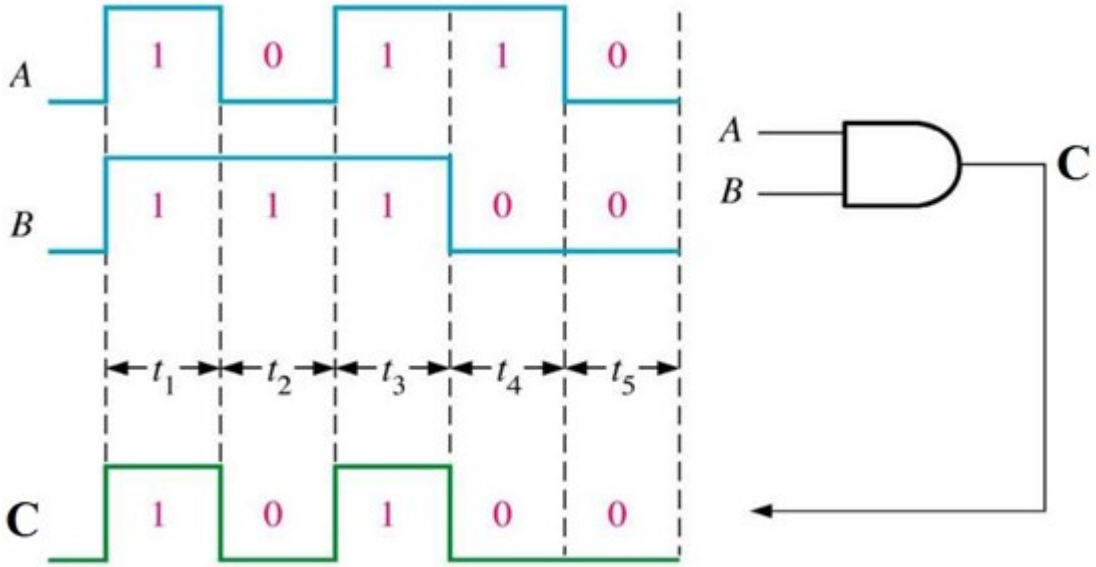
a	NOT
0	1
1	0

Example

- If C = 1, what is the value at the other points?



AND Timing



Truth tables:

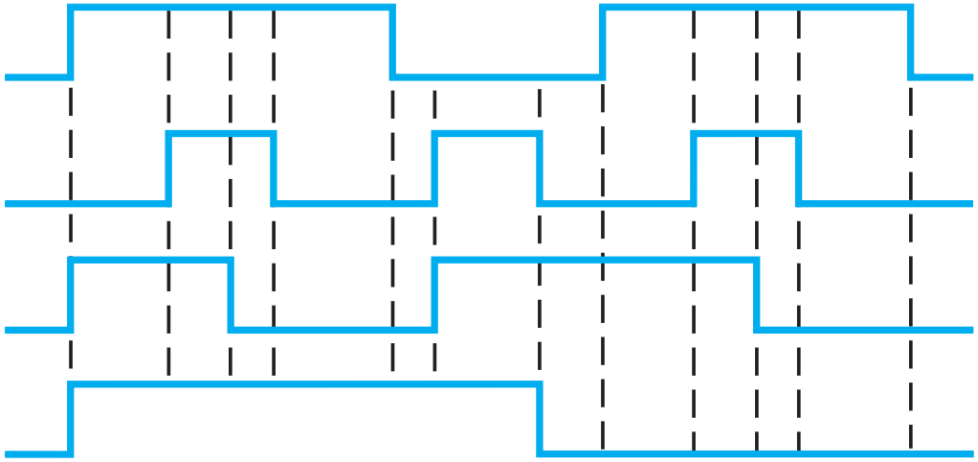
a	b	AND
0	0	0
0	1	0
1	0	0
1	1	1

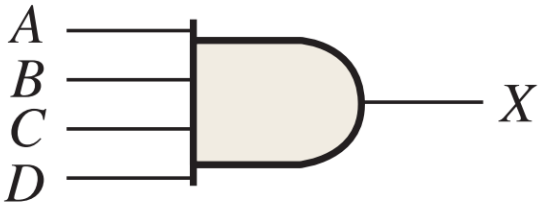
a	b	OR
0	0	0
0	1	1
1	0	1
1	1	1

a	NOT
0	1
1	0

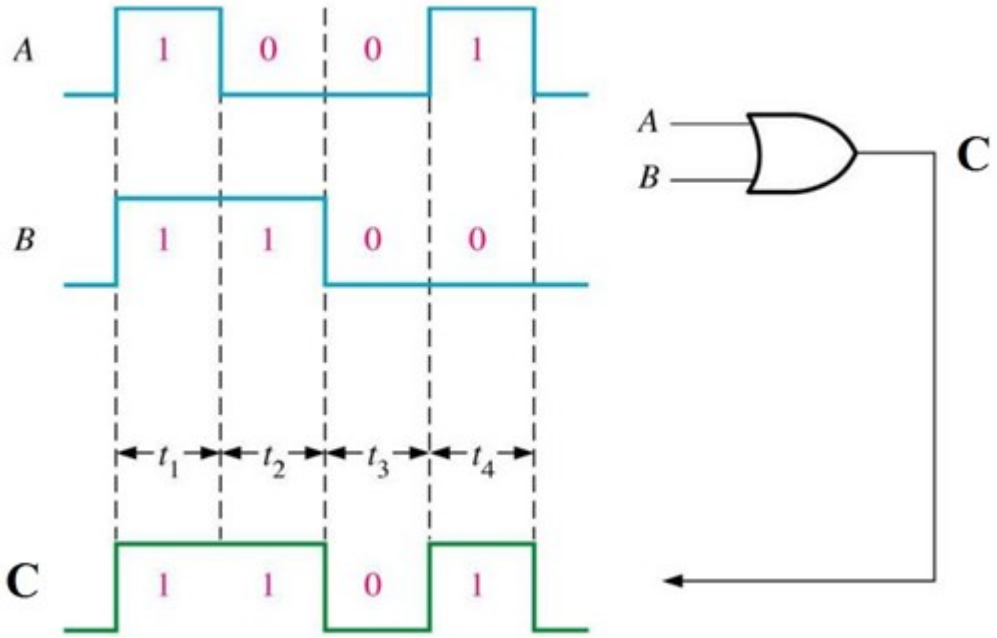
Example

- Draw the output waveform.





OR Timing



Truth tables:

a	b	AND
0	0	0
0	1	0
1	0	0
1	1	1

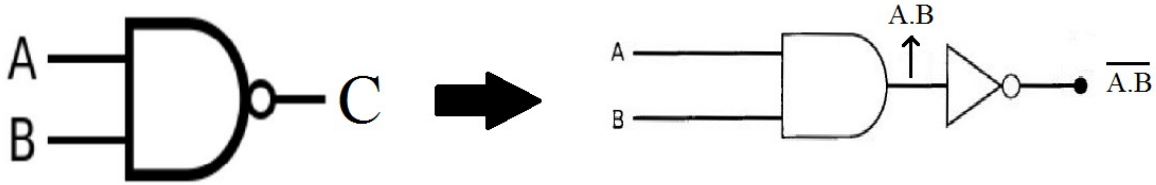
a	b	OR
0	0	0
0	1	1
1	0	1
1	1	1

a	NOT
0	1
1	0

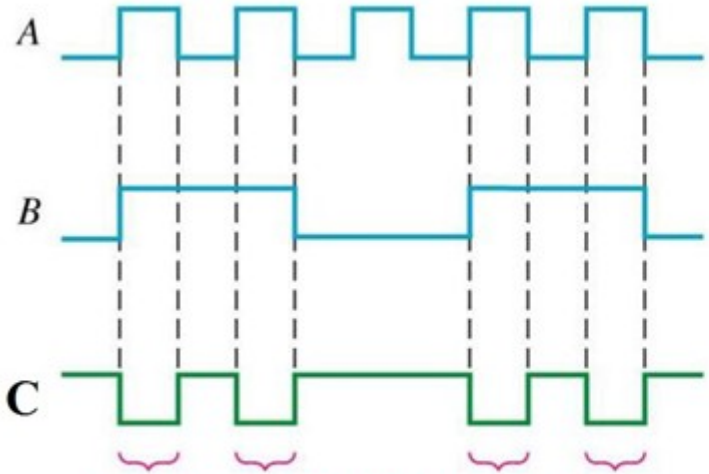
NAND Gates

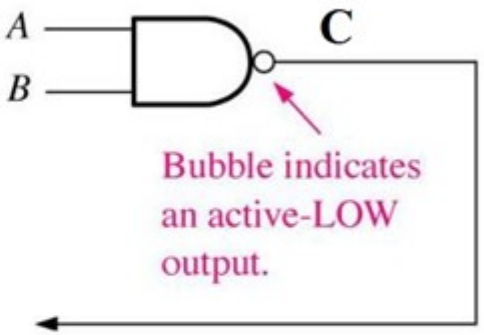
- NAND = NOT AND
- AND with inverted output
- C = $\overline{AB}$ = (AB)’

A	B	A **NAND** B
0	0	1
0	1	1
1	0	1
1	1	0



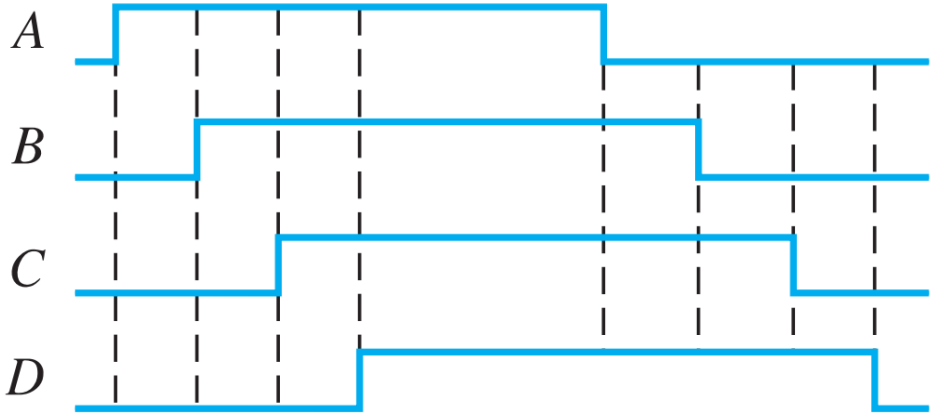
NAND Timing

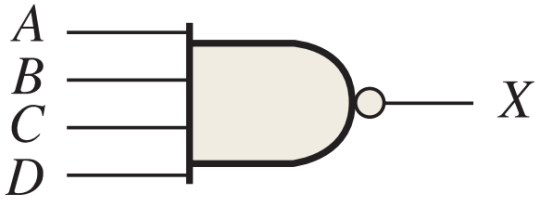

A
B
C
A and B are both HIGH during these four time intervals. Therefore X is LOW.


A
B
C
Bubble indicates an active-LOW output.

Example

- Draw the output waveform.



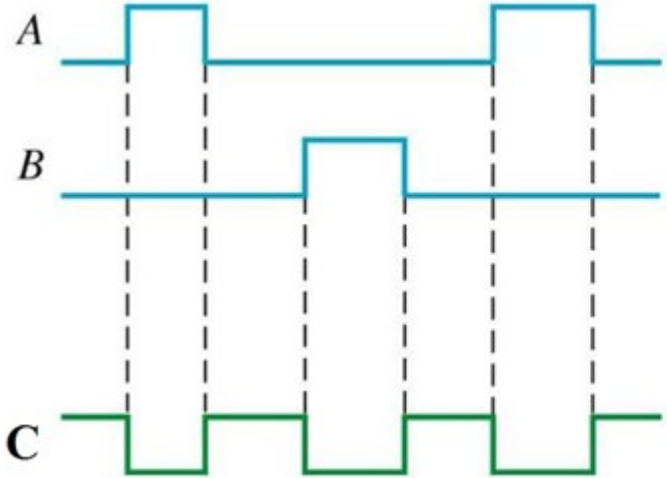


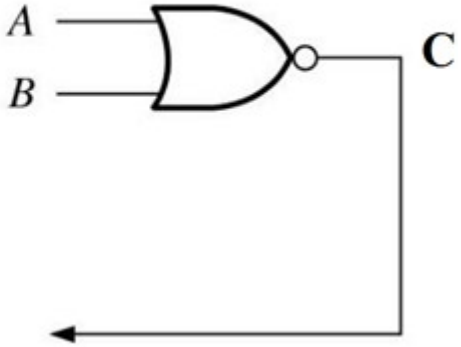
NOR Gates

- NOR NOT OR
- OR with inverted output
- $C = \overline{A+B} = (A+B)'$

A	B	A **NOR** B
0	0	1
0	1	0
1	0	0
1	1	0

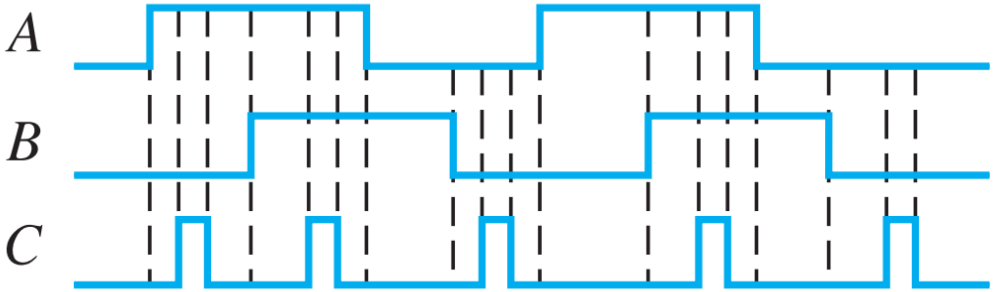
NOR Timing

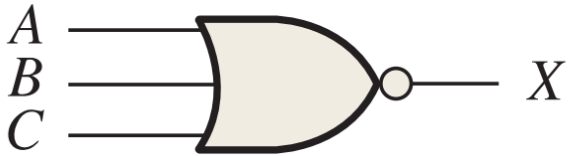




Example

- Draw the output waveform

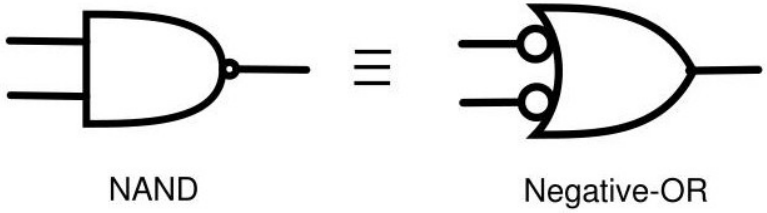


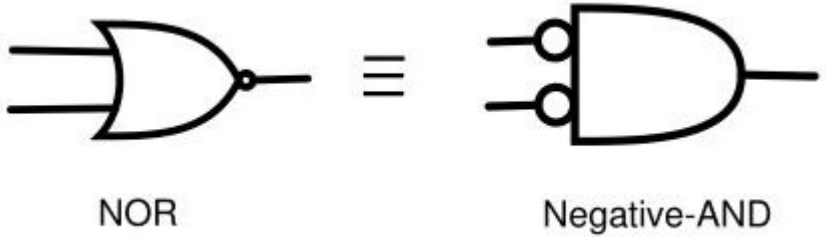


Why NAND and NOR?

- Universal gates (to be discussed later)
  - Any of the other gates (and more) can be built from NAND, NOR, and NOT
- Smaller sized implementations
- Faster logic

NAND and NOR Equivalents





A	B	A **NAND** B
0	0	1
0	1	1
1	0	1
1	1	0

A	B	A **NOR** B
0	0	1
0	1	0
1	0	0
1	1	0

- Foreshadowing…

XOR and XNOR

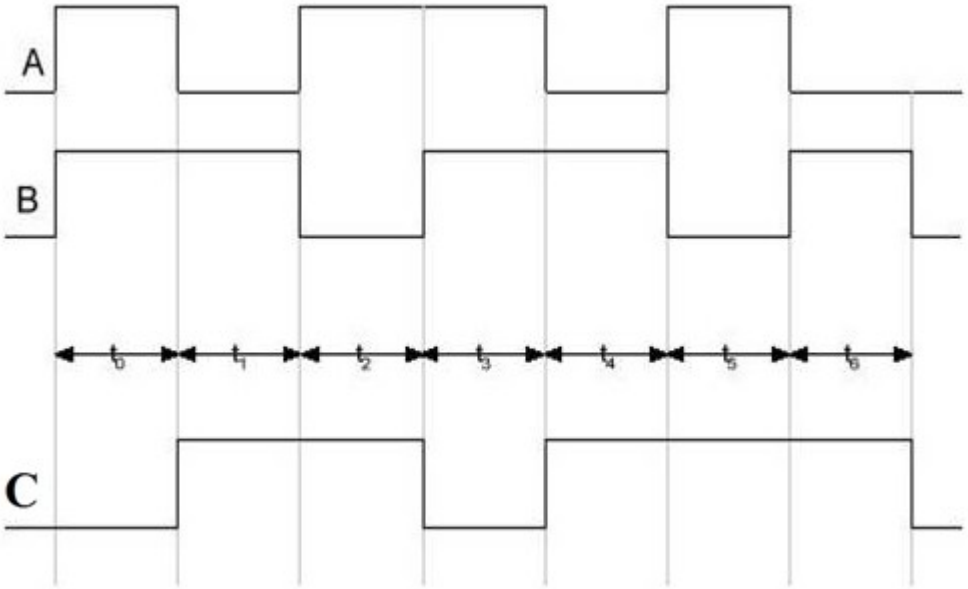
- Exclusive-OR and Exclusive-NOR
  - A combination of the logic already discussed
  - Given their own unique

XOR

- Outputs a 1 when either of the inputs is 1 (exclusively one of the inputs is 1)
- Outputs a 0 otherwise
- C = B
- Example application: addit

A	B	A **XOR** B
0	0	0
0	1	1
1	0	1
1	1	0

XOR Timing

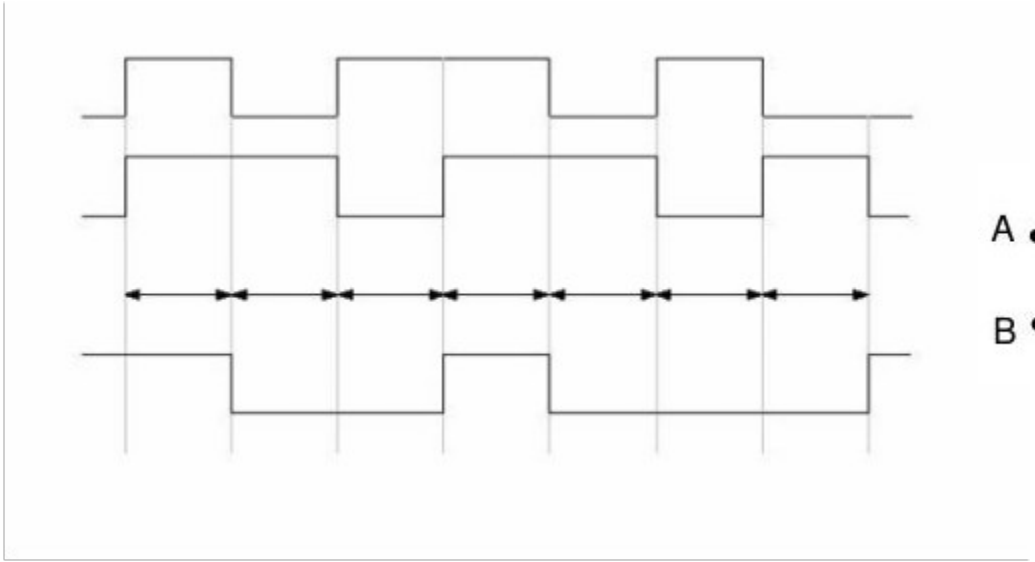


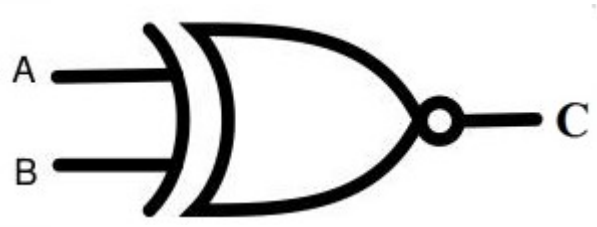
XNOR

- Invert the output of XOR
- $C = \overline{A\ B} = (A\ B)'$

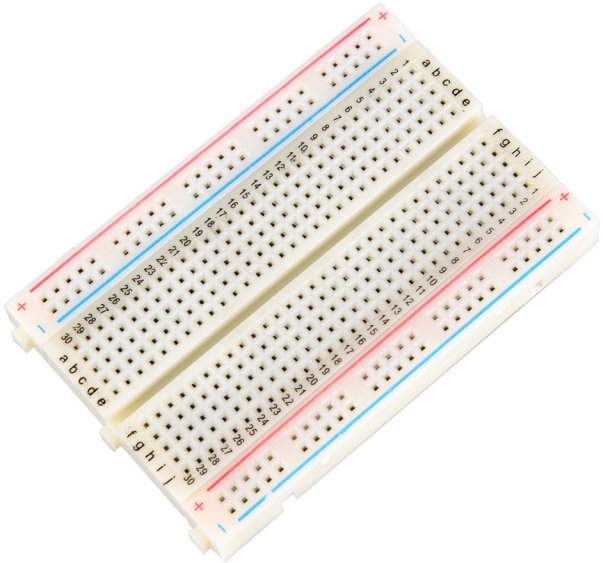
A	B	A **XNOR** B
0	0	1
0	1	0
1	0	0
1	1	1

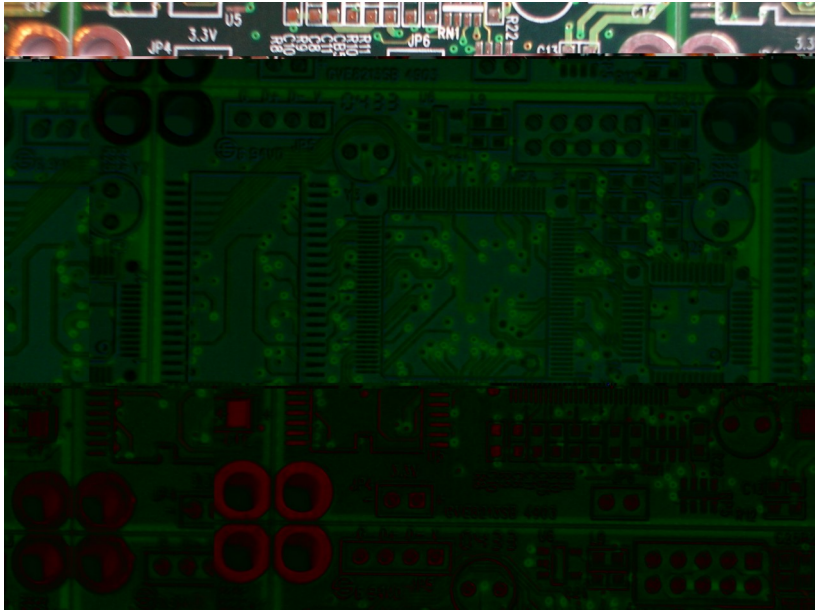
XNOR Timing



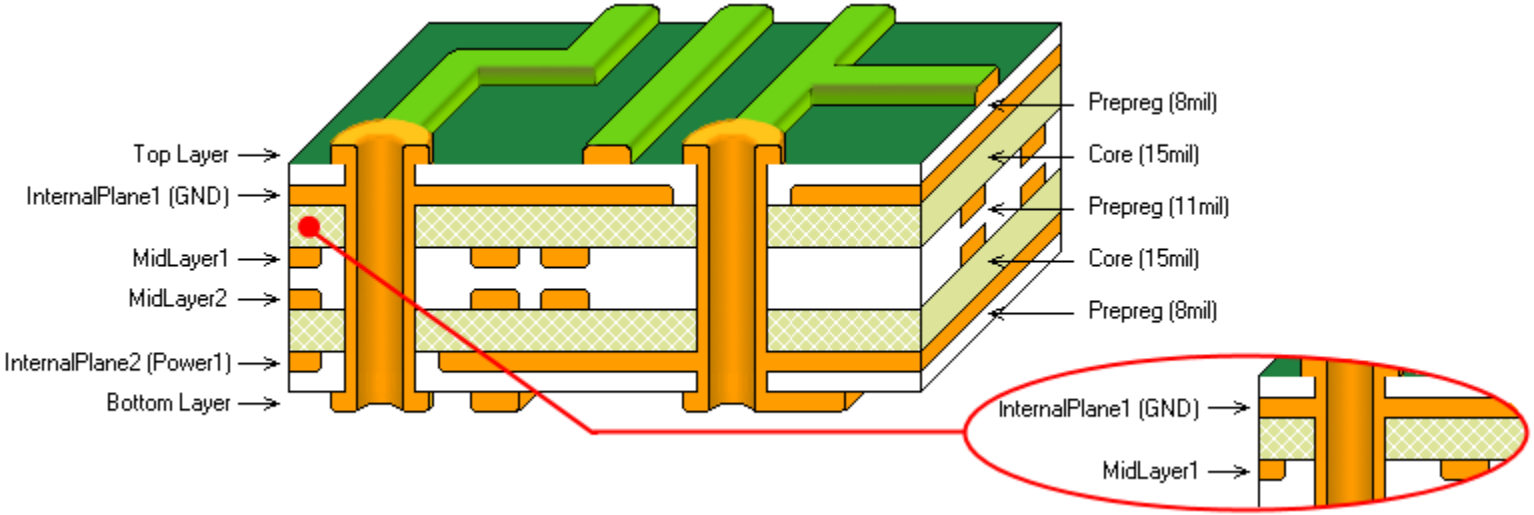


Breadboards vs PCBs

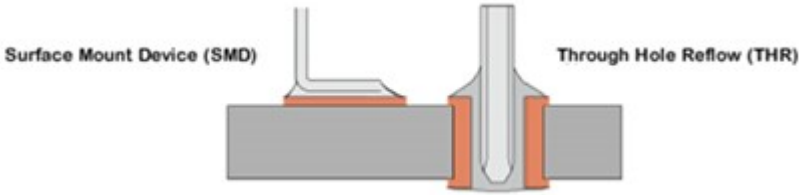


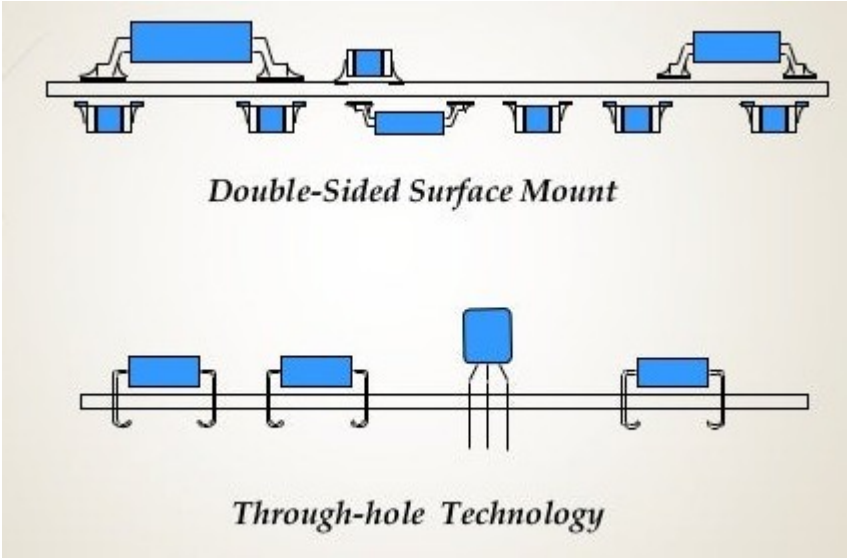


PCBs

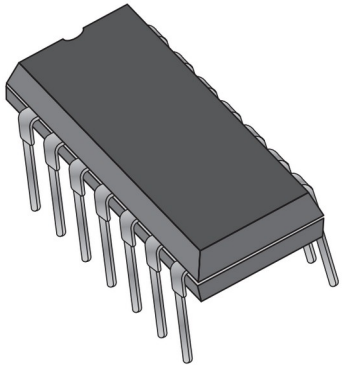

Top Layer
InternalPlane1 (GND)
MidLayer1
MidLayer2
InternalPlane2 (Power1)
Bottom Layer
Prepreg (8mil)
Core (15mil)
Prepreg (11mil)
Core (15mil)
Prepreg (8mil)
InternalPlane1 (GND)
MidLayer1

Through hole vs Surface Mount

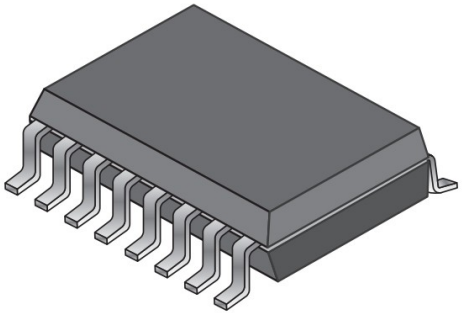




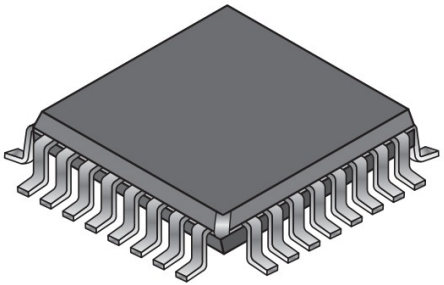
IC Packages



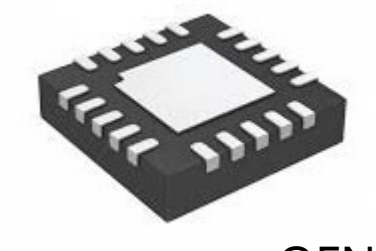
Dual in-line package (DIP)



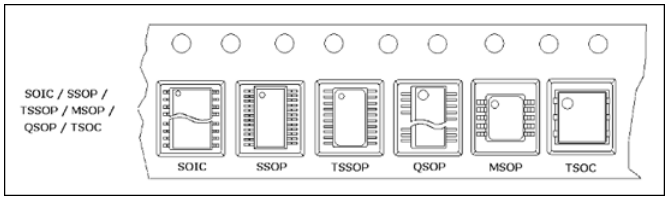
SSOP (153 × 193 mils)

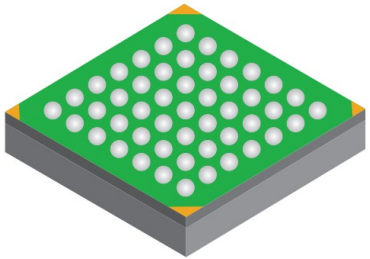


LQFP (7 × 7 mm)



QFN



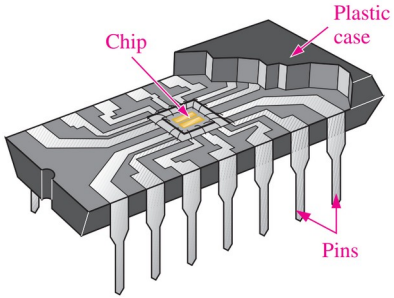


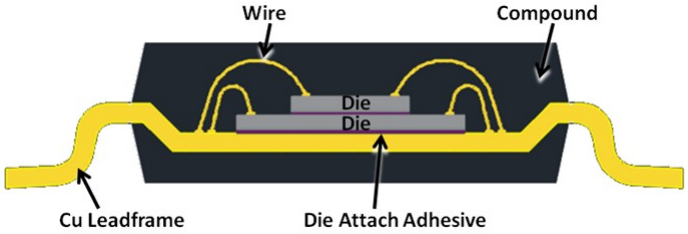
FBGA bottom view
(4 × 4 mm)

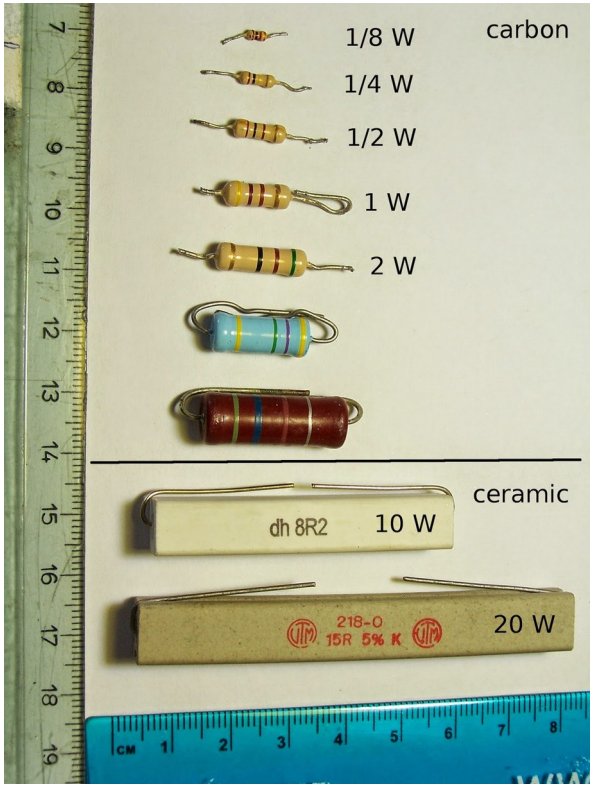
Packages

Metric code	Imperial code
0402	01005
0603	0201
1005	0402
1608	0603
2012	0805
2520	1008
3216	1206
3225	1210
4516	1806
4532	1812
5025	2010
6332	2512

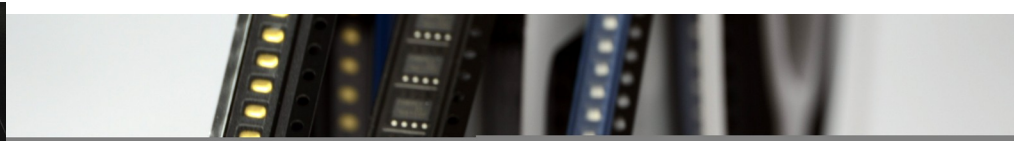
Actual size



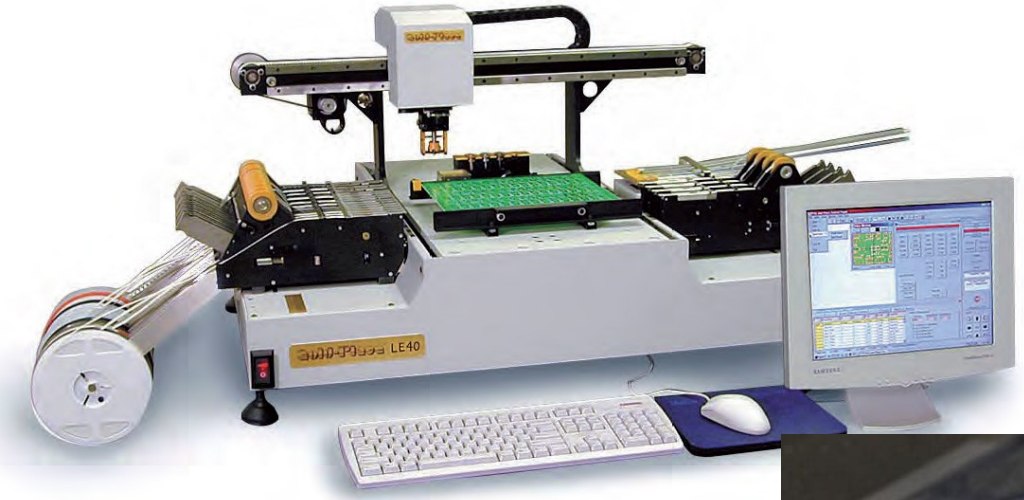




Tape and Reel

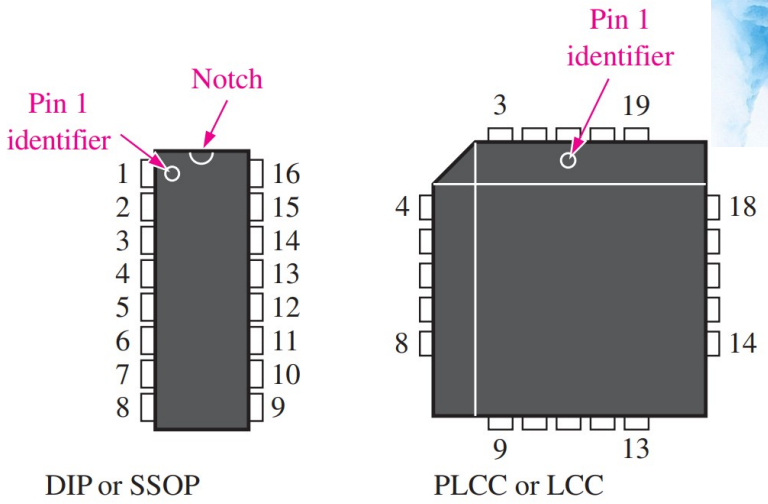


Pick and Place/Wave Solder



Pins

- Check the datasheet!



Example

Figure 5-1. LQFP64 package outline

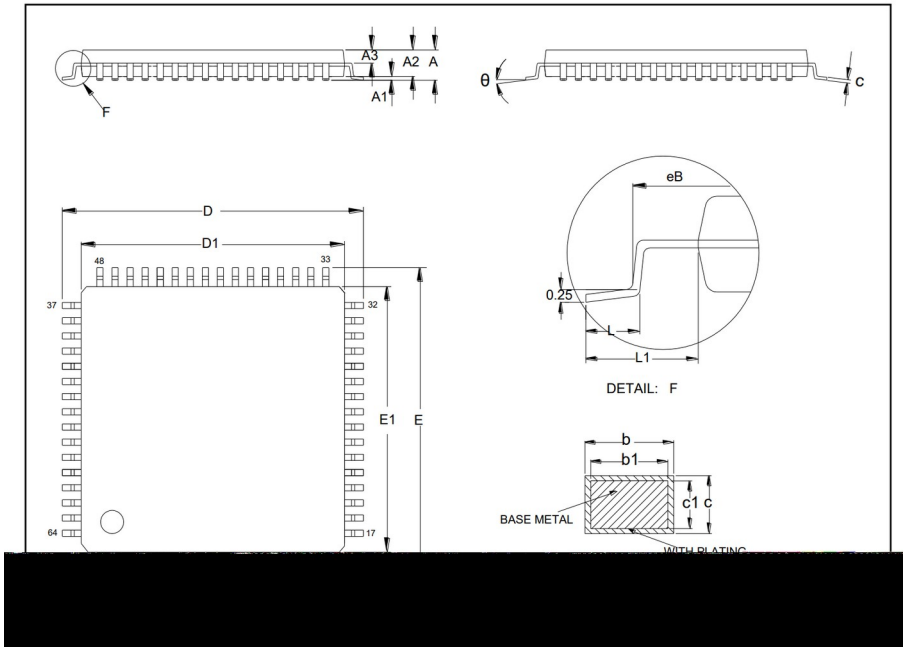


Table 5-1. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	—	0.50	—
eB	11.25	—	11.45
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

Reading

- This lecture
  - Sections 3.4-3.6, 1.6
- Next lecture
  - Sections 3.7, 1.7, 4.1-4.2