CPE201
Digital Design

By Benjamin Haas

Class 21: Shift Registers

University of Nevada, Reno

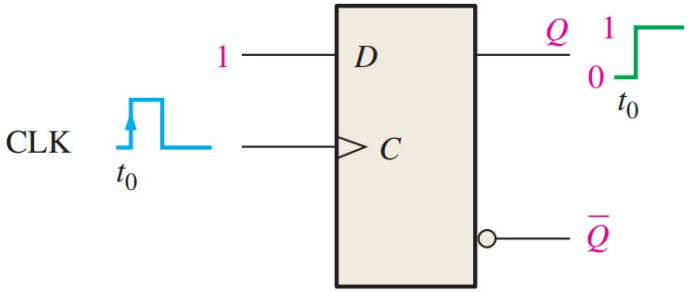
Outline

- Flip-Flop Review
- Shift Register Intro
- 5 Types of shift register configurations
- Notes on real chips

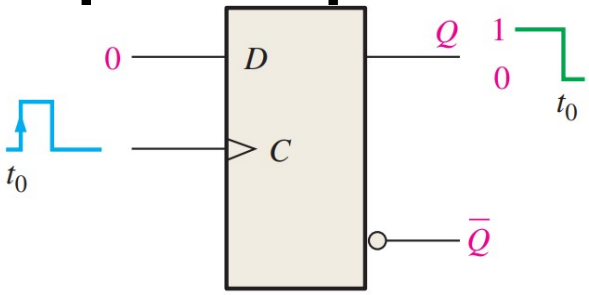
Flip-Flop Applications

- Data Storage
  - Ch8
- Frequency Division
- Counting
  - Ch9

D Flip-Flop



(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	**CLK**	***Q***	$\overline{Q}$	**Comments**
0	↑	0	1	RESET
1	↑	1	0	SET

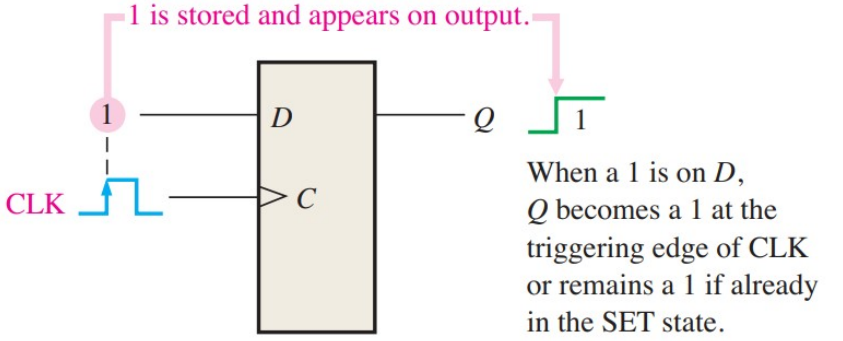
↑ = clock transition LOW to HIGH

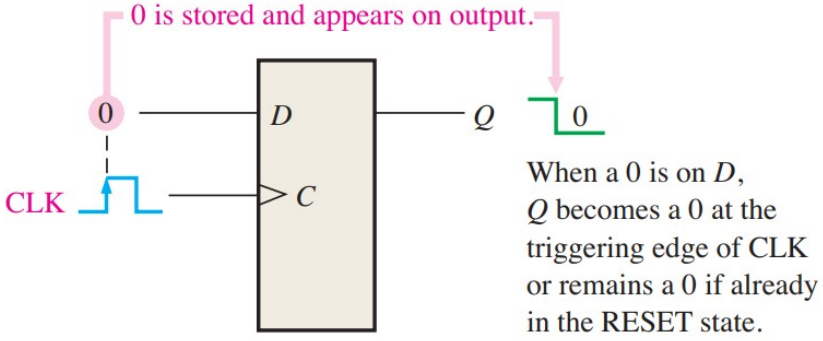
Shift Registers

- No set state machine
- Shift data in from external sources
- A series of flip-flops

Register

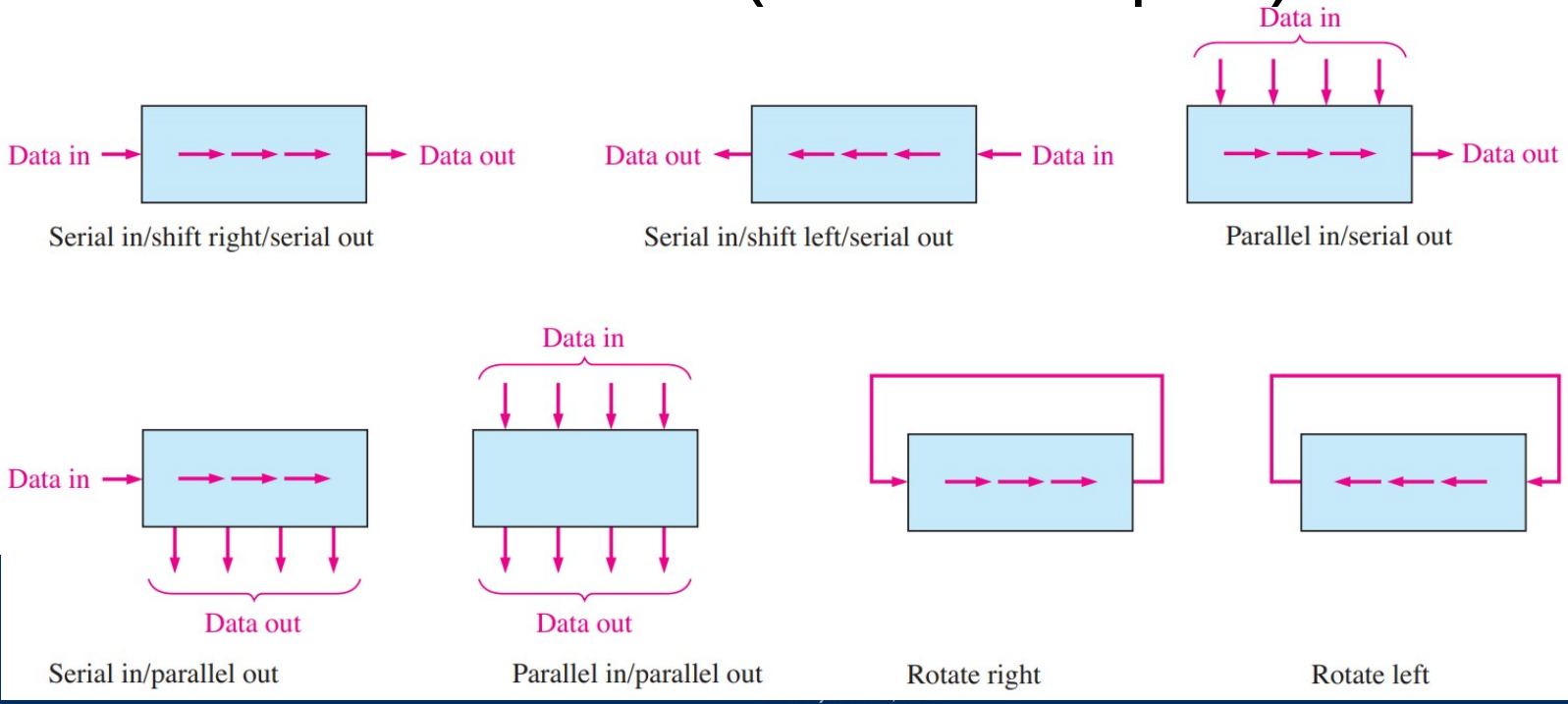
- A digital circuit with 2 functions
  - Data storage





Register

– Data movement (4-bit examples)

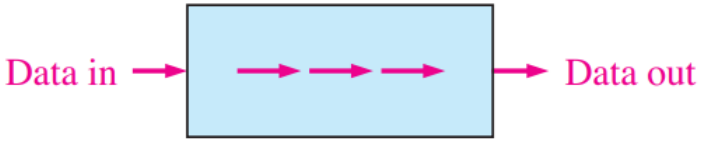


Serial vs. Parallel

- Serial is one line
  - Connection count is small and takes little space
  - Used in long distance comms
- Parallel is one line per bit
  - Very fast because all bits are xferred at once
  - Takes up much more space than serial
  - Used in short distance comms (moving variables)

Serial in / Serial out (SISO)

- Like a queue or buffer
  - Buffering in a long xfer line
- Destructive readout (all these regs do this)

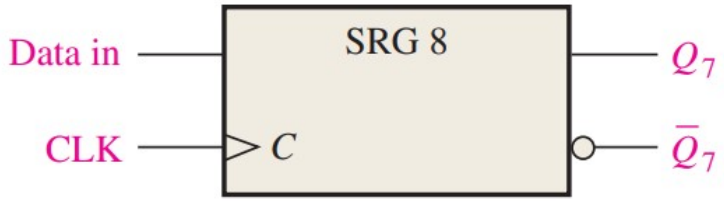


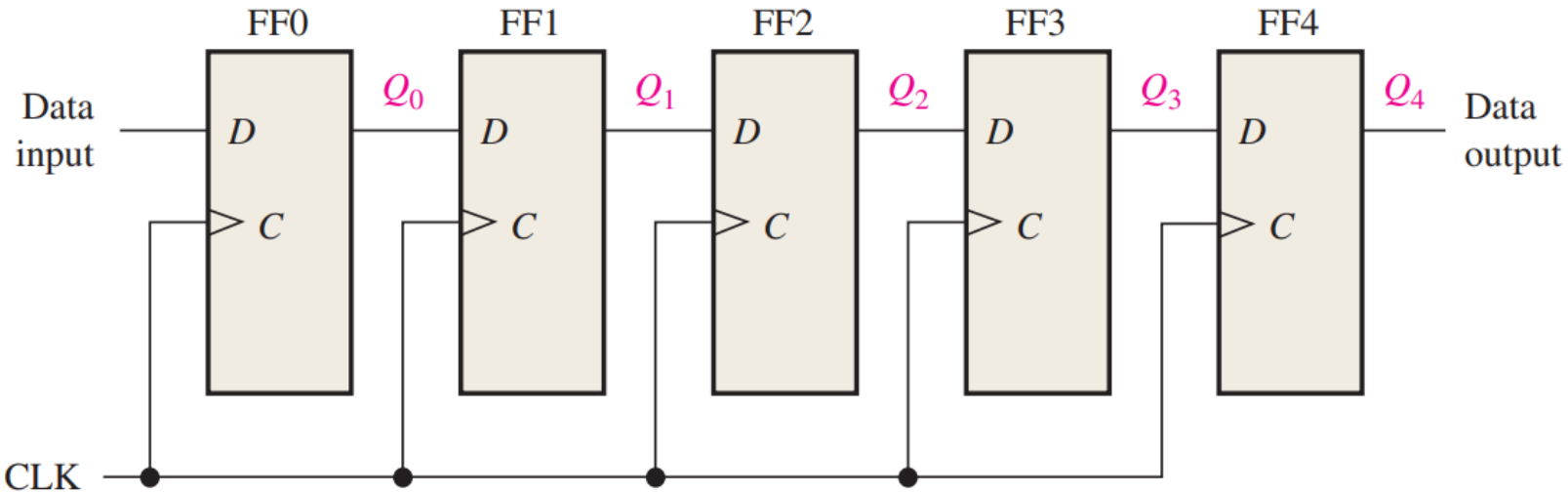
Serial in/shift right/serial out

Serial in/shift left/serial out

SISO Circuit

- Simplest versio





SISO Data Table Example

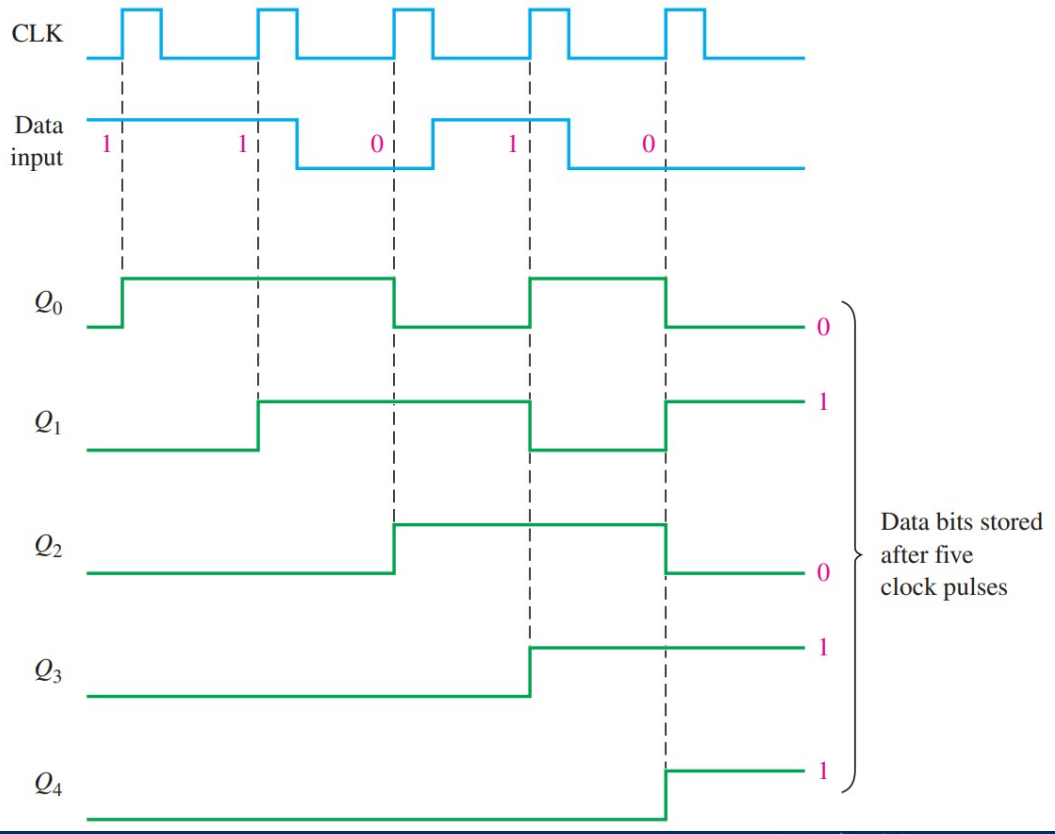
Shifting a 4-bit code into the shift register
Data bits are indicated by a beige screen.

CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	0	0	0	0
1	**0**	0	0	0
2	**1**	**0**	0	0
3	**0**	**1**	**0**	0
4	**1**	**0**	**1**	**0**

Shifting a 4-bit code out of the shift register
Data bits are indicated by a beige screen.

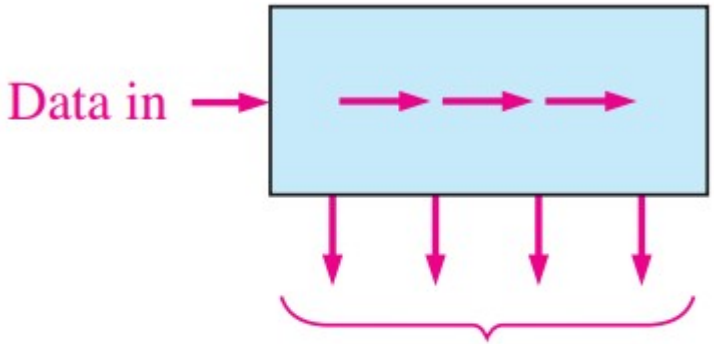
CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	**1**	**0**	**1**	**0**
5	0	**1**	**0**	**1**
6	0	0	**1**	**0**
7	0	0	0	**1**
8	0	0	0	0

SISO Signal Example



Serial in / Parallel out (SIPO)

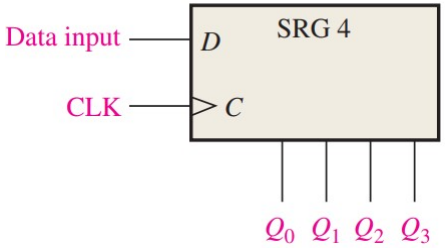
- Converts data format
- Receives data from serial bus and stores into variable

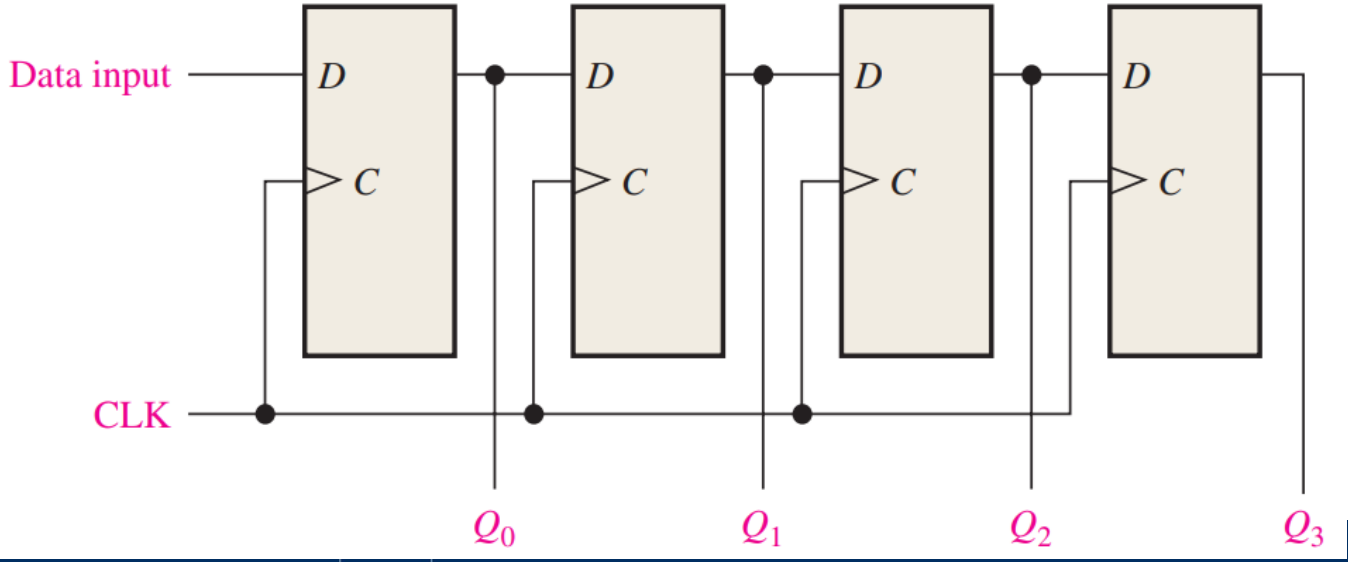


Serial in/parallel out

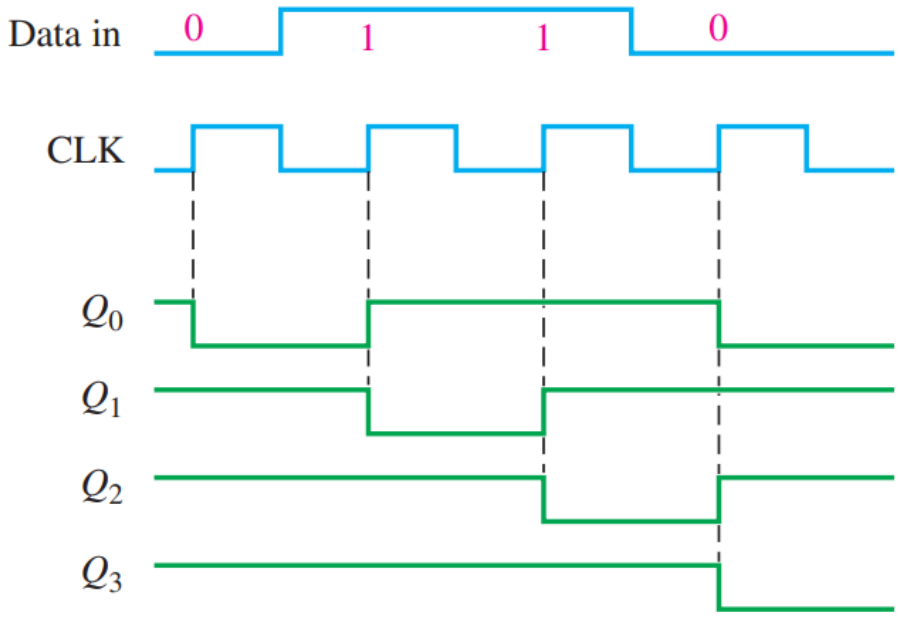
SIPO Circuit

- Read all outputs at any time



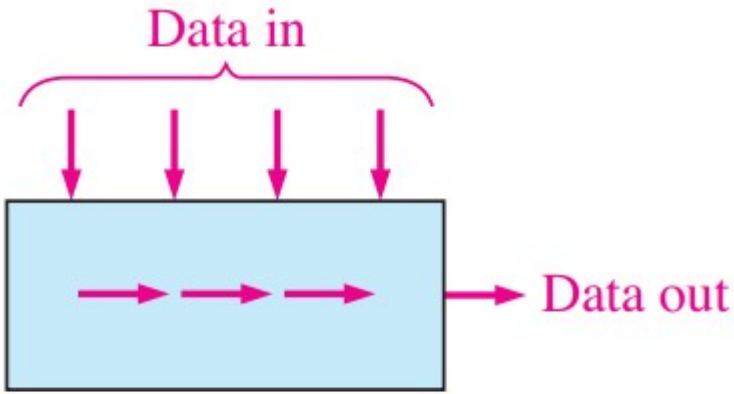


SIPO Signal Example



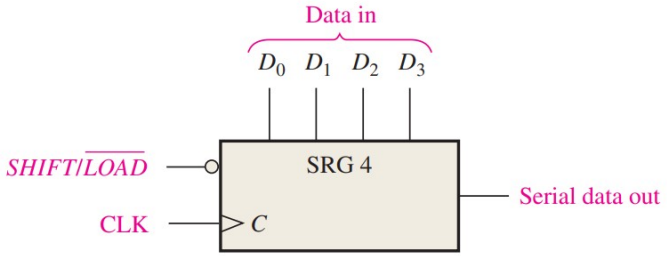
Parallel in / Serial out (PISO)

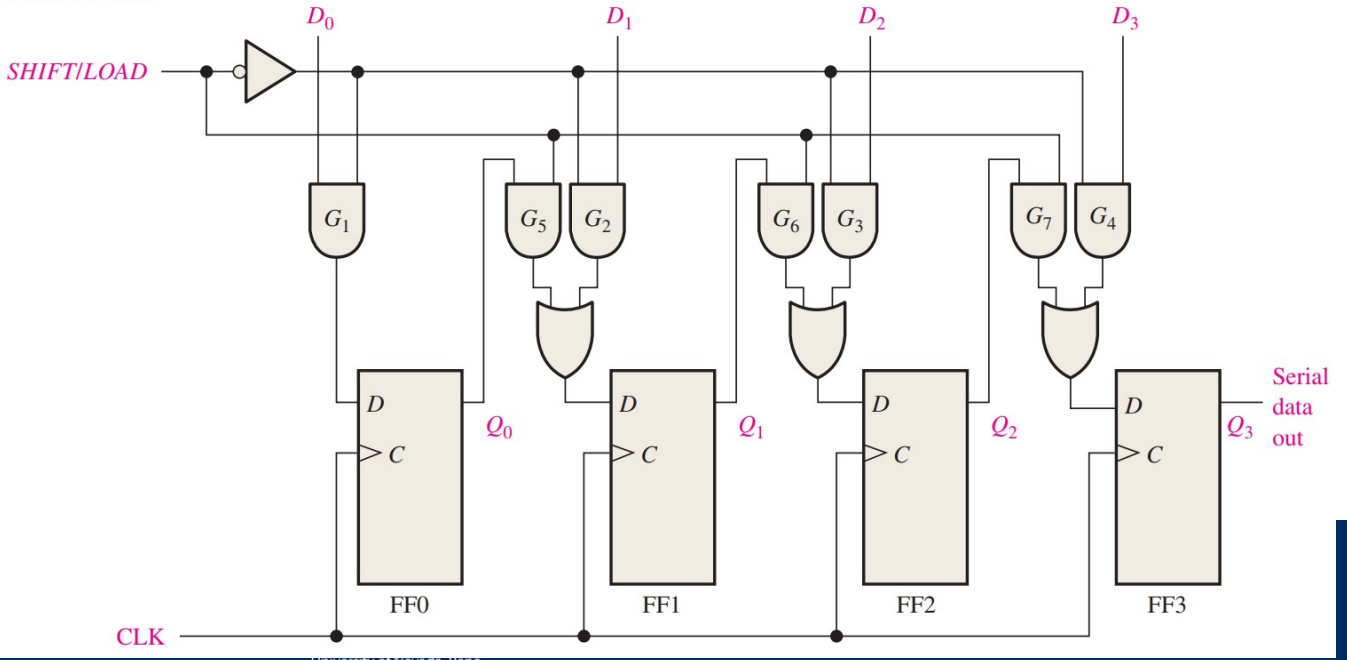
- Converts data format
- Gets data ready to be xferred on serial bus



Parallel in/serial out

PISO Circuit



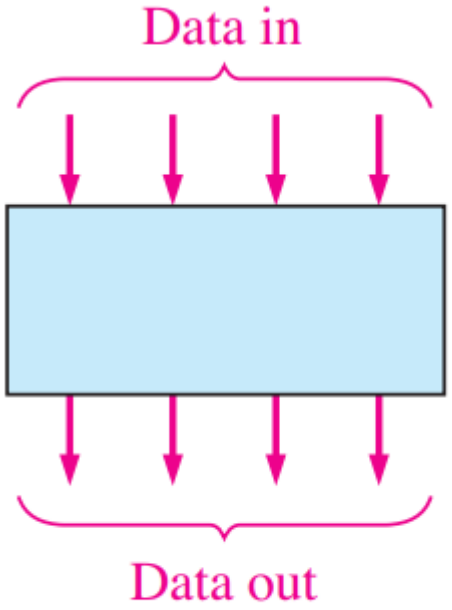


PISO Signal Example

- || data is 0101

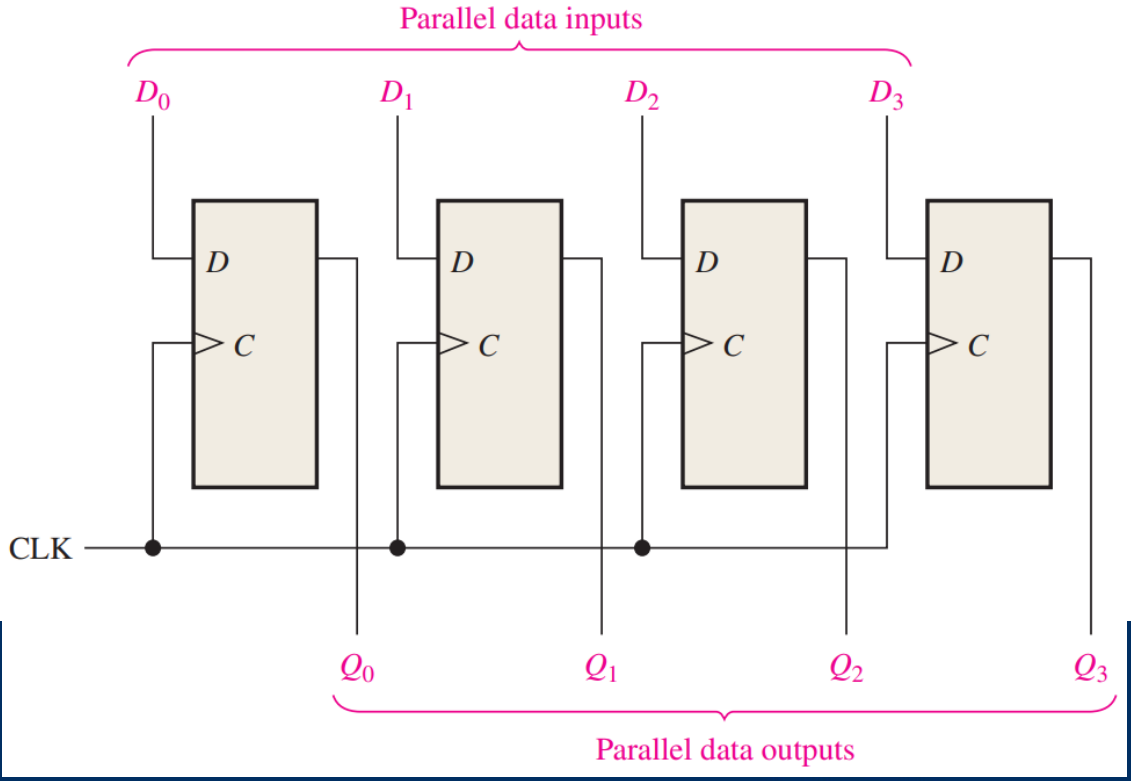
Parallel in / Parallel out (PIPO)

- Move variables around
  - Between registers
  - Into/out of memory

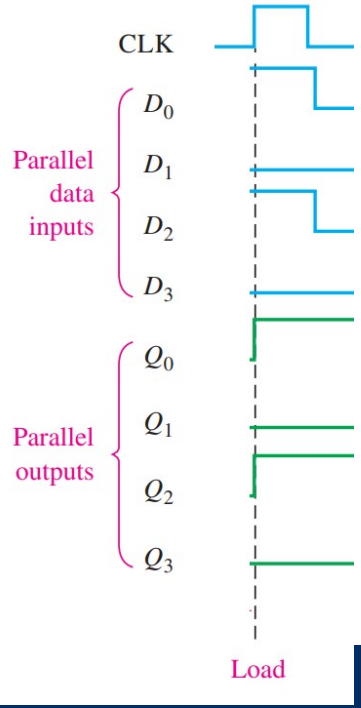


Parallel in/parallel out

PIPO Circuit

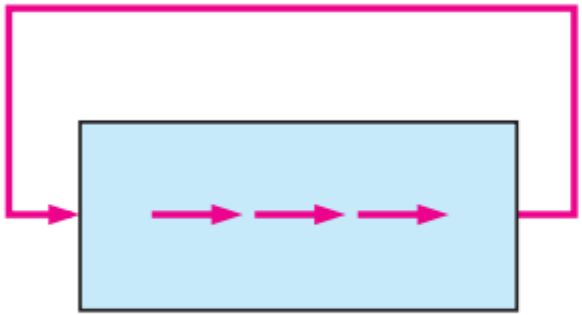


PIPO Signal Example



Bit Rotation

- Usually bidirectional (data can go both directions)
  - Using direction input line



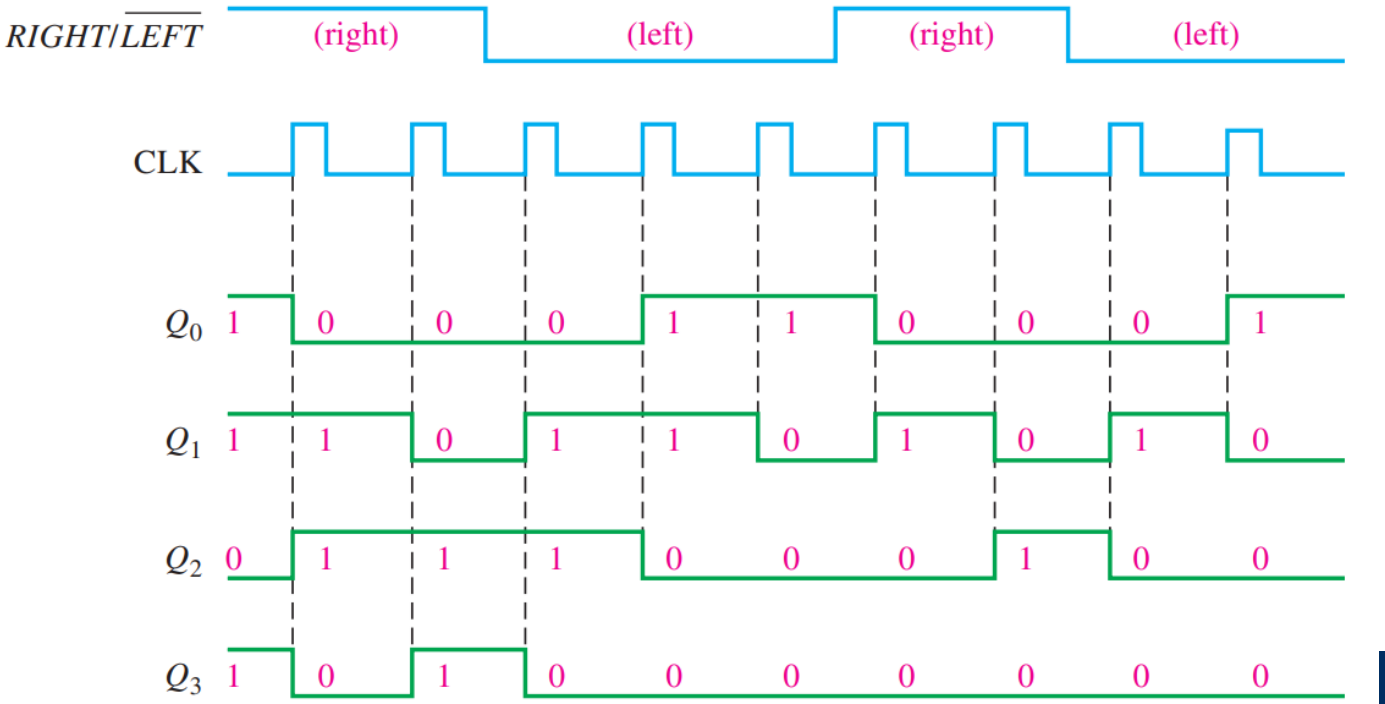
Rotate right

Rotate left

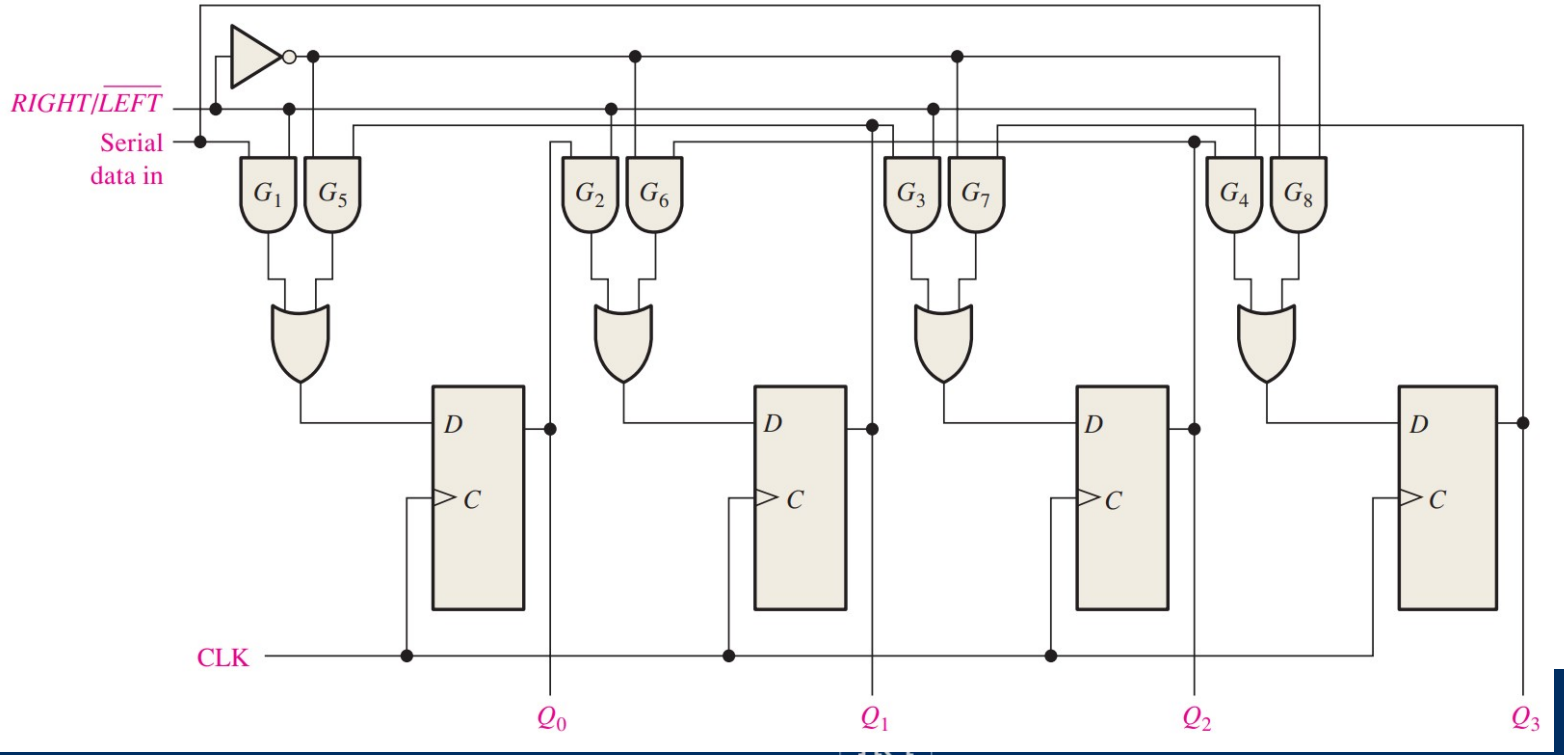
Bit Rotation

- Shift 0100 to the left, get 1000 (0100 << 1)
  - What is that equivalent to?
- Shift 0100 to the right, get 0010 (0100 >> 1)
  - What is that equivalent to?
- What is 5<<1? 7>>1? 9>>2? 1<<4? 3>>3?

Signal Example



Circuit


RIGHT/$\overline{LEFT}$
Serial data in
G_1
G_5
G_2
G_6
G_3
G_7
G_4
G_8
D
C
CLK
Q_0
Q_1
Q_2
Q_3

Real Chips

- The real chips have additional functionality
  - PIPO and SIPO in one chip
  - SISO and PISO in one chip
  - SISO, SIPO, PISO, and PIPO in one chip
    - Universal shift register

Reading

- This lecture
  - Sections 8.1-8.3
- Next lecture
  - Sections 8.4-8.7