CPE201
Digital Design

By Benjamin Haas

Class 13: NAND/NOR Combinational Logic, Chip Properties

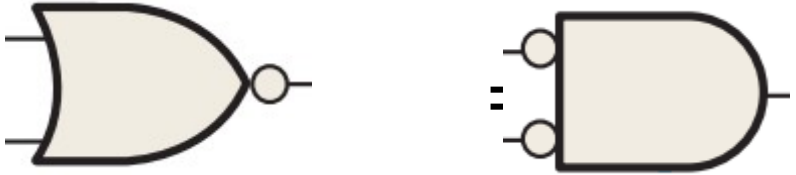
University of Nevada, Reno

Dual Symbols

- (AB)′ = A′ + B′

  - NAND = negative-OR

- (A + B)′ = A′B′



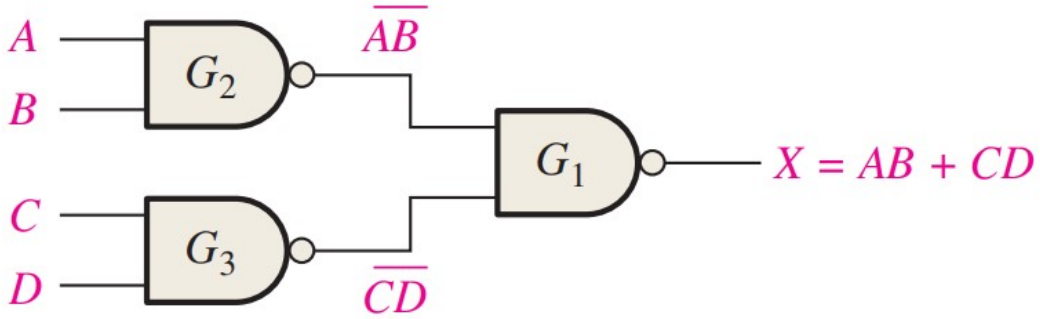
  - NOR = negative-AND

NAND Example

- ((AB)′(CD)′)′

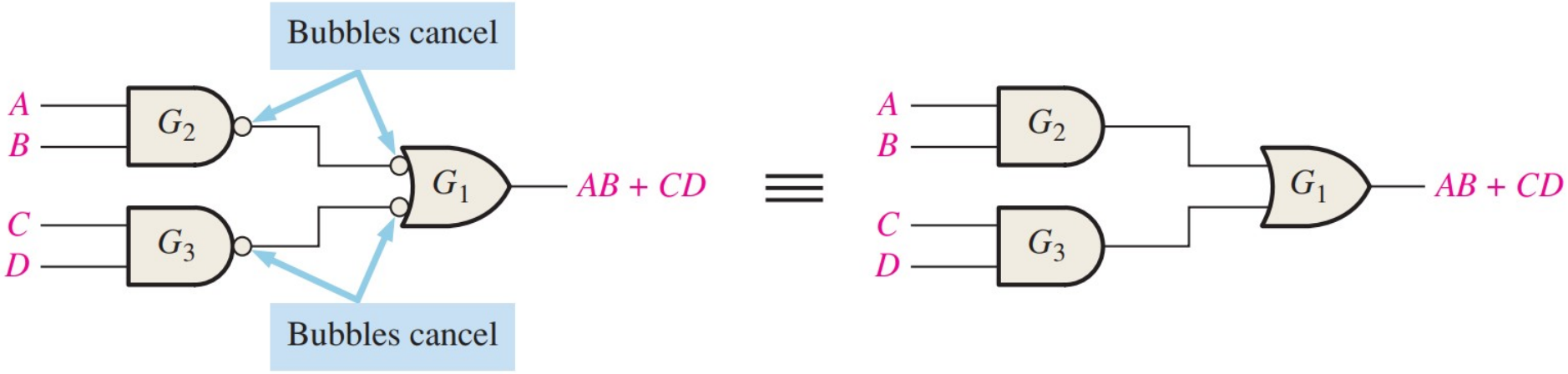
= (AB)″ + (CD)″

= AB + CD



- Now SOP

NAND Example



Equivalent NAND/Negative-OR logic diagram

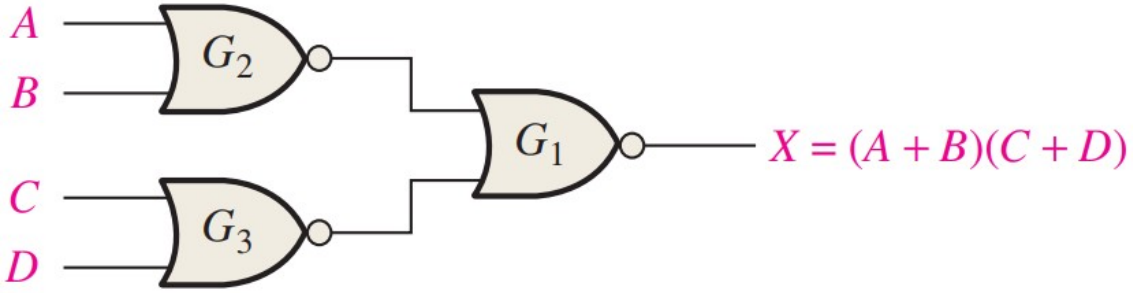
AND-OR equivalent

NOR Example

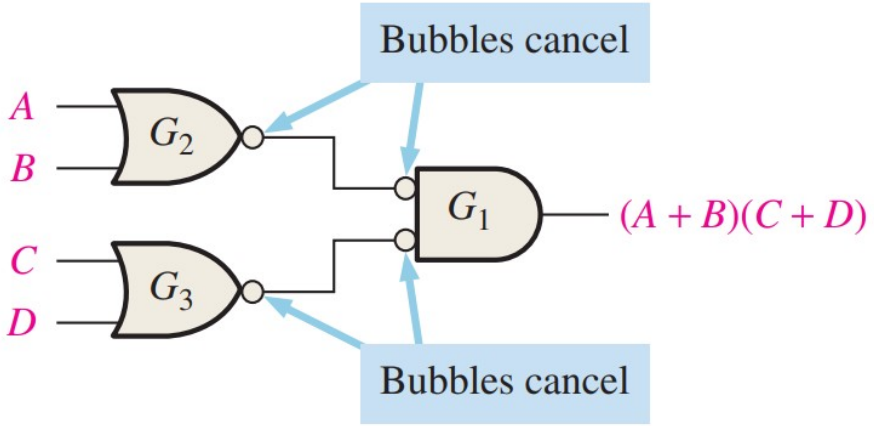
- ((A+B)′+(C+D)′)′

=(A+B)″(C+D)″

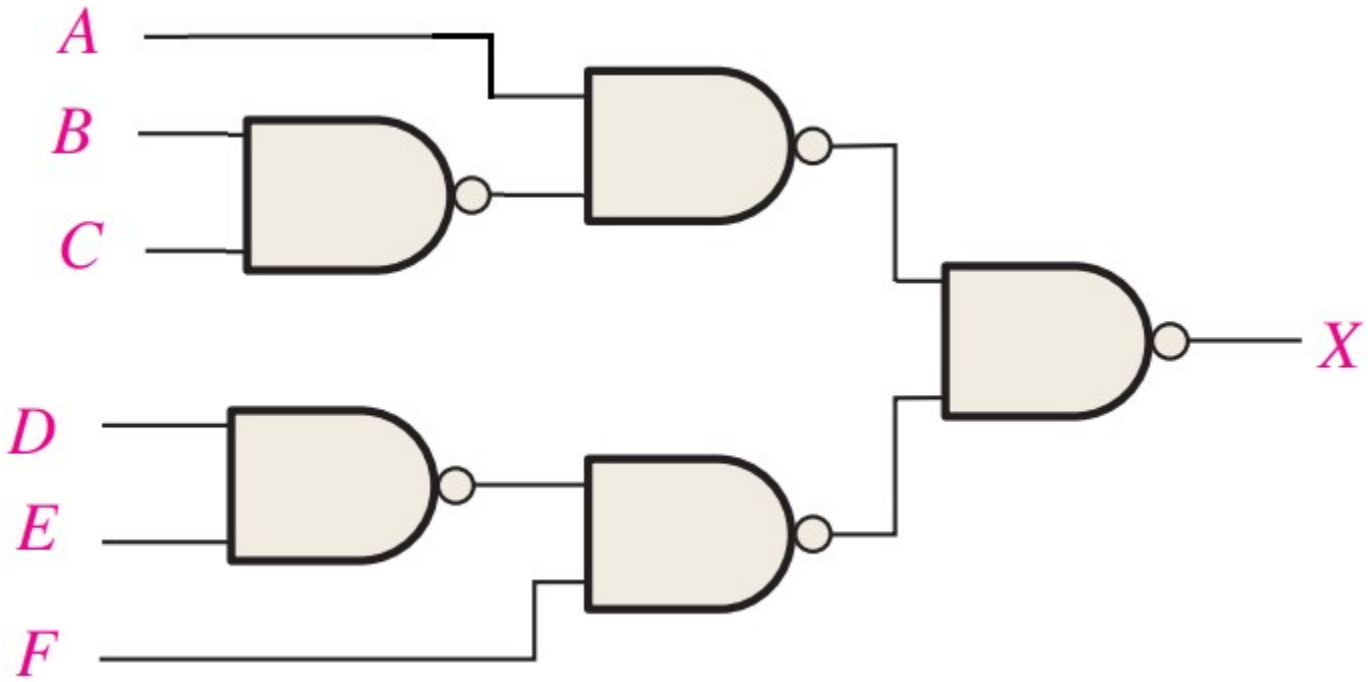
=(A+B)(C+D)



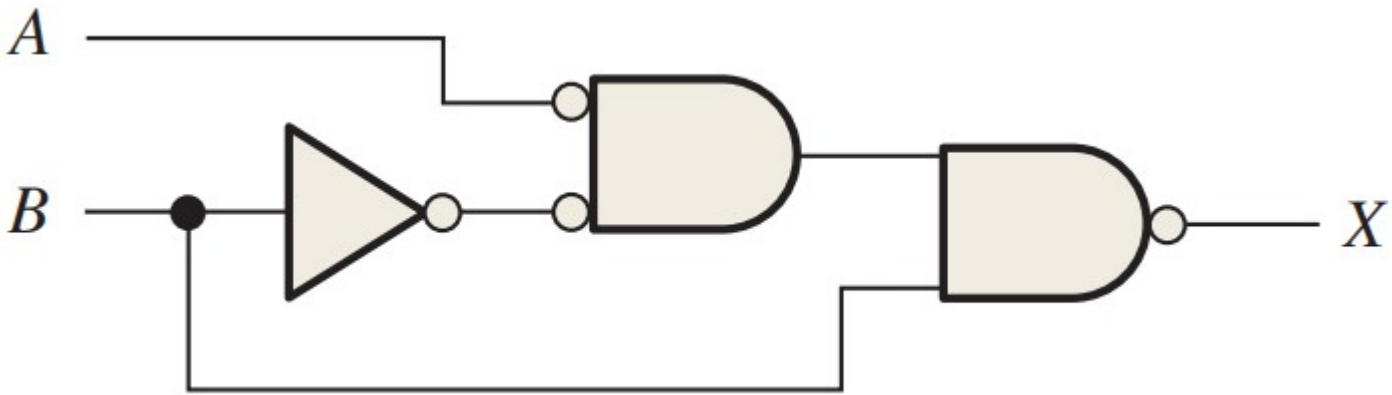
- Now POS



Example



Example

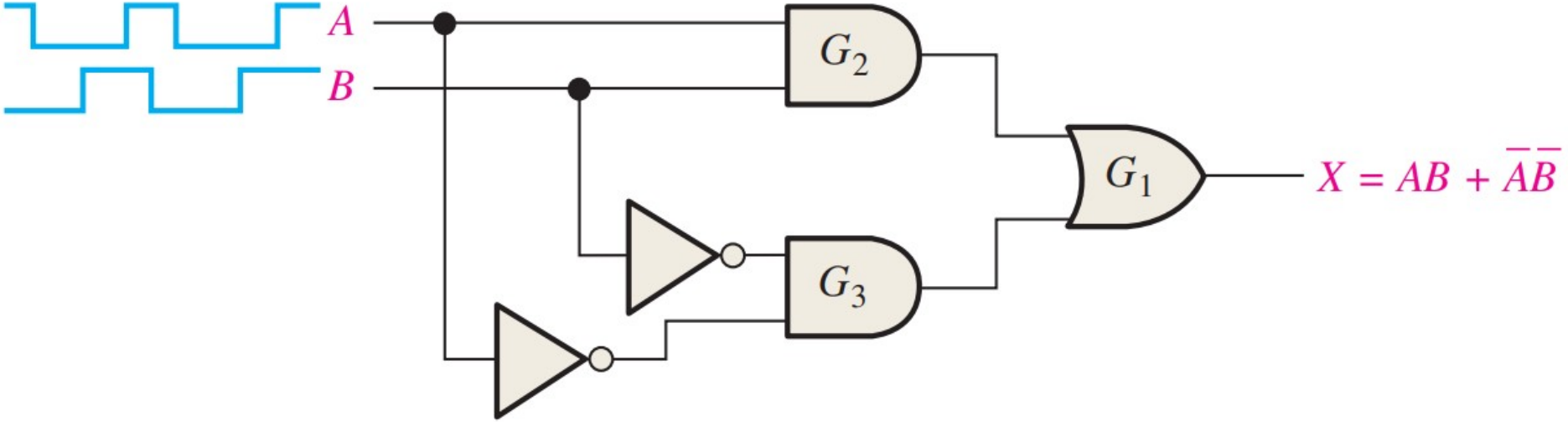


Example

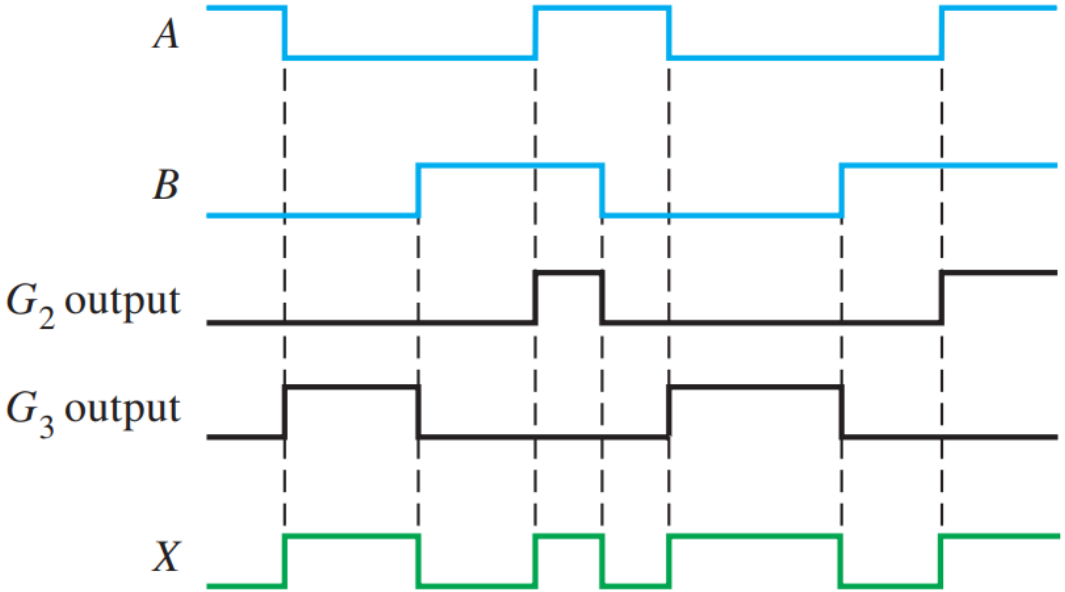
- Implement using only NOR gates
  - X = ABC
- Redo with only NAND gates

Waveforms

- Logic applied at each transition



Waveforms



Real ICs

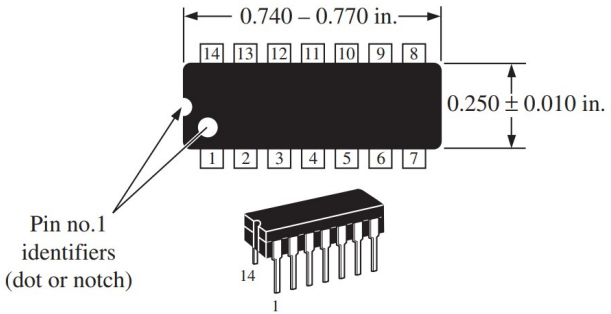
- TTL vs CMOS
  - TTL is older and consumes more power
  - CMOS is more common
  - Usually used now to refer to the logic high level
    - 5V vs 3.3V

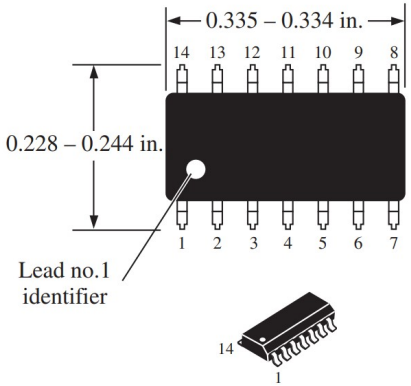
Handling

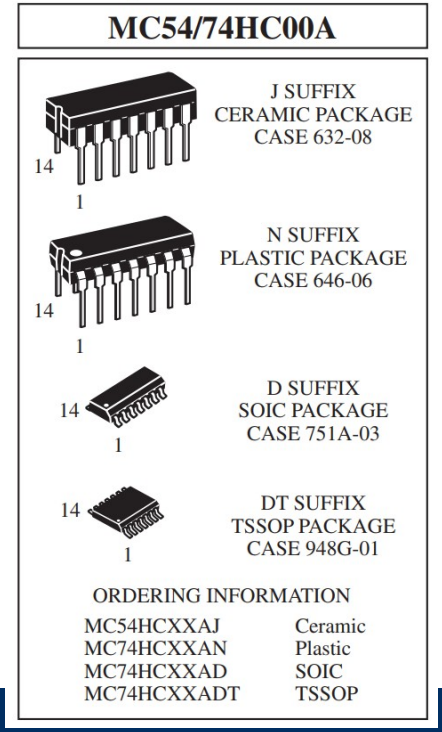
- Electrostatic Discharge (ESD)
  - Will let out the blue smoke, every time
- Safe handling and usage
  - Carrying/Transport (cases, touching, storage)
  - Using (power up last, move unpowered)

Glue Logic or Bubblegum Logic

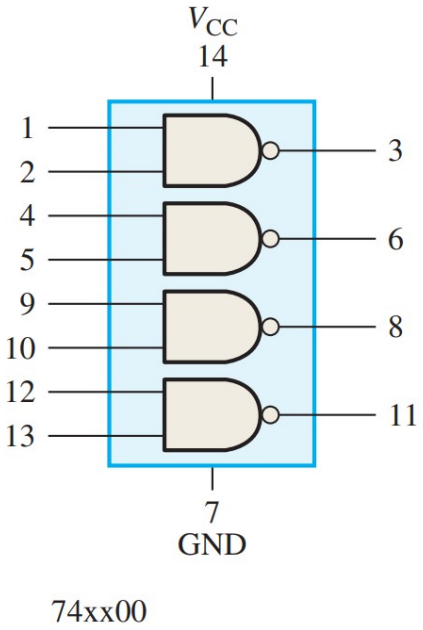
- Info review on ICs



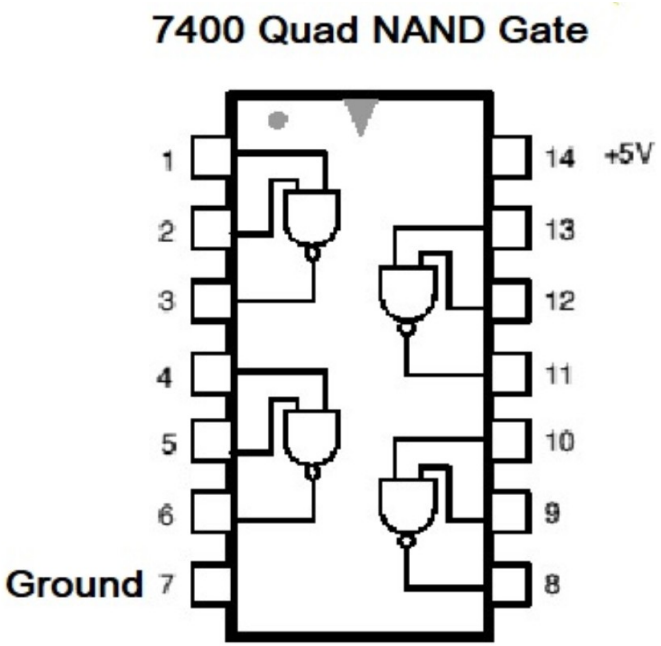




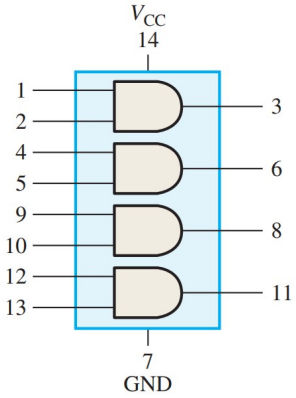
74 Series parts



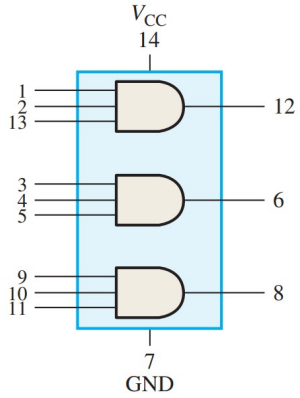
74xx00



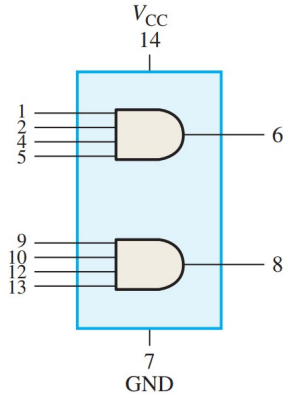
74 Series Parts



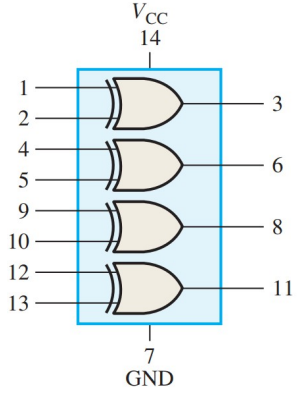
(a) 74xx08



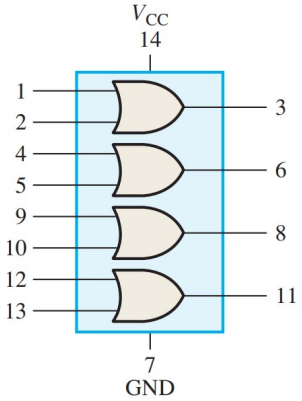
(b) 74xx11



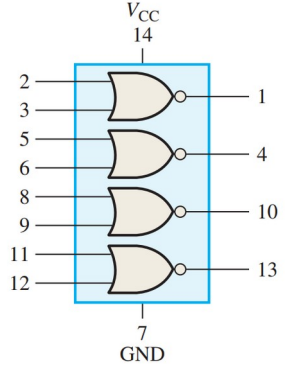
(c) 74xx21



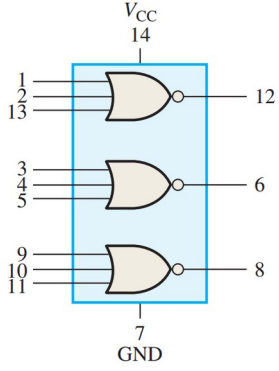
74xx86



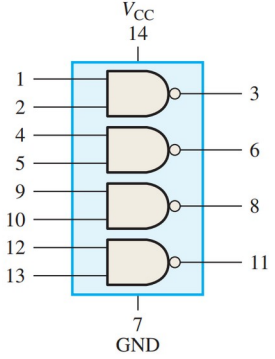
74xx32



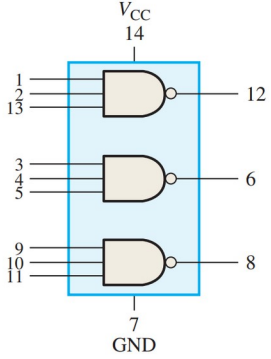
(a) 74xx02



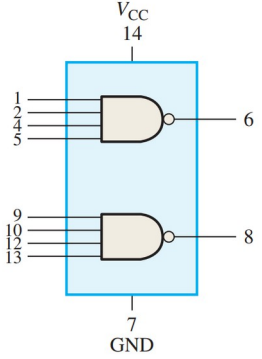
(b) 74xx27



(a) 74xx00



(b) 74xx10



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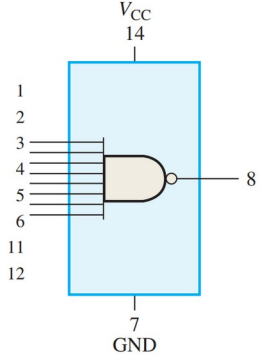


(d) 74xx30

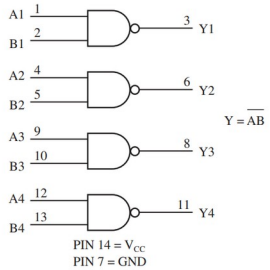
Reading a Datasheet

Quad 2-Input NAND Gate High-Performance Silicon–Gate CMOS

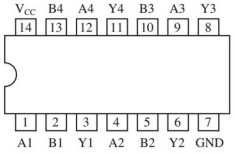
The MC54/74HC00A is identical in pinout to the LS00. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 32 FETs or 8 Equivalent Gates

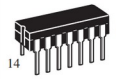
LOGIC DIAGRAM



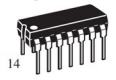
Pinout: 14–Load Packages (Top View)



MC54/74HC00A



J SUFFIX
CERAMIC PACKAGE
CASE 632-08



N SUFFIX
PLASTIC PACKAGE
CASE 646-06

D SUFFIX
SOIC PACKAGE
CASE 751A-03

DT SUFFIX
TSSOP PACKAGE
CASE 948G-01

ORDERING INFORMATION

MC54HCXXAJ	Ceramic
MC74HCXXAN	Plastic
MC74HCXXAD	SOIC
MC74HCXXADT	TSSOP

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
	TSSOP Package†	450	
T_{stg}	Storage Temperature	−65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	Plastic DIP, SOIC or TSSOP Package	260	
	Ceramic DIP	300	

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: – 10 mW/°C from 65° to 125° C
Ceramic DIP: – 10 mW/°C from 100° to 125° C
SOIC Package: – 7 mW/°C from 65° to 125° C
TSSOP Package: – 6.1 mW/°C from 65° to 125° C

RECOMMENDED OPERATING CONDITIONS

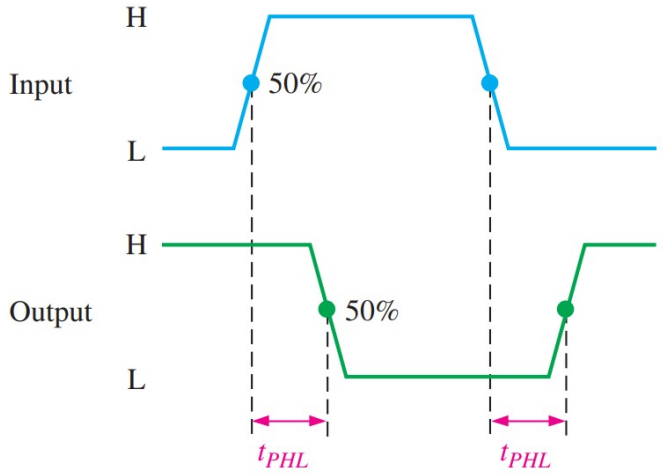
Symbol	Parameter		in	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

DC CHARACTERISTICS (Voltages Referenced to GND) MC54/74HC00A

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit −55 to 25°C	≤85°C	≤125°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\lvert I_{out}\rvert \le 20\mu A$	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\lvert I_{out}\rvert \le 20\mu A$	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	

Propagation Delay

- Switching speed limit
  - t_{PHL} – high to low propagation time
  - t_{PLH} – low to high propagation time
  - 9ns for 7400 above
  - Be aware of race conditio

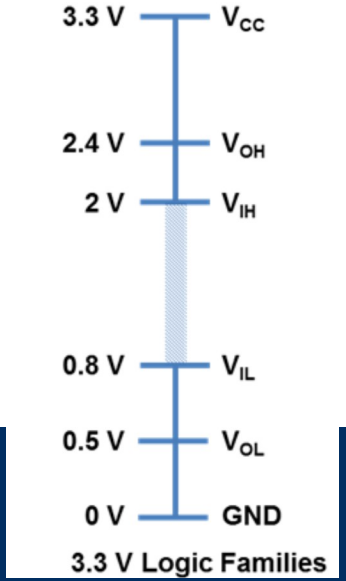


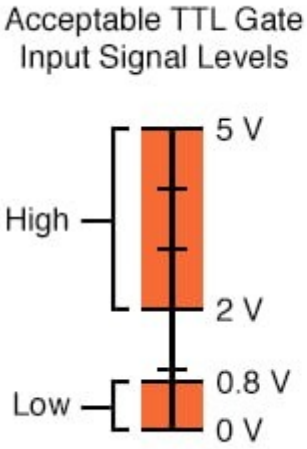
Supply voltage (Vcc)

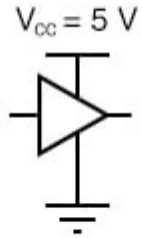
- 5V, 3.3V, 2.5V, 1.8V
  - Input range can vary
  - Must match the rest of your circuits

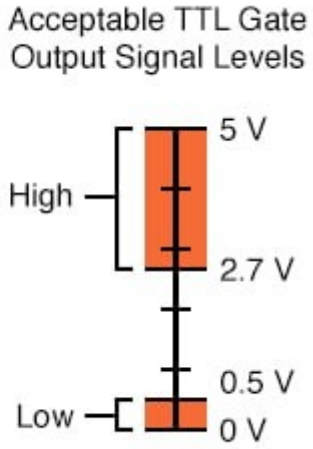
Input/Output Logic Levels

- Varies with supply voltage
  - Stay out of the indeterminant zone









Power Dissipation

- Each part draws power
  - Usually lost to heat
  - Keep it well below your maximum
  - Sometimes dependent on frequency of use

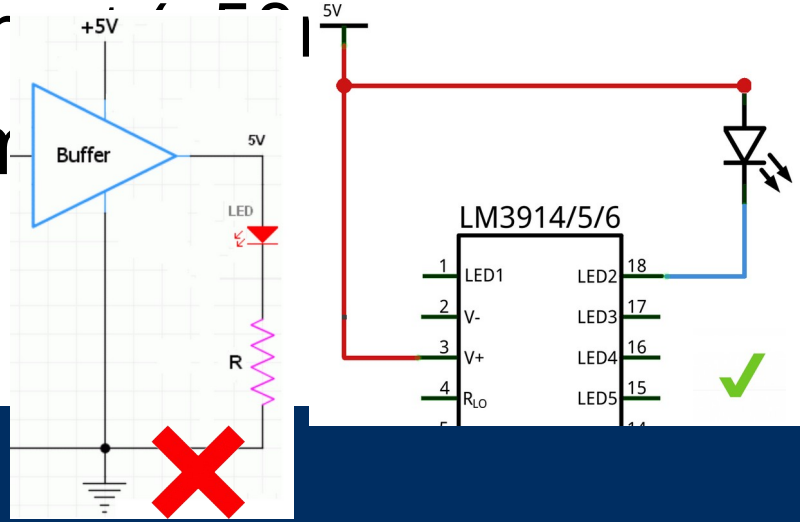
Fan-Out and Loading

- Each chip can only output so much current
- Fan-Out is how many of the same chips one chip could drive
- Ratio of output current to input current

$$\text{Unit loads} = \frac{I_{OL}}{I_{IL}} = \frac{8.0\ \text{mA}}{0.4\ \text{mA}} = 20$$

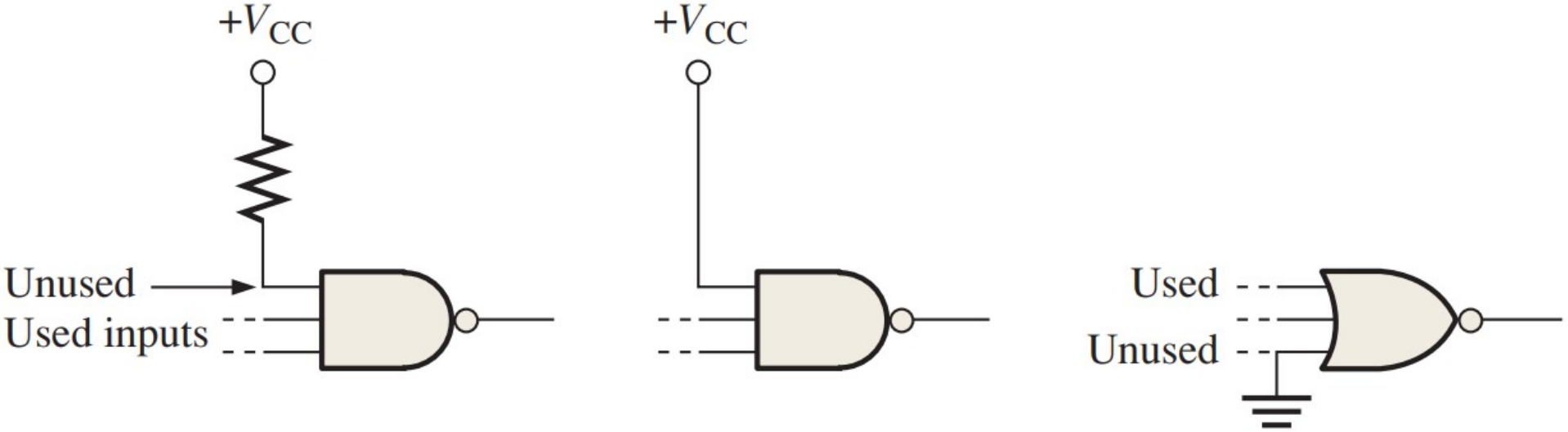
Driving LEDs

- ICs can’t usually source much current (~10mA)
  - ICs can sink more curr
- LEDs usually take 30m



Terminating Un-used Inputs

- Floating inputs is bad



Reading

- This lecture
  - Sections 5.4-5.5, 3.8
- Next lecture
  - Sections 6.1-6.3