CPE201 HW 5 (100 points)

Answer all questions completely. Put a box around the final solution. Put your name on it. Show your work.

By hand:

1. Write the output expression for the circuits in Figure 1 and Figure 2.

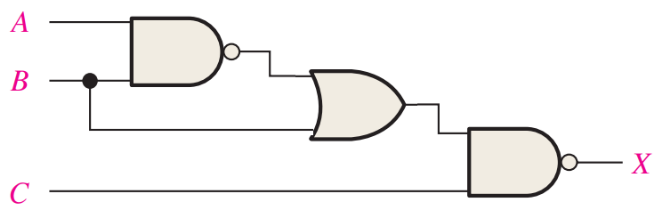


Figure 1

Starting from the left, the first gate gives (AB)’
Then adding the next gate gives (AB)’ + B
Then adding the last gate gives X = (((AB)’ + B)C)’

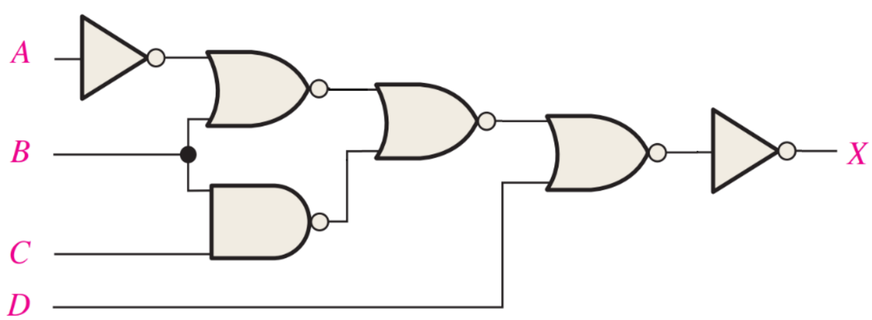
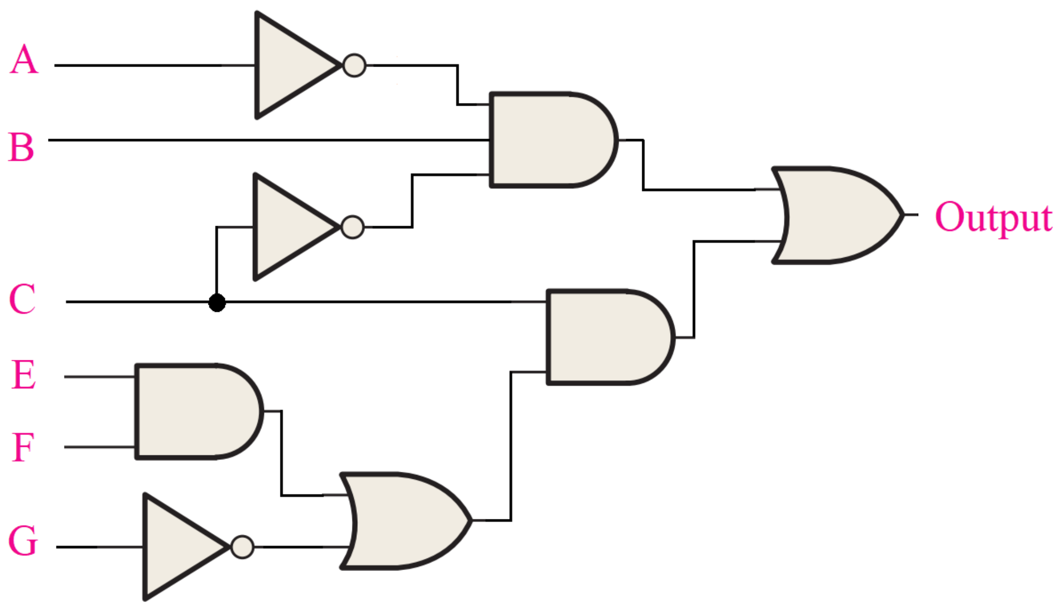


Figure 2

Starting on the left, the first NOR gate gives (A’ + B)’
The first NAND gate gives (BC)’
Putting both of these into the next gate gives ((A’ + B)’ + (BC)’)’
Adding the next NOR gate gives (((A’ + B)’ + (BC)’)’ + D)’
Then the last NOT gives X = ((A’ + B)’ + (BC)’)’ + D
You can distribute one of the NOTs to give X = (A’ + B)BC + D

2. Implement the following expression using only AND, OR, and NOT gates: A’BC’ + C(EF + G’)

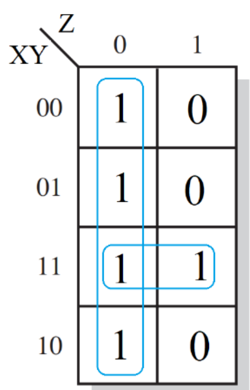
This is one way to implement the circuit



3. Create a circuit that implements the following truth table.

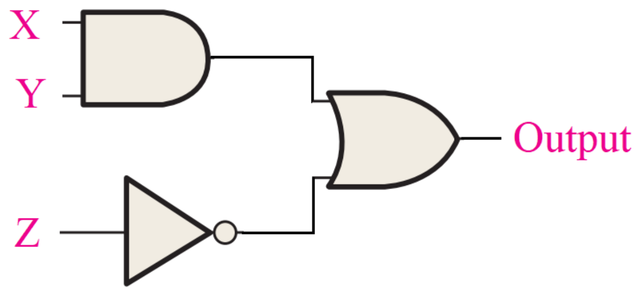
X	Y	Z	Output
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

One option is a minimized SOP expression using a Karnaugh map. The map would be



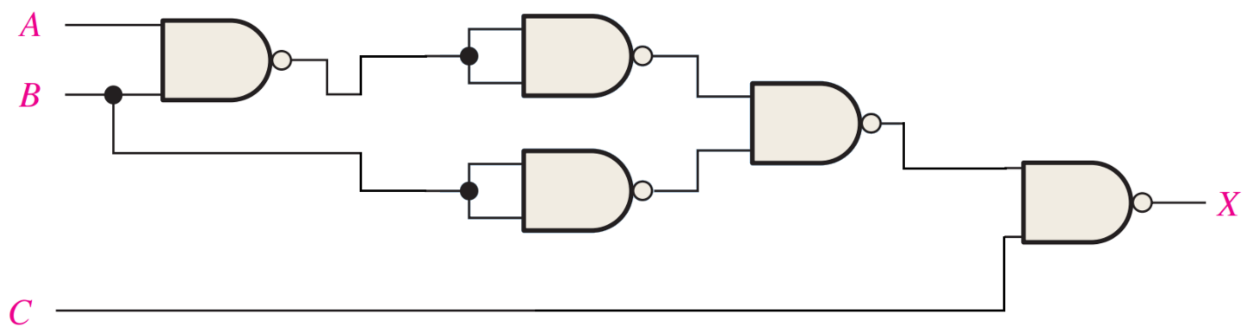
Writing the SOP expressions for the two circles gives
Z’ + XY

Creating a circuit for this expression would look like



4. Implement the circuit in Figure 1 using only NAND gates.

Only one OR gate needs to be replaced with NAND gates using the table that shows the equivalents



5. Implement the circuit in Figure 2 using only NOR gates.

The two NOT gates and the one NAND gate needs to be replaced with NOR gates using the table that gives the equivalents.