CPE201
Digital Design

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Class 22: Shift Registers 2

University of Nevada, Reno

Outline

- Shift Register Counters
  - Johnson Counter
  - Ring Counter
- Shift Register Applications
- Troubleshooting

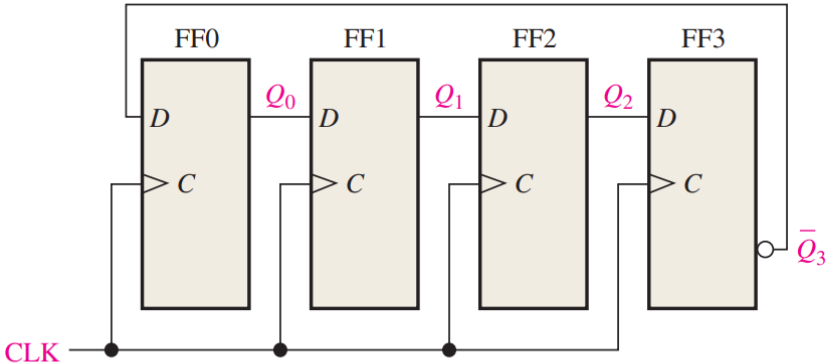
Shift Register Counter

- Output is connected back to input
  - Are also considered counters (Ch9)
- Have a specified sequence of states

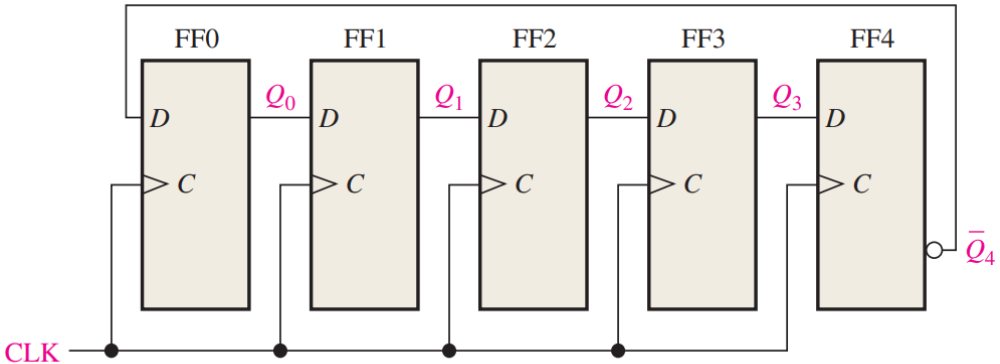
Johnson Counter

- Creates a clock frequency that is 2n slower that CLK
  - n is the number of bits in the counter
- Ex: if CLK is 1MHz and the counter has 5 bits
  - Johnson counter freq = 1MHZ/(2*5) = 100kHz

Circuit



Four-bit Johnson counter



Five-bit Johnson counter

Four-bit Johnson sequence.

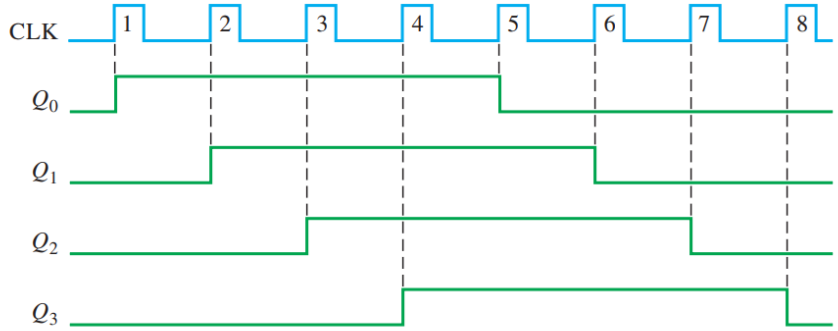
Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Five-bit Johnson sequence.

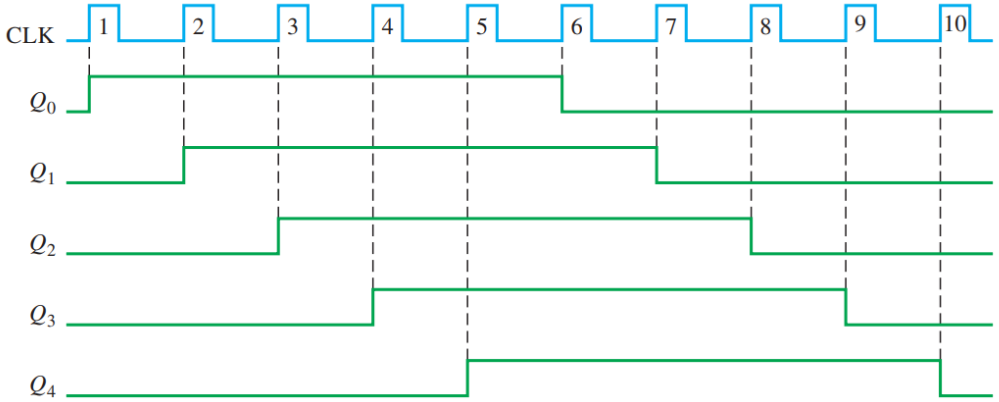
Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

Signal Example

- Measure output i
  one spot
- No signal
  setup required



Timing sequence for a 4-bit Johnson counter.



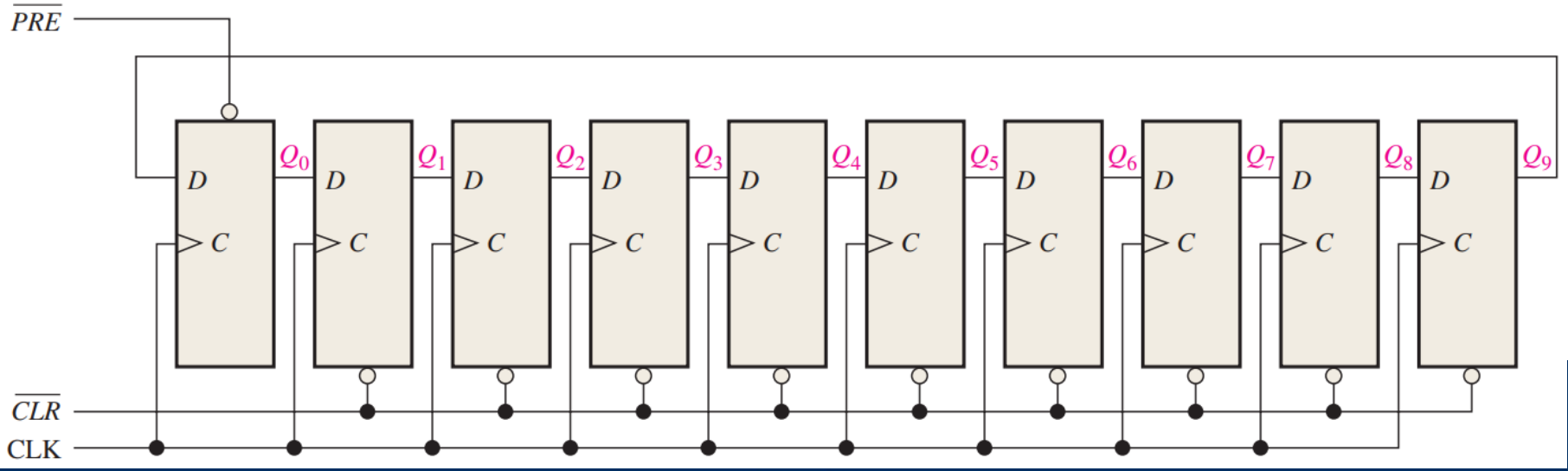
Timing sequence for a 5-bit Johnson counter.

Ring Counter

- Like a Johnson counter, but with any bit pattern
- The pattern continuously goes through all flip-flops and then back to the beginning

Circuit

- No use of Q’
- Use Preset to insert bit sequence



Logic Table

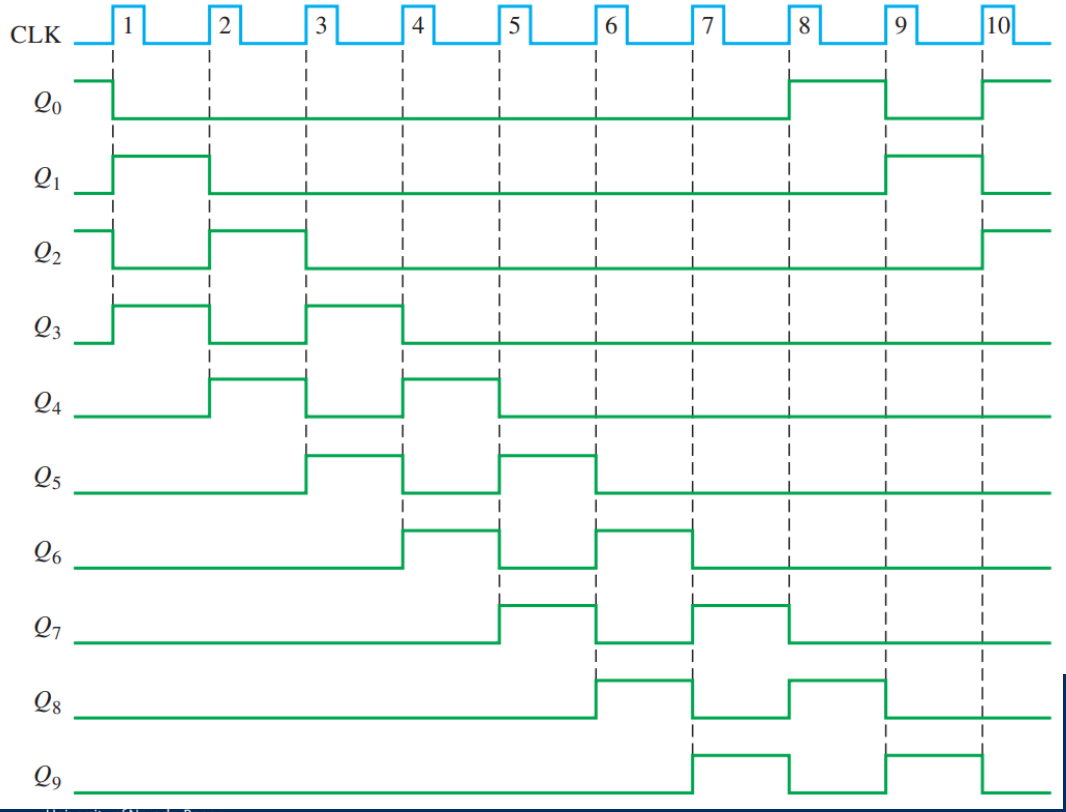
- Read any flip-flop output to watch the sequence

Ten-bit ring counter sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1

Signal Example

- Needs PRE’ on CLK 1 & 3 to set the seq
  - You set that up externally

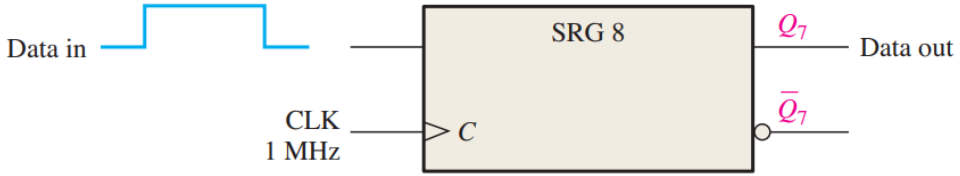


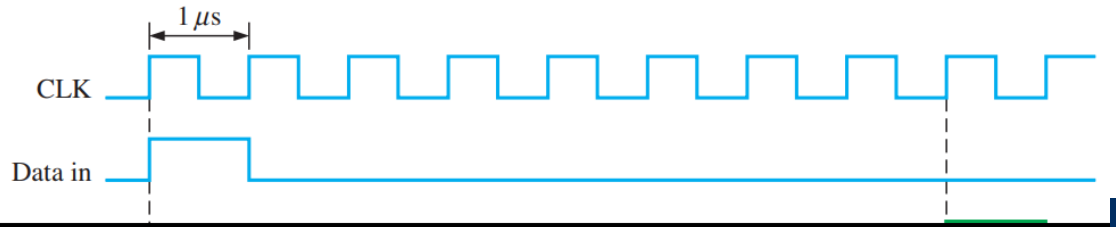
Applications

- Time Delay
- Serial to Parallel Converter
- UART Transmitter
- Keyboard Encoder

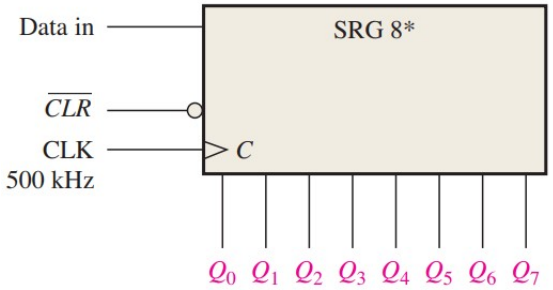
Time Delay

- Insert a delay into some signals
  - Allow for setup time on a part w/o delaying

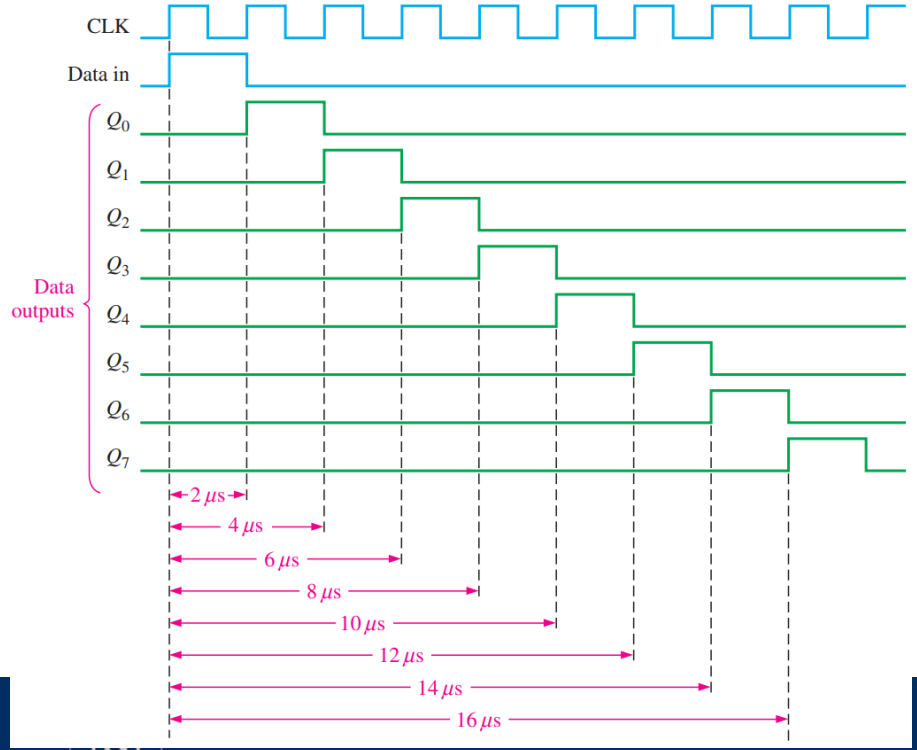




Another Option



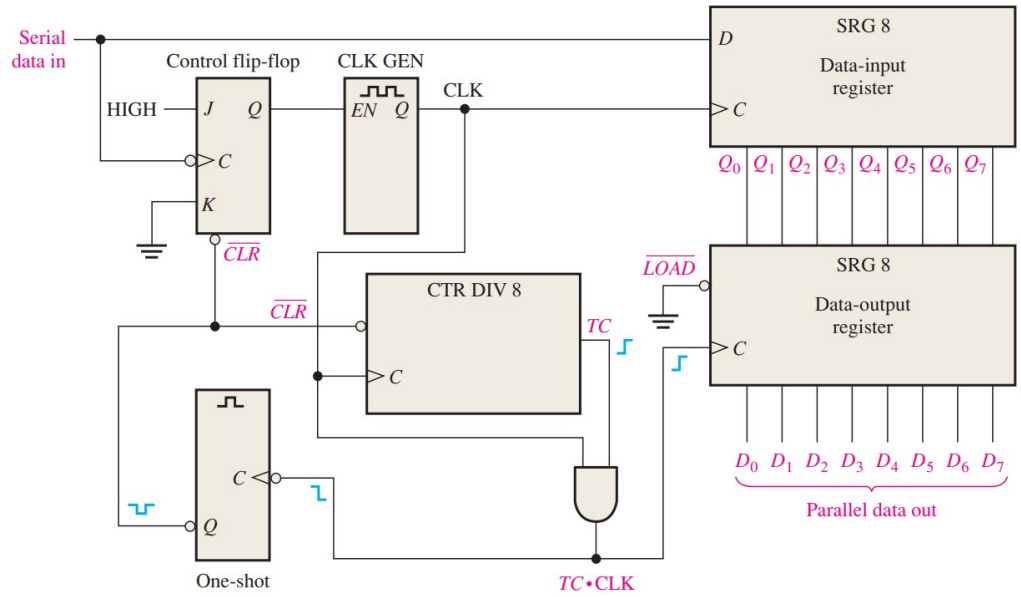
* Data shifts from Q_0 toward Q_7.

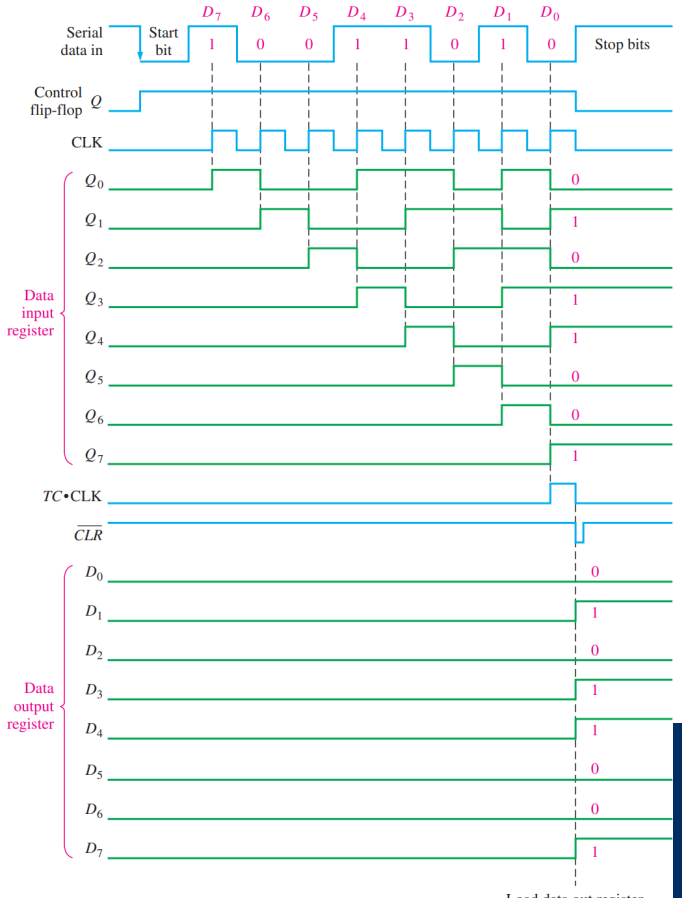


Serial to Parallel Converter

- Serial is one line
  - Connection count is small and takes little space
- Parallel is one line per bit
  - Very fast because all bits are xferred at once
  - Takes up much more space than serial

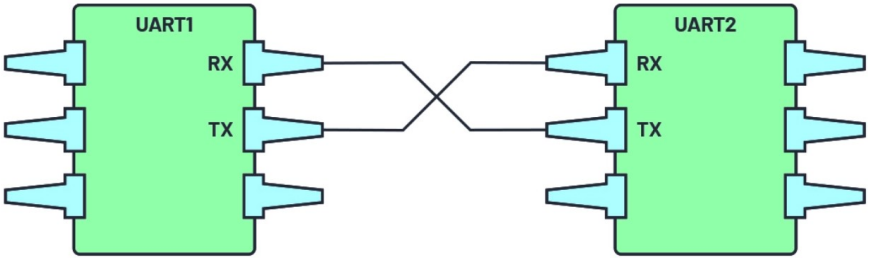
Serial to Parallel Converter





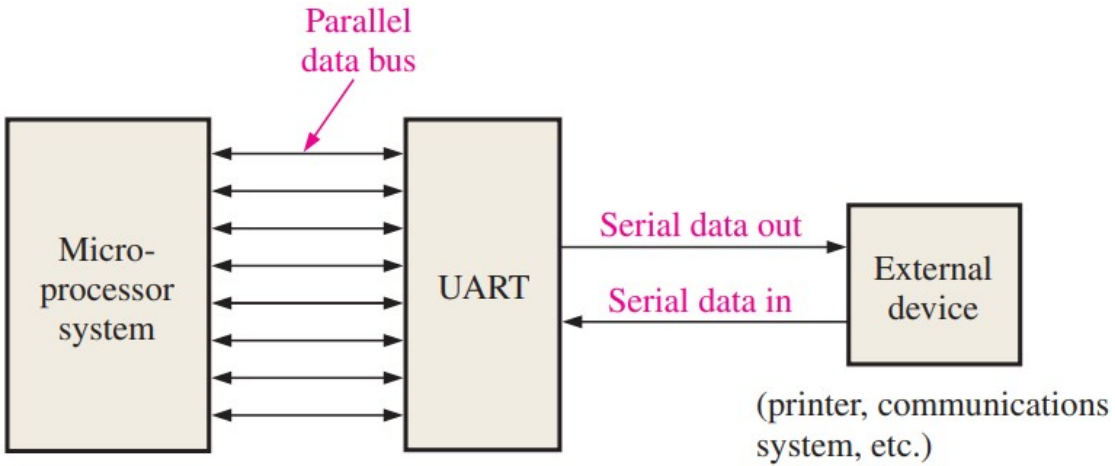
UART

- Universal Asynchronous Receiver Transmitter
  - Full Duplex (RX and TX as same time)
  - Asynchronous (no cl
  - Serial data xfer
  - Low overhead



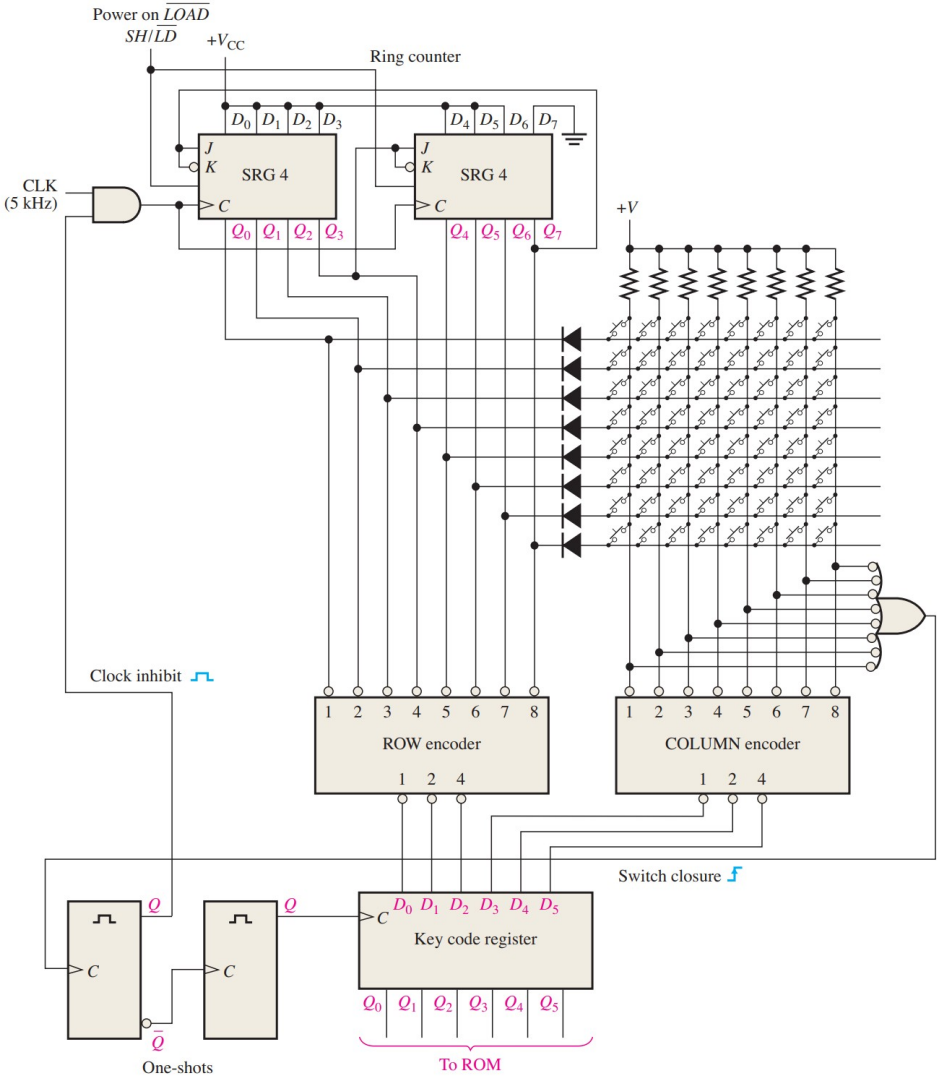
UART

- PISO transmit / SIPO receive



Keyboard Encoder

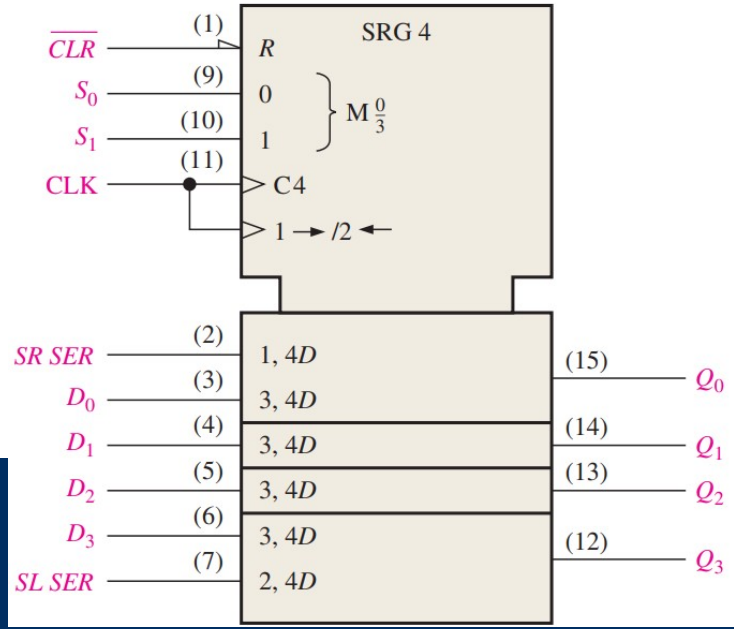
- Get key press data to send over USB to computer
  - Simplified with no key press memory buffer
- Scans for pressed keys
- Encodes key presses and stores for TX
- Debounces a key press


Power on $\overline{LOAD}$
$SH/\overline{LD}$
$+V_{CC}$
Ring counter
D_0 D_1 D_2 D_3
D_4 D_5 D_6 D_7
J
K
SRG 4
C
SRG 4
CLK
(5 kHz)
Q_0 Q_1 Q_2 Q_3
Q_4 Q_5 Q_6 Q_7
+V
Clock inhibit
1 2 3 4 5 6 7 8
ROW encoder
1 2 4
1 2 3 4 5 6 7 8
COLUMN encoder
1 2 4
Switch closure
Q
C
Q
C
D_0 D_1 D_2 D_3 D_4 D_5
Key code register
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5
$\overline{Q}$
One-shots
To ROM

Real Chip – 74HC194

- Universal shift reg

Do nothing:	$S_0 = 0, S_1 = 0$	(mode 0)
Shift right:	$S_0 = 1, S_1 = 0$	(mode 1, as in 1, 4D)
Shift left:	$S_0 = 0, S_1 = 1$	(mode 2, as in 2, 4D)
Parallel load:	$S_0 = 1, S_1 = 1$	(mode 3, as in 3, 4D)

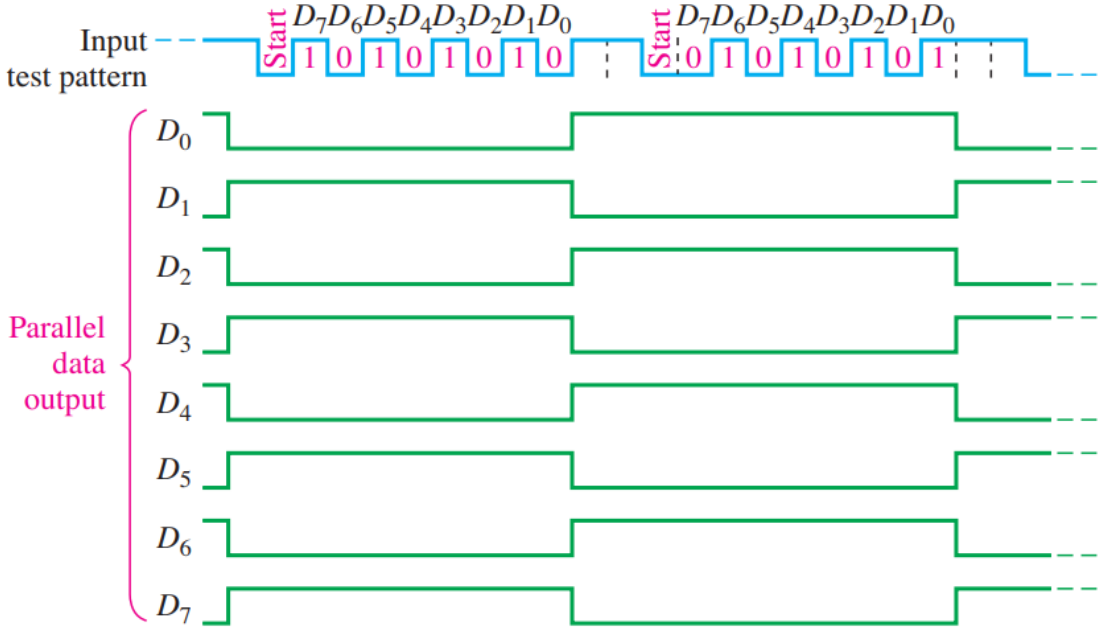


Exercising a Circuit

- Put all parts of the circuit through all possible states
  - Tests all chips for working status
  - Tests all circuit connections
  - More complicated with more memory parts or complexity

Example (SIPO Test)

- Using circuit from Serial to Parallel Converter ea



Reading

- This lecture
  - Sections 8.4-8.7
- Next lecture
  - 9.1-9.4