Design of On-Board Battery Charger using Interleaved Bridgeless Type PFC and Phase Shifted Full Bridge Converter

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***Abstract*— With increase of DC micro grids and electrical vehicles (EV), battery charging application has gained a lot of prominence. Many of these systems are fed by utility. The AC/DC conversion is done by classical diode bridge rectification which causes low input power factor and adversely affects the utility supply. Thus input power factor correction is one of the major concerns. Also, switched mode power converter incurs high switching losses at high frequencies of operation. Reduction of switching frequency is not a solution to reduce the losses as higher frequencies yield in many advantages such as reduction in converter size. This paper describes systematic design of 1.5 kW high power factor bridgeless interleaved boost converter fed on-board battery charger for EVs. Phase shifted full bridge converter having zero voltage switching (ZVS) up to 50% of the rated load is integrated with the high power factor AC/DC stage. The detailed design methodology of PFC controller, and phase shifted full bridgeless converter for EV is given in this paper. To validate the design of power stage and controller, PSIM simulation has been carried out and results are provided. Results show that power factor is greater than 0.99 and THD is less than 2 % at full load which is under the IEC standard.**

Keywords—Interleaved bridgeless (ILBL) Boost type PFC, phase shifted full bridge (PSFB) converter, zero voltage switching (ZVS).

I. INTRODUCTION

Efficiency, high power factor and fast charging are the desired qualities for a utility fed on-board EV charger. Boost converter is normally preferred for PFC applications because it can draw continuous current and also allows wide input voltage variations. For front end AC-DC converter, diode bridge rectifier with conventional PFC using boost converter can be used only up to 1 kW due to less power handling capacity and power loss in diode bridge rectifier.

Interleaved bridgeless (ILBL) PFC converter can be used for higher power ratings. Interleaving can be done in bridgeless topology to reduce input current ripple and switch stresses. Different PFC topologies are explained in the literature [1], [6]. For EV chargers, usually phase shifted full bridge (PSFB) converter is used as the DC-DC converter stage. PSFB converter provides isolation between source and battery. It uses leakage inductance of isolation transformer and parasitic capacitance of switch to achieve ZVS [5]. Various isolated, non-isolated, one stage and two stage battery charger topologies are discussed in [7] – [10]. However, a detailed design procedure for controller part and the power stage part is not properly addressed in many literatures.

As a solution to the aforementioned problem, this paper discusses detailed and systematic design procedure of controller for PFC stage and design of PSFB converter for a 1.5 kW on-board battery charger. To handle the high power with high efficiency, interleaved bridgeless boost converter is used for PFC stage. The block diagram of the scheme is depicted in Fig. 1. Here the output of PFC stage is powering a DC link capacitor of voltage V_{dc} . To regulate the output voltage (V_{dc}) from the PFC stage, voltage controller is designed. Average current control technique is used to design voltage control loop and current control loop of PFC [2]-[3]. The following sections discuss the PFC stage, controller design, PSFB converter design and simulation results.

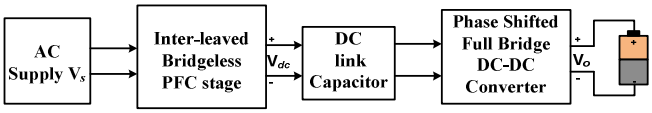

Fig.1. Block diagram of ILBL PFC fed On-board battery charger

II. TOPOLOGY

A. PFC Stage

An interleaved two channel bridgeless boost converter is designed for the front-end PFC stage. To regulate the output voltage and to improve the input power factor, outer voltage and inner current loops are essential. Average current controller is used to achieve PFC. Voltage control loop is a slow acting pre-regulator that maintains output voltage at reference value. Current control loop is fast acting and it shapes inductor currents to be sinusoidal and in phase with input rectified line voltage. The interleaved bridgeless (ILBL) boost type PFC front end stage along with controller is shown in Fig. 2. Output voltage of PFC stage V_{dc} is compared with reference voltage $V_{dc(ref)}$. The error signal is passed through a low pass filter and the output of filter is multiplied with a unit magnitude rectified sinusoidal signal synchronized with input line voltage. The resultant signal is compared with inductor current and error signal is given to pulse width modulator, which is a PWM controller. PWM signals are phase shifted for interleaved operation and given to the switches to ensure that inductor current is in phase with rectified line voltage. ILBL PFC topology uses switches and their body diodes to perform rectification. This topology operates with either duty ratio $D > 0.5$ or $D < 0.5$ depending on whether input voltage is less than or greater than half of

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output voltage. Working of the ILBL PFC topology is explained in [1]. Interleaving is provided by giving 180° phase shift between the carrier ramp signals of PWM controllers of switches SW_1/SW_3 and SW_2/SW_4. Two current loops are provided for two inductors L_1 and L_2. During operation, L_1 and L_3 are in series. Similarly, L_2 and L_4 are in series. For equal load sharing between converter channels, the resultant current reference output of voltage controller is halved and given as a reference for each current controller.

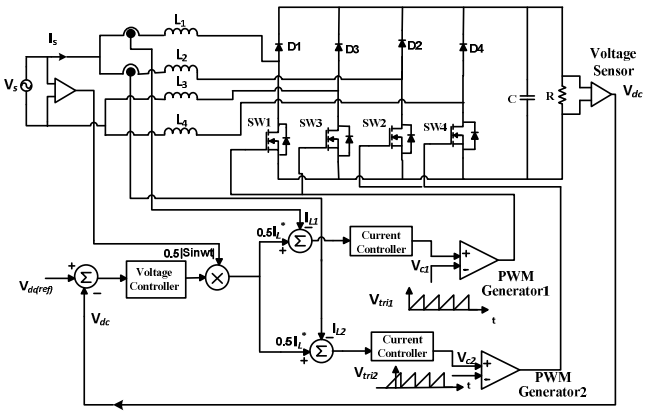

Fig.2. Interleaved bridgeless (ILBL) boost PFC converter with controller

B. Phase Shifted Full Bridge DC to DC stage

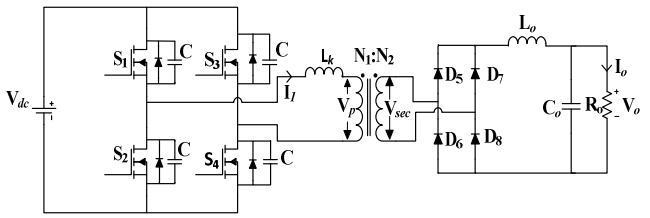

Fig.3. Circuit diagram of PSFB converter.

In PSFB Converter [5], switches operate with 50% duty, but there is a phase shift provided between two legs of converter (leading leg: S_1/S_2 and lagging leg: S_3/S_4). This phase shift determines voltage gain and helps in achieving ZVS. The parasitic capacitance of switch is discharged before it is turned on. Dead time is provided between the switching pulses given to two switches in a leg in order to provide enough time for parasitic capacitance to charge/discharge. Discharge/charge of leading leg capacitors occurs due to energy transfer with leakage inductance L_k and filter inductance L_o reflected to primary. Since L_o is high, charge/discharge of leading leg capacitors occurs almost linearly. But for lagging leg capacitors, charge/discharge occurs due to energy transfer with leakage inductance. Working of PSFB converter is explained in detail in [5].

The voltage gain of the converter is affected by duty cycle loss. There are two reasons for duty cycle loss in PSFB converter. One is due to the dead time between switches of one leg and other is due to ΔD which occurs when the primary current reverses. This reversal makes all four diodes (D_5-D_8) conduct on the secondary side to make up for the deficit primary current, thus making secondary voltage zero. Effective duty ratio (D_e) is given by

$$D_e = D - \mu - \Delta D \quad (1)$$

Where μ is duty cycle loss due to dead time.

III. Controller Design

Small signal modeling of the converter is essential to properly design the controllers. Parameters of the controllers are obtained from the desired dynamic performance, specifications and objectives [2],[3]. The power stage of Interleaved bridgeless (ILBL) is very similar to the conventional boost converter. Hence only one channel of the converter is modelled. In Fig. 4, linearized model of boost converter about a steady state point is depicted. $\widetilde{v_s}(s)$, $\widetilde{\iota_L}(s)$, $\tilde{d}(s)$, $\widetilde{V_{dc}}(s)$ represents small perturbations in V_s, I_L, D and V_{dc} respectively.

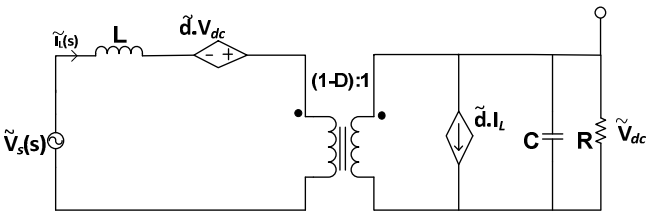

Fig.4. Small signal model of the front end stage.

Transfer function of the front end power stage at high frequency is obtained as:

$$\frac{I_L(s)}{d(s)} = \frac{V_{dc}}{sL} \quad (2)$$

Where $L = (L_1 + L_3) = (L_2 + L_4)$

A. Design of Current Control Loop [3]

The schematic of the inner current loop of PFC stage is given in Fig. 5. Specifications and objectives for the design of current control loop are as follows:

- Switching frequency of power converter f_{sw} = 100 kHz
- Bandwidth of current control loop f_{BW} = 10 kHz
- Phase margin PM = 60° (High PM makes the system settle quickly without oscillations)
- Output voltage of PFC stage V_{dc} = 450 V
- Phase margin should not be less than -180° for frequencies below gain cross over frequency f_{BW}.

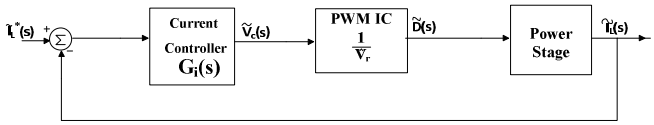

Fig.5. Schematic of current control loop.

Reference (I_L^*) for inner current control loop is obtained from outer voltage control loop. Current Controller output $v_c(t)$ is compared with a saw tooth carrier signal with amplitude V_r (= 1) and duty cycle pulses D(t) are generated. Transfer function of PWM controller is given as follows:

$$\frac{\tilde{D}(s)}{v_c(s)} = \frac{1}{V_r} \quad (3)$$

In order to provide a PM of 60° the transfer function of current controller is selected as follows:

$$G_i(s) = \frac{k_i}{s}\frac{1+\frac{s}{w_1}}{1+\frac{s}{w_2}} \quad (4)$$

Current controller $G_i(s)$ has maximum phase at frequency equal to geometric mean of w_1 and w_2. So w_1 and w_2 are

designed such that their geometric mean is gain cross over frequency and lead-lag portion (i.e. $\frac{1+\frac{s}{w_1}}{1+\frac{s}{w_2}}$) of $G_i(s)$ provides 60° phase boost.

$$\sqrt{w_1 w_2} = 2\pi f_{BW} \quad (5)$$

$$\tan^{-1}\frac{w_2}{w_1} = 60° \quad (6)$$

Solving (5) and (6) we can find w_1 and w_2.

Magnitude of current control loop transfer function should be equal to one at gain cross over frequency. By solving equation (7) we can find k_i.

$$\left|G_i(s).\frac{1}{V_r}.\frac{V_{dc}}{sL}\right|_{f_{BW}} = 1 \quad (7)$$

After designing current control loop, bode plot of lead-lag portion of current controller and loop transfer function are plotted in fig.6 and fig.7 respectively. From fig.6, we can say that $G_i(s)$ provides a phase boost of 60°.

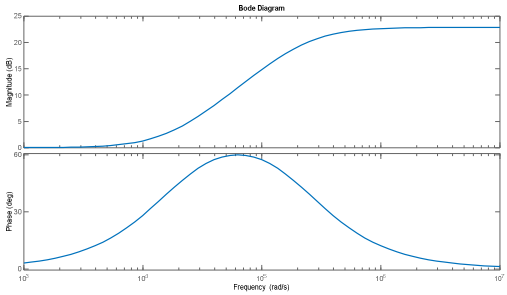

Fig.6. Bode plot of lead-lag portion of current controller transfer function showing 60° phase boost

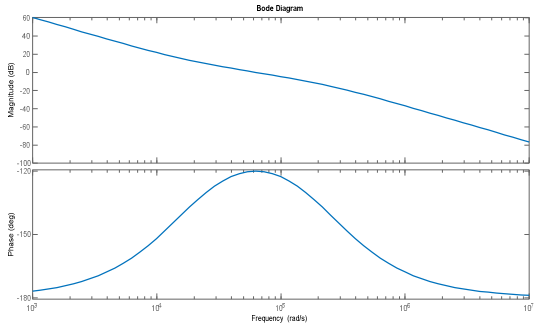

Fig.7. Bode plot of current control loop

B. *Design of Voltage Control Loop* [3]

The simplified schematic of voltage controller is given in Fig. 8. Main specification of this loop is as follows:

- Limit the effect of second harmonic component of output voltage (V_{dc2}) and other lower harmonics on voltage controller output to less than 1.5 % of rated current.
- Band width of voltage control loop $f_{BW}^{'} = 15\ Hz$ helps in achieving first objective.

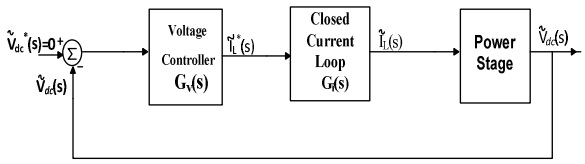

Fig.8. Schematic of voltage control loop

The transfer function of voltage controller is selected in the form of a low pass filter as follows:

$$G_v(s) = \frac{\tilde{I}_L(s)}{\tilde{V}_{dc}(s)} = \frac{k_v}{1+\frac{s}{w_{cv}}} \quad (8)$$

Derivation for transfer function of power stage is explained in [3] and it is as follows:

$$\frac{\tilde{v}_{dc}(s)}{\tilde{\imath}_L(s)} = 0.5\frac{V_{s(peak)}}{V_{dc}}.\frac{0.5R}{1+0.5RCs} \quad (9)$$

As current control loop is fast acting, its effect on voltage control loop can be neglected.

$$\frac{\tilde{I}_L(s)}{\tilde{I}_L^*(s)} \cong 1 \quad (10)$$

At gain cross over frequency, magnitude of voltage control loop transfer function should be equal to 1.

$$\left|\frac{k_v}{1+\frac{s}{w_{cv}}}.0.5.\frac{V_{s(peak)}}{V_{dc}}.\frac{0.5R}{1+0.5RCs}\right| = 1 \quad (11)$$

To meet the first objective following equation must be satisfied:

$$I_{L2} = \left|\frac{k_v}{1+\frac{s}{w_{cv}}}\right|.V_{dc2} < 0.015.I_L \quad (12)$$

Here I_{L2} is the output of voltage controller for second harmonic voltage input V_{dc2} $(=\frac{V_{s(peak)}.\ I_{L(peak)}}{4wCV_{dc}})$. By solving equations (11) and (12) we can find k_v and w_{cv}.

IV. Design of DC-DC Stage

Modelling, analysis, and design of PSFB converter is described in [4]. The phase shift is decided based on duty cycle and losses in it. Typical duty cycle under rated input and output conditions is given as:

$$D = \left(\frac{V_o + 2V_{D(ON)}}{V_{dc} - 2V_{SW(ON)}}\right) \times \frac{N_1}{N_2} \quad (13)$$

Where, $V_{D(ON)}$ and $V_{SW(ON)}$ are ON state voltage drops of diode and switch respectively.

Duty cycle loss ΔD is given as $\Delta D = \frac{I_1+I_2}{\frac{V_{dc}T}{2L_k}}$ (14)

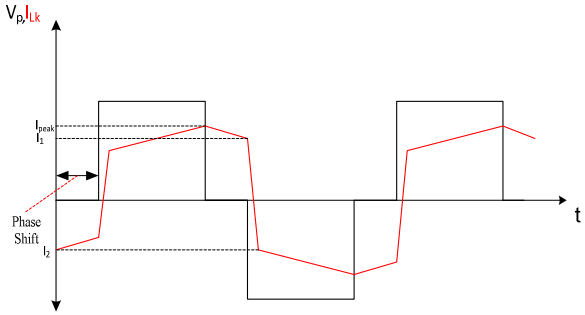

Fig.9. Waveforms of transformer primary voltage and primary current.

The primary side leakage inductance current and voltage of primary winding is shown in Fig.9. The current at which charging and discharging of lagging leg switches occur is given by

$$I_1 = \frac{N_2}{N_1}\left(I_o + \frac{\Delta I_L}{2} - \frac{V_o}{L_o}(1-D)\frac{1}{2f}\right) \quad (15)$$

Where f is the switching frequency and ΔI_L is the ripple current of filter inductor of PSFB converter. To achieve ZVS up to 50% of load condition ($0.5I_O$), I_1 is calculated using (14) and transformer leakage inductance (L_k) is selected so that energy stored in it is more than energy stored in parasitic capacitance under same load condition.

$$L_k > 2\, C_{o_{Avg(eff)}} \times \frac{V_{dc}^2}{I_1^2} \quad (16)$$

Here $C_{o_{Avg(eff)}}$ is the average effective capacitance of the switch.

Dead time is provided between the switches of a leg to avoid shoot through and to allow switch capacitors to charge/discharge is given by [4].

$$T_d > \frac{\pi}{2}\sqrt{L_k\, 2\, C_{o_{Avg(eff)}}} \quad (17)$$

Filter inductance and filter capacitance are calculated by selecting current ripple (ΔI_L) and voltage ripple (ΔV_O) respectively.

$$L_o = \frac{V_o(1-D)}{\Delta I_L\, 2\, f} \quad (18)$$

$$C_o = \frac{I_o\, D}{\Delta V_o\, 2\, f} \quad (19)$$

V. Simulation Results

To validate the design and controller performance, a 1.5kW on-board battery charging system is designed. The parameters of the system are given in Table. 1. The simulation is done using PSIM circuit simulator. The simulation schematic of the complete system is shown in Fig. 10. The simulation result of source voltage and source current waveforms are given in Fig.11. Here, the designed controller is able to shape the input current and obtain high power factor which is found to be more than 0.99. For input current waveform, THD is obtained as 2% which is satisfying the IEC Standards. Voltage control loop accurately tracks the DC Link voltage and regulates the output voltage to 450 V as shown in Fig. 12.

TABLE.I SIMULATION PARAMETERS

Parameter	Value
Power	1.5 kW
Input Voltage, V_S	230 V (RMS)
Switching Frequency, f	100 kHz
DC Link Voltage, V_{dc}	450 V
$L_1 = L_2 = L_3 = L_4$	1 mH
DC Link Capacitor, C	1.2 mF
Transformer Turns Ratio, N_1:N_2	7:3
Leakage Inductance, L_k	30 µH
Filter Inductor, L_O	1.5 mH
Filter Capacitor, C_O	220 µF
PSFB output voltage	100 V

The output voltage of PSFB converter is regulated to 100V, as shown in Fig. 13. The phase shifted primary and secondary side voltage of high frequency transformer is shown in Fig. 14. Voltages across and current through leading and lagging leg switches are obtained for rated load and half load conditions respectively in Fig.15 and Fig.16. The simulated result shows that ZVS is successfully achieved for power ratings greater than 750 W.

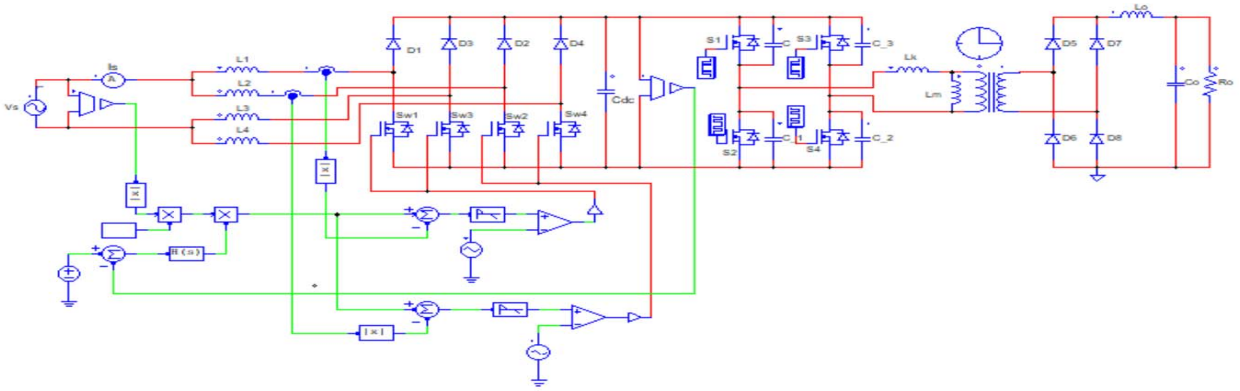

Fig.10. PSIM Simulation diagram of the on-board charger.

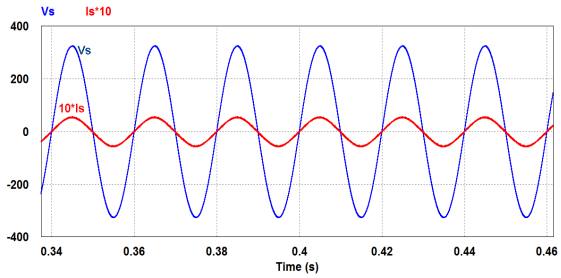

Fig.11. Source Voltage and Current with high power factor

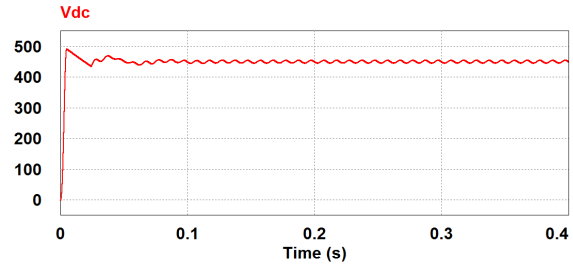

Fig.12. Regulated DC Link Voltage V_{dc}

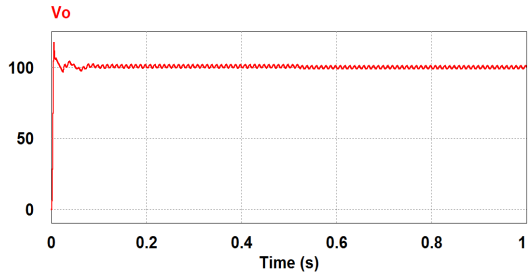

Fig.13. Output Voltage of PSFB converter V_o

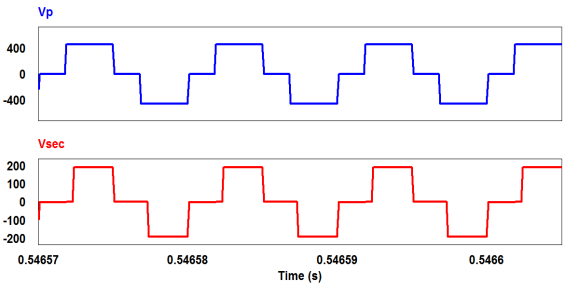

Fig.14. Primary and Secondary Voltages of Isolation Transformer

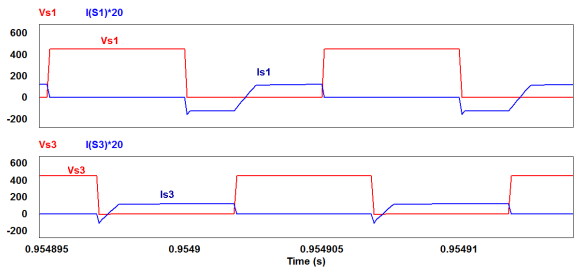

Fig.15. ZVS in Switches S_1 & S_3 under Full Load Condition

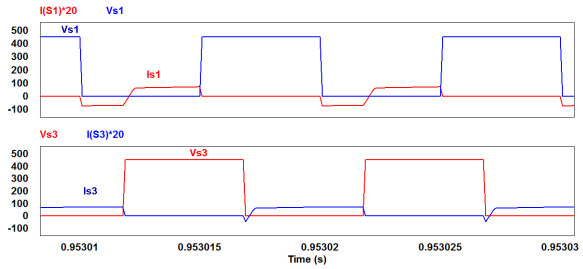

Fig.16. ZVS in Switches S_1 & S_3 under Half Load Condition

VI. Conclusion

Design of On-board battery charger, which consists of ILBL type PFC and PSFB converter is described in this paper. Voltage and current control loop design of PFC stage is elaborated with design equations. Design of PSFB converter is also explained for achieving ZVS with design equations. ZVS is achieved for all the switches in PSFB converter. Input power factor is obtained very close to unity. Simulation results are presented with schematics and graphs. This topology reduces switching losses, increases input power factor and can be used for high power ratings.

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