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Rohan Shah

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Fremont, CA/Champaign, IL

Education

University of Illinois at Urbana-Champaign — Champaign, IL
B.S. in Computer Engineering, GPA: 3.7/4.0 — *Est. Grad - Dec. 2026*

- **Coursework**: Data Structures & Algorithms, Digital Systems Lab, Computer Systems & Programming, Probability with Engr. Applications, Discrete Math, Intro to Circuits & Electronics

Work Experience

Siemens — Palo Alto, CA
Incoming FPGA Engineer Intern — *May 2025 – Aug 2025*

Varian — Palo Alto, CA
Software Automation Intern — *May 2024 – Aug 2024*

- Designed and deployed a **Tkinter**-based **Python** application leveraging **Pandas** and **OpenPyXL** to parse and transform PDF exports from database exports, delivering an intuitive **GUI** to eliminate **1,000+** hours of labor.
- Engineered a metadata-mapping pipeline to index, normalize and reconcile **4+ years** of legacy design documentation—over **1,000 files**—enabling audit readiness and data-driven decision support.
- Automated SBOM validation in Python—processing **100+ components** per run and embedding updates for **5+** cybersecurity regulations—to bolster compliance scores, reduce audit cycle times, and boost software security.

BioSensors Laboratory — University of Illinois — Champaign, IL
Research Assistant — *Jan 2024 – Jan 2025*

- **Co-authored a paper** with Dr. Viktor Gruev and **5 + PhD students** on novel in-vivo microscopic cancer imaging protocols, enhancing cellular contrast and improving diagnostic accuracy across diverse samples.
- Engineered a precision camera mount in Fusion 360, achieving stable outputs, increasing image resolution by **20%**.
- Prototyped and validated multiple 3D-printed components to streamline equipment assembly and data collection, saving over **100 R&D hours** and accelerating project milestones.

The Jay Koo Academy — Saratoga, CA
Research and Development Intern — *May 2023 – Aug 2023*

- **Led** the prototyping and user testing of a modular **digital SAT platform**, coordinating with 10 top-university contributors to refine accessibility, resulting in a deployment to over **1,500 students**.
- Authored and curated a library of **1,000+** tiered Mathematics and English questions in **LaTeX**—leveraging user-accuracy to enable adaptive, performance-based scaling and reduce content production time by **40%**.
- Developed and executed comprehensive **QA protocols**—including unit tests and integration checks, **saving 100+ hours** to ensure software functionality

Projects

- **FPGA Based Game - Jetpack Joyride**: Devised and implemented an interactive FPGA-based game on a **Xilinx Spartan-7** using SystemVerilog, leveraging BRAM, frame buffers, and VGA for dynamic on-screen graphics; integrated a **MicroBlaze** soft-core to manage **SPI/UART** peripherals for real-time input, state, and game logic.
- **Self-Guiding Autonomous Rover**: Modeled the rover chassis in SOLIDWORKS; programmed **Arduino** in C to interface with u**ltrasonic and IR sensors** for real-time obstacle detection, path planning, and motor control to achieve fully **autonomous** navigation.
- **FIRST Tech Challenge**: Outlined robot designs in Fusion360 and managed code in **Git**; developed Java control software integrating actuators and wiring, and implemented TensorFlow-based **image detection** for autonomous tasks. Coordinated outreach, arranged field tests and competition runs, conducting post-run analyses to drive iterative design improvements.

Skills

Languages: Python, C++, C, SystemVerilog, VHDL (Summer 2025), SQLite

Technologies: Xilinx Vivado, Vitis, MicroBlaze SoC, SDLC, Object-Oriented Programming,

Libraries and Tools: Communication Protocols: UART, SPI; NumPy, pandas, matplotlib, Tabula, OpenPyXL, Tkinter, Microsoft Office, Adobe Creative Cloud, Docker, Git; CAD: Autodesk Fusion 360, SOLIDWORKS

Honors & Awards: Siemens STEM Scholar, Presidential Volunteer Service Award - Gold, California State Honor Seal