|  |  |  |  |
| --- | --- | --- | --- |
| **SR.NO.** | **DATE** | **LIST OF EXPERIMENTS** | **GRADES/MARKING** |
| 1. | 6th OCT,2020 | PARKING INDICATOR |  |
| 2. | 13th  OCT,2020 | OCTAL DECODER |  |
| 3. | 20th  OCT,2020 | MAGNITUDE COMPARATOR |  |
| 4. | 3rd  NOV,2020 | HALF ADDER |  |
| 5. | 11th  NOV,2020 | FULL ADDER |  |
| 6. | 17th  NOV,2020 | 7 SEGMENTS |  |
| 7. | 24th  NOV,2020 | SHIFT REGISTER |  |
| 8. | 1st  DEC,2020 | COUNTERS |  |
| 9. | 15th  DEC,2020 | CROSSWALK CONTROLLER |  |

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F2020 EECE 8005 ESD PROGRAM

LAB #11. CROSSWALK CONTROLLER

15th DECEMBER 2020, 8:00AM to 10:00AM

PATEL, ROHAN

Date: 15th December 2020

LAB 11. CROSSWALK COUNTER

**OBJECTIVE:** Design a Crosswalk Controller in Quartus with VHDL and Verilog code and observe the output on DE1-SOC Board.

**1.) VHDL**

**CODE:**

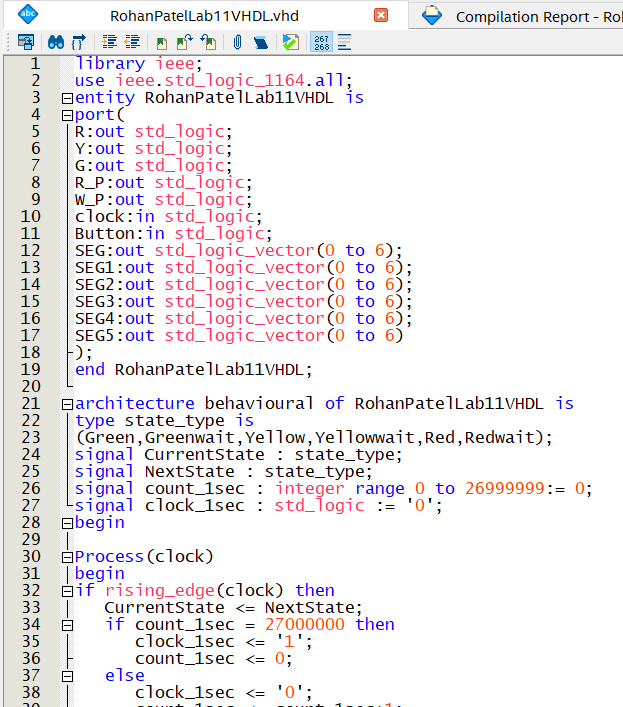


Figure 1 Crosswalk counter VHDL Code

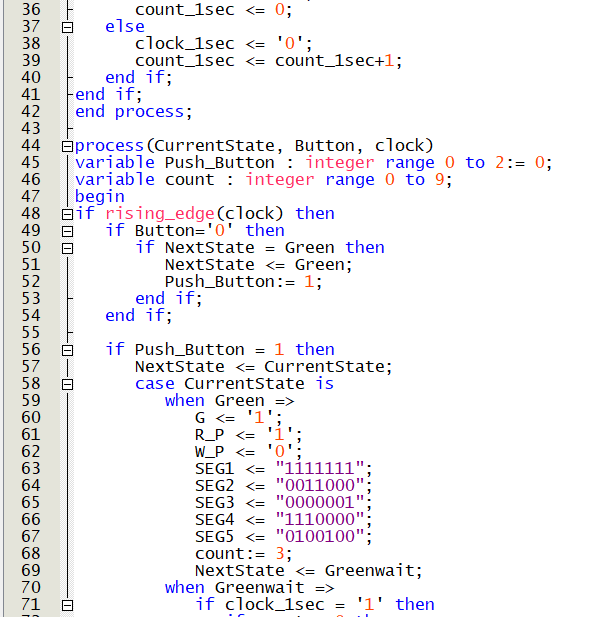


Figure 2 Crosswalk counter VHDL Code

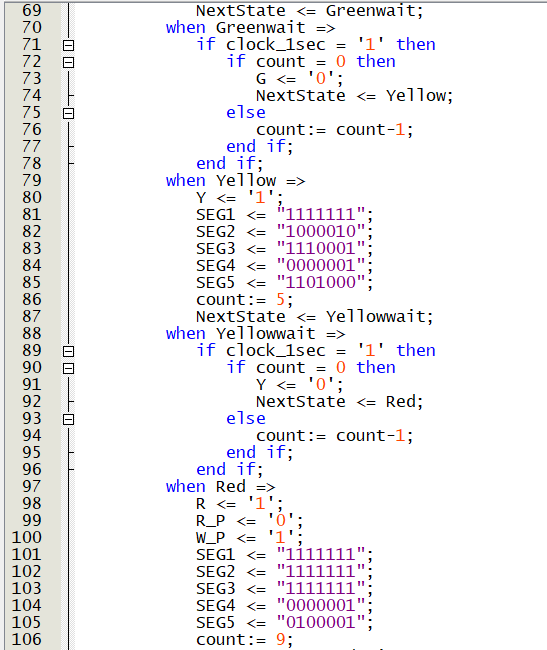


Figure 3 Crosswalk counter VHDL Code

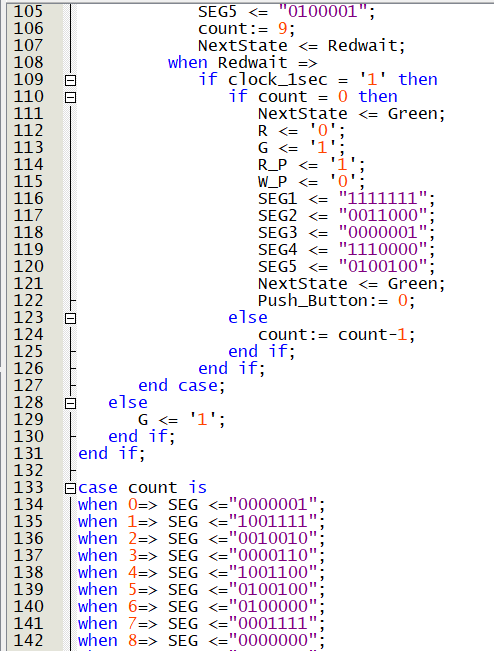


Figure 4 Crosswalk counter VHDL Code

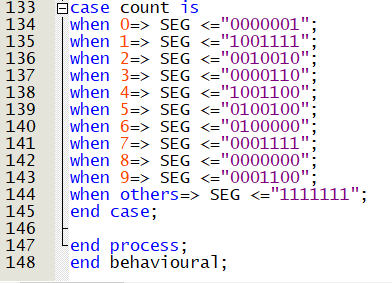


Figure 5 Crosswalk counter VHDL Code

**COMPILATION REPORT:**

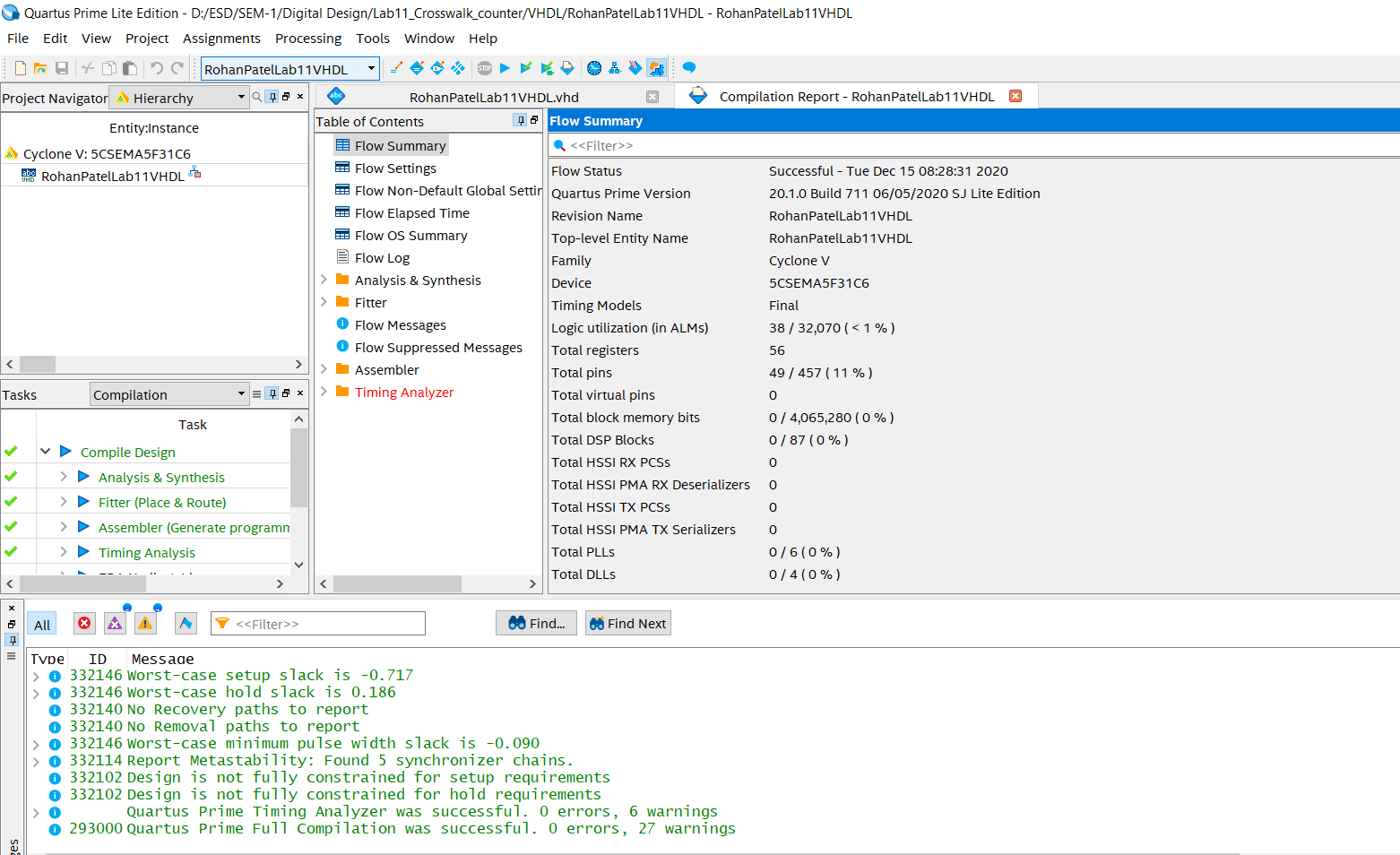


Figure 6 Compilation Report

**PIN PLANNER:**

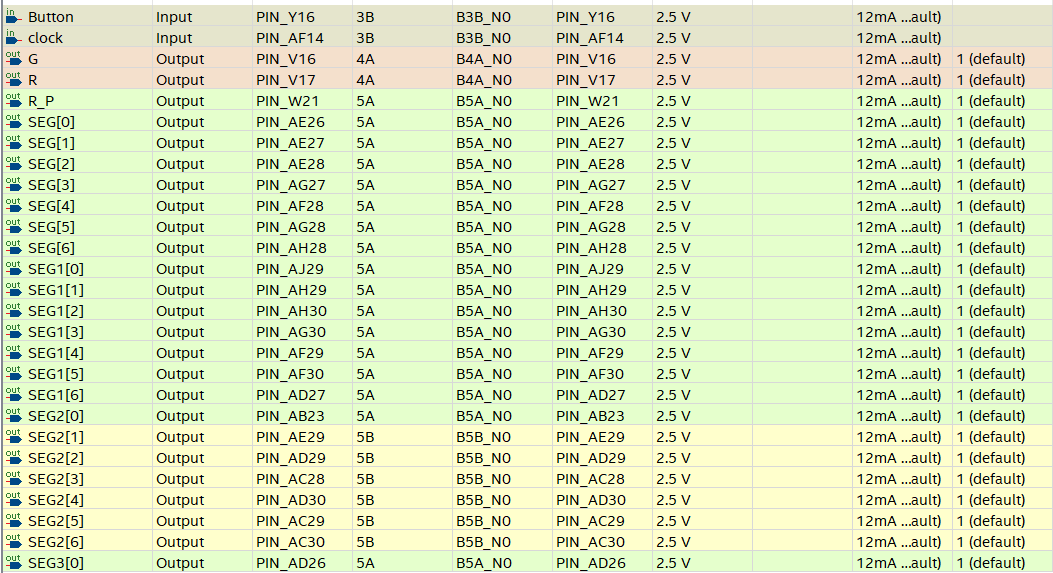


Figure 7 Pin Planner

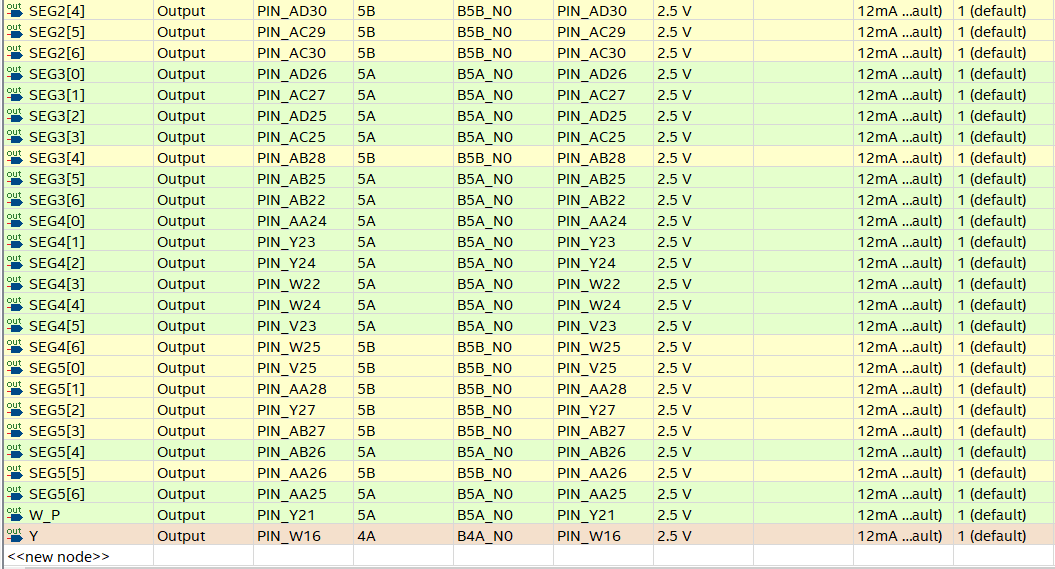


Figure 8 Pin Planner

**LOADED:**

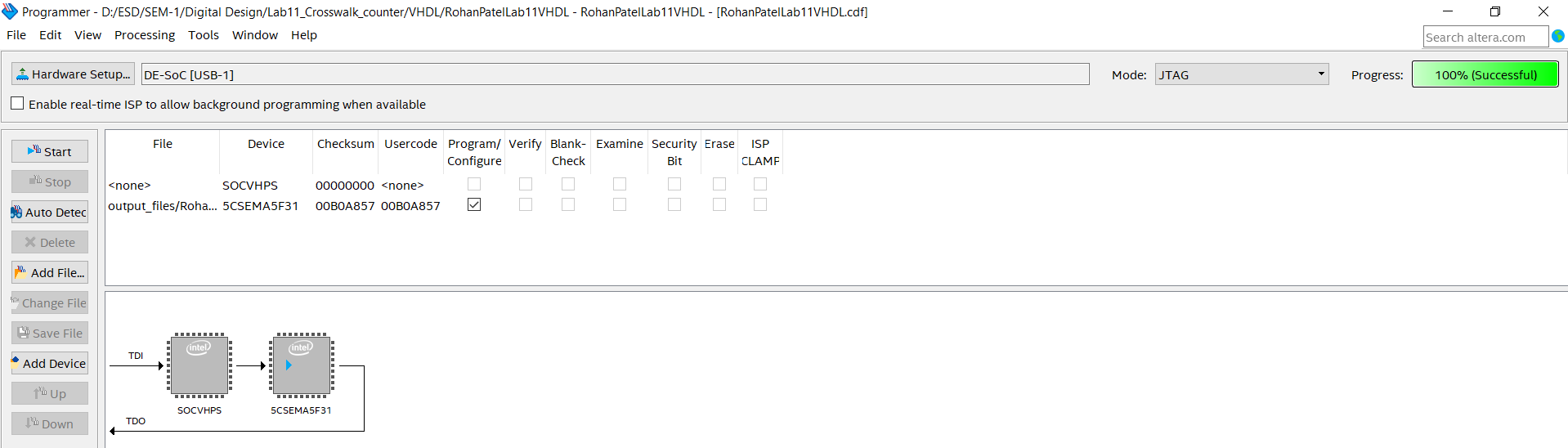


Figure 9 Loaded on Board

**OUTPUT:**

1.)

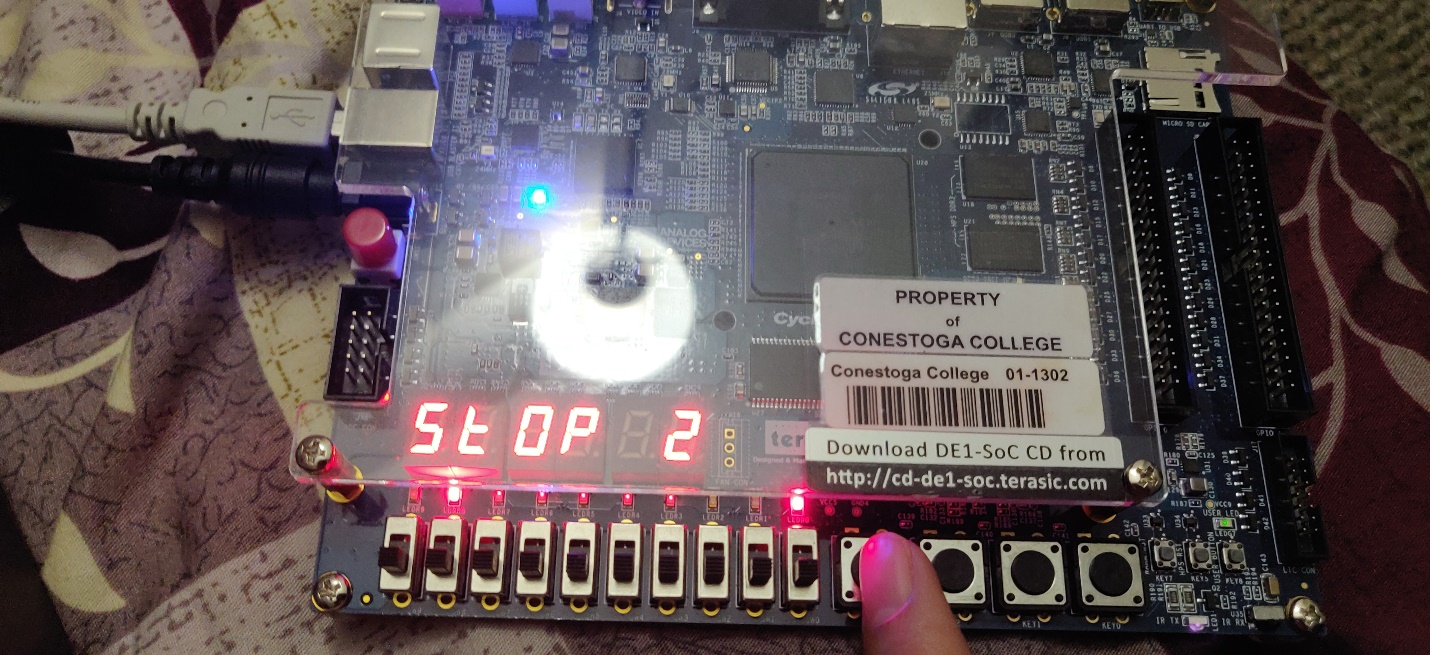


Figure 10 Output

2.)

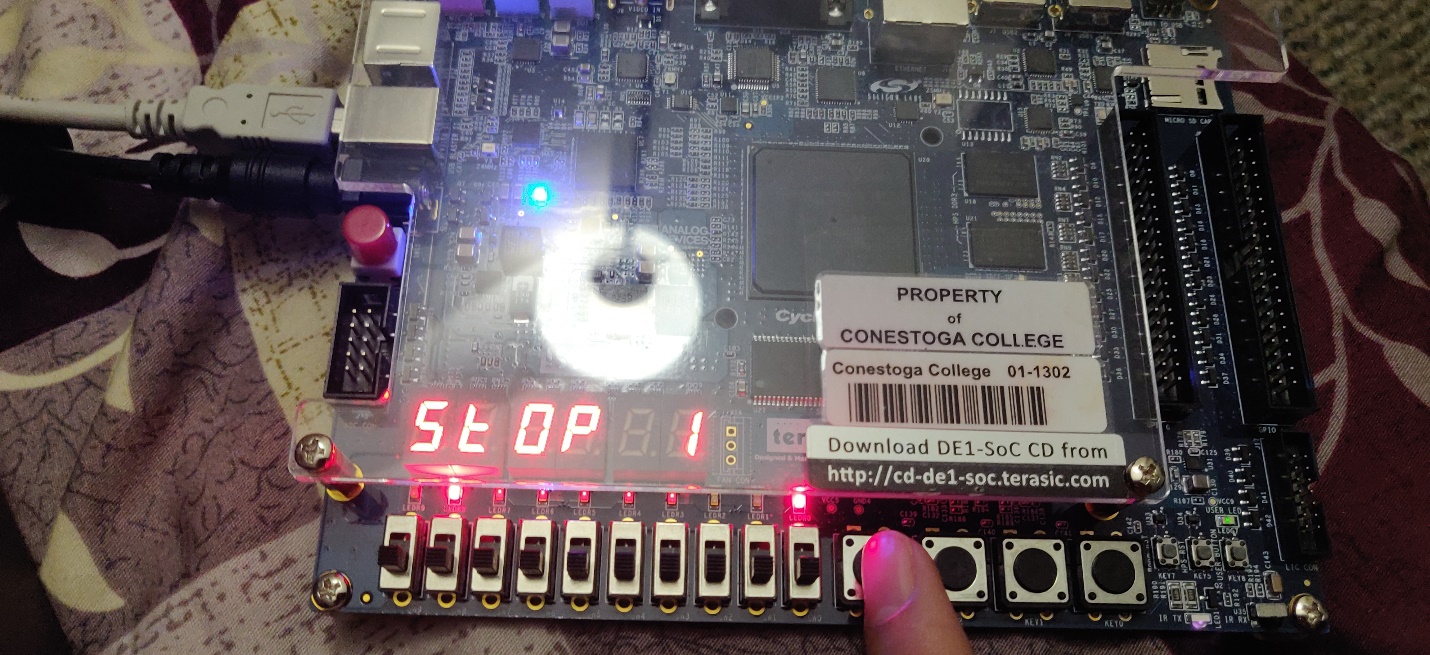


Figure 11 Output

3.)



Figure 12 Output

4.)



Figure 13 Output

5.)

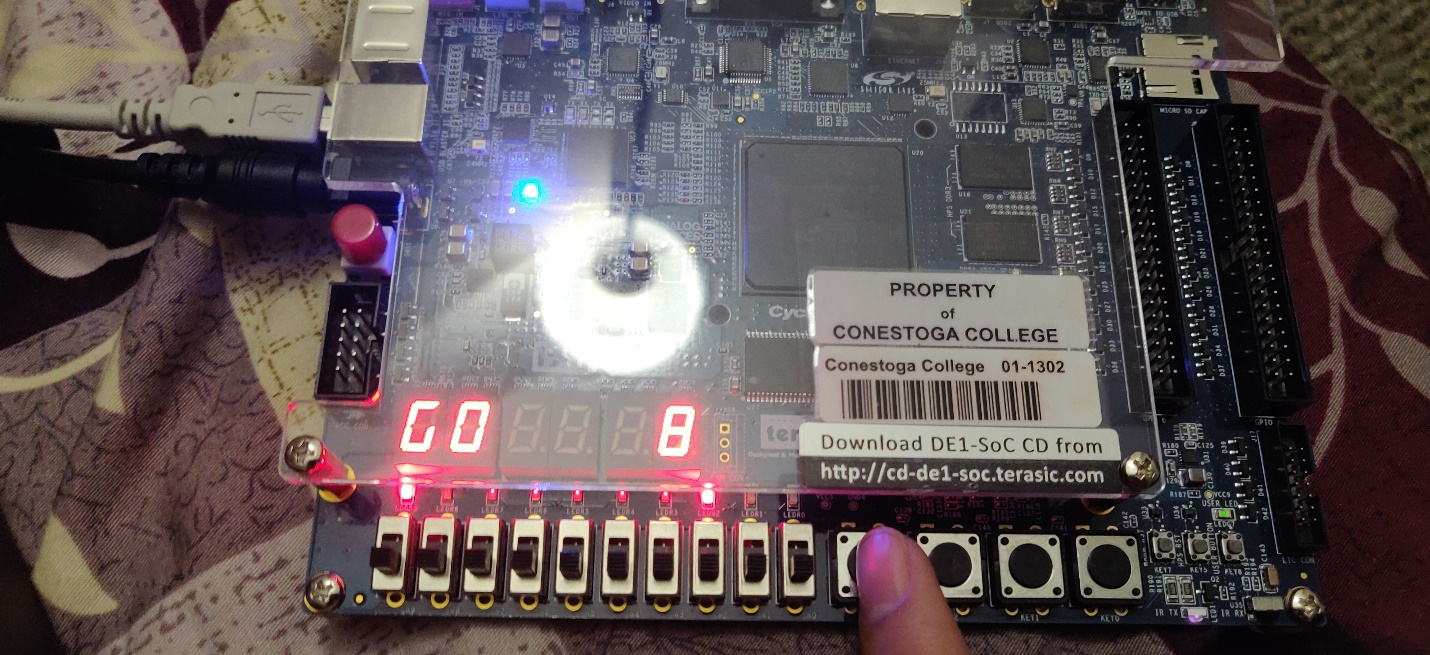


Figure 14 Output

6.)

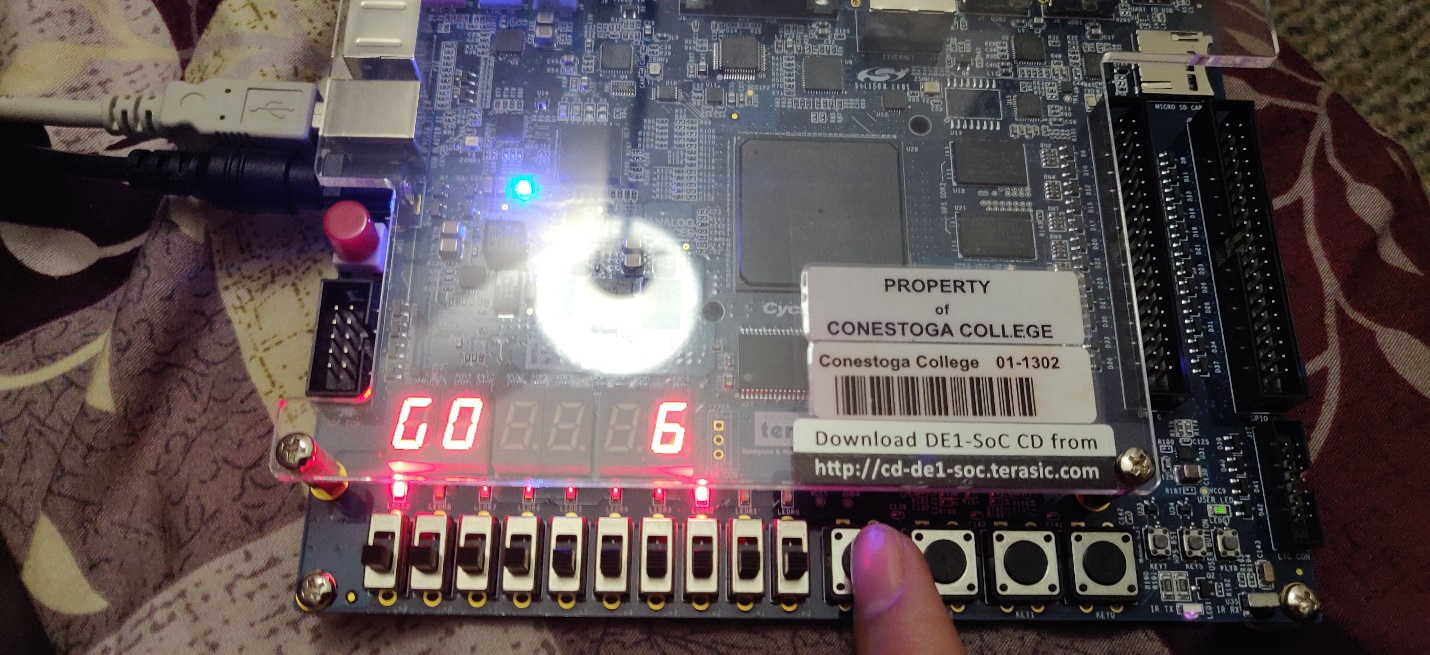


Figure 15 Output