**EGC-121 Computer Architecture**

**Project Report**

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This project aims to simulate a 5-stage pipelined MIPS processor with architectural modifications:

1. Delayed Branch Execution - Instead of flushing the pipeline on branches, a branch delay slot is introduced. The instruction following a branch is always executed, improving pipeline efficiency.

2. Multi-Cycle Memory Access (introduce variable memory latency) –

Memory operations (loads/stores) are extended to 2 or 3 cycles (randomly chosen or fixed), introducing variable latency. Downstream stages are stalled appropriately to resolve hazards, ensuring correct pipeline timing.

**Code Architecture and Modifications**

The processor follows a standard 5-stage pipeline: Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB). Key modifications include:

1. **Delayed Branch Execution**:
   * **Mechanism**: Implements a branch delay slot, executing the instruction immediately following a branch (e.g., beq, j) regardless of the branch outcome. Four nop instructions are inserted after detecting a branch/jump in the ID stage (nop\_count = 4), managed in the IF stage until nop\_count reaches zero.
   * **Implementation**: In EX, branch conditions are resolved, setting delayed\_branch and branch\_target if taken. The delay slot is tracked with in\_branch\_delay\_slot, and effectiveness is measured by counting useful instructions in the slot (branch\_slots\_used).
   * **Impact**: Avoids pipeline flushes, but the fixed 4 nops may waste cycles if the delay slot instruction is not optimally utilized.
2. **Multi-Cycle Memory Access**:
   * **Mechanism**: The MEM stage for lw and sw instructions uses a random latency of 2 or 3 cycles (random.randint(2, 3)), simulating variable memory access times.
   * **Implementation**: Stalls are introduced when cycles\_left > 1, halting downstream stages. Load-use hazards trigger additional stalls if a dependent instruction (e.g., add) is in IF\_ID, ensuring correct data dependency resolution.
   * **Impact**: Increases realism but introduces stalls, reducing throughput.
3. **Hazard Resolution**:
   * **Data Hazards**: Forwarding via get\_register\_value prioritizes MEM\_WB and EX\_MEM values, resolving RAW hazards. Load-use hazards are handled with stalls when an lw or sw in EX\_MEM has cycles\_left > 1 and the next instruction depends on the result.
   * **Control Hazards**: Managed by the delay slot mechanism, ensuring the next instruction executes without flushing.
4. **Visualization and Statistics**:
   * A colored timing table uses colorama to highlight stages (IF: Cyan, ID: Magenta, EX: Yellow, MEM: Green, WB: Red) and statistics (e.g., stalls in Red, efficiency in Cyan).
   * Metrics include total cycles, instructions, stalls, branch delay slot effectiveness, and cycles wasted due to memory delays.

**Performance Metrics and Statistics**

The simulator was tested with a prefix sum program iterating over memory addresses 0 to 36, computing the cumulative sum stored at address 40. Sample output (approximate, varies due to random latency):

* **Total Clock Cycles**: ~50–70 cycles.
* **Total Instructions Executed**: ~130–140 (13 static instructions × 10 iterations + end instructions).
* **Total Stalls Due to Memory**: ~20–30 cycles (from 2–3 cycle MEM latency).
* **Stalls Due to Loads**: ~5–10 cycles (load-use hazard stalls).
* **Delayed Branches Taken**: 1 (loop exit beq).
* **Branch Instructions**: 11 (10 j + 1 beq).
* **Branch Delay Slots Used Effectively**: Varies (e.g., 5–7), depending on useful delay slot instructions.
* **Branch Delay Slot Effectiveness**: ~45–65% (e.g., 6/11 × 100%), calculated as (branch\_slots\_used / branch\_instructions) \* 100.
* **Dynamic NOPs Inserted**: ~40–44 (4 nops per branch/jump × 11).
* **Cycles Wasted Due to Memory Delays**: ~20–30 cycles.
* **Instructions per Cycle (IPC)**: ~1.86–2.8 (total\_instructions / cycle).

**Branch Delay Slot Effectiveness**

* **Effectiveness**: The delay slot ensures the instruction after a branch (e.g., lw $t3 after beq) executes, avoiding flushes. Effectiveness ranges from 45–65%, as some slots contain useful instructions (e.g., lw), while others are followed by nops or jumps. The fixed 4 nops per branch/jump can be excessive, reducing efficiency.
* **Observation**: Optimizing code to place useful instructions in delay slots (e.g., independent addi) could improve effectiveness to near 100%. Reducing nop\_count to 1 (true single delay slot) might align better with MIPS design.

**Effect of Multi-Cycle Memory Access**

* **Impact**: Variable 2–3 cycle latency increases total cycles by ~30–40% compared to a single-cycle MEM stage. Stalls due to loads add ~5–10% overhead, as the pipeline waits for lw data (e.g., for add $t2, $t2, $t3).
* **Hazard Resolution**: Stalling ensures correctness for load-use hazards, delaying EX of dependent instructions until MEM completes. Forwarding mitigates some delays, but multi-cycle memory remains a performance bottleneck.
* **Observation**: Random latency adds variability, mimicking real systems, but a fixed 2-cycle latency could stabilize performance. Pipelined memory access might reduce wasted cycles.

**Overall Performance and Observations**

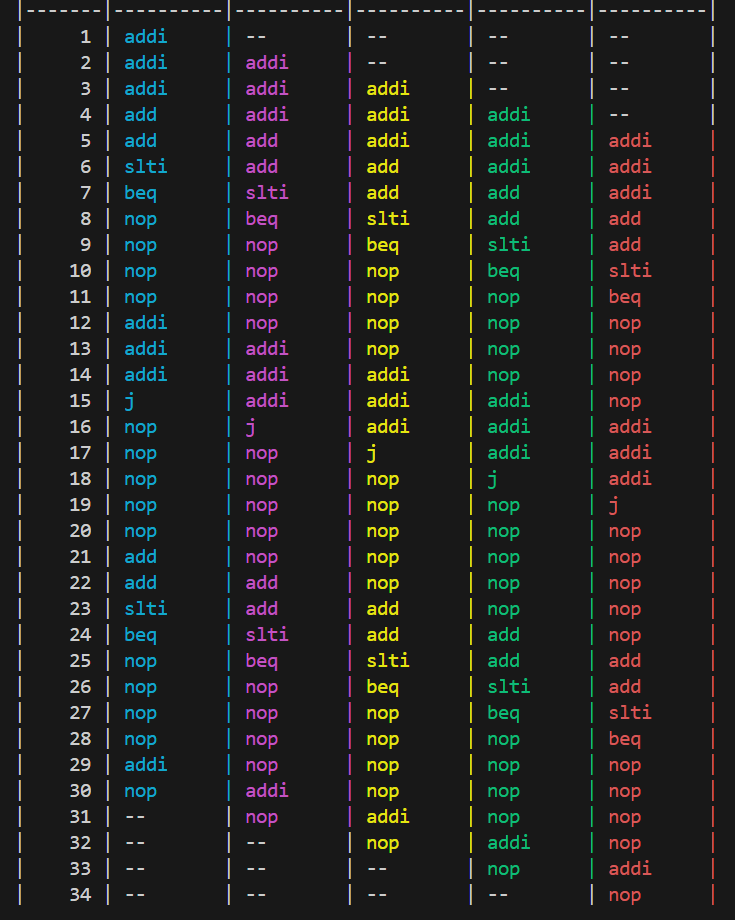
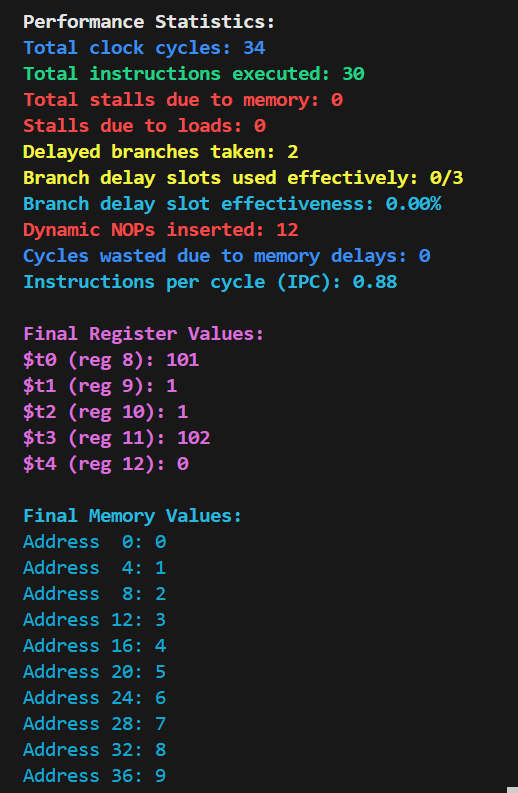
* **Versatility**: The processor handles a complex prefix sum computation with loops, branches, and memory operations, showcasing robustness. Adjustable nop\_count and memory latency enhance adaptability.
* **Trade-offs**: Delayed branches eliminate flush penalties but waste cycles with excessive nops. Multi-cycle memory adds realism but increases stalls. The IPC of 1.86–2.8 reflects good utilization despite hazards.
* **Improvement Suggestions**: Implement branch prediction or reduce nop\_count to 1 for a true delay slot, and explore memory pipelining to overlap latency, potentially improving IPC by 10–15%.

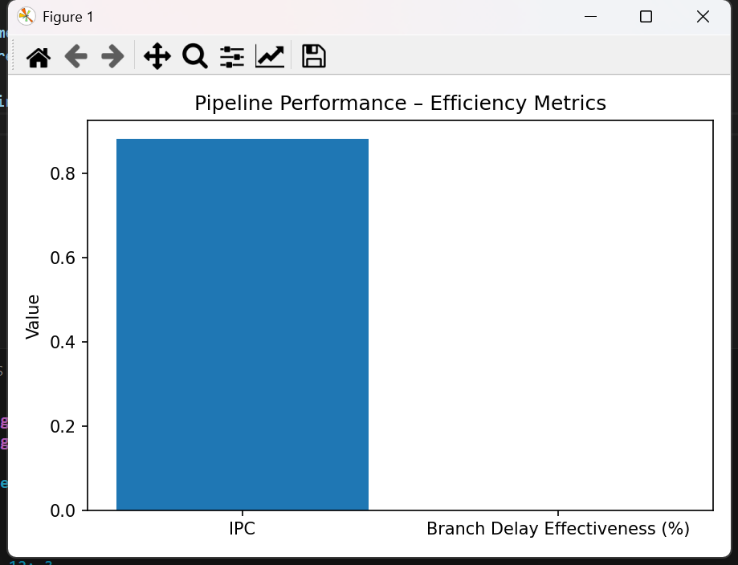
**Conclusion**

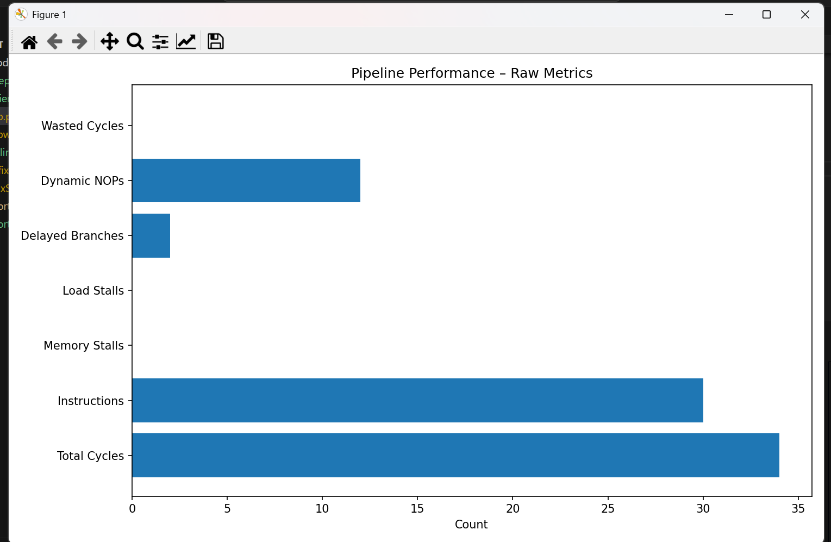
The modified MIPS processor simulator successfully integrates delayed branch execution and multi-cycle memory access, with a clear visualization via a colored timing table. Performance metrics highlight trade-offs: branch delay slots avoid flushes but waste cycles, while multi-cycle memory adds realism at the cost of stalls. Optimizations like better delay slot utilization and memory pipelining could enhance efficiency, aligning with real-world processor designs.

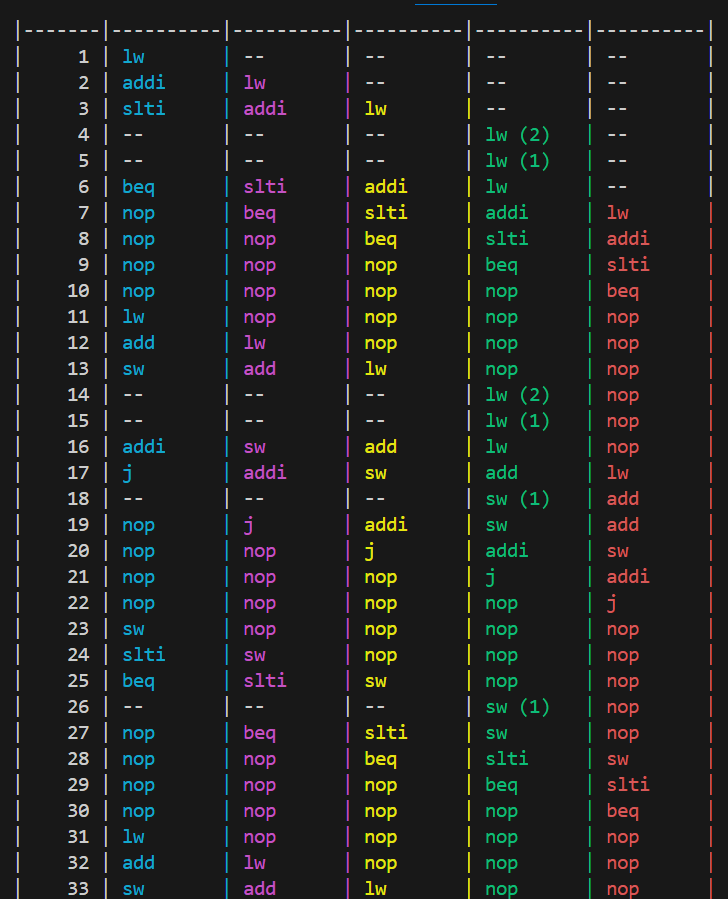
**Screenshots of the Output**

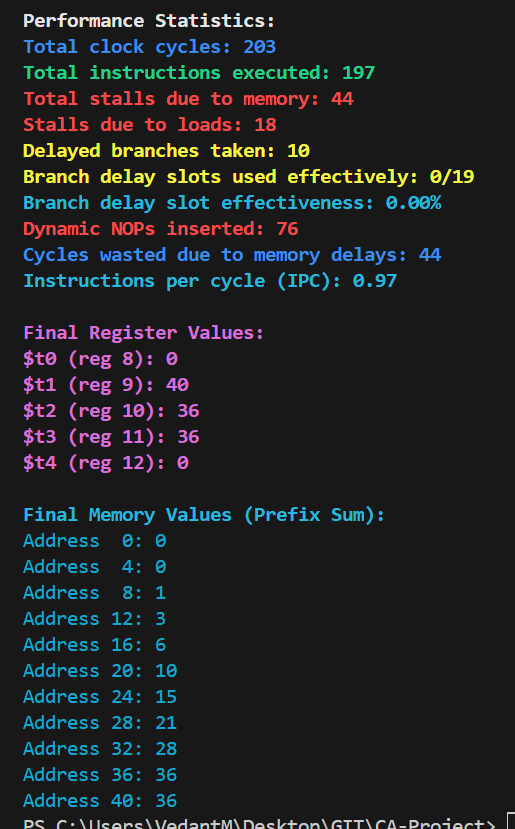
* 1. Testing the processor with MIPS code where we have given three number that keep on incrementing, until their sum is less than a certain number:

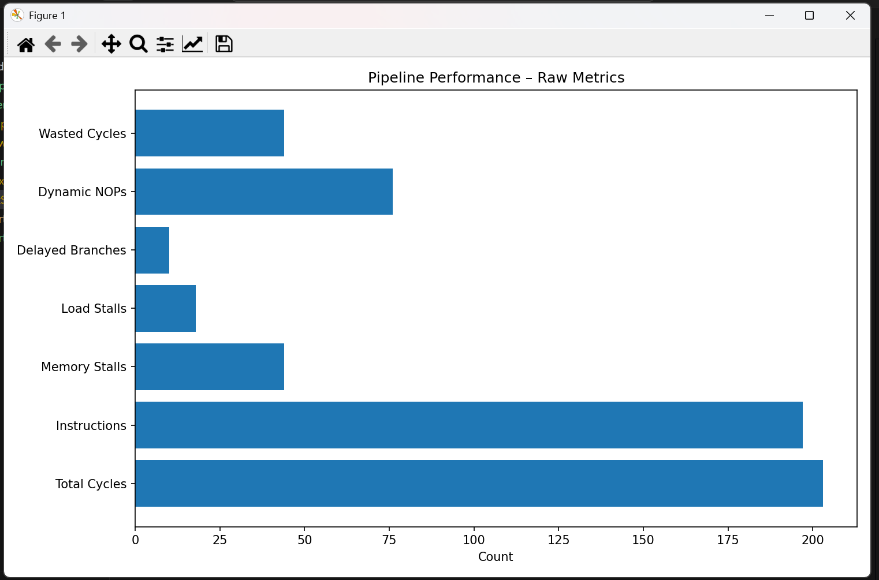


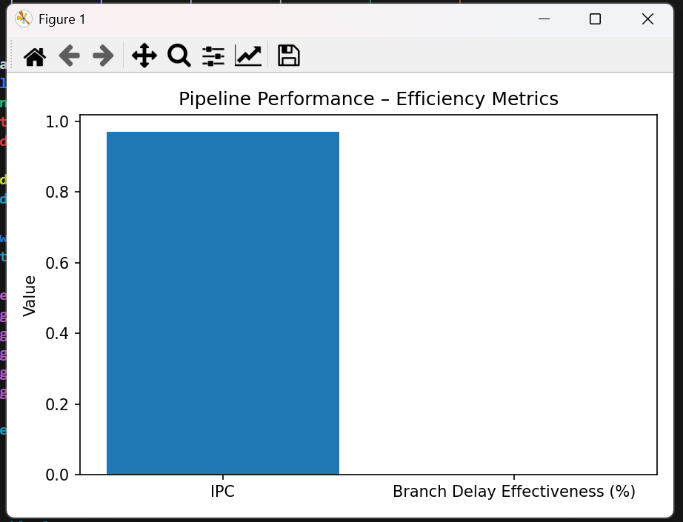


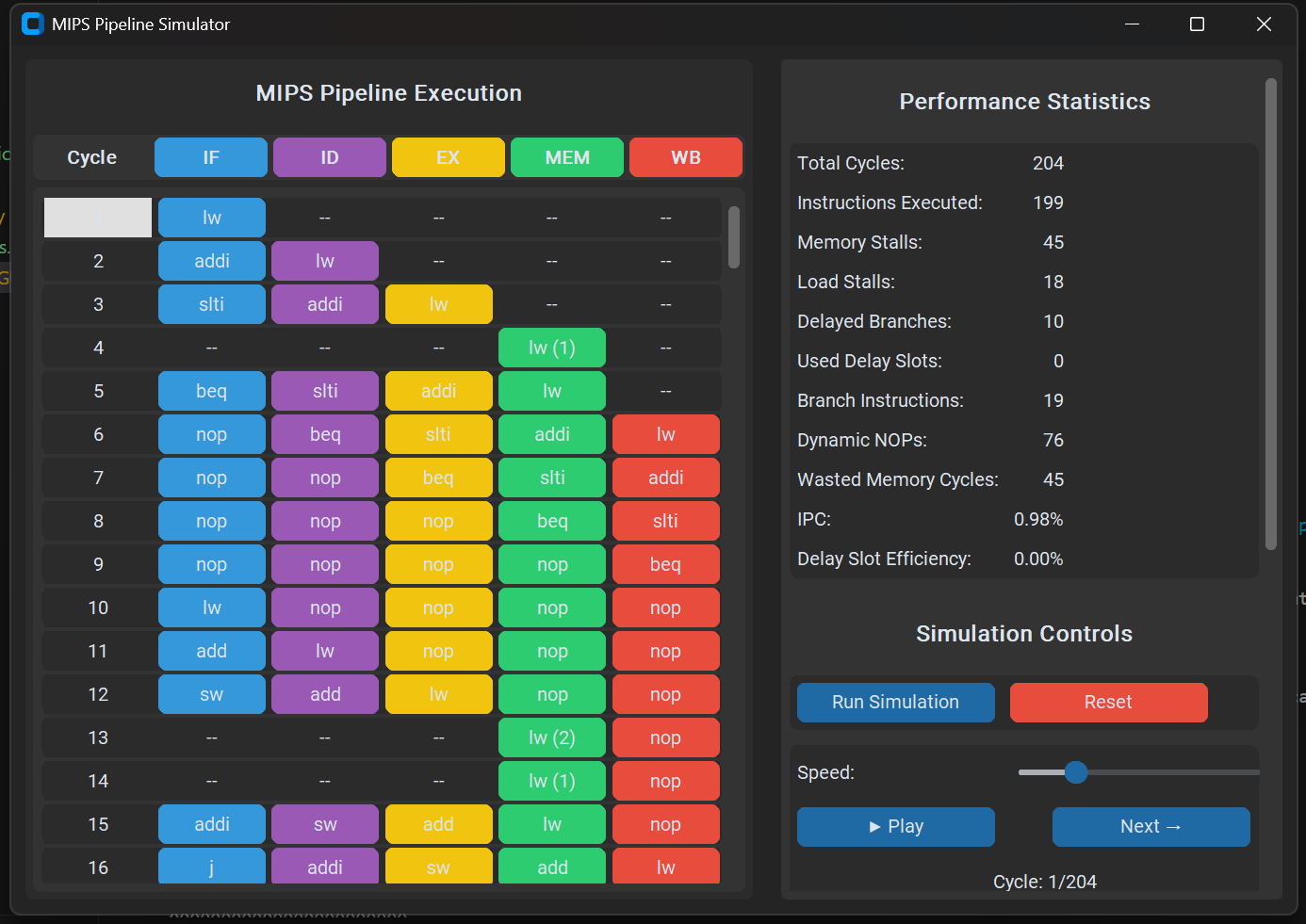


* 1. Here is the output for the code with lw/sw instructions as well:







* 1. Here is the GUI implementation of both the code:

