IITB CPU
EE 224 Project Report

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Overview of the experiment

- We were tasked with the making of a simple programmable device.
- The device has a clock as the input and a sequence of instructions to be executed
- The contents of this report include:
  1. Technical Specifications
  2. Approach
  3. RTL View

1 Technical Specifications

- Processing speed of upto 50MHz on FPGA
- Memory with (specify number) of addresses
- Register file with 7 registers and 1 programme counter making for a total of 8 registers.
- Finite State Machine having only 8 states to simplify logic as much as possible.
- Memory with 64 slots, each storing 16 bit values, meaning 2^{10} = 1Kb approximately

2 Approach

1. Pen Paper Design
2. Instructions
3. Components Description
4. States
5. Control Design

2.1 Pen Paper Design

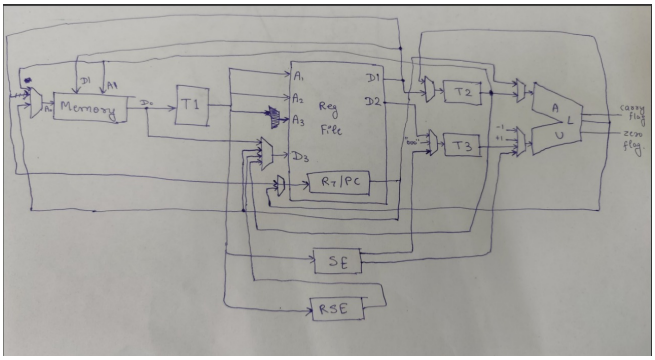


Figure 1: Pen Paper Design

2.2 Instructions

2.2.1 Types of Instruction

1. R Type
   This type of instruction has on position(s):

   - 15 to 12 - OP Code
   - 11 to 9 - RA
   - 8 to 6 - RB
   - 5 to 3 - RC
   - 2 - Unused 0
   - 1 to 0 - Condition (CZ)

2. I Type
   This type of instruction has on position(s):

   - 15 to 12 - OP Code
   - 11 to 9 - RA
   - 8 to 6 - RC
   - 5 to 0 - Immediate

3. J Type
   This type of instruction has on position(s):

   - 15 to 12 - OP Code
   - 11 to 9 - RA
   - 8 to 0 - Immediate

2.2.2 The 16 Bits of Each Instructions

Instruction	15 to 12 (OP Code)	11 to 9	8 to 6	5 to 3	2	1 to 0 (Condition CZ)
ADD	0000	RA	RB	RC	0	00
ADC	0000	RA	RB	RC	0	10
ADZ	0000	RA	RB	RC	0	01
ADI	0001	RA	RB	6 bit Immediate		
NDU	0010	RA	RB	RC	0	00
NDC	0010	RA	RB	RC	0	10
NDZ	0010	RA	RB	RC	0	01
LHI	0011	RA	9 bit Immediate			
LW	0100	RA	RB	6 bit Immediate		
SW	0101	RA	RB	6 bit Immediate		
LM	0110	RA	0 + 8 bits corresponding to Reg R7 to R0			
SM	0110	RA	0 + 8 bits corresponding to Reg R7 to R0			
BEQ	1100	RA	RB	6 bit Immediate		
JAL	1000	RA	9 bit Immediate Offset			
JLR	1001	RA	RB	000000		

Table 1: Instructions 16 bits

2.3 Components Description

2.3.1 Arithmetic and Logic Unit

- Two 16 bit input
- One 16 bit output, carry and zero flags too
- 2 bit control line to switch between 3 operations - ADD, SUB, NAND

2.3.2 Control Unit

- Input as current state (3 bit)
- Output as 6 control lines (of write enable)
- Decides which control line should be enables

2.3.3 Register File

- 3 bit input address line and 16 bit data line
- two 3 bit output address line and two 16 bit data line
- Stores the values to be immediately read or written

2.3.4 Memory Unit

- 16 bit data and address line each
- Output is same too
- Stores all the

2.3.5 Temporary Registers

- These just act as connections with an enabler for controlled flow

2.3.6 Finite State Machine

- Initial state and inputs of CPU as input
- Next state as output
- Decides the next state

2.4 States

- Total 8 States
- Control decides the inputs

S1	PC → Mem_A0	PC_WR
	Mem_D0 → T1	T1_WR
	PC → ALU_A	ADD
	+1 → ALU_B	
	ALU_C → PC	
S2	$T1_{11-9}$/$T1_{8-6}$ → RF_A1	T2_WR
	RD_D1 → T2	T3_WR
	$T1_{8-6}$/$T1_{5-0}$ → RF_A2	
	RF_D2 → T3	
S3	T2 → ALU_A	ADD/NAND
	T3/+1 → ALU_B	
	ALU_C → T2	
	(by op code) c=c+1	
S4	(If Mem_D0 coming) T2 → Mem_A0	RF_WR
	$T1_{8-0}$(with SE)/T2/PC/Mem_D0 → RF_D3	
	$T1_{11-9}$/$T1_{8-6}$/$T1_{5-3}$/c(binary) → RF_A3	
S5	$T1_{11-9}$/c(binary) → RF_A1	Mem_WR
	RF_D1 → Mem_DI	
	T2 → Mem_AI	
S6	PC → ALU_A	PC_WR
	$T1_{5-0}$/$T1_{8-0}$	
	ALU_C → PC	

Table 2: States

S7	PC $\rightarrow$ ALU_A +1 $\rightarrow$ ALU_B ALU_C $\rightarrow$ PC	SUB
S8	$T1_{8-6} \rightarrow$ RF_A1 RF_D1 $\rightarrow$ PC	PC_WR

Table 3: States Continued

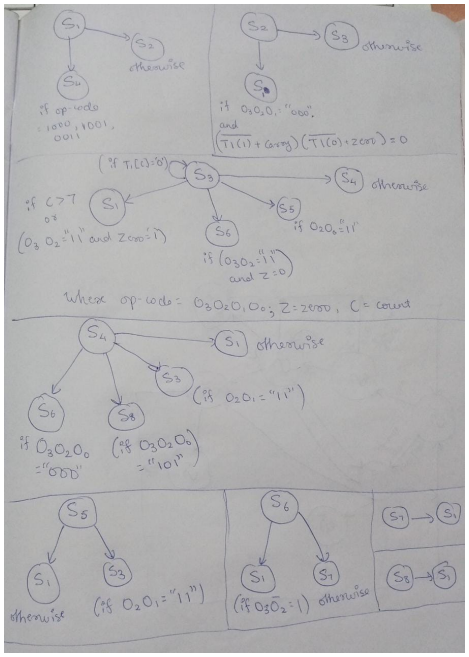


Figure 2: State transition

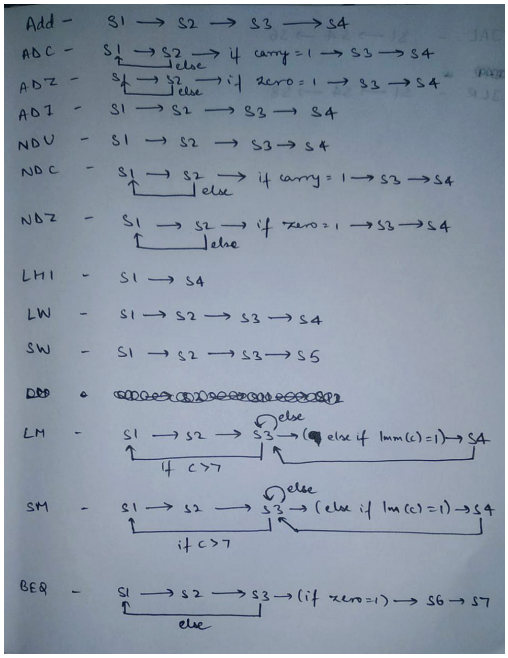


Figure 3: State Usage

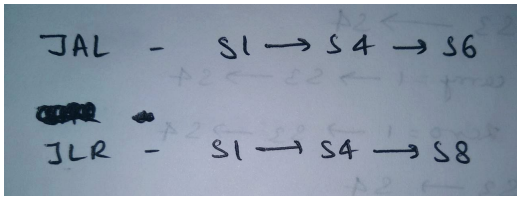
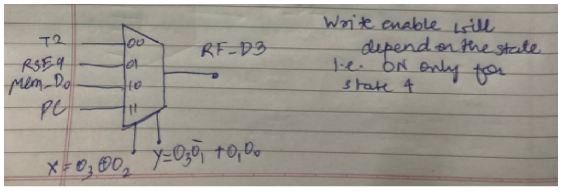
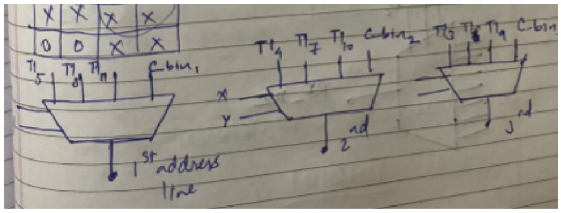
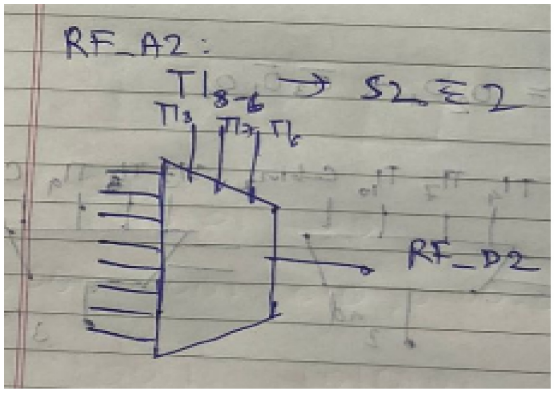


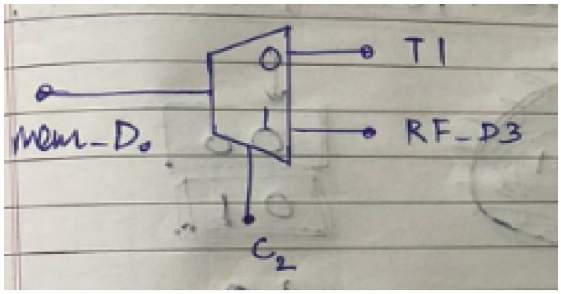
Figure 4: State Usage Continued

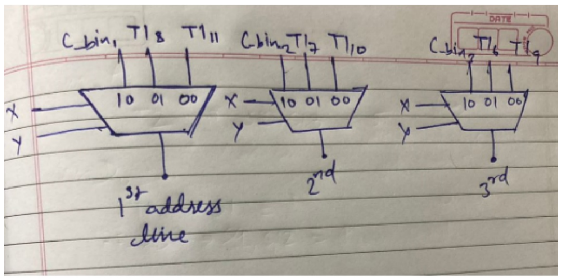
2.5 Control Design

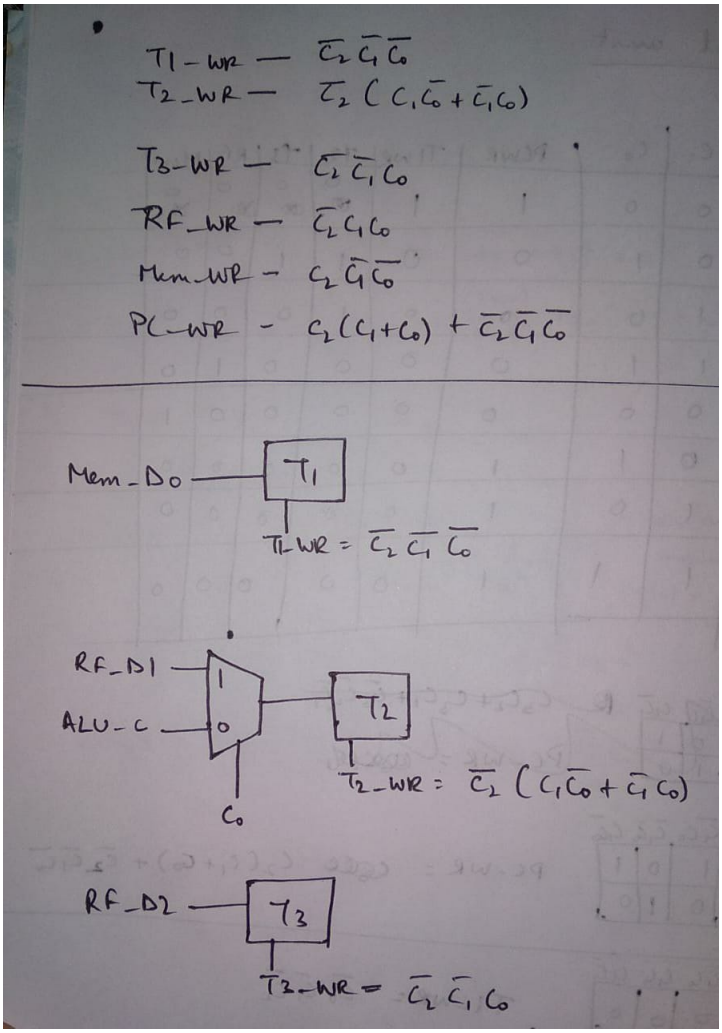


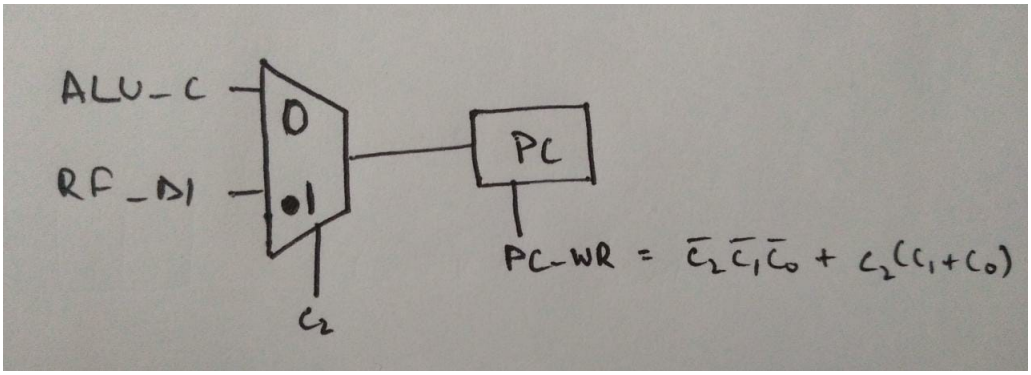

X X X X
0 0 X X
C-bin1
1st address line
C-bin2
x
y
2nd
3rd
C-bin

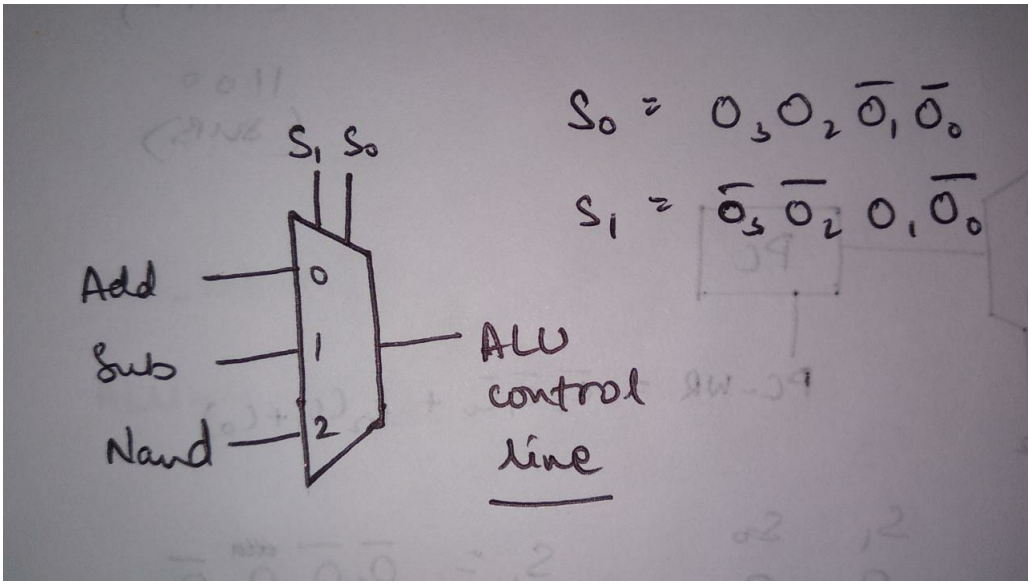

RF_A2 :
T|8-6 → S2_E2
T3
T3
T6
RF_D2

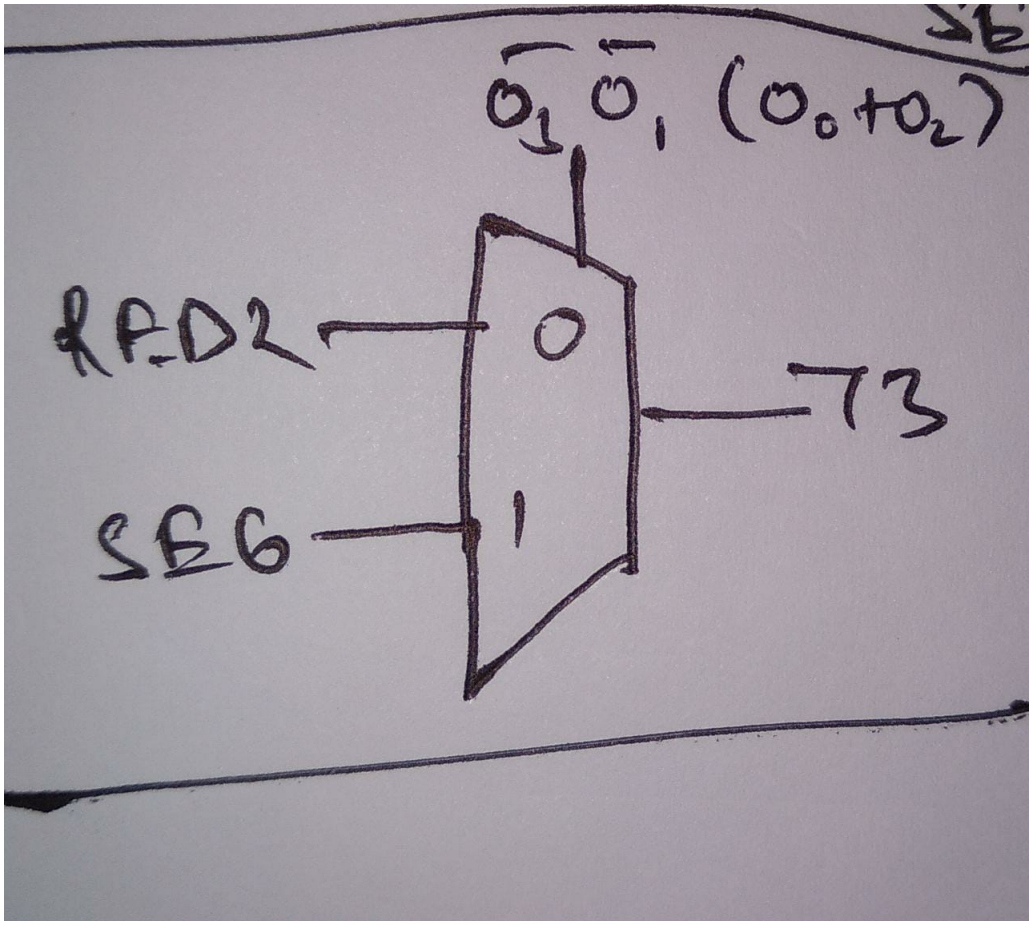

T1
RF_D3
mem_D0
C2


C_bin1 T18 T111
C_bin2 T17 T110
C_bin3 T16 T19
10 01 00
X
Y
1st address line
2nd
3rd


T1_WR — $\bar{C}_2\bar{C}_1\bar{C}_0$
T2_WR — $\bar{C}_2(C_1\bar{C}_0 + \bar{C}_1C_0)$
T3_WR — $\bar{C}_2\bar{C}_1C_0$
RF_WR — $\bar{C}_2C_1C_0$
Mem_WR — $C_2\bar{C}_1\bar{C}_0$
PC_WR — $C_2(C_1+C_0) + \bar{C}_2\bar{C}_1\bar{C}_0$
Mem_D0
T1
T1_WR = $\bar{C}_2\bar{C}_1\bar{C}_0$
RF_D1
ALU_C
1
0
T2
C_0
T2_WR = $\bar{C}_2(C_1\bar{C}_0 + \bar{C}_1C_0)$
RF_D2
T3
T3_WR = $\bar{C}_2\bar{C}_1C_0$


ALU_C
RF_DI
0
1
PC
C2
PC_WR = $\bar{C}_2\bar{C}_1\bar{C}_0 + C_2(C_1+C_0)$


$S_0 = O_3 O_2 \bar{O}_1 \bar{O}_0$
$S_1 = \bar{O}_3 \bar{O}_2 O_1 \bar{O}_0$
S_1 S_0
Add
Sub
Nand
0
1
2
ALU control line


$\overline{O_1}\,\overline{O_1}\,(O_0+O_2)$
RAD2
SEG
0
1
73

3 RTL View

1. RTL View of Entire CPU

3.1 RTL View of Entire CPU

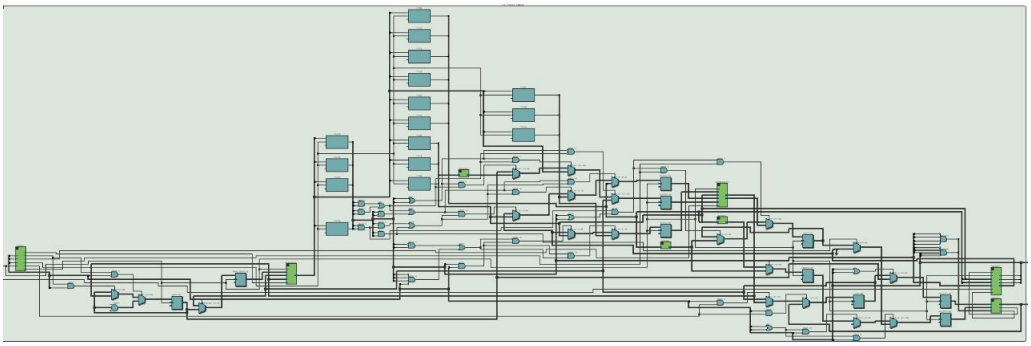


Figure 5: RTL View

4 Conclusion

- All the components are constructed correctly
- The components are connected correctly with the appropriate condition dependent inputs
- Instructions are correctly read
- State transitioning happens correctly
- Memory and registers are read and written correctly
- Output of all logical operations are performed correctly