Run file

```
#library creation
create_lib -technology ../../ref/tech/saed32nm_1p9m.tf -ref_libs  \
{../../ref/CLIBs/saed32_1p9m_tech.ndm ../../ref/CLIBs/saed32_hvt.ndm  \
../../ref/CLIBs/saed32_lvt.ndm ../../ref/CLIBs/saed32_rvt.ndm  \
../../ref/CLIBs/saed32_sram_lp.ndm} risc_v

#reading netlist and SDC
read_verilog  ../netlist/risc.v
read_sdc ../constraints/risc_sdc2.sdc


#floor plan
link_design
initialize_floorplan -side_ratio {2 3} -core_offset {2}

#parasitic reading
read_parasitic_tech -name {new_model} -tlup
{../../ref/tech/saed32nm_1p9m_Cmin.lv.tluplus} -layermap  \
{../../ref/tech/saed32nm_tf_itf_tluplus.map}
current_corner default
set_parasitic_parameters -early_spec new_model -late_spec new_model
set_process_number 0.99 -corners default
set_temperature 125 -corners default
set_voltage 0.75 -corners default
current_mode default
read_sdc ../constraints/risc_sdc2.sdc
set_scenario_status default -active true -setup true -hold true -max_transition true -
max_capacitance true -min_capacitance true -leakage_power true  \
-dynamic_power true

#pg

set_app_options -name plan.place.auto_create_blockages -value auto

create_placement -floorplan

place_pins -self

check_pg_drc

check_pg_connectivity

check_pg_missing_vias

#placement

create_placement -congestion -congestion_effort high

# re run untile good congestion is obtained
# set_app_options -name place.coarse.max_density -value 0.4
# set_app_options -name place.coarse.pin_density_aware -value true
# create_placement and routing blockages

set_app_options place_opt.place.congestion_effort -value high

place_opt

check_legality -verbos

report_congestion

report_utilization
report_constraints

# cts stage

# remove unnessary routing blockages
```

```
check_design -checks pre_clock_tree_stage
set_app_options -name time.remove_clock_reconvergence_pessimism -value true
set_app_options -name clock_opt.flow.enable_ccd -value true
set_app_options -name clock_opt.place.congestion_effort -value high
set_app_options -name cts.optimize.enable_congestion_aware_ndr_promotion -value true
#congestion aware NDR promotion for SI
# source ./scripts/ndr.tcl

report_qor -summary
report_clock_settings
clock_opt

report_timing
report_constraints
report_qor -summary
save_block -as after_cts

#routing

check_design -checks pre_route_stage
set_app_options -name route.track.timing_driven     -value true
set_app_options -name route.track.crosstalk_driven  -value true
set_app_options -name route.detail.timing_driven    -value true

set_routing_rule all -clear -default_rule -min_routing_layer 1 -max_routing_layer 9
route_auto -max_detail_route_iterations 30
route_eco
check_lvs

save_block -as after_routing

write_script -force -format icc2 -output ../reports/risc_spef
write_parasitics -output ../reports/spef_generation_1
write_sdf ../results/risc.sdf
write_verilog ../results/risc.v
write_gds ../results/risc.gds
write_sdc -output ../results/risc.sdc
```

REPORTS

Report_timing

```
icc2_shell> report_timing
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
        -report_by design
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Fri Dec  8 16:37:36 2023
****************************************
Information: Timer using 'CRPR'. (TIM-050)

  Startpoint: REG2/alu_opcode_reg_out_reg[1] (rising edge-triggered flip-flop clocked by clock)
  Endpoint: MC/cause_out_reg[2] (rising edge-triggered flip-flop clocked by clock)
  Mode: default
  Corner: default
  Scenario: default
  Path Group: clock
  Path Type: max

  Point                                                  Incr       Path
  -----------------------------------------------------------------------
  clock clock (rise edge)                                0.00       0.00
  clock network delay (propagated)                       0.12       0.12

  REG2/alu_opcode_reg_out_reg[1]/CLK (DFFX1_RVT)         0.00       0.12 r
  REG2/alu_opcode_reg_out_reg[1]/Q (DFFX1_RVT)           0.35       0.47 r
  ALU/U25/Y (INVX0_HVT)                                  0.27       0.74 f
  ALU/U27/Y (AND3X1_RVT)                                 0.41       1.15 f
  ALU/U210/Y (NAND2X0_RVT)                               0.31       1.46 r
  ALU/U211/Y (INVX1_HVT)                                 0.65       2.11 f
  ALU/U212/Y (NAND2X4_HVT)                               1.29       3.39 r
  ALU/U783/Y (OA22X2_HVT)                                1.52       4.91 r
  ALU/U784/Y (AND2X1_RVT)                                0.23       5.14 r
  ALU/U786/Y (AND2X1_RVT)                                0.11       5.26 r
  ALU/U792/Y (NAND4X0_RVT)                               0.16       5.41 f
  WBMUX/U85/Y (AO22X1_RVT)                               0.21       5.63 f
```

```
  BU/U89/Y (OA221X1_LVT)                               0.18       7.70 f
  BU/U91/Y (AO222X1_LVT)                               0.14       7.84 f
  BU/U93/Y (AO222X1_LVT)                               0.13       7.97 f
  BU/U96/Y (OA222X1_LVT)                               0.13       8.10 f
  BU/U98/Y (OA22X1_LVT)                                0.10       8.21 f
  BU/U100/Y (NAND2X2_LVT)                              0.11       8.32 r
  BU/U101/Y (AO222X1_LVT)                              0.15       8.46 r
  BU/U102/Y (AO22X1_LVT)                               0.08       8.55 r
  BU/U129/Y (AO221X1_LVT)                              0.11       8.66 r
  BU/U130/Y (OA221X1_LVT)                              0.09       8.75 r
  BU/U131/Y (NAND2X0_LVT)                              0.04       8.78 f
  BU/U132/Y (OA221X1_LVT)                              0.10       8.88 f
  BU/U134/Y (AO21X1_LVT)                               0.13       9.02 f
  BU/U135/Y (AND4X4_LVT)                               0.18       9.20 f
  PC/U233/Y (AND2X1_LVT)                               0.08       9.27 f
  MC/U26/Y (OR2X2_LVT)                                 0.10       9.37 f
  MC/U27/Y (INVX1_LVT)                                 0.05       9.42 r
  MC/U41/Y (NAND3X0_LVT)                               0.04       9.46 f
  MC/U42/Y (NAND2X0_LVT)                               0.07       9.54 r
  MC/U43/Y (NAND3X1_LVT)                               0.13       9.67 f
  MC/U45/Y (NAND4X0_LVT)                               0.10       9.77 r
  MC/ZBUF_24_inst_3650/Y (NBUFFX2_LVT)                 0.08       9.85 r
  MC/U48/Y (INVX4_LVT)                                 0.03       9.88 f
  MC/U73/Y (NAND2X0_LVT)                               0.05       9.93 r
  MC/U74/Y (NAND2X0_RVT)                               0.07      10.00 f
  MC/cause_out_reg[2]/D (DFFX1_RVT)                    0.00      10.00 f
  data arrival time                                              10.00

  clock clock (rise edge)                             10.00      10.00
  clock network delay (propagated)                     0.10      10.10
  clock reconvergence pessimism                        0.01      10.10
  MC/cause_out_reg[2]/CLK (DFFX1_RVT)                  0.00      10.10 r
  library setup time                                  -0.10      10.00
  data required time                                             10.00
  -----------------------------------------------------------------------
  data required time                                             10.00
  data arrival time                                             -10.00
  -----------------------------------------------------------------------
  slack (MET)                                                    0.00
```

Report_constraints

```
icc2_shell> report_constraints[14Goute_eco[K[14Geport_constraints[20Gdesign[K[20Gqor[K
****************************************
Report : qor
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Fri Dec  8 16:36:44 2023
****************************************
Information: Timer using 'CRPR'. (TIM-050)


Scenario           'default'
Timing Path Group  'clock'
-----------------------------------------
Levels of Logic:                    44
Critical Path Length:             9.88
Critical Path Slack:              0.00
Critical Path Clk Period:        10.00
Total Negative Slack:             0.00
No. of Violating Paths:              0
Worst Hold Violation:             0.00
Total Hold Violation:             0.00
No. of Hold Violations:              0
-----------------------------------------


Cell Count
-----------------------------------------
Hierarchical Cell Count:            27
Hierarchical Port Count:          4120
Leaf Cell Count:                  8683
Buf/Inv Cell Count:               1052
Buf Cell Count:                    455
Inv Cell Count:                    597
CT Buf/Inv Cell Count:               0
Combinational Cell Count:         7069
   Single-bit Isolation Cell Count:                     0
   Multi-bit Isolation Cell Count:                      0
   Isolation Cell Banking Ratio:                        0.00%
   Single-bit Level Shifter Cell Count:                 0
   Multi-bit Level Shifter Cell Count:                  0
```

```
   Multi-bit Isolation Cell Count:                      0
   Isolation Cell Banking Ratio:                        0.00%
   Single-bit Level Shifter Cell Count:                 0
   Multi-bit Level Shifter Cell Count:                  0
   Level Shifter Cell Banking Ratio:                    0.00%
   Single-bit ELS Cell Count:                           0
   Multi-bit ELS Cell Count:                            0
   ELS Cell Banking Ratio:                              0.00%
Sequential Cell Count:            1614
   Integrated Clock-Gating Cell Count:                  0
   Sequential Macro Cell Count:                         0
   Single-bit Sequential Cell Count:                    1614
   Multi-bit Sequential Cell Count:                     0
   Sequential Cell Banking Ratio:                       0.00%
   BitsPerflop:                                         1.00
Macro Count:                         0
-----------------------------------------


Area
-----------------------------------------
Combinational Area:           17530.85
Noncombinational Area:        11191.23
Buf/Inv Area:                  2296.45
Total Buffer Area:             1313.92
Total Inverter Area:            982.52
Macro/Black Box Area:              0.00
Net Area:                             0
Net XLength:                  132284.76
Net YLength:                  141171.22
-----------------------------------------
Cell Area (netlist):                        28722.08
Cell Area (netlist and physical only):      28722.08
Net Length:                   273455.98


Design Rules
-----------------------------------------
Total Number of Nets:             9052
Nets with Violations:                0
Max Trans Violations:                0
```

```
Area
-----------------------------------------
Combinational Area:           17530.85
Noncombinational Area:        11191.23
Buf/Inv Area:                  2296.45
Total Buffer Area:             1313.92
Total Inverter Area:            982.52
Macro/Black Box Area:              0.00
Net Area:                             0
Net XLength:                  132284.76
Net YLength:                  141171.22
-----------------------------------------
Cell Area (netlist):                        28722.08
Cell Area (netlist and physical only):      28722.08
Net Length:                   273455.98


Design Rules
-----------------------------------------
Total Number of Nets:             9052
Nets with Violations:                0
Max Trans Violations:                0
Max Cap Violations:                  0
-----------------------------------------
```

Report_qor

```
icc2_shell> report_qor
****************************************
Report : qor
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Fri Dec  8 18:08:44 2023
****************************************
Information: Timer using 'CRPR'. (TIM-050)


Scenario           'default'
Timing Path Group  'clock'
----------------------------------------
Levels of Logic:                    44
Critical Path Length:             9.88
Critical Path Slack:              0.00
Critical Path Clk Period:        10.00
Total Negative Slack:             0.00
No. of Violating Paths:              0
Worst Hold Violation:             0.00
Total Hold Violation:             0.00
No. of Hold Violations:              0
----------------------------------------


Cell Count
----------------------------------------
Hierarchical Cell Count:            27
Hierarchical Port Count:          4120
Leaf Cell Count:                  8683
Buf/Inv Cell Count:               1052
Buf Cell Count:                    455
Inv Cell Count:                    597
CT Buf/Inv Cell Count:               0
Combinational Cell Count:         7069
   Single-bit Isolation Cell Count:                     0
   Multi-bit Isolation Cell Count:                      0
   Isolation Cell Banking Ratio:                        0.00%
   Multi-bit Isolation Cell Count:                      0
   Isolation Cell Banking Ratio:                        0.00%
   Single-bit Level Shifter Cell Count:                 0
   Multi-bit Level Shifter Cell Count:                  0
   Level Shifter Cell Banking Ratio:                    0.00%
   Single-bit ELS Cell Count:                           0
   Multi-bit ELS Cell Count:                            0
   ELS Cell Banking Ratio:                              0.00%
Sequential Cell Count:            1614
   Integrated Clock-Gating Cell Count:                  0
   Sequential Macro Cell Count:                         0
   Single-bit Sequential Cell Count:                    1614
   Multi-bit Sequential Cell Count:                     0
   Sequential Cell Banking Ratio:                       0.00%
   BitsPerflop:                                         1.00
Macro Count:                       0
----------------------------------------


Area
----------------------------------------
Combinational Area:           17530.85
Noncombinational Area:        11191.23
Buf/Inv Area:                  2296.45
Total Buffer Area:             1313.92
Total Inverter Area:            982.52
Macro/Black Box Area:             0.00
Net Area:                            0
Net XLength:                  132284.76
Net YLength:                  141171.22
----------------------------------------
Cell Area (netlist):                        28722.08
Cell Area (netlist and physical only):      28722.08
Net Length:                   273455.98


Design Rules
----------------------------------------
Total Number of Nets:              9052
Nets with Violations:                 0
Max Trans Violations:                 0
Max Cap Violations:                   0
----------------------------------------
```

Report_utilization

```
icc2_shell> report_utilization
****************************************
Report : report_utilization
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Fri Dec  8 16:36:53 2023
****************************************
Utilization Ratio:                      0.7520
Utilization options:
 - Area calculation based on:           site_row of block final_report_project
 - Categories of objects excluded:      hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area:                             38196.0642
Total Capacity Area:                    38196.0642
Total Area of cells:                    28722.0842
Area of excluded objects:
 - hard_macros         :                0.0000
 - macro_keepouts      :                0.0000
 - soft_macros         :                0.0000
 - io_cells            :                0.0000
 - hard_blockages      :                0.0000

Utilization of site-rows with:
 - Site 'unit':                         0.7520

0.7520
```

Check_route

```
Verify Summary:

Total number of nets = 9044, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                 0 ports without pins of 0 cells connected to 0 nets
                                 0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 0
Total number of antenna violations = no antenna rules defined
Total number of tie to rail violations = not checked
Total number of tie to rail directly violations = not checked
```

Report_design

```
icc2_shell> report_design
****************************************
Report : design
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Fri Dec  8 16:39:27 2023
****************************************

Total number of std cells in library : 1025
Total number of dont_use lib cells   : 80
Total number of dont_touch lib cells : 80
Total number of buffers              : 69
Total number of inverters            : 45
Total number of flip-flops           : 318
Total number of latches              : 36
Total number of ICGs                 : 36

Cell Instance Type  Count         Area
--------------------------------------
TOTAL LEAF CELLS     8683    28722.084
Standard cells       8683    28722.084
Hard macro cells        0        0.000
Soft macro cells        0        0.000
Always on cells         0        0.000
Physical only           0        0.000
Fixed cells             0        0.000
Moveable cells       8683    28722.084
Sequential           1614    11191.231
Buffer/inverter      1052     2296.445
ICG cells               0        0.000

Logic Hierarchies                    : 27
Design Masters count                 : 162
Total Flat nets count                : 9052
Total FloatingNets count             : 8
Total no of Ports                    : 241
Number of Master Clocks in design    : 1
Number of Generated Clocks in design : 0
```

```
Design Masters count                 : 162
Total Flat nets count                : 9052
Total FloatingNets count             : 8
Total no of Ports                    : 241
Number of Master Clocks in design    : 1
Number of Generated Clocks in design : 0
Number of Path Groups in design      : 7 (1 of them Non Default)
Number of Scan Chains in design      : 0
List of Modes                        : default
List of Corners                      : default
List of Scenarios                    : default

Core Area                            : 38196.064
Chip Area                            : 40625.152
Total Site Row Area                  : 38196.064
Number of Blockages                  : 6
Total area of Blockages              : 191.370
Number of Power Domains              : 1
Number of Voltage Areas              : 1
Number of Group Bounds               : 0
Number of Exclusive MoveBounds       : 0
Number of Hard or Soft MoveBounds    : 0
Number of Multibit Registers         : 0
Number of Multibit LS/ISO Cells      : 0
Number of Top Level RP Groups        : 0
Number of Tech Layers                : 71 (61 of them have unknown routing dir.)

Total wire length                    : 216690.61 micron
Total number of wires                : 99446
Total number of contacts             : 102517
1
```

Report_congestion

```
icc2_shell> report_congestion
****************************************
Report : congestion
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Fri Dec  8 16:39:48 2023
****************************************

Layer     |    overflow     |              # GRCs has
Name      |  total   |  max   | overflow (%)      | max overflow
------------------------------------------------------------------
Both Dirs |    1438 |     7 |    1167  ( 4.01%) |       2
H routing |     942 |     3 |     850  ( 5.84%) |       4
V routing |     496 |     7 |     317  ( 2.18%) |       2
```