



[SL.NO:-85951728]

## **CERTIFICATE OF WORKSHOP COMPLETION**

**This certifies that**

**B ROHAN SRIVATSAV**

**has successfully completed the workshop in**

**VLSI RTL Design & Verification Using Synopsys Tool**



**Period of Training From: 20-01-2025 To: 24-01-2025**

**During this period he has gained expertise on the following:**

- Understanding ASIC Design Flow
- Design and Verify Asynchronous FIFO with Verilog
- Master Lint, CDC, and UPF Concepts
- Develop TB Components and Achieve Coverage.
- Set Up SV and UVM TB for Asynchronous FIFO
- Hands-on Labs



**27-01-2025**

**Issue Date**

**Signature**