Flexible Processor Architecture Design

Paper id 178

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Idea behind the project

- To design a processor architecture, for which custom instructions can be defined and executed.

- Which can execute wide variety of instruction sets.

But Why ?

Any benefits of such a microarchitecture?

- Application specific Instructions.
- Hardware VMs.
- Application binaries bundled with Instruction set implementations.

Approach

- TTA is the template for our Microarchitecture.

- To break down any complex instruction into a sequence of move instructions and instead execute those move instructions.

TTA Conceptual Design

- Transport Triggered Architecture is at the core of our microarchitecture design.

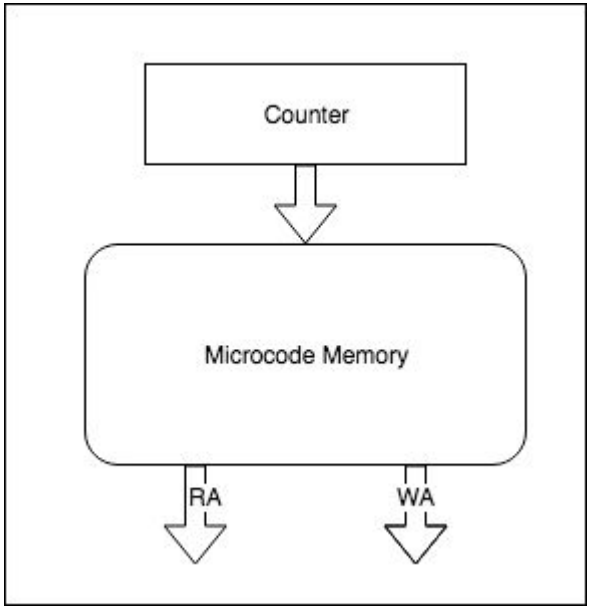
- Every microinstruction is RA : WA

- Register[WA] = Register[RA]

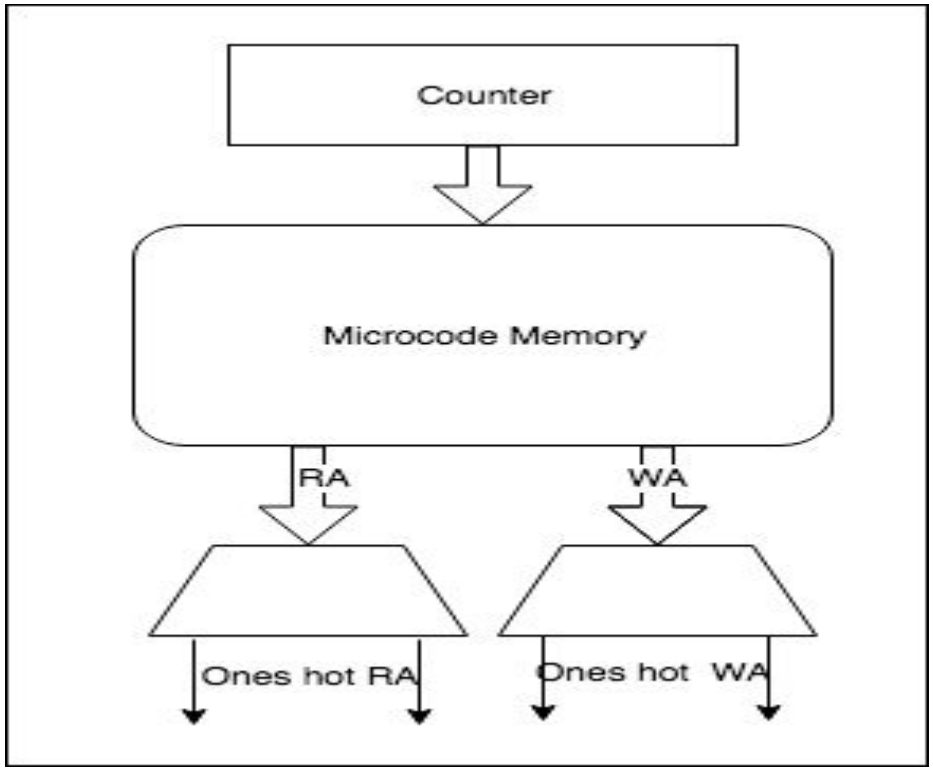
TTA Microarchitecture

- Microcode Fetch Block
  - Counter
  - Microcode Memory
- Microcode Decode Block
  - Simple Decoders to convert microcode addresses to one shot encoding
- Microcode Execute Block
  - Consists of Internal peripherals of the processor

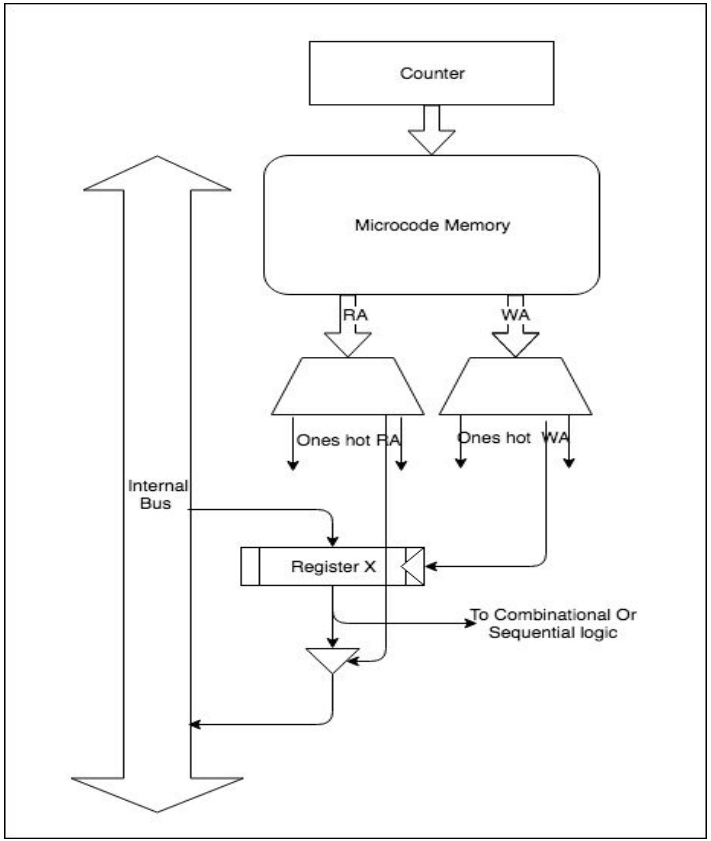
Fetch Block



Decode Block



Final rudimentary design



POC Design Specs

- Microinstruction size : Bit width of each of RA and WA is 6 bits, with additional fields opWAR and opRAR and the Microcode address width is 18 bits.

- All the registers used in internal peripherals are 8 bits wide.

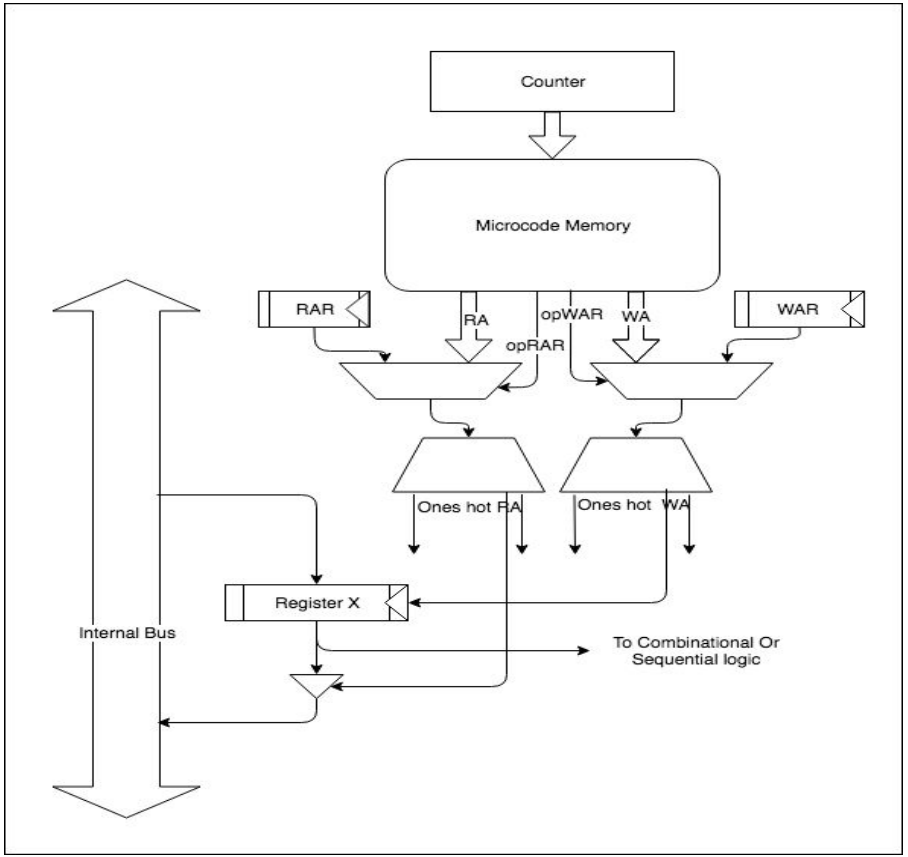
- 18 General purpose registers.

POC Design Internal peripherals

- 4 Input/Output registers and 1 Input/Output Control register
- 1 Immediate register, to generate any immediate operand values required
- Arithmetic and Logic functions : And, Or, Not, Logical shift, and addition.

POC Design Internal peripherals

- RAR and WAR registers.



POC Design Internal peripherals

- Microcode Jump Address Register and Microcode Jump Register
- Internal memory bank

Further Extension

- Implementation on FPGA, rather than logic ics.
- Implement simple instruction sets, like 6502, 8051 or 8086 for POC.
- Evaluate efficiency and necessary overhead, of actual processors vs implementation of their ISAs.
- Pipeline the Microarchitecture Design.
- Experiment and figure out issues that come with multiple internal busses.

Thank you