Rohan Juneja

Email : rohan@comp.nus.edu.sg
https://rohanjuneja.github.io/
Mobile : +65 81324894
Linkedin: junejarohan25
Skype : junejarohan25

Education

- **National University of Singapore** — Singapore
  Ph.D. in Computer Science (CGPA: 4.75/5) — *Januray 2021 - Present*
  Advisors: Prof Peh Li Shiuan, Prof Tulika Mitra

- **IIIT Delhi** — Delhi, India
  B.Tech in Electronics and Communications Engineering (CGPA: 8.41/10) — *May 2014 - May 2018*
  Advisors: Prof Lam Siew Kei, Prof Sujay Deb
  Thesis: Securing untrusted memories in embedded systems

Experience

- **National University of Singapore** — Singapore
  PhD Student — *Januray 2021 - Present*
  - Contributed to designing REACT, an accelerator for transfer learning for wearables, guided by Prof Li-Shiuan Peh and Prof Weng-Fai Wong. (Accepted in DAC 2022)
    - It proposes heterogeneous cores that can support both training and inference.
    - The architecture is NoC-centric, with weights, features and gradients distributed across cores, accessed, and computed efficiently through software-configurable NoCs.
    - It's online learning realizes up to 75% accuracy improvement and is up to 25× faster and 520× more energy-efficient than state-of-the-art accelerators with similar memory and computation footprint.
  - Contributed to testing and emulation of PACE silicon, a coarse-grain reconfigurable processor.

- **Qualcomm** — Bangalore, India
  CPU Design Engineer — *July 2018 - January 2021*
  - Worked as a CPU design engineer for Qualcomm Snapdragon Processors.
  - Responsible for multi-clock domain and Low Power (UPF) RTL delivery of ARM Kryo cores in Snapdragon 765G and other medium, high tier and compute chips.
  - Responsible for restructuring memory model RTL to support partial power gating.
  - Exposure to Power Manager IP, DCVS and Low Power Modes using ARM's P-channel, and boot RTL in Snapdragon CPUs.
  - Experienced in writing SystemVerilog assertions, code coverage and functional coverage closure.
  - Experienced in Synthesis flows, reviewing Design Constraints, timing arcs, and optimised registers.

- **Nanynag Technological University** — Singapore
  Research Assistant + NTU-India Connect Scholar — *August 2017 - December 2017*
  - Designed a dynamic memory authentication scheme for cyberphysical systems and improved upon it using cache-oblivious algorithms.
  - The design was initially studied on FPGA's and further integrated in Multi2sim system simulator to study the performance impact with various SPEC and PARSEC benchmarks.
  - Resulted in an average reduction of performance overhead by 20-30%.

Publications

Conferences

- Mohit Upadhyay, **Rohan Juneja**, Bo Wang, Jun Zhou, Weng-Fai Wong and Li-Shiuan Peh, "REACT: A Heterogeneous Reconfigurable Neural Network Accelerator with Software-Configurable NoCs for Training and Inference on Wearables" in Design Automation Conference (DAC), 2022. [Accepted]
- Sidhartha Shankar, Hemanta K. Mondal, **Rohan Juneja**, Sri Harsha Gade, Sujay Deb, "Dynamic NoC Platform for Varied Application Needs" in International Symposium on Quality Electronic Design (ISQED), 2018.
- Saru Vig, **Rohan Juneja**, Siew Kei Lam, Guiyuan Jian, "DISSECT: Dynamic Skew-and-Split Tree forMemory Authentication" in Design, Automation and Test in Europe Conference (DATE), 2020.
- Saru Vig, **Rohan Juneja**, Siew Kei Lam, "Cache-Aware Dynamic Skewed Tree for Fast Memory Authentication" in Asia and South Pacific Design Automation Conference (ASP-DAC), 2021.

Journals

- Saru Vig, **Rohan Juneja**, Guiyuan Jiang, Siew Kei Lam, Changhai Ou, "Framework for Fast Memory Authentication using Dynamically Skewed Integrity Tree" in IEEE Transactions on Very Large Scale Integration (TVLSI) Systems, vol. 27, pp. 2331–2341, October 2019.

Teaching Assistant

- **IIIT Delhi** Delhi, India
  Teaching Assistant, GPU Computing *January 2018 - April 2018*
  - Held weekly lab sessions for CUDA, helped prepare and grade assignments and exams.
- **IIIT Delhi** Delhi, India
  Teaching Assistant, Digital Circuits *January 2017 - April 2017*
  - Held weekly tutorials related to SystemVerilog and FPGA, and helped prepare and grade assignments and exams.

Selected Projects

- **Dynamic Network on chip**: Proposed a dynamic Network on Chip (DNoC) platform that optimises virtual channels and energy consumption without having any effect on the performance.
- **Work Sharing Scheduler**: Built a light weight work-sharing runtime for async-finish parallelism, which uses pthread library with coding in C. [Code]
- **ARM Simulator**: Built a functional simulator for execution of ARM assembly language instructions with coding in C language. [Code]
- **Game designing on FPGA**: Designed a visual ping pong game on FPGA using VGA technology. Studied the architectural design flow by Behavioral, Functional, and Static Timing Simulation. [Code]

Awards and Recognitions

- INAE travel grant, ISQED 2018.
- NTU-India Scholar - one of the 50 selected out of 2000+ applicants worldwide in 2017