Rohan Juneja

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Education

- **National University of Singapore** — Singapore
  Ph.D. in Computer Science (CGPA: 4.58/5) — *Januray 2021 - Present*
  Advisors: Prof Peh Li Shiuan, Prof Tulika Mitra

- **IIIT Delhi** — Delhi, India
  B.Tech in Electronics and Communications Engineering (CGPA: 8.41/10) — *May 2014 - May 2018*
  Advisors: Prof Lam Siew Kei, Prof Sujay Deb
  Thesis: Securing untrusted memories in embedded systems

Experience

- **National University of Singapore** — Singapore
  PhD Student — *Januray 2021 - Present*
  - Contributed to designing NOVA, a noc-based vector unit for mapping attention layers on a CNN accelerator, guided by Prof Li-Shiuan Peh and Prof Weng-Fai Wong. (Accepted in DATE 2024)
  - Contributed to designing FLEX, an accelerator for transfer learning for wearables, guided by Prof Li-Shiuan Peh and Prof Tulika Mitra. (Published in ICCAD 2023)
  - Contributed to designing REACT, an accelerator for transfer learning for wearables, guided by Prof Li-Shiuan Peh and Prof Weng-Fai Wong. (Published in DAC 2022)
  - Contributed to designing CTScan, a CGRA-based Platform for Emulation of Power Side-Channel Attacks on CPUs, guided by Prof Li-Shiuan Peh and Prof Trevor Carlson. (Submitted in IOTJ)
  - Contributed to testing and emulation of PACE silicon, a coarse-grain reconfigurable processor. (Submitted in ISSCC 2023)

- **Advanced Micro Devices** — Singapore
  PhD Research Intern — *May 2022 - July 2022*
  - Worked as a PhD Research Intern, responsible for designing accelerator for Ethereum's Beacon Chain (based on Proof-of-Stake).

- **Renesas Electronics Corporation** — Singapore
  PhD Engineering Intern — *Jan 2022 - April 2022*
  - Worked as a PhD Engineering Intern on Renesas' Dynamically Reconfigurable Processor (DRP).

- **Qualcomm** — Bangalore, India
  CPU Design Engineer — *July 2018 - January 2021*
  - Worked as a CPU design engineer for Qualcomm Snapdragon Processors.
  - Responsible for multi-clock domain and Low Power (UPF) RTL delivery of ARM Kryo cores in Snapdragon 765G and other medium, high tier and compute chips.
  - Responsible for restructuring memory model RTL to support partial power gating.
  - Exposure to Power Manager IP, DCVS and Low Power Modes using ARM's P-channel, and boot RTL in Snapdragon CPUs.
  - Experienced in writing SystemVerilog assertions, code coverage and functional coverage closure.
  - Experienced in Synthesis flows, reviewing Design Constraints, timing arcs, and optimised registers.

- **Nanynag Technological University** — Singapore
  Research Assistant + NTU-India Connect Scholar — *August 2017 - December 2017*

- Designed a dynamic memory authentication scheme for cyberphysical systems and improved upon it using cache-oblivious algorithms.
- The design was initially studied on FPGA's and further integrated in Multi2sim system simulator to study the performance impact with various SPEC and PARSEC benchmarks.
- Resulted in an average reduction of performance overhead by 20-30%.

Publications

Conferences

- **Rohan Juneja**, Thilini Kaushalya, Pranav Dangi, Tulika Mitra and Li-Shiuan Peh, "Nexus Machine: An Active Message-Driven CGRA for Accelerating Irregular Applications" in International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2024.
- Mohit Upadhyay, **Rohan Juneja**, Weng-Fai Wong and Li-Shiuan Peh, "NOVA: NoC-based Vector Unit for Mapping Attention Layers on a CNN Accelerator" in Design, Automation and Test in Europe Conference (DATE), 2024.
- Thilini Kaushalya, Dan Wu, **Rohan Juneja**, Dhananjaya Wijerathne, Tulika Mitra and Li-Shiuan Peh, "FLEX: Introducing FLEXible Execution on CGRA with Spatio-Temporal Vector Dataflow" in International Conference on Computer-Aided Design (ICCAD), 2023.
- Mohit Upadhyay, **Rohan Juneja**, Bo Wang, Jun Zhou, Weng-Fai Wong and Li-Shiuan Peh, "REACT: A Heterogeneous Reconfigurable Neural Network Accelerator with Software-Configurable NoCs for Training and Inference on Wearables" in Design Automation Conference (DAC), 2022.
- Saru Vig, **Rohan Juneja**, Siew Kei Lam, "Cache-Aware Dynamic Skewed Tree for Fast Memory Authentication" in Asia and South Pacific Design Automation Conference (ASP-DAC), 2021.
- Saru Vig, **Rohan Juneja**, Siew Kei Lam, Guiyuan Jian, "DISSECT: Dynamic Skew-and-Split Tree forMemory Authentication" in Design, Automation and Test in Europe Conference (DATE), 2020.
- Sidhartha Shankar, Hemanta K. Mondal, **Rohan Juneja**, Sri Harsha Gade, Sujay Deb, "Dynamic NoC Platform for Varied Application Needs" in International Symposium on Quality Electronic Design (ISQED), 2018.

Journals

- Yaswanth Tavva, **Rohan Juneja**, Trevor E. Carlson and Li-Shiuan Peh, "CTScan: A CGRA-based Platform for Emulation of Power Side-Channel Attacks on CPUs" in Transactions on Architecture and Code Optimization (TACO), 2023. [Submitted]
- Saru Vig, **Rohan Juneja**, Guiyuan Jiang, Siew Kei Lam, Changhai Ou, "Framework for Fast Memory Authentication using Dynamically Skewed Integrity Tree" in IEEE Transactions on Very Large Scale Integration (TVLSI) Systems, vol. 27, pp. 2331–2341, October 2019.

Teaching Assistant

- **National University of Singapore** — Singapore
  Teaching Assistant, Introduction to Operating Systems — *January 2023 - April 2023*
  - Worked as Teaching Assistant under Prof Djordje Jevdjic and Prof Prabhu Natarajan.
  - Held weekly tutorial sessions for a set of 48 students, and graded assignments and exams.
- **National University of Singapore** — Singapore
  Teaching Assistant, Introduction to Operating Systems — *August 2022 - November 2022*
  - Worked as Teaching Assistant under Prof Weng-Fai Wong.
  - Held weekly tutorial sessions for a set of 48 students, and graded assignments and exams.
- **IIIT Delhi** — Delhi, India
  Teaching Assistant, GPU Computing — *January 2018 - April 2018*
  - Worked as Teaching Assistant under Prof Ojaswa Sharma.
  - Held weekly lab sessions for CUDA, prepared and graded assignments and exams.

- **IIIT Delhi** Delhi, India
  Teaching Assistant, Digital Circuits *January 2017 - April 2017*
  - Worked as Teaching Assistant under Prof Sumit Darak.
  - Held weekly tutorials related to SystemVerilog and FPGA, prepared and graded assignments and exams.

Selected Projects

- **Dynamic Network on chip**: Proposed a dynamic Network on Chip (DNoC) platform that optimises virtual channels and energy consumption without having any effect on the performance.
- **Work Sharing Scheduler**: Built a light weight work-sharing runtime for async-finish parallelism, which uses pthread library with coding in C. [Code]
- **ARM Simulator**: Built a functional simulator for execution of ARM assembly language instructions with coding in C language. [Code]
- **Game designing on FPGA**: Designed a visual ping pong game on FPGA using VGA technology. Studied the architectural design flow by Behavioral, Functional, and Static Timing Simulation. [Code]

Awards and Recognitions

- Young Fellowship, DAC 2022.
- INAE travel grant, ISQED 2018.
- NTU-India Scholar - one of the 50 selected out of 2000+ applicants worldwide in 2017