Rohan Juneja

rohanjuneja.github.io | rohan14156@iiitd.ac.in | +91 9711495476 | junejarohan25

EDUCATION

IIIT-DELHI
B. Tech in Electronics and Communication Engineering
May 2018 | Delhi, India
4 years
CGPA: 8.41

NTU, SINGAPORE
Computer Science
Fall 2017 | Singapore

COURSEWORK

UNDERGRADUATE
Computer Organisation
Foundations of Parallel Programming
GPU Computing
Embedded Logic Design
Digital Circuits
Linear Circuits
Digital VLSI Design
Digital Hardware Design
Data Structures and Algorithms

TEACHING ASSISTANT

GPU Computing
Digital Circuits
Java Refresher Module

SKILLS

PROGRAMMING
System Verilog • Perl • Python • Tcl • C++ • C • ARM Assembly • Arduino • Java

TOOLS AND TECHNOLOGIES
ModelSim • Synopsys Verdi • Cadence Conformal Low Power • Synopsys Spyglass • Xilinx Vivado • Xilinx FPGA • AVR • ARMSim • OpenMP • MPI • Cuda • Habanero C • Multi2sim system simulator • Matlab

AWARDS

2018 Awardee of prestigious INAE travel grant for presenting my paper in California
2015 Awardee of consistent performance at Programming Club of IIIT-Delhi
2010 Awardee of Gold medal by Science Olympiad Foundation

EXPERIENCE

NUS | PHD STUDENT
January 2021 - Present | Singapore
PhD student at School of Computing.

QUALCOMM | CPU DESIGN ENGINEER
July 2018 - January 2021 | Bengaluru, India
Working as a CPU design engineer for Qualcomm Snapdragon Processors. Responsible for multi-clock domain and Low Power (UPF) RTL delivery of ARM Kryo cores in Snapdragon 765G and other medium, high tier and compute chips.
• Responsible for restructuring memory model RTL to support partial power gating.
• Exposure to Power Manager IP, DCVS and Low Power Modes using ARM's P-channel, and boot RTL in Snapdragon CPU's.
• Experienced in writing SystemVerilog assertions, code coverage and functional coverage closure.
• Experienced in Synthesis flows, reviewing Design Constraints, timing arcs, and optimised registers.

NANYNAG TECHNOLOGICAL UNIVERSITY | Research Assistant + NTU-India Connect Scholar
August 2017 – December 2017 | Singapore | Prof. Lam Siew Kei
• Designed a dynamic memory authentication scheme for cyberphysical systems .
• The design was integrated in Multi2sim system simulator to study the performance impact with various SPEC and PARSEC benchmarks.
• Resulted in an average reduction of performance overhead by 20-30%.

• Designed a scalable cache architecture with optimised coherency protocol in Multi2sim, and evaluated using various SPEC and PARSEC benchmarks.
• Resulted in average reduction in coherence traffic by 50% and runtime by 32.67%.

PUBLICATIONS

CONFERENCES
Sidhartha Shankar, Hemanta K. Mondal, Rohan Juneja, Sri Harsha Gade, Sujay Deb, "Dynamic NoC Platform for Varied Application Needs" in ISQED, 2018.

Saru Vig, Rohan Juneja, Siew Kei Lam, Guiyuan Jian, "DISSECT: Dynamic Skew-and-Split Tree forMemory Authentication" in DATE, 2020.

Saru Vig, Rohan Juneja, Siew Kei Lam, "Cache-Aware Dynamic Skewed Tree for Fast Memory Authentication" in ASP-DAC, 2021.

JOURNALS
Saru Vig, Rohan Juneja, Guiyuan Jiang, Siew Kei Lam, Changhai Ou, "Framework for Fast Memory Authentication using Dynamically Skewed Integrity Tree" in IEEE TVLSI, vol. 27, pp. 2331–2341, October 2019.

PROJECTS

NETWORK ON CHIP | Research Project
May 2016 - July 2016 | Delhi, India | Prof. Sujay Deb
Proposed a dynamic Network on Chip (DNoC) platform that optimises virtual channels and energy consumption without having any effect on the performance.

ARM SIMULATOR
February 2015 - April 2015 | Delhi, India | Prof. Neeraj Goel
Built a functional simulator for execution of ARM assembly language instructions with coding in C language. [Code]