# Rohan Juneja

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## EDUCATION

### IIIT-DELHI

B. Tech in Electronics and Communication Engineering
Expected May 2018 | Delhi, India
4 years
CGPA: 8.41

## COURSEWORK

### UNDERGRADUATE

Computer Organisation
Foundations of Parallel Programming
GPU Computing
Embedded Logic Design
Digital Circuits
Linear Circuits
Digital VLSI Design
Digital Hardware Design
Data Structures and Algorithms

## TEACHING ASSISTANT

GPU Computing
Digital Circuits
Java Refresher Module

## SKILLS

### PROGRAMMING

C++ • C • Python • Java • System C • ARM Assembly • Verilog • Arduino • JavaScript • HTML5 • CSS3 • Latex

### TOOLS AND TECHNOLOGIES

ModelSim • Verdi • Xilinx Vivado • Xilinx FPGA • AVR • ARMSim • OpenMP • MPI • Cuda • Habanero C • Multi2sim system simulator • OpenCV • Matlab • Octave • Visual Studio • Eclipse • RStudio • Excel • Latex

## AWARDS

2018 Awardee of prestigious INAE travel grant for presenting my paper in California

2015 Awardee of consistent performance at Programming Club of IIIT-Delhi

2010 Awardee of Gold medal by Science Olympiad Foundation

## EXPERIENCE

### QUALCOMM | CPU DESIGN ENGINEER

July 2018 - Present | Bengaluru, India
Working as a CPU design engineer for Qualcomm Snapdragon Processors (Medium, High Tier and Compute chips). Responsible for RTL and Power Aware designing, and looking at the interactions between Software and hardware design.

### NANYNAG TECHNOLOGICAL UNIVERSITY | Research Assistant + NTU-India Connect Scholar

August 2017 – December 2017 | Singapore | Prof. Lam Siew Kei
• Designed a dynamic memory authentication scheme for cyberphysical systems and improved upon it using cache-oblivious algorithms.
• The design was integrated in Multi2sim system simulator to study the performance impact with various SPEC and PARSEC benchmarks.
• Resulted in an average reduction of performance overhead by 20-30%.

### IIIT-DELHI | Research Assistant

August 2016 – April 2017 | Delhi, India | Prof. Sujay Deb
• Designed a scalable cache architecture with optimised coherency protocol.
• Integrated the design in Multi2sim system simulator and evaluated it using various SPEC and PARSEC benchmarks with different system sizes and cache configuration.
• Resulted in average reduction in coherence traffic by 50% and runtime by 32.67%. Also achieves a network energy savings of around 37.13%.

## PUBLICATIONS

### CONFERENCES

Sidhartha Shankar, Hemanta K. Mondal, Rohan Juneja, Sri Harsha Gade, Sujay Deb, "Dynamic NoC Platform for Varied Application Needs" in International Symposium on Quality Electronic Design (ISQED), 2018.

Saru Vig, Rohan Juneja, Siew Kei Lam, Guiyuan Jian, "Cache Oblivious Dynamic Skewed Tree for Fast Memory Authentication" in IEEE International Conference on Computer Design (ICCD), 2019. (Submitted)

### JOURNALS

Saru Vig, Rohan Juneja, Guiyuan Jiang, Siew Kei Lam, Changhai Ou, "Framework for Fast Memory Authentication using Dynamically Skewed Integrity Tree" in IEEE Transactions on Very Large Scale Integration (VLSI) Systems.

## PROJECTS

### NETWORK ON CHIP | Research Project

May 2016 - July 2016 | Delhi, India | Prof. Sujay Deb
Proposed a dynamic Network on Chip (DNoC) platform that optimises virtual channels and energy consumption without having any effect on the performance.

### WORK SHARING SCHEDULER

February 2017 - March 2017 | Delhi, India | Prof. Vivek Kumar
Built a light weight work-sharing runtime for async-finish parallelism, which uses pthread library with coding in C. [Code]

### ARM SIMULATOR

February 2015 - April 2015 | Delhi, India | Prof. Neeraj Goel
Built a functional simulator for execution of ARM assembly language instructions with coding in C language. [Code]