M.Sc. (INFORMATICS) / 1st Semester 2017

Paper IT12 – COMPUTER ARCHITECTURE

Time: 3 hrs. *Attempt any 5 questions.* **Max Marks: 75**

Question No.1 is compulsory.

(Write your Roll No. on the top immediately on receipt of this question paper)

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1. Each part carries 3 marks.

   a. Explain the truth table and working of an *exclusive-NOR* gate?

   b. Explain the need for "Timing and Control signals" in a digital computer?

   c. What should be the base (or radix) of the number system such that the following equation holds:

   $$[312 / 20]_r = [13.1_{10}]$$

   d. How many 128 X 8 memory chips are needed to provide a memory capacity of 4096 X 16?

   e. Differentiate between Dynamic and Static RAM? What do we mean by a Memory Address Map?

2.

   a. Simplify the Boolean function F together with don't care conditions d in
      i. Sum-of-products form
      ii. Product-of-sums form

   $$F(m, n, o, p) = \sum (2, 3, 5, 6, 13)$$
   $$d(m, n, o, p) = \sum (1, 4, 11)$$

   Compare their hardware implementations. **(8)**

   b. Show how a 9-bit microoperation field in a microinstruction can be divided into subfields to specify 46 microoperations. How many microoperations can be specified in one microinstruction? **(4)**

   c. What are the two instructions needed in the basic computer to set the E flip-flop to 1? **(3)**

3.

   a. Design a 4-bit count-down counter and derive a sequential circuit for the same. **(6)**

b. Write a program to unpack two characters from location WRD and store them in bits 0 through 7 of locations CH1 and CH2. Bits 8 through 15 should contain zeros. **(5)**

c. Show the bit configuration of a 24-bit register when its content represents the decimal equivalent of 295: **(4)**

i. in binary
ii. binary-coded octal
iii. binary-coded hexadecimal
iv. binary-coded decimal

4.

a. Show how a binary counter with parallel load can be made to operate as divide-by-10 counter (i.e. a counter that counts from 0 to 10 and back to 0)? **(7)**

b. A composite Adder-Subtractor circuit has the following values of mode M and data inputs A and B. In each case, determine the values of the outputs: S_3, S_2, S_1, S_0 and C_4 **(5)**

M	A	B
0	0111	0110
0	1000	1001
1	1100	1000
1	0101	1010
1	0000	0001

c. Obtain the 5's and 4's complement of the following numbers: **(3)**

i. $(132231)_5$
ii. $(100001)_5$
iii. $(444444)_5$

5.

a. Write an assembly program that evaluates the logic *exclusive-NOR* of two logic operands? **(5)**

b. Design a digital circuit that performs the four logic operations of *exclusive-OR, exclusive-NOR, NOR,* and *NAND*. Use two selection variables. Show the logic diagram of one typical stage. **(5)**

c. What is an interrupt procedure? Explain the differences between interrupt procedure and a sub-routine call? **(5)**

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6.

a. A computer has 16 registers, an ALU with 32 operations, and a shifter with 8 operations, all connected to a common bus system. **(5)**

i. Formulate a control word for a microoperation

ii. Specify the number of bits in each field of the control word and give a general encoding scheme

iii. Show the bits of the control word that specify the microoperation R4 ← R5 + R6

b. List and discuss the sequence of microoperations executed during the instruction cycle of ISZ (Increment and Skip if Zero) computer instruction. **(5)**

c. The 16-bit 2's complement representation of an integer is

1111 1111 1111 0101

What is its decimal representation? **(3)**

d. Which is the smallest integer that can be represented by an 8-bit number in 2's complement form? **(2)**