IC1512

M.Sc. (INFORMATICS) / 1st Semester 2015
Paper IT-12 – COMPUTER ARCHITECTURE

Max Marks: 75

Attempt any 5 questions.
Question No.1 is compulsory.
(Write your Roll No. on the top immediately on receipt of this question paper)

1. Each part carries 3 marks.

   a. List the truth table of a five-variable exclusive-OR function:
   x = A *xor* B *xor* C *xor* D *xor* E (3)

   b. Obtain the 4's complement for the following numbers: (3)
      i. $(1010101)_4$
      ii. $(123123)_5$
      iii. $(43214321)_5$

   c. What is the difference between hardwired control and micro-programmed control? Is it possible to have a hardwired control associated with a control memory? (3)

   d. Match the following: (3)

i. CMOS	(a) high speed operation
ii. MOS	(b) low power consumption
iii. ECL	(c) high component density

   e. What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? (3)

2.

   a. Design a three-bit count-up counter. This is a sequential circuit with 3 flip flops and one input x. When $x = 0$, the state of the flip-flops does not change. When $x = 1$, the state sequence is 000, 001, 010, 011… 111, and, repeat. (7)

   b. Derive the Boolean expression for the gate structure that clears the sequence counter SC to 0. Draw the logic diagram of the gates and show how the output is connected to the INR and CLR inputs of SC. *(Refer the Control functions and Micro-operations for the basic computer give at the end).* (6)

   c. Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro-operation to be performed in order to change the value in A to: (2)

i. 01101101
ii. 11111101

3.

a. Given the Boolean expression $F = x'y + xyz'$
   i. Derive an algebraic expression for the complement F
   ii. Show that $F.\bar{F} = 0$
   iii. Show that $F + \bar{F} = 1$
   (3)

b. Discuss the different shift micro-operations? (5)

c. What happens during the 2nd pass of an assembler? Explain the working using a flowchart. (7)

4.

a. Simplify the following Boolean function using a 6-variable K-map (4)

F (a, b, c, d, e, f) =Σ (0, 1, 2, 3, 12, 13, 14, 15, 24, 25, 26, 27, 36, 37, 38, 39, 48, 49, 50, 51)

b. Derive the circuits for a 3-bit parity generator and 4-bit parity checker using an even-parity bit. (6)

c. List the assembly language program generated by the compiler from the following high-level language program. Assume integer variables. (5)

```
SUM = 0
SUM = SUM + A + B
DIF  = DIF – C
SUM = SUM + DIF
```

5.

a. Show the value of all bits of a 12-bit register that hold the number equivalent to decimal 205 in (4)

   i. Binary
   ii. Binary-coded octal
   iii. Binary-coded hexadecimal
   iv. Binary-coded decimal

b. Design a combinational circuit with three inputs x, y, z and three outputs A, B, C. When the binary input is 0, 1, 2 or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. (3)

c. Discuss the mapping procedure used for mapping from instruction code to a micro instruction address? (5)

d. Define the following terms: (3)
   i. Encoder
   ii. Combinational Circuit
   iii. Register

6.

a. Consider the following register transfer statements for two 4-bit registers R1 and R2.

xT: R1 ← R1 + R2
$x'T$: R1 ← R2

Every time that variable T = 1, either the content of R2 is added to the content of R1 if x = 1, or the content of R2 is transferred to R1 if x = 0. Draw a diagram showing the hardware implementation of the two statements. Use block diagrams for the two 4-bit registers, a 4-bit adder, and a quadruple 2-to-1 line multiplexer that selects the inputs to R1. In the diagram, show how the control variables x and T select the inputs of the multiplexer and the load input of register R1. (5)

b. Design and explain the working of a 4-bit bidirectional shift register with parallel load.

(7)

c. Perform the arithmetic operations (+46) + (-23) and (-46) - (-23) in binary using signed-2's complement representation for negative numbers. (3)

Fetch	$R'T_0$:	$AR \leftarrow PC$
	$R'T_1$:	$IR \leftarrow M[AR]$, $PC \leftarrow PC + 1$
Decode	$R'T_2$:	$D_0, \ldots, D_7 \leftarrow$ Decode $IR(12\text{–}14)$, $AR \leftarrow IR(0\text{–}11)$, $I \leftarrow IR(15)$
Indirect	D_7IT_3:	$AR \leftarrow M[AR]$
Interrupt:		
$T_0T_1T_2(IEN)(FGI + FGO)$:		$R \leftarrow 1$
	RT_0:	$AR \leftarrow 0$, $TR \leftarrow PC$
	RT_1:	$M[AR] \leftarrow TR$, $PC \leftarrow 0$
	RT_2:	$PC \leftarrow PC + 1$, $IEN \leftarrow 0$, $R \leftarrow 0$, $SC \leftarrow 0$
Memory-reference:		
AND	D_0T_4:	$DR \leftarrow M[AR]$
	D_0T_5:	$AC \leftarrow AC \wedge DR$, $SC \leftarrow 0$
ADD	D_1T_4:	$DR \leftarrow M[AR]$
	D_1T_5:	$AC \leftarrow AC + DR$, $E \leftarrow C_{out}$, $SC \leftarrow 0$
LDA	D_2T_4:	$DR \leftarrow M[AR]$
	D_2T_5:	$AC \leftarrow DR$, $SC \leftarrow 0$
STA	D_3T_4:	$M[AR] \leftarrow AC$, $SC \leftarrow 0$
BUN	D_4T_4:	$PC \leftarrow AR$, $SC \leftarrow 0$
BSA	D_5T_4:	$M[AR] \leftarrow PC$, $AR \leftarrow AR + 1$
	D_5T_5:	$PC \leftarrow AR$, $SC \leftarrow 0$
ISZ	D_6T_4:	$DR \leftarrow M[AR]$
	D_6T_5:	$DR \leftarrow DR + 1$
	D_6T_6:	$M[AR] \leftarrow DR$, if $(DR = 0)$ then $(PC \leftarrow PC + 1)$, $SC \leftarrow 0$
Register-reference:		
		$D_7I'T_3 = r$ (common to all register-reference instructions)
		$IR(i) = B_i$ $(i = 0, 1, 2, \ldots, 11)$
	r:	$SC \leftarrow 0$
CLA	rB_{11}:	$AC \leftarrow 0$
CLE	rB_{10}:	$E \leftarrow 0$
CMA	rB_9:	$AC \leftarrow \overline{AC}$
CME	rB_8:	$E \leftarrow \overline{E}$
CIR	rB_7:	$AC \leftarrow$ shr AC, $AC(15) \leftarrow E$, $E \leftarrow AC(0)$
CIL	rB_6:	$AC \leftarrow$ shl AC, $AC(0) \leftarrow E$, $E \leftarrow AC(15)$
INC	rB_5:	$AC \leftarrow AC + 1$
SPA	rB_4:	If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$
SNA	rB_3:	If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$
SZA	rB_2:	If $(AC = 0)$ then $PC \leftarrow PC + 1)$
SZE	rB_1:	If $(E = 0)$ then $(PC \leftarrow PC + 1)$
HLT	rB_0:	$S \leftarrow 0$
Input-output:		
		$D_7IT_3 = p$ (common to all input–output instructions)
		$IR(i) = B_i$ $(i = 6, 7, 8, 9, 10, 11)$
	p:	$SC \leftarrow 0$
INP	pB_{11}:	$AC(0\text{–}7) \leftarrow INPR$, $FGI \leftarrow 0$
OUT	pB_{10}:	$OUTR \leftarrow AC(0\text{–}7)$, $FGO \leftarrow 0$
SKI	pB_9:	If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$
SKO	pB_8:	If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$
ION	pB_7:	$IEN \leftarrow 1$
IOF	pB_6:	$IEN \leftarrow 0$

(Control functions and Micro-operations for the basic computer)