

1613

**M.Sc. (Informatics), I Semester, 2013**  
**IT 15 – MICROPROCESSOR AND INTERFACE PROGRAMMING**

**Time: 3 Hours**

**Max. Marks: 75**

*Note: Attempt five questions in all, Question No. 1 is compulsory*

- 1 a) Registers AX, BX, CX, and DX contain, respectively, 1111H, 2222H, 3333H, and 4444H. What are the contents of each register after this sequence of instructions?

PUSH AX  
 PUSH CX  
 PUSH BX  
 POP DX  
 POP AX  
 POP BX

(2)

- b) Memory locations 00490H through 00493H contain, respectively, 0A, 9C, B2, and 78. What does AX contain after each instruction? (Assume that SI contains 00490H and that BP contains 0002.)

- (i) MOV AX, [SI+1]  
 (ii) MOV AX, [SI][BP]

(2)

- c) What is the difference between MOV AX, [40H] and LEA AX, [40H]?

(1)

- d) Using shift instruction how can you divide the number in BX by 32?

(2)

- e) Is it possible to perform a conditional jump that has a target address outside of the relative range of +127/-128 bytes?

(1)

- f) Why are input ports buffered rather than latched?

(2)

- g) Determine the mode words for each 8255 configurations :

- (i) Mode 0,  $A_{in}, B_{out}, C_{in}$   
 (ii) Mode 1,  $A_{out}, B_{in}$

(2)

- h) Counter 2 is to be programmed to generate a 63μs pulse when triggered. A 1-MHz clock is connected to CLK. What instructions are needed to use counter 2 as a one shot? Assume address for control word as 0CC83H and for output initial count as 0CC82H.

(3)

- 2 a) Given an array A(I) of 100 16 bit signed integer numbers. Write a programme to generate a new array B(I) so that

$B(I) = A(I) \quad \text{for } I = 1 \text{ and } 100$   
 and  $B(I) = A(I+2) \quad \text{for all other } I\text{'s}$

(7)

- b) Explain various flags of Processor Status Word.

(3)

- c) Explain various addressing modes of 8086  $\mu$ p.

(5)

- 3 a) Write a programme sequence to calculate the following

$(AX) \leftarrow \text{Quotient of } ((V - (X * Y + Z - 540)) / X)$

$(DX) \leftarrow \text{Remainder}$

Where V, X, Y and Z are of word length.

(5)

- b) Two byte - sized BCD Integers are stored at the symbolic offset addresses NUM1 and NUM2, respectively. Write an instruction sequence to generate their difference and store it at NUM3. The difference is to be formed by subtracting the value at NUM1 from that at NUM2. Assume that all storage locations are in the current data segment.

(5)

- c) Write an instruction sequence that generates a byte - size integer in the memory location defined as RESULT. The value of the integer is to be calculated from the logic equation

$$(RESULT) = (AL) * (NUM1) + (\overline{NUM2}) * (AL) + (BL)$$

(5)

Assume that all parameters are byte-sized. NUM1, NUM2, and RESULT are the offset addresses of memory locations in the current data segment.

- 4 a) Write a complete data segment DATA\_SEG that would assign the integer 1 to a byte NUM and the integers -1, 0, 2, 5, and 4 to the first five elements of the 10-word array DATA\_LIST. Then write a complete code segment that would :

- (i) Place the largest and smallest of the five numbers of DATA\_LIST in BX and DX, respectively.
- (ii) Calculate the sum and the product of the first five numbers in DATA\_LIST and store the result in SUM and PRODUCT, respectively.

(5)

- b) Design an Interface of an input port 74LS245 to read the status of switches SW<sub>1</sub> to SW<sub>8</sub>, and an output port 74LS373 with 8086. Display the number of a key that is pressed, i.e., from 1 to 8 on a seven segment display with the help of an output port. The input port address is 0008H and the output port address is 000AH.

(5)

c) Explain strobed bidirectional I/O mode of IC 8255.

(5)

5 a) Design a programmable timer using 8254 and 8086. Interface 8254 at an address 0040H for counter 0 and write the following assembly language programs. The 8086 and 8254 run at 6MHz and 1.5 MHz respectively.

- (i) To generate a square wave of period 0.5 ms.
- (ii) To interrupt the processor after 15ms.
- (iii) To derive a monoshot pulse with quasi stablestate duration of 7.5 ms.

(10)

b) Write a control for counter 1 that selects the following options : load least significant byte only, mode 5 of operation, and binary counting. What are the logic levels of inputs  $\overline{CS}$ ,  $\overline{RD}$ ,  $\overline{WR}$ ,  $A_1$  and  $A_0$  when the byte is written to 8254 ?

(5)

6 a) Interface DAC AD 7523 with an 8086 CPU running at 8MHz and write an assembly language programme to generate sawtooth waveform.

(4)

b) Explain the command words ICW1, ICW2, ICW3 and ICW4 of 8259 PIC.

(8)

c) What should be the OCW1 code if interrupt inputs  $IR_0$  through  $IR_3$ , are to be unmasked and  $IR_4$  through  $IR_7$  are to be masked ?

(3)