M.Sc. (Informatics) – Ist Semester - 2012
Paper IT12 – COMPUTER ARCHITECTURE

Time: 3 Hrs.   Max. Marks: 75
Total pages: 04

Write your Roll No. on the top immediately on receipt of the paper.

Note: Attempt any 5 questions. Question No.1 is compulsory.

1. Attempt any 5 parts. Each part carries 3 marks.

   a. Differentiate between Dynamic and Static RAM? What do we mean by a Memory Address Map?

   b. Define the following terms:
      i.   Computer Architecture
      ii. Computer Organization
      iii. Computer Design

   c. Obtain the 7's and 8's complement of the following 7 digit Octal numbers:
      i.   6543210
      ii. 0010101
      iii. 1000000

   d. While designing any basic computer, what should comprise as the "Inputs" and "Outputs" for a Control Logic circuit?

   e. Define the "Stack" data structure. Write pseudo code for the 'push' and 'pop' operations performed on a Stack?

   f. Explain the computer Interrupt cycle with the help of a flowchart?

2.
   a. Explain how Address Sequencing is performed in a Micro-programmed Control Unit?   (6)

   b. Draw the logic diagram of a 2-to-4 line decoder with only NOR gates. Include an Enable input?   (3)

   c. Write an Assembly Program used to calculate the XOR of two 8-bit numbers.   (3)

d. Write a program to evaluate the arithmetic statement: (3)

$$X = (A - B + (C * (D * E - F))) / (G + (H * K))$$

  i. Using a general register computer with three address instructions.
  ii. Using an accumulator type computer with one address instructions.
  iii. Using a stack organized computer with zero-address operation instructions.

3.

a. Design a memory system having 4096 bytes of RAM and 4096 bytes of ROM, using 128 X 8 RAM and 512 X 8 ROM chips. (4)

b. Convert the following: (3)
  i. $(13796)_{13}$ to be converted to Decimal.
  ii. $(13796)_{10}$ to be converted to Binary Coded Octal.
  iii. $(13796)_{10}$ to be converted to Binary Code Hexadecimal.

c. Define the following: (2)
  i. Micro-operations
  ii. Micro-instructions

d. Design a sequential circuit with two JK Flip Flops A and B and two inputs E and x. If E = 0, the circuit remains in the same state regardless of the value of x. When E = 1 and x = 1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00, and repeat. When E = 1 and x = 0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeat. (6)

4.

a. What is the need of a Common Bus System in a computer organization? Mention two different ways of constructing such a bus system. (2+4)

b. A digital computer has a memory unit of 64K X 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. (4)
  i. How many bits are there in the tag, index, block, and word fields of the address format?
  ii. How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.
  iii. How many blocks can the cache accommodate?

c. Formulate a mapping procedure that provides eight consecutive microinstructions for each routine. The operation code has six bits and the control memory has 2048 words. (3)

d. Explain the following addressing modes: (2)
   i. Register Indirect
   ii. Auto-Decrement

5.

a. Define the following: (4)
   i. Assembler
   ii. Address Symbol Table
   iii. Pseudo Instruction
   iv. Program Status Word

b. Design a four bit combinational circuit "Decrementer" using four full-adder circuits. (4)

c. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.
   i. How many bits are there in the operation code, the register code part, and the address part?
   ii. Draw the instruction word format and indicate the number of bits in each part.
   iii. How many bits are there in the data and address inputs of the memory? (3)

d. Describe the organization and working of an Associative memory? (4)

6.

a. What is an interrupt procedure? Explain the differences between interrupt procedure and a sub-routine call? (4)

b. First obtain an expression for the following circuit. Then simplify it by means of a K-Map and compare the two hardware implementations. (3)
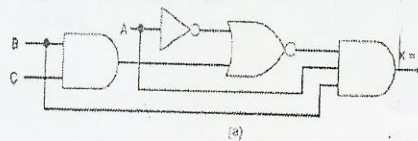
(a)

$$\left(\overline{A} + ab \cdot A \cdot B \right)$$

c. A digital computer has a memory unit with a capacity of 16,384 words, 40 bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no indirect mode bit). Two instructions are packed in one memory word, and a 40-bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer. (4)

d. Perform the following arithmetic operations with the decimal numbers using signed-10s complement representation for negative numbers. (4)
   i. (- 450) + (+ 360)
   ii. (- 450) – (+ 360)