Item #: LNA6112 Batch: *γηαρστοντεστ* Type: Substrate Item #:
Route: LN60AMXX Devices Full Flow, Rev 0 gharstontest WO: Substrate ID:
Expected Qty: 1 pc Comment: Traveler Review

1 LNCH9-1 Prepare Housing *HousePrep* Date In | Initial | Date Out | Initial

Prepare the housing: **P/N: MEC-100-0438**
Inspect and clean housing.
RF connector Instructions: **Install P/N: 30047-000**
Link to specification "Housing Preparation":
http://infocenter.thorlabs.local/sites/JSP/layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0236.docx

2 LNCH9-2 Mount Transition and Router in Housing *PartsInHouse1* Date In | Initial | Date Out | Initial

Install transition chip in housing **P/N: ELB-100-0066**
Install router chip in housing **P/N: ELB-100-0090**
Record the Transition and Router lot numbers.

RouterLot# _____
TransitionLot# _____
EpoxyLot# _____

List any additional installation parts and instructions:
Add epoxy from the RF Pin to the Transition.

Link to specification **"Housing Preparation":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0236.docx

3 LNCH9-3 Epoxy Cure *EpoxyCure* Date In | Initial | Date Out | Initial

4 LNCH9-4 Chip Inspection *ChipInspection* Date In | Initial | Date Out | Initial

Verify that the chip inspection has been completed.
If not, inspect chip and verify that the test data from the Fab was passing.
Link to specification "Chip Inspection":
http://infocenter.thorlabs.local/sites/JSP/layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0233.docx

AxProductionOrder _____

5 LNCH9-5 Attach Polarcor *AttachPolarcor* Date In | Initial | Date Out | Initial

Inspect chip and verify the Polarcor has been attached.
If not, attach Polarcor.
Link to specification **"Polarcor Attach Work Instructions":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0235.docx

6 LNCH9-6 Chip Paint *ChipPaint* Date In | Initial | Date Out | Initial

Inspect chip and verify the sides have been painted.
If not, paint sides before proceeding.
Link to specification **'Side Paint':**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0234.docx

Item #: LNA6112 Batch: *γηαρστοντεστ* Type: Substrate Item #:
Route: LN60AMXX Devices Full Flow, Rev 0 gharstontest WO: Substrate ID:
Expected Qty: 1 pc Comment: Traveler Review

Item #: LNA6112 Batch: *γηαρστοντεστ* Type: Substrate Item #:
Route: LN60AMXX Devices Full Flow, Rev 0 gharstontest WO: Substrate ID:
Expected Qty: 1 pc Comment: Traveler Review

7 LNCH9-7 Mount Chip in Housing *ChipInHouse* Date In | Initial | Date Out | Initial

Link to specification **"Epoxy Dispense":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0186.docx

Link to specification **"Chip Mount":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0238.docx

8 LNCH9-8 Check Alignment of Chip in Housing *ChipInHouseCheck* Date In | Initial | Date Out | Initial

Check the alignment of the chip to the TFN.

Link to specification **"Chip Mount":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0238.docx

9 LNCH9-9 Epoxy Cure *EpoxyCure* Date In | Initial | Date Out | Initial

10 LNCH9-10 Mount Termination Chip in Housing *TermInHouse* Date In | Initial | Date Out | Initial

Install Termination Assembly in housing **P/N: ELB-100-0045** TerminationLot# _____
Record the Termination Assembly lot number.

List any additional installation parts and instructions:

Link to specification **"Termination Installation":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0237.docx

11 LNCH9-11 Epoxy Cure *EpoxyCure* Date In | Initial | Date Out | Initial

12 LNWB-1 Wire bond *LNWirebond* Date In | Initial | Date Out | Initial

Wire bond chip to transition chips and termination chips.
Link to specification **"Wirebond Illustrations":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0239.docx

Item #: LNA6112 Batch: *γηαρστοντεστ* Type: Substrate Item #:
Route: LN60AMXX Devices Full Flow, Rev 0 gharstontest WO: Substrate ID:
Expected Qty: 1 pc Comment: Traveler Review

13 LNWB-2 Chips Split Off Here *ChipSelection* Date In | Initial | Date Out | Initial

This is an admin operation to stage batch prior to S11 test after wirebond.

Do not Track Out of this operation until the last chip is ready to continue to S11 after wirebond!!

Use the Split Batch function to separate chips for S11 test after wirebond into individual batches.
When Split Batch function offers a new batch name change the suffix from "sub#" to "###" of the ChipID.
Complete action of creating split lot, then select new split lot number from Tracking drop-down menu and TrackIn to continue processing chip.

14 LNWB-3 Register Serial Number for Chip *RegisterSerialNo* Date In | Initial | Date Out | Initial

Record chip and housing numbers.

ChipSerial# _____
HousingSerial# _____
HousingLot# _____

15 LNWB-4 Verify Chip Passed ChipTest *ChipVerification* Date In | Initial | Date Out | Initial

Verify chip serial number was from passing part at the Fab Chip Test
Passing Results meet these 3 criteria:

- RF Test: Pass
- Chip Test: Pass
- Defects: ____ (None - This should be empty for passing chips)

If data displayed in Pink Box at the bottom of the screen does not meet criteria, or the Pink Display Box is empty place lot on hold for engineering.

16 LNWB-5 S11 Test *S11Test* Date In | Initial | Date Out | Initial

Perform tests and indicate pass or fail.
Link to specification **"S11 after Wirebonding":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0267.docx

17 LNWB-6 Endface Cleaning before Pigtailing *EndfaceCln* Date In | Initial | Date Out | Initial

Clean end faces to prepare for pigtail.

18 LNWB-7 Package Inspection *PackageInsp* Date In | Initial | Date Out | Initial

Perform microscopic defect inspection.

Item #: LNA6112 Batch: *γηαρστοντεστ* Type: Substrate Item #:
Route: LN60AMXX Devices Full Flow, Rev 0 gharstontest WO: Substrate ID:
Expected Qty: 1 pc Comment: Traveler Review

19 LNPT-1 FTA Attach/Pigtailing *FTAAttach* Date In | Initial | Date Out | Initial

Pigtail Wavelength: **1550nm**
Connect Input Fiber: **P/N: FIB-100-0277**
For both fibers use Solder: **P/N: MEC-100-0508**
Connect Output Fiber: **P/N: FIB-100-0264**
Record all required data.
Link to specification **"Pigtail":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0241.docx

Note!! **Only measure and enter data for Out-PER on "P" devices - Otherwise leave field blank.**

SolderLot# _____
EpoxyLot# _____
In-PER _____
Out-PER (P ONLY) _____
LossWithEpoxy _____
In-LossAfterUV _____
In-PostSolderLoss _____
Out-LossAfterUV _____
Out-PostSolderLoss _____
In-InputFiberSN _____
Out-InputFiberSN _____

20 LNPT-2 Pigtailing Bake *PigtailBake* Date In | Initial | Date Out | Initial

Put the pigtailed LN device in the oven.
Temp: 90C degrees
Time: >= 3 hours
Link to specification **"Pigtail":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0241.docx

21 LNIT1-1 Initial Test *LNInitialTest* Date In | Initial | Date Out | Initial

Modulator and S-Parameter
Link to specification **"Initial & Final Test (Modulator, S-Parameter)":** http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0250.docx

Initial Test Loss _____

22 LNIT1-2 VPi at 1GHz Test *1GHzVPiTest* Date In | Initial | Date Out | Initial

Link to specification **"1GHz Vpi":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0251.docx

23 LNIT1-3 70 GHz S Parameter Testing *70GHzRFTest* Date In | Initial | Date Out | Initial

Perform 70 GHz S Parameter Testing

24 LNSL-1 Prepare Lid for Seal *PrepareLid* Date In | Initial | Date Out | Initial

Use Lid: **P/N: MEC-100-0462**
Use Moisture Getter: **P/N: CRS-100-0028**
Install RF Absorber? **YES**

Link to specification **"Getter & RF Absorber Application":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0268.docx

Item #: LNA6112 Batch: *γηαρστοντεστ* Type: Substrate Item #:
Route: LN60AMXX Devices Full Flow, Rev 0 gharstontest WO: Substrate ID:
Expected Qty: 1 pc Comment: Traveler Review

Item #: LNA6112 Batch: *γηαρστοντεστ* Type: Substrate Item #:
Route: LN60AMXX Devices Full Flow, Rev 0 gharstontest WO: Substrate ID:
Expected Qty: 1 pc Comment: Traveler Review

25 LNSL-2 Visual Inspection Before Seal *VisualInsp* Date In | Initial | Date Out | Initial

Collect and review all test data for all parts passing.
Link to specification **'Visual Inspection':**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0253.docx

26 LNSL-3 Seal Seam Vacuum Bake *SeamSealBake* Date In | Initial | Date Out | Initial

Bake the device in Vacuum Bake Schedule: 16 hours at 95°C
Link to specification **'Seam Seal Bake':**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0254.docx

27 LNSL-4 Seal Lid Seam *SeamSeal* Date In | Initial | Date Out | Initial

Use Lid: **P/N: MEC-100-0462**
Seal Seal Program **Recipe: 24**
Link to specification **'Seam Seal':**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0255.docx

28 LNSL-5 Leak Test *LNLeakTest* Date In | Initial | Date Out | Initial

Link to specification **"Leak Test":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0245.docx

29 LNBI1-1 BurnIn with Active Test *BurnInActive* Date In | Initial | Date Out | Initial

Perform BurnIn with device mounted in correct Optical/Electric configuration.
Link to specification **"Burn-In":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0256.docx

30 LNBI1-2 Post Seal Final Test *PostSealFinalTest* Date In | Initial | Date Out | Initial

Modulator and S-Parameter Final Test Loss _____
Link to specification **"Initial & Final Test (Modulator, S-Parameter)":** http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0250.docx

31 LNBI1-3 VPi at 1GHz Test *1GHzVPiTest* Date In | Initial | Date Out | Initial

Link to specification **"1GHz Vpi":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0251.docx

Item #: LNA6112 Batch: *γηαρστοντεστ* Type: Substrate Item #:
Route: LN60AMXX Devices Full Flow, Rev 0 gharstontest WO: Substrate ID:
Expected Qty: 1 pc Comment: Traveler Review

Item #: LNA6112 Batch: *γηαρστοντεστ* Type: Substrate Item #:
Route: LN60AMXX Devices Full Flow, Rev 0 gharstontest WO: Substrate ID:
Expected Qty: 1 pc Comment: Traveler Review

32 LNBI1-4 70 GHz S Parameter Testing *70GHzRFTest* Date In | Initial | Date Out | Initial

Perform 70 GHz S Parameter Testing

33 LNFR-1 Final Prep & Packaging for Shipment *LNFinalPrep* Date In | Initial | Date Out | Initial

Link to specification **"Final Packaging":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0202.docx

34 LNFR-2 Final Review and Seal *LNFinalReview* Date In | Initial | Date Out | Initial

Review device labeling.
Link to specification **"Final Packaging":**
http://infocenter.thorlabs.local/sites/JSP/_layouts/WordViewer.aspx?id=/sites/JSP/PackageAssembly/WI-0202.docx

Item #: LNA6112 Batch: *γηαρστοντεστ* Type: Substrate Item #:
Route: LN60AMXX Devices Full Flow, Rev 0 gharstontest WO: Substrate ID:
Expected Qty: 1 pc Comment: Traveler Review