Baud Rate Generator Using Verilog

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Abstract— **This paper aims on designing a Baud Rate generator. Baud Rate is the number of symbols transmitted or received per second. It helps two devices to communicate with each other. It also specifies how fast data can be sent over a serial line or serial interface.**

Keywords— **Baud Rate, Baud Rate Generator, Verilog code, Sampling**

I. INTRODUCTION

The Baud rate generator is nothing but a frequency divider. It helps two devices in communicating with each other. When data is sent from transmitter to receiver then the data at the receiver side is sampled at a particular baud rate. [1] If there is a high mismatch between the baud rate of transmitter and receiver then the sampling will not happen at the centre of the bit period and there will be an offset. Due to the offset, there will be information that will be missed and communication will not occur efficiently. For example, if transmitter transmit at a particular rate and the receiving device only expects half of that data rate then half of the information will be lost [2].

II. PROJECT IMPLEMENTATION

The block diagram of the baud rate generator is given in the fig 1. The input to the system is Clock, Baud rate select, reset. The output is the clock with the frequency corresponding to the baud rate. The Verilog code for this system works is based on the following logic.

[3]The system works on positive edge triggered clock and has a divisor parameter. The select line is used to decide which baud rate to be selected. There is counter variable which count to a certain calculated value depending on the selected Baud rate. The clock goes from high to low or low to high each time the counter reaches the calculated value thus leading to different frequency of clock. The output clock is set to system clock, in case the reset button is pressed.
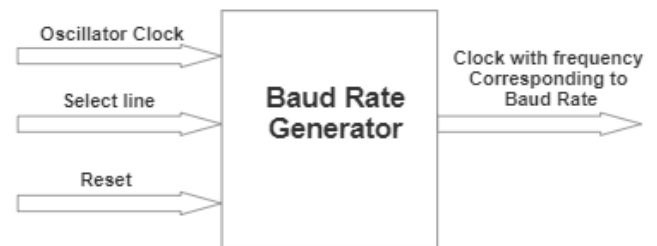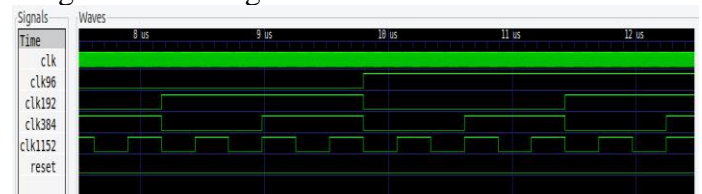

Fig 1. Block Diagram for Baud Rate Generator

Fig 2. Output waveform of Clock for different Baud Rate

REFERENCES

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