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An Advanced Traffic Light Controller using Verilog HDL

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Abstract: Traffic control is a challenging problem in many cities. This is due to the large number of vehicles and the high dynamics of the traffic system. Poor traffic systems are the big reason for accidents, time losses. In this it will reduce waiting time of the vehicles at traffic signals. Traffic Light Control (TLC) system also based on microcontroller and microprocessor. But the disadvantage of with microcontroller or microprocessor is that it works on fixed time, which is functioning according to the program that does not have the flexibility of modification on real time basis. In traffic light controller, density of traffic is sensed by using IR sensors throughout day and night, and accordingly time is allotted for users to pass. Other advantages of this system are: i) System senses emergency vehicles on the individual road moreover it gives priority to the traffic of that particular road where the emergency vehicles is sensed. ii) Finds out defaulter who crosses the red signal by capturing images using camera. In this, we are using FPGA with traffic sensors to control traffic according requirement means we can change the program if it require and thus reduces the waiting time. The hardware design has been developed using Verilog Hardware Description Language (HDL) programming. The output of system has been tested using Xilinx14.3.

Keywords: FPGA, FSM (Finite state machine), Traffic Light Controller.

I. INTRODUCTION

At road intersections traffic lights or traffic lamps or traffic signals are generally positioned so as to control the traffic flow. It is an electronic system generally installed on an intersection so as to notify the safety related issues with the help of specific predefined color system (usually red, yellow and green). Traffic Light controller (TLC) has been implemented using ASICs, FPGAs and microcontrollers. Some of the advantages of FPGA over microcontroller, it includes the number of I/O ports, speed of processing and performance, all of which are extremely critical in the design of TLC. The cost also is an extremely important issue in design of TLC. The reduced cost increasing the use of FPGAs (Field Programmable Gate Arrays) for verification and implementation of an Implemented system. Conventional traffic control systems has two major drawbacks: First, due to lack of adjustments in timings of traffic signals, the traffic has to wait a long on the lane with few vehicles while on same lane, the traffic cannot pass through in short time due to rush on lane. Second, there is no provision of movement of emergency vehicles like ambulance and fire brigades etc. In rush hours these emergency vehicles have to wait a long and results in human and financial loss. So, there is a need to develop a secure, fast and reliable traffic control system capable to control the vehicular traffic in rush hours without a need of traffic sergeant. In this, we implemented a real traffic control system using Verilog Hardware Description language. We use different modeling styles to implement state machines to improve the readability of code and to increase the speed. The effect of state encoding on the size of synthesized circuit is also realized. The implemented architecture is then tested for the validation of the design on Xilinx software.

II. FSM MODELING AND STATE DIAGRAM

The traffic light controller is a sequential circuit and is modeled as a finite state machine. The number of states is a function of the number of intersections chosen and hence variable. For the purpose of description, a state machine for preliminary case of four intersections is described. The working of the state machine is described as follows. Each state in the state diagram corresponds to a traffic intersection. The transition from one state to other is dependent on the timer.

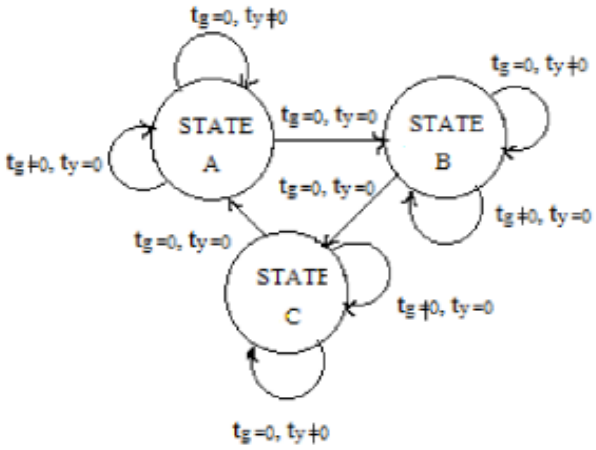

Fig 1. FSM State Diagram.

When the state machine is in a particular state, first of all, the green light corresponding to a particular lane glows for the duration as predefined by the user. Afterwards, the yellow light for the corresponding intersection is turned on for a predefined specific duration. Till this time, the remaining lanes show red light. Once the timer counts down completely, the machine switches to the next state. The state diagram is as shown in Fig.1.tg and ty correspond to duration of green light and yellow light respectively. When tg, ty are non-zero, green light is turned on for the particular intersection and red for all the remaining ones. When tg is zero, ty is non-zero, yellow light is switched on for the particular intersection and when both the timers reach zero, red light is switched on the particular intersection and the machine moves to next state and the same procedure is repeated for the next intersection.

A. TLC FLOW CHART

The Flow Chart shown in Fig. 2 illustrates the actions to be taken by the road users. Initially, all RED signals are ON and after few seconds, GREEN of a signal light in one particular direction will be ON to allow traffic in straight, right and left (left also sometimes needed) paths. The yellow light is split into two phases as yellow signal1 (Y1) and yellow signal2 (Y2). Pedestrian will be “OFF” in yellow signal1 (Y1) and pedestrian will be “ON” in yellow signal2 (Y2) so as to allow the pedestrians to cross the road.

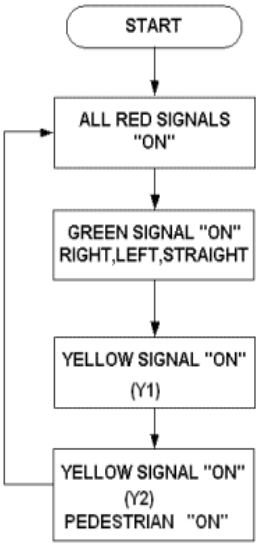

Fig 2. TLC Flow Chart.

At first the North traffic will be allowed to move and then traffic in the East, South and West direction will be allowed to move in sequence. The advantage of writing Traffic Light Controller program is that in a program, modifications as per requirements can be done easily i.e., suppose the traffic on main road should be allowed for more time and for side roads the traffic should be allowed for less time; then the clock is divided in such a way that for main road the clock period will be more and for side roads the clock period will be less, this is because the main road traffic is heavy when compared to the side road traffic. In general TLC System will be having three lights (red, green and yellow) in each direction where red light stands for traffic to be stopped, green light stands for traffic to be allowed and yellow light stands for traffic is going to be stopped in few seconds. But in this paper, yellow light is split into two phases and are included in the signaling lights along with red and green lights in order to indicate that in the first phase of yellow light, pedestrian will be OFF and in the second phase, pedestrian will be ON. The sequential order of the flow chart helps the programmer in the design regarding the flow of the program. North/ south-bound traffic will start with a green signal light while all the other lanes being red, the traffic will be stopped. After a predetermined time, the north/south traffic light turns yellow and then to red, allowing the east/west signal light to be green and the same sequence as the north/south-bound traffic is followed. The system will continue to be in this loop until an indication of a vehicle in a left turn lane occurs. When the signal light turns yellow, the controller scans the inputs. If high, then the program will jump to a subroutine which has a different light sequence. This sequence controls the main lights along with the left turn lights. After completion of the subroutine sequence, the program returns to the main loop.

III. FIELD PROGRAMMABLE LOGIC ARRAY

A field-programmable gate array (FPGA) is a semiconductor device that can be configured by the designer after manufacturing hence the name "field-programmable". By using a logic circuit diagram or a source code in a hardware description language (HDL) FPGAs are programmed. This program is reprogrammable by designer when it necessary .If FPGA is programmed by user then also user can edit or change the program. Implemented program in FPGA shows the working of chip or kit. They can be used to implement any logical function that an application-specific integrated circuit (ASIC) could perform, but the ability to update the functionality after shipping offers advantages for many applications. The system has been implemented in hardware using Spartan-3E FPGA.

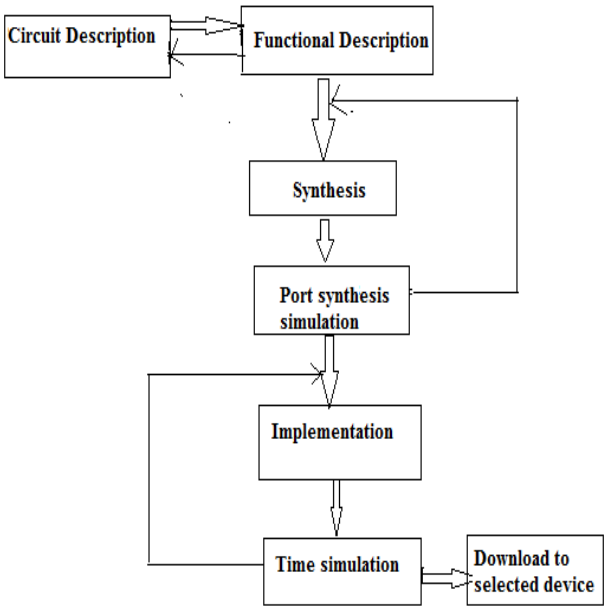

Fig3. FPGA Design Flow.

FPGA design flow is shown in Fig3. According to that start with circuit description in which all the circuit is designed by logic gats which is done by using Hardware Description Language (HDL). Then functional description was done which is followed synthesis and post Synthesis simulation. FPGAs have gained rapid acceptance and growth over the past decade because they can be applied to a very wide range of applications. A list of typical applications includes: random logic, integrating multiple SPLDs, device controllers, communication encoding and filtering, small to medium sized systems with SRAM blocks. Other interesting applications of FPGAs are prototyping of designs later to be implemented in gate arrays, and also emulation of entire large hardware systems.

IV. FOUR ROAD TRAFFIC STRUCTURE:

Here Ti is the traffic of I road, e.g. Tl- traffic of 1st road, RC is Infrared sensor for activation of camera module. SS is a sound sensor for detection of emergency vehicle. For traffic T1, sensors a1, a2, a3 are installed at different distances, respectively. Similarly for traffic T2, T3 and T4 sensors installed b, c, d respectively. All these sensors are installed as per the earlier said distance of Tl traffic. Fig. 4. Shows, four way traffic with sensor module .

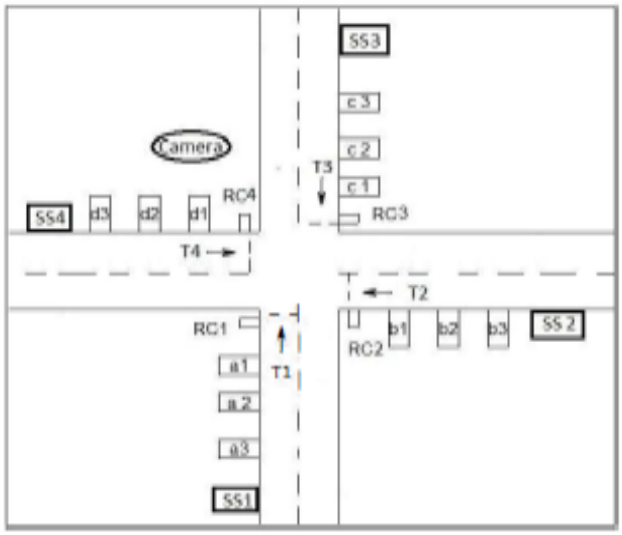

Fig 4. Four way traffic with sensor module.

If any one of the road's IR sensor is sensed, respective time is given as per the no. of sensors, which sensed the input for the particular traffic to pass. But if again the same sensor senses the signal then controller checks for other roads sensor's status and provides the service accordingly. For switching of traffic lights from one state to another, following method is executed:

1. When provided pass time for a particular traffic is about to finish and still vehicles are available on current traffic road then current pass signal turns red only if vehicle on other Road is sensed, otherwise current traffic road signal remains green.
2. When the allotted time of a current traffic finishes and still there is no traffic on current as well as on other roads, then current traffic road signal remains green unless other roads Sense traffic .

V. SIX ROAD TRAFFIC STRUCTURE

A. State Diagram

The State diagram contains states SOS50. There will be transition from one state to other as per the traffic available on the road. State S22 is for allowing the traffic of road in which emergency vehicle is sensed, accordingly any one out of S23, S24, S25, S26, S43, S46 is executed. State Sl is executed only if no road is having emergency vehicle. State Sl checks the activated sensor with priority of checking sequence a, b, c, d, e, f and accordingly pass time is given for traffic to pass.

Table1. IR Sensor Status As Per State Table

Traffic of Road	State responsible For allowing to Traffic to pass	Traffic light	Sensor status			Time alloted for Respective traffic light(SEC)
	S0	Red	If sound sensor sensed states=s22 ,otherwise s1			
	S1	Red	For a=>s2, b=>s3, c=>s4, d=>s5			
T1	S2	Red	a[2]	a[1]	a[0]	0 [Sensor a is sensed]
	S6		1	0	0	6
	S7		1	1	0	12
	S8	Green	1	1	1	15
	S9	Yellow				3
T2	S3	Red	b[2]	b[1]	b[0]	0 [Sensor b is sensed]
	S10		1	0	0	6
	S11		1	1	0	12
	S12	Green	1	1	1	15
	S13	Yellow				3
T3	S4	Red	c[2]	c[1]	c[0]	0[Sensor c is sensed]
	S14		1	0	0	6
	S15		1	1	0	12
	S16	Green	1	1	1	15
	S17	Yellow				3
T4	S5	Red	d[2]	d[1]	d[0]	0[Sensor d is sensed]
	S18		1	0	0	6
	S19	Green	1	1	0	12
	S20		1	1	1	15
	S21	Yellow				3
T5	s5	Red	e[2]	e[1]	e[0]	0[Sensor e is sensed]
	S35		1	0	0	6
	S36	Green	1	1	0	12
	S37		1	1	1	15
	S38	Yellow				3
T6	s6	Red	f[2]	f[1]	f[0]	0[Sensor f is sensed]
	S39		1	0	0	6
	S40	Green	1	1	0	12
	S41		1	1	1	15
	S42	Yellow				3

Table2 shows an interpretation of States, Traffic of corresponding roads, sensors status, and time given for green and yellow light. If sensor al detects the traffic, al=l, Otherwise al =0. e.g. sensors a[2],a[1],a[0] are used to check the traffic intensity of road 1.

Table 2. Traffic pass time with sensors activation

Road	State	Light	Sound sensor	Time
T1	S22	Red	Ss1=1	
	S31	Red		3
	S27	Yellow		4
	S23	Green		15
T2	S32	Red	Ss2=1	3
	S28	Yellow		4
	S24	Green		15
T3	S33	Red	Ss3=1	3
	S29	Yellow		4
	S25	Green		15
T4	S34	Red	Ss4=1	3
	S30	Yellow		4
	S26	Green		15
T5	S45	Red	Ss5=1	3
	S44	Yellow		4
	S43	Green		15
T6	S48	Red	Ss6=1	3
	S47	Yellow		4
	S46	Green		15

C. Provision of Allowing Emergency Vehicles

It is our social responsibility to allow the emergency vehicle to pass first. But sometimes the emergency vehicles get stuck in the traffic jams or they have to wait in a queue till they are allowed to pass. Here an emergency vehicle is detected by using the sound sensors (ss1, ss2, ss3, ss4, ss5, and ss6). According to the signal sensed by the sound sensor, controller checks whether the detected sound signal is from the same road and then allows the traffic to flow until emergency vehicle has passed. Otherwise allow the traffic of road in which emergency Vehicle is in queue to pass, blocking other traffic. After passing of emergency vehicle default sequence of traffic flow continues.

D. Camera module

When the allowed traffic is passing that is respective RC sensor senses logic 1 and remaining RC sensor receives logic 0, then logic 0 is provided to the camera and camera is in ideal position. If along with the allowed traffic, traffic of a restricted road is trying to cross the respective RC sensor then logic 1 is provided to camera module and it captures images, which are forwarded to Road Traffic Authority for further action.

V. SIMULATION RESULTS

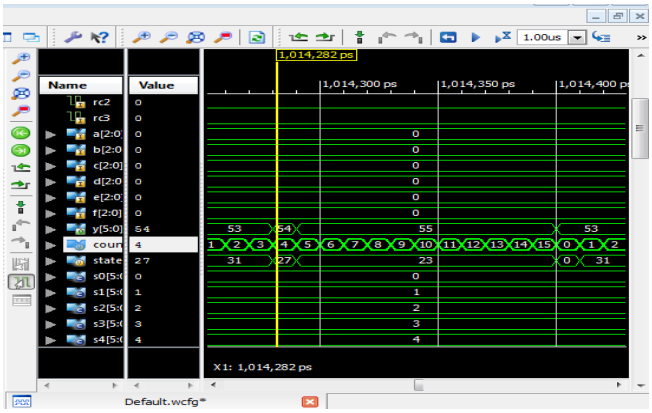

Fig5.

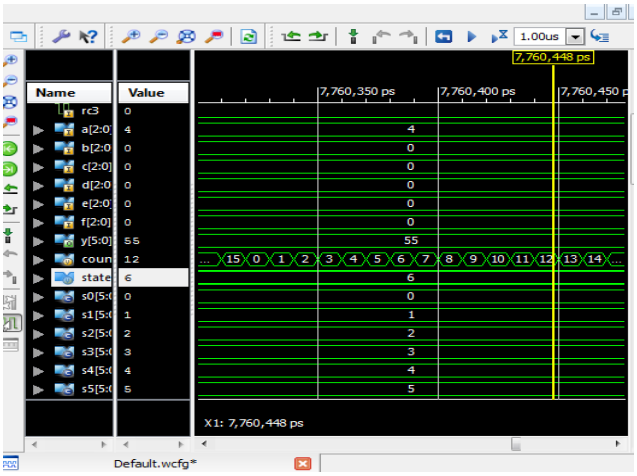

Fig6.

VI. CONCLUSION AND FUTURE WORK

The modern ways of multi-way traffic management improves the traffic condition up to a large extent. Traffic intensity is sensed and accordingly time is allotted for traffic to pass. The main feature of this study is the dynamic traffic pass time allocation and provision to detect the emergency vehicles like ambulance, fire brigade etc, giving them priority to pass first and then traffic resumes normally. Camera module is used to find the defaulter for crossing the red signal by means of sensors. This Design works with same efficiency at day and night time due to installation of IR sensors for providing dynamic traffic time. Verilog HDL is used to circuit description, code is generated which is simulated using xilinx14.3. This can be enhanced in such away as to control automatically the signals depending on the traffic density on the roads using sensors like IR detector/receiver module extended with automatic turn off when no vehicles are running on any side of the road which helps in power consumption saving.

A lot of development ideas for work in future such as using solar energy (independent power supply, i.e. saving the power). Using the GPRS map as an additional step for development and choosing the best road for the emergency and police vehicles. For national highways we can also design the 8 road traffic light controllers.

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