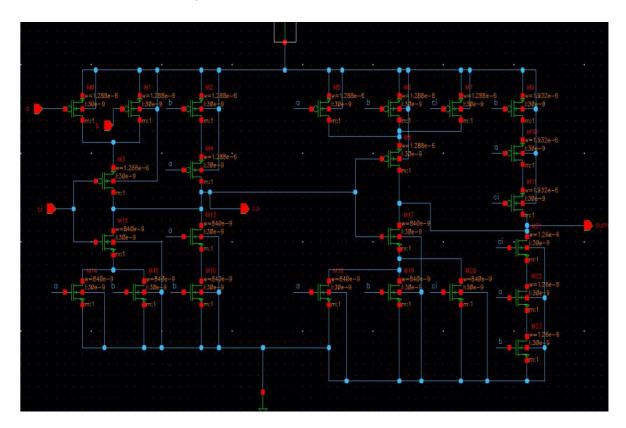
EEE 591

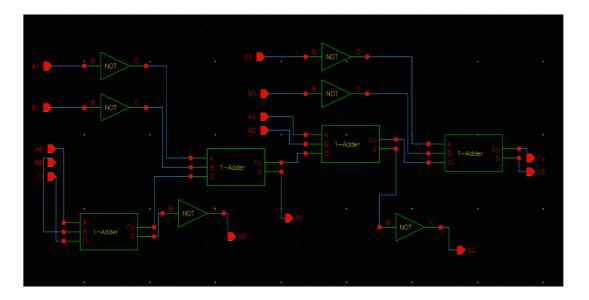
LAB #04

- 1. Full adder schematic and sizing
 - Explain the sizing criteria used
 Width of NMOS is 420nm
 Width of PMOS as 630nm.
 - b. Provide the sizes (W/L) of all your transistors



TRANSISTORS	TYPE	WIDTHS
M0-M9	pmos	1.288µm
M9-M11	pmos	1.932µm
M12-M20	nmos	840nm
M21-M23	nmos	1.260µm

c. Provide the schematic of your 4-bit design



d. Provide any scaling you choose to do for the 4-bit design and justification for the choice No scaling is required because met all the requirements.

2. Simulation results

a. Include the worst-case delay plots

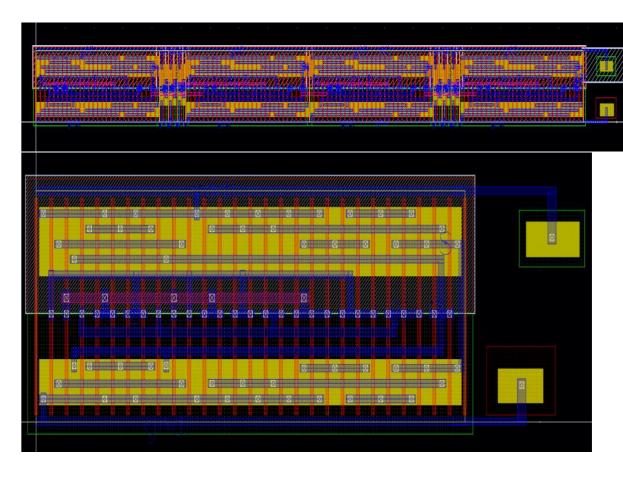


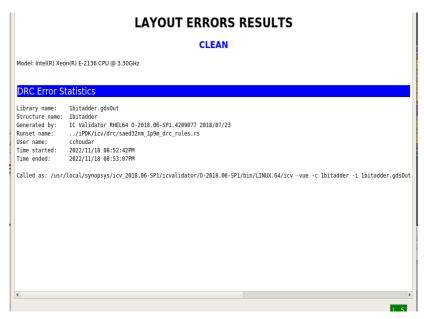
b. Include the power consumption analysis results

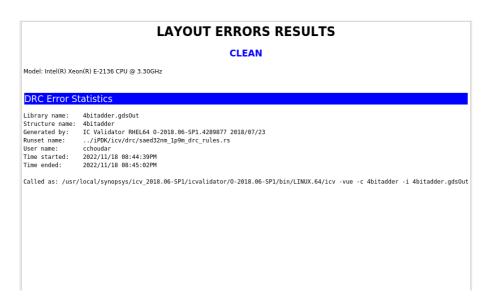
```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.temp 25'
pow totcurrent temper alter#
7.879e-05 -4.2411e-13 25.00000 1
```

Power consumption =78.79 micro watts.

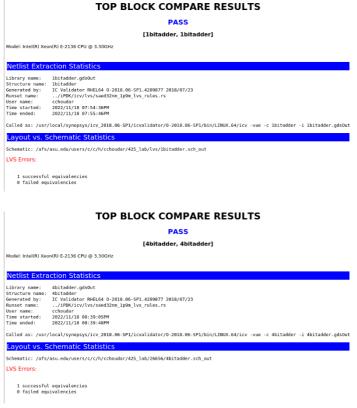
- 3. Include confirmation of
 - a. Layout & DRC Pass







b. Layout & LVS Pass



4. Report the total area of your layout Total Area=1.52*21.542 μ m= 32.743 μ m²

5. Report your overall score as outlined in the lab document

```
Score = (400 \text{ps/Delay}) + (100 \mu \text{W/Power}) + (150 \mu \text{m}^2/\text{Area})

Score = (400 \text{ps/}80.4 \text{ps}) + (100 \mu \text{W/}78.79 \mu \text{W}) + (150 \mu \text{m}^2/32.743 \mu \text{m}^2)

Score = 10.825
```

Name :- Chandra Rohith Choudary.

ASUID:-1226277600

PARAMETERS	VALUE'S
Delay	80.4ps
Power Consumption	78.79µW
Area	32.74µm²
Score	10.825