**VERIFICATION TEST PLAN**

ECE-593: Fundamentals of Pre-Silicon Validation  
Maseeh College of Engineering and Computer Science  
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A close up of a logo

AI-generated content may be incorrect.

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# Introduction:

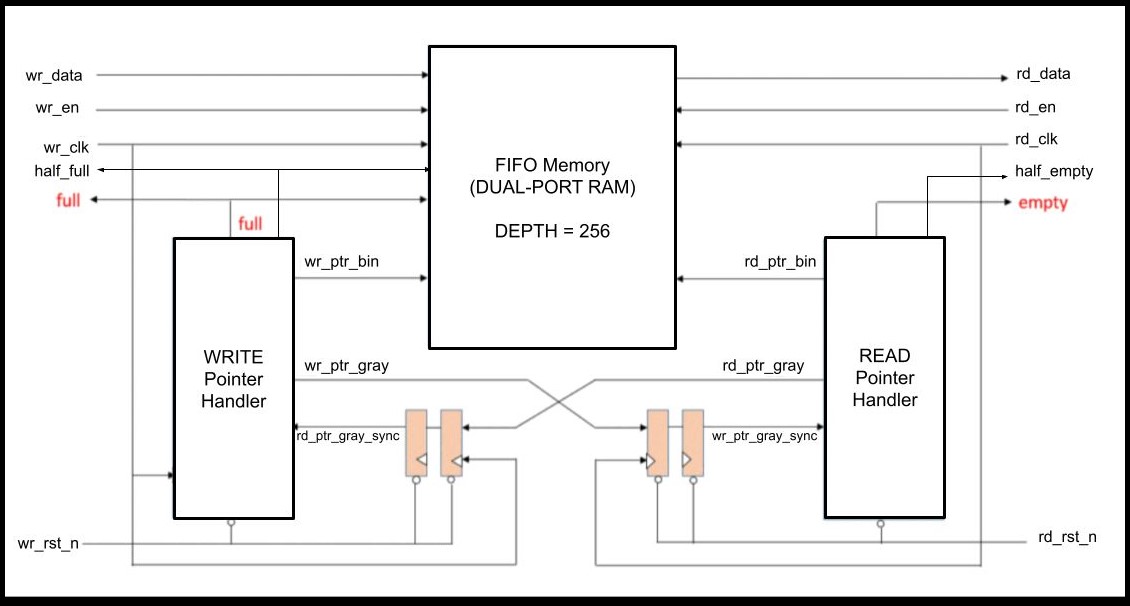
This document outlines the verification plan for the Asynchronous FIFO designed by Team 8.

## Objective of the Verification Plan

This verification effort aims to catch every corner-case and verify that the async\_fifo reliably transfers data between the 500 MHz write domain and the 250 MHz read domain. Confirmations include:

* Data written by the write interface emerges correctly on the read side in order, even when the FIFO wraps around.
* Status indicators (full, empty, half\_full, half\_empty) behave precisely at defined thresholds.
* Reset logic returns the FIFO to a known, empty state in every scenario.

**Top Level block diagram**

Below is the custom block diagram for our async‑FIFO design. It highlights the dual‑port memory, write and read pointer handlers, and two‑stage CDC synchronizers for pointer crossing between the 500 MHz write and 250 MHz read domains.  
  


**Figure 1.1:** Async FIFO Top‑Level Architecture

Key elements shown in the diagram:

* **FIFO Memory (Dual‑Port RAM):** 256‑deep, 32‑bit width, supports simultaneous write and read.
* **Write Pointer Handler:** Drives wr\_ptr\_bin and wr\_ptr\_gray; synchronizes incoming rd\_ptr\_gray via two flip‑flop CDC (rd\_ptr\_gray\_sync1\_w, rd\_ptr\_gray\_sync2\_w). Generates full and half\_full flags.
* **Read Pointer Handler:** Drives rd\_ptr\_bin and rd\_ptr\_gray; synchronizes incoming wr\_ptr\_gray via two flip‑flop CDC (wr\_ptr\_gray\_sync1\_r, wr\_ptr\_gray\_sync2\_r). Generates empty and half\_empty flags.
* **Status Flags:** full asserted when the write pointer in Gray domain is about to overlap the synchronized read pointer. half\_full when occupancy ≥128. empty when synchronized write pointer equals read pointer Gray. half\_empty when occupancy ≤128.

## Design Specifications

* **Data Width:** 32 bits
* **Depth:** 256 entries (ADDR\_WIDTH = 8 + 1 bit extra MSB)
* **Write Clock (wr\_clk):** 500 MHz (2 ns period)
* **Read Clock (rd\_clk):** 250 MHz (4 ns period)
* **Idle Cycle Assumptions:** write idle = 2 cycles, read idle = 1 cycle;
  + Effective write idle period = 3×2 ns = 6 ns
  + Effective read idle period = 2×4 ns = 8 ns
* **Burst Length:** 1024 words
* **FIFO Depth Calculation:**
  + Total write time = 1024 × 6 ns = 6144 ns
  + Words read in that time = 6144 ns ÷ 8 ns = 768
  + Depth required = 1024 – 768 = 256 entries
* **Key Functions:** Gray↔Binary pointer conversion, CDC synchronization, status flag generation.

# Verification Requirements

## Verification Levels

### What hierarchy level are you verifying and why?

We will verify the async\_fifo module at the RTL block level, as it encapsulates all logic for memory, pointer manipulation, CDC, and flag generation. Verifying at this level allows full control over stimuli and direct observation of internal state.

### How is controllability and observability at the level you are verifying?

**Controllability:** All primary inputs (wr\_clk, wr\_rst\_n, wr\_en, wr\_data, rd\_clk, rd\_rst\_n, rd\_en) are directly driven by the testbench.

**Observability:** Primary outputs (rd\_data, full, half\_full, empty, half\_empty) and internal pointers (wr\_ptr\_bin, rd\_ptr\_bin) are monitored.

### Are the interfaces and specifications clearly defined at the level you are verifying. List them.

**Interface & Specification Listing**

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal** | **Direction** | **Width** | **Description** |
| wr\_clk | input | 1 | Write-side clock (500 MHz) |
| wr\_rst\_n | input | 1 | Active-low reset for write domain |
| wr\_en | input | 1 | Write enable |
| wr\_data | input | 32 | Data bus for write |
| rd\_clk | input | 1 | Read-side clock (250 MHz) |
| rd\_rst\_n | input | 1 | Active-low reset for read domain |
| rd\_en | input | 1 | Read enable |
| rd\_data | output | 32 | Data bus for read |
| full | output | 1 | FIFO full status |
| half\_full | output | 1 | FIFO half-full status |
| empty | output | 1 | FIFO empty status |

# Required Tools

## List of required software and hardware tool sets needed.

* **Simulation:** Mentor Graphics QuestaSim or Synopsys VCS
* **Verification Language:** SystemVerilog
* Source code: <https://github.com/RohithInti/Team_8_Async_FIFO>

## Directory structure

Design, object oriented, and basic testbenches will be in separate source directories.

ECE593\_Team8

+ rtl\_source

+ testbench

+ work

+ results

# Risks and Dependencies

|  |  |  |
| --- | --- | --- |
| **Risk** | **Impact** | **Mitigation** |
| CDC metastability on pointer sync | Occasional synchronization failures | Two-stage synchronizer; assertion for max latency |
| Pointer arithmetic overflow | Incorrect full/empty signaling | Thorough corner-case tests; formal check of bin2gray/gray2bin |
| Reset-domain crossing | Inconsistent pointer initialization | Reset synchronization; stress tests at reset boundaries |

**Resolved Warnings and Errors from Milestone 1**

* **Implicit Net Type Warnings**: All signals are now declared logic or bit, and an explicit interface encapsulates DUT ports, eliminating implicit net-type compiler warnings.
* **Multiple Driver Conflicts**: Migrated from direct port assignments in top-level TB to a virtual interface in the class-based driver, removing multiple-driver warnings.
* **Port Mismatch & Missing Port Warnings**: Updated top.sv instantiation to match all DUT ports (half\_empty, half\_full, etc.), resolving port width and missing-connection errors.
* **Queue Underflow Errors**: In scoreboard, added model\_q.size() check before pop\_front(), eliminating runtime underflow errors when reads preceded writes.
* **Race Condition Warnings**: Replaced mixed blocking assignments in clocked contexts with non-blocking (<=) and always\_ff, ensuring consistent simulation semantics.
* **Sticky Flag Semantics**: Adjusted half\_empty update to include && !empty\_next guard, preventing flag assertion when FIFO is empty and resolving functional coverage holes.

# Functions to be Verified

## Functions Included

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| |  | | --- | | **Function** | | |  | | --- | | **Description** | | |  | | --- | | **Notes** | |
| |  | | --- | | Binary-to-Gray conversion | | |  | | --- | | bin2gray() function | | |  |  | | --- | --- | |  | Exhaustive input tests | |
| |  | | --- | | Gray-to-Binary conversion | | |  | | --- | | gray2bin() function | | |  | | --- | | Back-to-back conversion checks | |
| |  | | --- | | Write pointer increment & memory write | | |  |  |  | | --- | --- | --- | | Pointer increment when wr\_en && !full |  |  | | |  | | --- | | Verify data integrity and pointer wrap-around | |
| |  | | --- | | Read pointer increment & memory read | | |  | | --- | | Pointer increment when rd\_en && !empty | | |  | | --- | | Verify data matches write history | |
| |  | | --- | | Status flag generation | | |  | | --- | | full, half\_full, empty, half\_empty logic | | |  | | --- | | Boundary and mid-point checks | |
| |  | | --- | | CDC synchronizer | | |  | | --- | | Two-stage Gray-pointer sync across domains | | |  | | --- | | Monitor sync latency | |

## Critical vs. Non‑Critical Functions

|  |  |  |
| --- | --- | --- |
| **Function** | **Criticality** | **Description** |
| Full/Empty flag logic | Critical | Prevents overrun/underrun |
| Memory read/write operations | Critical | Data corruption risk |
| Pointer conversions | Critical | Ensures correct addressing |
| Half-full/half-empty flags | Non‑Critical | Used for flow-control hints, not for fundamental safety |

# Tests and Methods

## Testing Methodology

### Box-Level Approach

* **Black-Box:** Stimulate the DUT purely via its input ports (wr\_en, wr\_data, rd\_en) and observe outputs (rd\_data, full, empty, half\_full, half\_empty) without inspecting internal signals. This validates end-to-end functional behavior.
* **White-Box:** Leverage visibility into internal pointers (wr\_ptr\_bin, rd\_ptr\_bin) and synchronizer registers via hierarchical access for directed tests, ensuring correct implementation of Gray-to-binary conversions and CDC logic.
* **Gray-Box:** Combine external stimulus with selective internal checks (e.g., reading snapshot values of synchronization registers mid-simulation) to correlate interface behavior with internal state transitions.

### Pros and Cons

|  |  |  |
| --- | --- | --- |
| **Method** | **Pros** | **Cons** |
| Black-Box | Simple stimulus-driven tests; focus on spec. | Cannot target internal corner cases |
| White-Box | Full visibility; targeted tests for internal logic | Requires access to internals; more effort |
| Gray-Box | |  | | --- | | Balances depth and simplicity; catches interface–state mismatches | | Moderate complexity |

### Testbench Architecture

Our class-based UVM-like environment comprises the following components, all packaged in tb\_pkg.sv and instantiated in testbench\_top:

* **Interface** (interface.sv): Defines transaction-level signals (wr\_en, wr\_data, rd\_en, rd\_data, full, empty, half\_full, half\_empty), synchronized to wr\_clk and rd\_clk domains.
* **Generator** (generator.sv): Produces transaction objects for fill (256 writes) and drain (256 reads) phases via mailbox gen2drv, then signals completion via an event.
* **Driver** (driver.sv): Consumes transactions from gen2drv and drives DUT ports on the interface at clock edges, managing enable and data signals precisely.
* **Monitors**:
  + **monitor\_in** (monitor\_in.sv): Observes write-side events, captures write transactions, and forwards them via mailbox mon\_in2scb to the scoreboard.
  + **monitor\_out** (monitor\_out.sv): Observes read-side events, captures read transactions, and forwards them via mon\_out2scb.
* **Scoreboard** (scoreboard.sv): Maintains a reference queue of write data and compares it against read data, counting mismatches (err\_cnt) and reporting pass/fail.
* **Environment** (environment.sv): Instantiates generator, driver, monitors, and scoreboard; forks their main() tasks and awaits the generator’s completion event.
* **Top-level Module** (top.sv): Connects clocks, resets, the interface, DUT (async\_fifo.sv), and the test class (in test.sv), then invokes t0.run() to kick off simulation.

**Class Based Test Bench Architecture:**

The verification of the asynchronous FIFO is done with constrained-random simulation and self-check methods within a class-based System Verilog test bench. Even though UVM isn’t part of the test, its structure is based on the modularity and organization seen in UVM using System Verilog classes. This way of working guarantees organized signals, keeps track of all transactions and monitors DUT activity in multiple timescales automatically.

This section covers both Components and Architecture.

**Interface (interface.sv)**

Defines the DUT ports and sorts them with modports and clocking blocks to make driving and sampling easier. These two domains are represented by their own clock blocks.

**Generator (generator.sv)**

Produces valid wr\_en, rd\_en and wr\_data transaction inputs following constraints. To achieve separation of stimulus generation and application, all transactions are delivered to the driver through a digital mailbox (gen2drv).

**Driver (driver.sv)**

Simulates the interface of the targeted hardware when it sees transactions from the generator. It controls when and how clocks tick, events are sequenced and ensures proper enables and data are applied throughout the design.

**Monitors are included (monitor\_in.sv, monitor\_out.sv).**

These components just monitor the FIFO model’s interface. Both types of transactions are collected and delivered, by using mailboxes (mon\_in2scb, mon\_out2scb), to the scoreboard for review and processing.

**Scoreboard (scoreboard.sv)**

The service uses a queue-based self-service system. It saves data that is written to the ledger and uses it to check the data from untrusted sources to confirm the order, check for errors and manage special scenarios.

**Environment (environment.sv)**

It is the most encompassing element for the website. It creates the generator, driver, monitors and scoreboard on the fly and ensures their operation by task fork-join and events.

**The top module is called top.sv**

Uses the DUT, interface and environment all at the same time. Automates testbench simulation using a run() task implemented in a class.

**Verification Strategy  
Dynamic Simulation** is our primary strategy, enabling rapid development and iteration of directed and randomized tests under real-clock conditions. It exercises full DUT functionality, including flag generation.

## Testcase Scenarios **Basic Tests**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| |  | | --- | | Test Name | | |  | | --- | | Description | | |  | | --- | | Expected Results | |
| |  | | --- | | Reset Behavior | | |  | | --- | | Assert wr\_rst\_n=0 and rd\_rst\_n=0, then release resets and observe all outputs. | | |  | | --- | | wr\_ptr\_bin=0, rd\_ptr\_bin=0, empty=1, full=0, half\_full=0, half\_empty=0 | |
| |  | | --- | | Single Write/Read | | |  | | --- | | Issue one write (wr\_en=1, wr\_data=0xA5), then one read (rd\_en=1). | | |  | | --- | | rd\_data=0xA5, pointers increment to 1, empty=1, full=0, half flags update correctly | |
| |  | | --- | | Fill to Full | | |  | | --- | | Hold wr\_en=1 until full flag asserts (256 writes). | | |  | | --- | | full=1 at depth==256, half\_full=1 from depth>=128, no data overwrite beyond full | |

We also performed few iterations of purely random toggling of wr\_en and rd\_en across clock domains. All written data read in order, no missing/stale data, flags track depth correctly.

# Resources requirements

## Venkat Sahith

* Verification test plan + UVM Testbench

## Mrudula

* DUT Specification document + Verification Test plan documentation

## Vaishnavi

* RTL code + Coverage and Class based testbench

## Rohith

* Self-Checking testbench + UVM + Class based testbench

# Schedule

## Milestone 1

* Initial design and verification specifications written
* Block diagram is finalized and integrated into the document.
* RTL implementation of async\_fifo.sv is committed and compiling.
* Standalone tests for bin2gray and gray2bin functions are running.

## Milestone 2

## ● Basic validation of full and empty flags under simple operations. ● half\_full and half\_empty flag behavior verified at mid-depth thresholds. ● Scoreboard and monitor infrastructure set up in testbench.

## Milestone 3

● Constrained-random burst tests (burst length = 1024) will be developed and executed.  
● Wrap-around scenarios and underflow/overflow corner-case tests will be added.  
● Functional coverage models and coverpoints implemented for depth and flag transitions.

## Milestone 4

* Initial UVM testbench
* UVM verification plan

## Milestone 5

* UVM testbench will be completed

● Final verification report will be drafted, including coverage and bug-injection results.  
● Documentation will be updated with test results, coverage metrics,

# References

[1]<https://vlsiverify.com/verilog/verilog-codes/asynchronous-fifo/>

[2]OpenCores, "Asynchronous FIFO IP Core," [https://opencores.org/projects/async\_fifo](https://opencores.org/projects/async_fifo%20)

[3]Xilinx, "FIFO Generator v13.2 User Guide," Xilinx Application Note XAPP 501, 2017.

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