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Department of Electronics and Communication

CMOS VLSI Circuits Lab

(19EECC301)

OPEN ENDED PROJECT

Team – B1

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Guide Signature _____

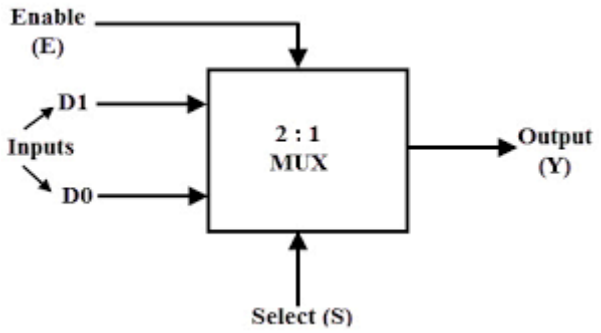
Statement:

Implementation of 2:1 MUX using pseudo NMOS logic and CMOS logic respectively.

Design:

Pseudo NMOS logic, an older approach, emulates NMOS technology using only PMOS transistors. In a pseudo NMOS 2:1 MUX, a pull-up network of PMOS transistors and a pull-down network with both NMOS and PMOS transistors are employed, with the control signal determining the input connection to the output. This design often uses an AND-OR gate structure to perform logical operations. On the other hand, CMOS logic, a more contemporary and widely used approach, combines NMOS and PMOS transistors to achieve low power consumption and enhanced noise margins. In a CMOS 2:1 MUX, the control signal activates the appropriate transistors to create a path from one input data line to the output, with NMOS forming the pull-down network and PMOS forming the pull-up network. CMOS circuits offer advantages such as low power consumption and high noise immunity, making them the preferred choice for modern integrated circuit designs, while pseudo NMOS has become less common due to its comparatively lower efficiency.

2x1 Multiplexer:



Truth table:

S	Y
0	I_0
1	I_1

Condensed Truth Table

LITERATURE REVIEW:

2:1 Multiplexer using Pseudo NMOS and CMOS Logic:

A 2:1 multiplexer is a digital circuit that selects one of the two input data lines and directs it to the output based on the select line. This implementation utilizes a combination of Pseudo NMOS and CMOS logic, providing a balanced approach between simplicity and efficiency.

Pseudo NMOS Logic: Pseudo NMOS logic is employed in the design of the 2:1 multiplexer to create a cost-effective and straightforward circuit. Pseudo NMOS gates consist of only NMOS transistors, eliminating the need for PMOS transistors and reducing the overall complexity. The multiplexer structure involves connecting each input line to Pseudo NMOS gates, and the output is determined by the select line.

In Pseudo NMOS logic, a low voltage represents a logical "1," and a high voltage represents a logical "0." During the evaluation phase, the selected input's Pseudo NMOS gate allows the signal to pass through, determining the final output state. This approach offers simplicity in design and ease of debugging.

CMOS Logic: Complementary Metal-Oxide-Semiconductor (CMOS) logic is integrated into the multiplexer design to address the limitations of Pseudo NMOS logic. CMOS logic utilizes both NMOS and PMOS transistors, offering improved noise margins and reduced static power consumption.

SHORTCOMINGS:

Shortcomings of CMOS Logic:

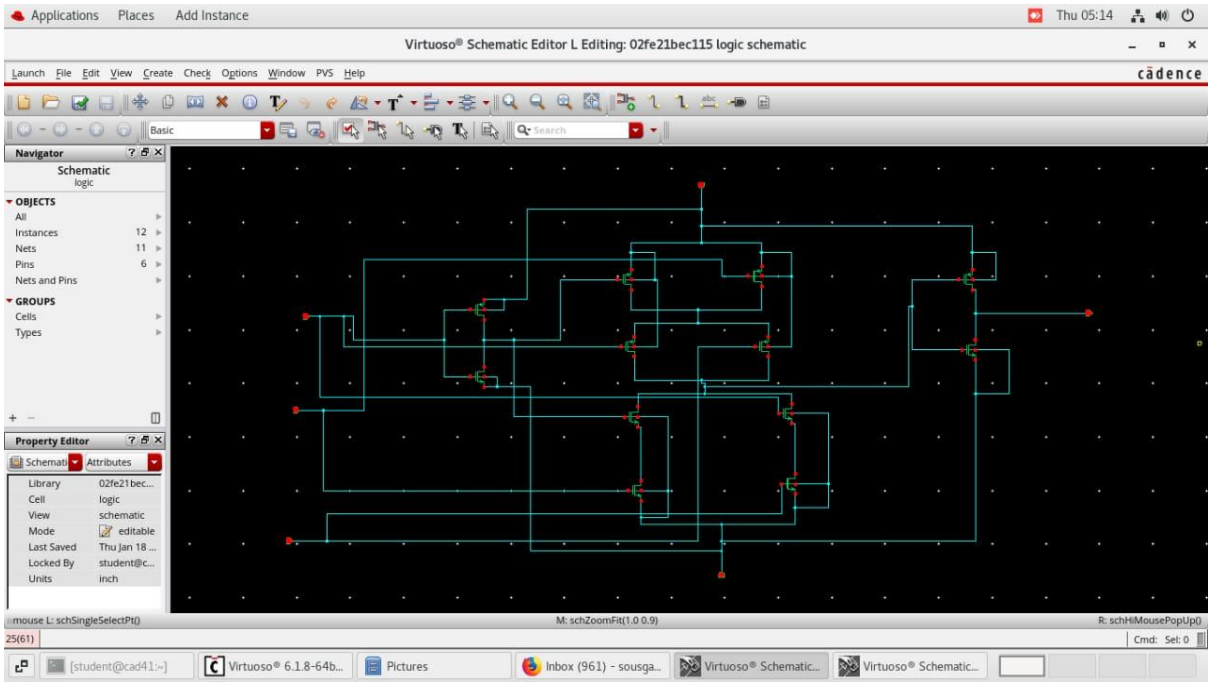
- **Complexity and Cost:** CMOS logic circuits tend to be more complex due to the integration of both NMOS and PMOS transistors. This complexity can lead to higher manufacturing costs, especially for larger and more intricate designs.
- **Power Consumption during Switching:** While CMOS logic generally has low static power consumption, during switching between logic states, there is a brief moment where both NMOS and PMOS transistors are conducting simultaneously. This can result in a higher power consumption spike during these transitions.
- **Propagation Delay Variability:** CMOS circuits may exhibit variations in propagation delay across different paths, known as skew. This variability can be influenced by factors such as process variations, temperature, and voltage fluctuations, making it challenging to achieve precise timing.

Shortcomings of Pseudo NMOS Logic:

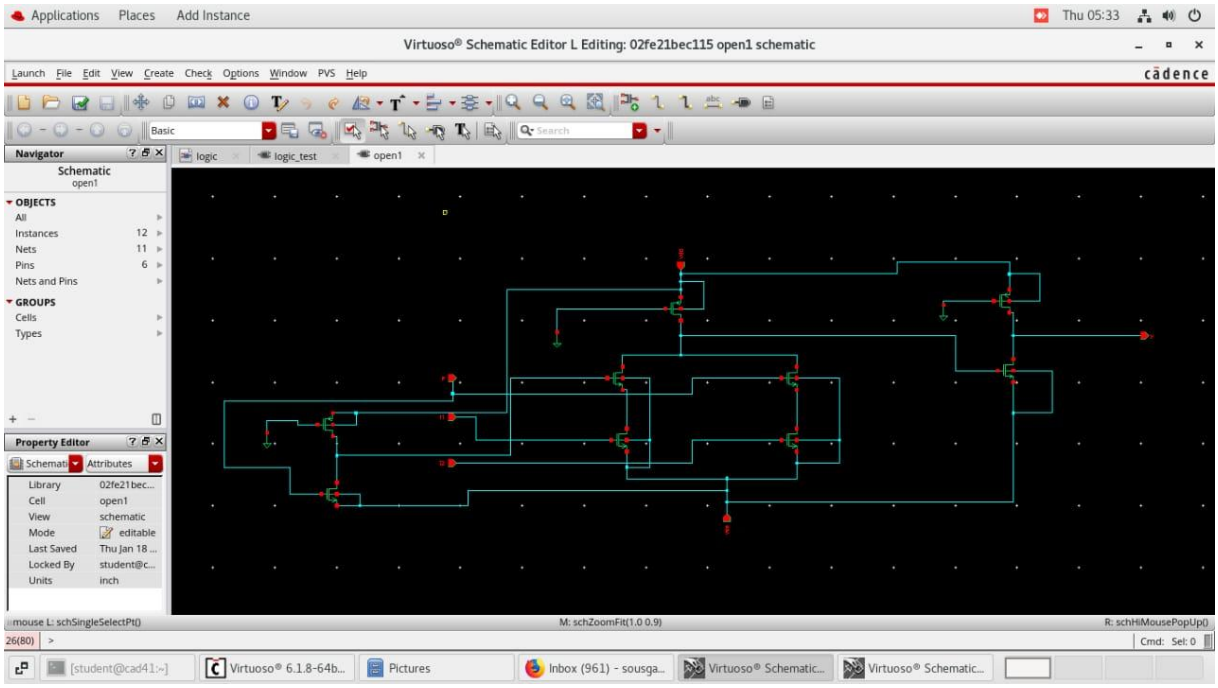
- **Limited Noise Margins:** Pseudo NMOS logic has limited noise margins compared to full CMOS logic. This makes the circuit more susceptible to external noise, potentially leading to incorrect logic state interpretation, especially in noisy environments.
- **Higher Static Power Consumption:** Pseudo NMOS logic may result in higher static power consumption due to the existence of potential DC paths. This issue arises because Pseudo NMOS gates only use NMOS transistors, which may allow a continuous current flow, contributing to static power dissipation.
- **Voltage Level Representation:** Pseudo NMOS logic uses a low voltage level to represent a logical "1" and a high voltage level for a logical "0." This unconventional voltage level representation can lead to compatibility issues when interfacing with standard CMOS circuits, requiring additional level-shifting circuitry.

In summary, while CMOS and Pseudo NMOS logics offer their own advantages, they also come with specific shortcomings. CMOS logic is known for its complexity and occasional power spikes during switching, while Pseudo NMOS logic may suffer from limited noise margins and higher static power consumption. Designers often need to carefully consider these trade-offs based on the specific requirements of their applications.

Schematic:

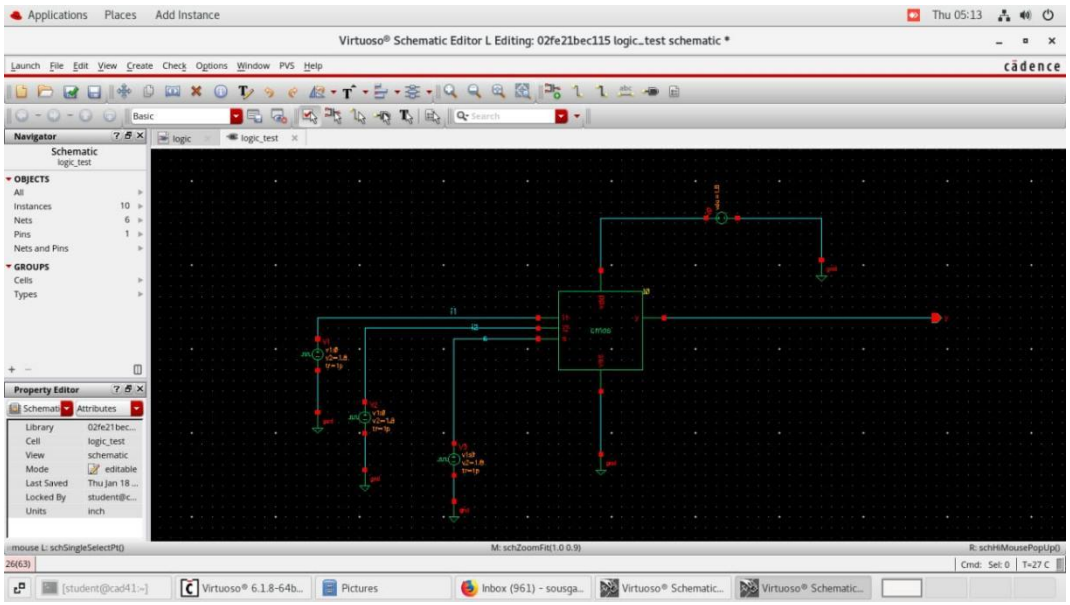


Schematic of 2:1 MUX using CMOS logic

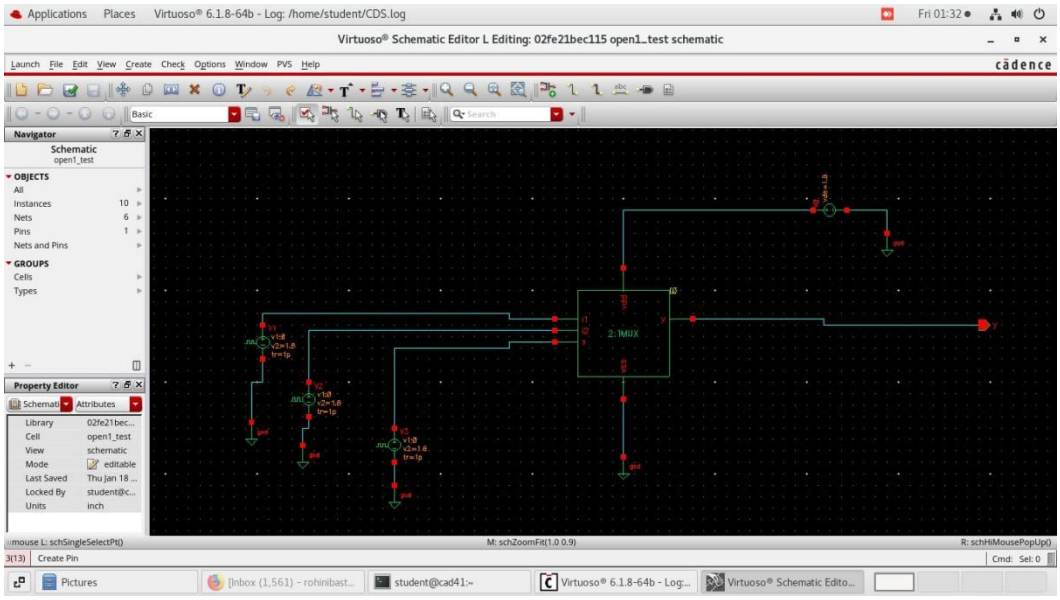


Schematic of 2:1 MUX using pseudo NMOS logic

Test schematic:

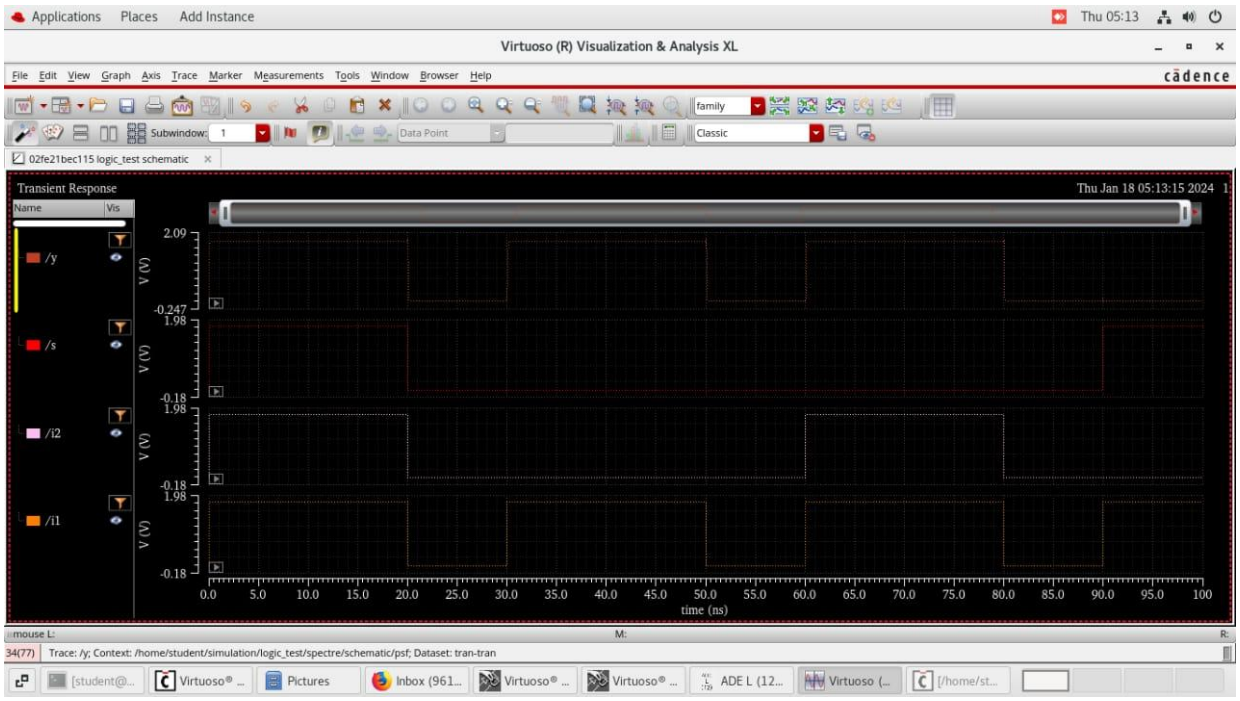


Test Schematic of 2:1 MUX using CMOS logic

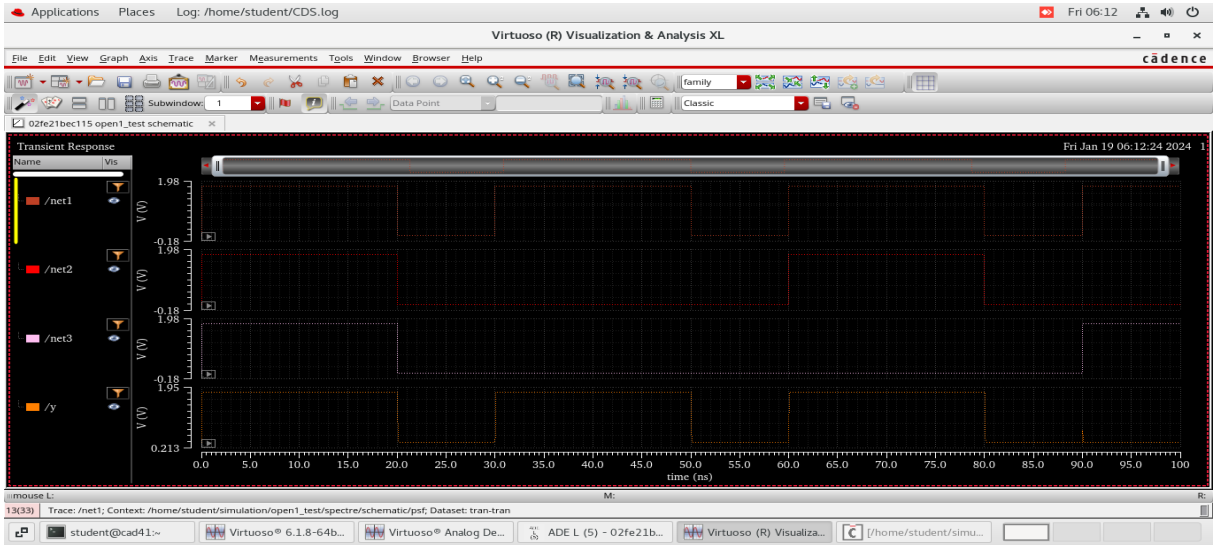


Test Schematic of 2:1 MUX using pseudo NMOS logic

Graph:



Graph of 2:1 MUX using pseudo NMOS logic



Graph of 2:1 MUX using CMOS logic

Comparison:

parameters	Pseudo Nmos logic	Cmos logic
Rise to fall time	20.07E-12	20.06E-9
Fall to rise time	-19.98E-9	-19.94E-9
Delay	-9.97E-9	-8.94E-9
Average Power	372.5E-3	2.53E-9

Conclusion:

In conclusion, the successful implementation of the 2:1 multiplexer (MUX) using both pseudo NMOS logic and CMOS logic has been successfully achieved.