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COURSE CODE :- 3EL42
COURSE NAME :- DIGITAL SYSTEM DESIGN

ASSIGNMENT - 3

1) CLOCK DIVIDER

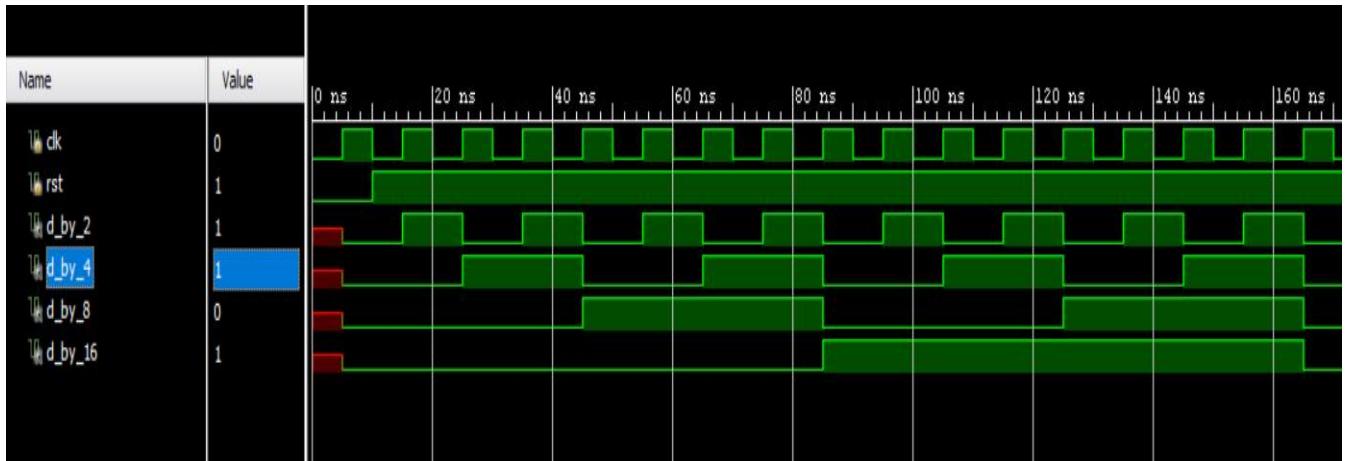
a) VERILOG CODE: -

```
module clock_divider(
    input rst,
    input clk,
    output reg d_by_2,
    output reg d_by_4,
    output reg d_by_8,
    output reg d_by_16
);
    reg [3:0]count;
    always @ (posedge clk)
        begin
            if(rst==0)
                count=4'b0000;
            else
                // clk= ~clk;
                count = count + 1;
                d_by_2 = count[0];
                d_by_4 = count[1];
                d_by_8 = count[2];
                d_by_16 = count[3];
        end
endmodule
```

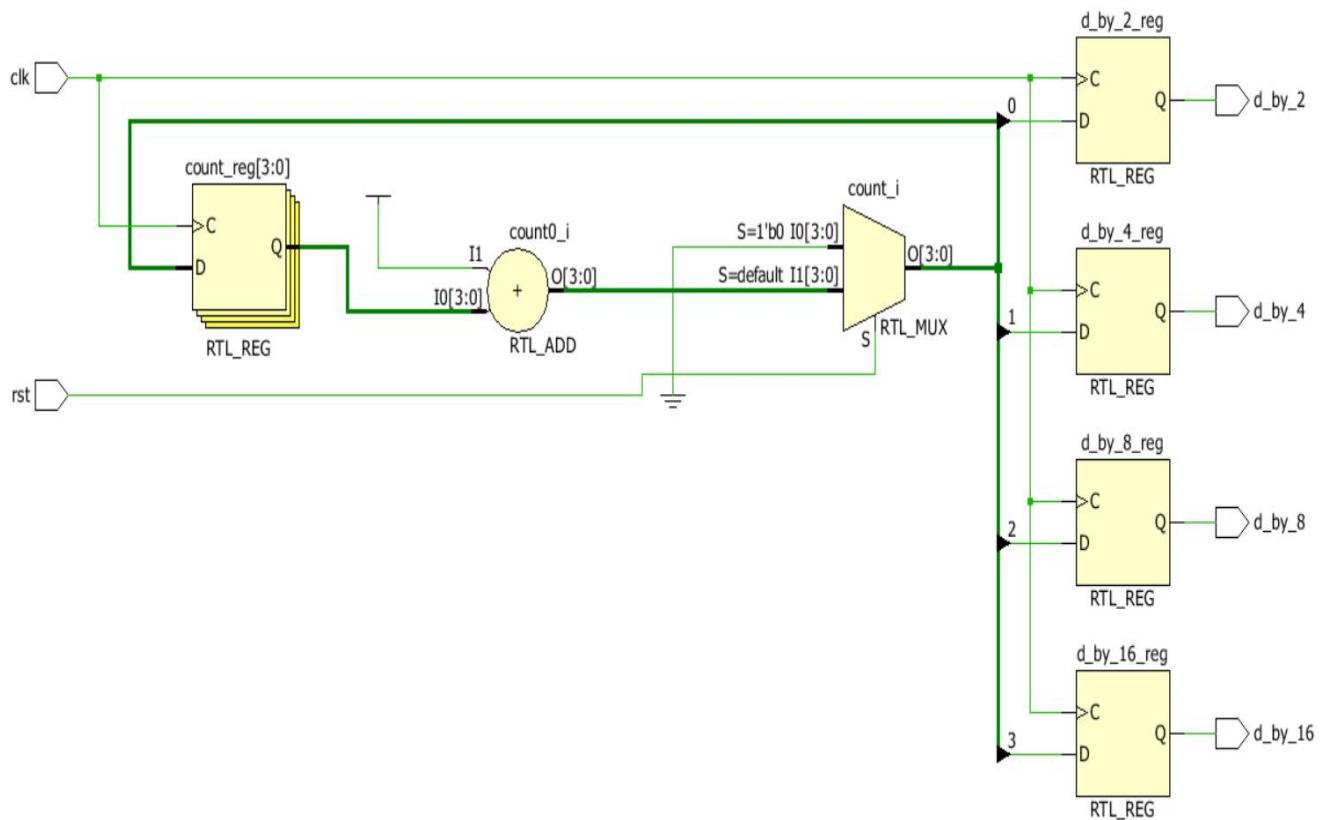
b) TESTBENCH :-

```
module clock_divider_tb(  
);  
reg clk;  
reg rst;  
wire d_by_2;  
wire d_by_4;  
wire d_by_8;  
wire d_by_16;  
  
clock_divider uut(rst,clk,d_by_2,d_by_4,d_by_8,d_by_16);  
  
initial begin  
    clk = 1'b0;  
    always #5 clk = ~clk;  
    End  
  
initial begin : test  
  
    rst = 1'b0;  
    #10  
    rst = 1'b1;  
  
    #6000  
    $finish;  
  
end  
  
endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



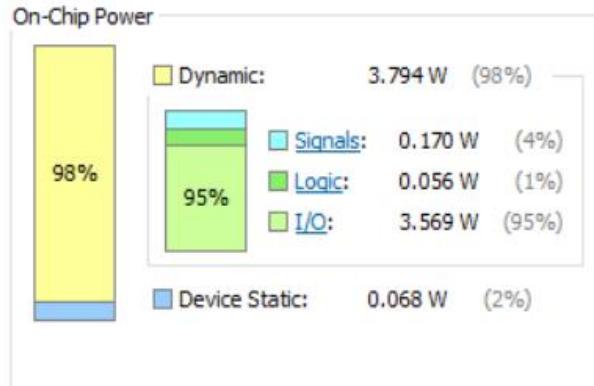
e) SYNTHESIS REPORT :-

```
Start Writing Synthesis Report
-----
Report BlackBoxes:
+-----+-----+
| BlackBox name | Instances |
+-----+-----+
+-----+-----+
Report Cell Usage:
+-----+-----+
| Cell | Count |
+-----+-----+
|1| BUFG | 1|
|2| LUT1 | 2|
|3| LUT2 | 1|
|4| LUT3 | 1|
|5| LUT4 | 1|
|6| FDRE | 4|
|7| IBUF | 2|
|8| OBUF | 4|
+-----+-----+
Report Instance Areas:
+-----+-----+
| Instance | Module | Cells |
+-----+-----+
|1| top | | 16|
+-----+-----+
Finished Writing Synthesis Report : Time (s): cpu = 00:00:05 ; elapsed = 00:00:07 . Memory (MB): peak = 412.129 ; gain = 252.445
```

f) POWER REPORT :-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 3.862 W
Junction Temperature: 43.5 °C
Thermal Margin: 56.5 °C (11.8 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



2) JOHNSON COUNTER :-

a) VERILOG CODE:-

```
module Dff(
    input clk,
    input reset,
    input d,
    output reg q
);

    always @ (posedge clk)
    begin
        if(reset)
            q=0;
        else if(clk)
            q = d ;
    end
endmodule

module _4bit_johnson_counter(
    input clk,
    input reset,
    output [3:0] q
);

    Dff d1(clk,reset,~q[3],q[0]);
    Dff d2(clk,reset,q[0],q[1]);
    Dff d3(clk,reset,q[1],q[2]);
    Dff d4(clk,reset,q[2],q[3]);

endmodule
```

b) TESTBENCH :-

```
module rbit_johnson_counter_tb;

reg clk,reset;
wire [3:0] q;

_4bit_johnson_counter uut(clk,reset,q);

initial
begin

    reset = 1'b1;
    clk = 1'b1;

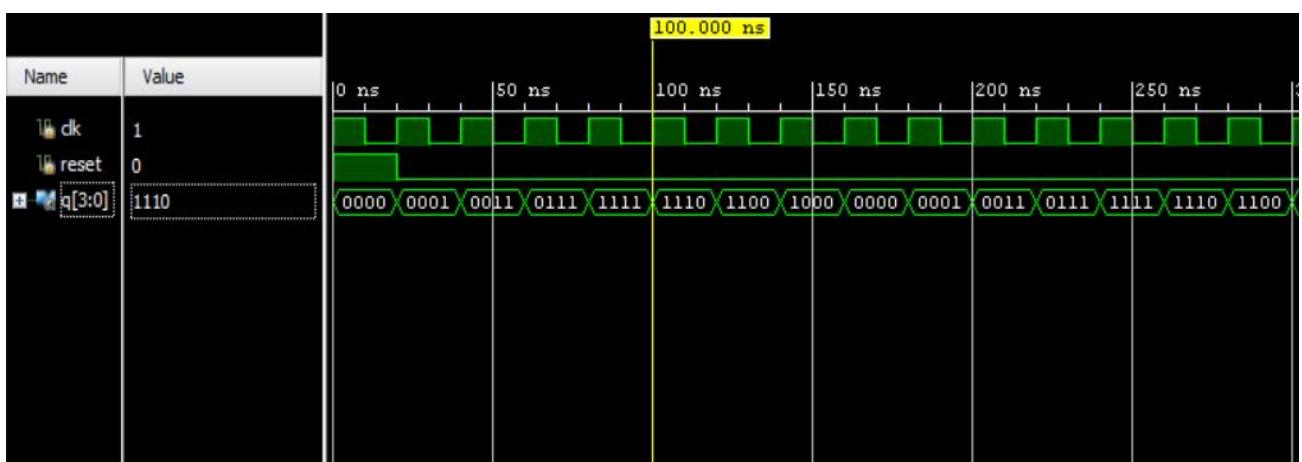
end

always #10 clk = ~clk;

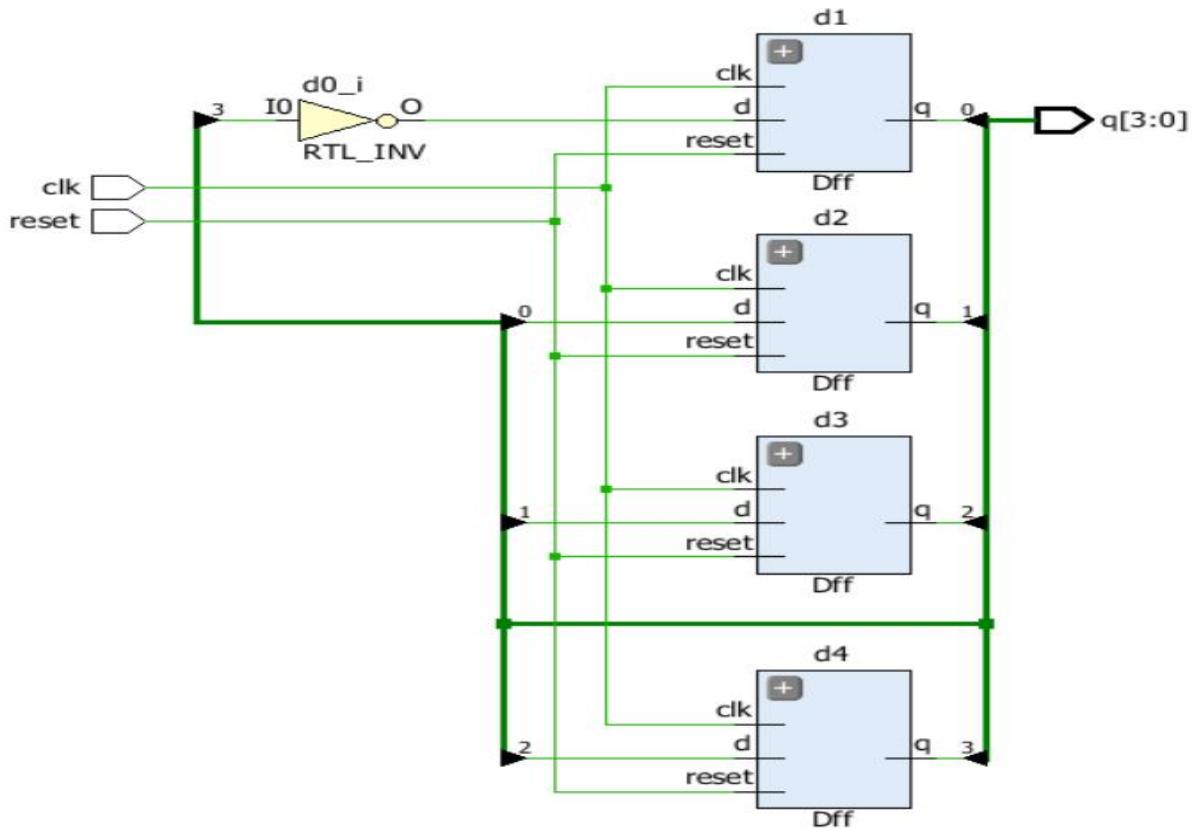
initial
begin
#00 reset = 1'b1;
#20 reset = 1'b0;
#500 $finish;

end

endmodule
```

c) EPWAVE :-

d) RTL SCHEMATIC :-



e) SYNTHESIS REPORT :-

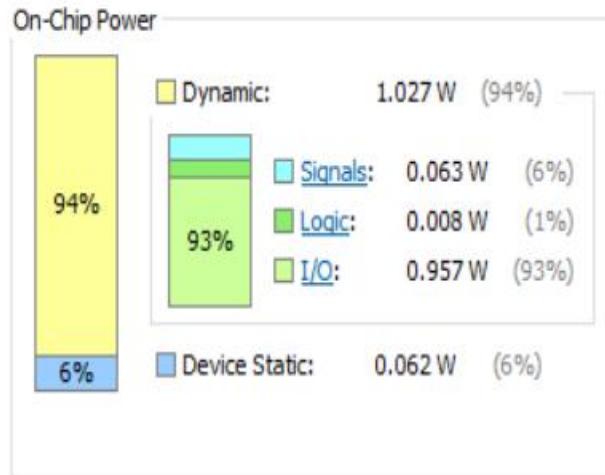
```

Start Writing Synthesis Report
-----
Report BlackBoxes:
+---+-----+
| |BlackBox name |Instances |
+---+-----+
+---+-----+
Report Cell Usage:
+---+-----+
| |Cell |Count |
+---+-----+
|1|BUFG|1|
|2|LUT1|1|
|3|FDRE|4|
|4|IBUF|2|
|5|OBUF|4|
+---+-----+
Report Instance Areas:
+---+-----+-----+
| |Instance |Module |Cells |
+---+-----+-----+
|1|top| |12|
|2||d1|Dff|1|
|3||d2|Dff|1|
|4||d3|Dff|1|
|5||d4|Dff|2|
+---+-----+-----+
Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:07 . Memory (MB): peak = 412.262 ; gain = 252.645
-----
```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 1.089 W
Junction Temperature: 30.2 °C
Thermal Margin: 69.8 °C (14.5 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



3) RING COUNTER :-

a) VERILOG CODE:-

```
module ring_counter(
    input clk,
    input rst,
    output reg [3:0] q
);
//reg [3:0]q;
always @(posedge clk)
begin
    if(rst==1)
        q <= 4'b0001;

    else
        begin
            q[0]<=q[3];
            q[1]<=q[0];
            q[2]<=q[1];
            q[3]<=q[2];
        end
    end
Endmodule
```

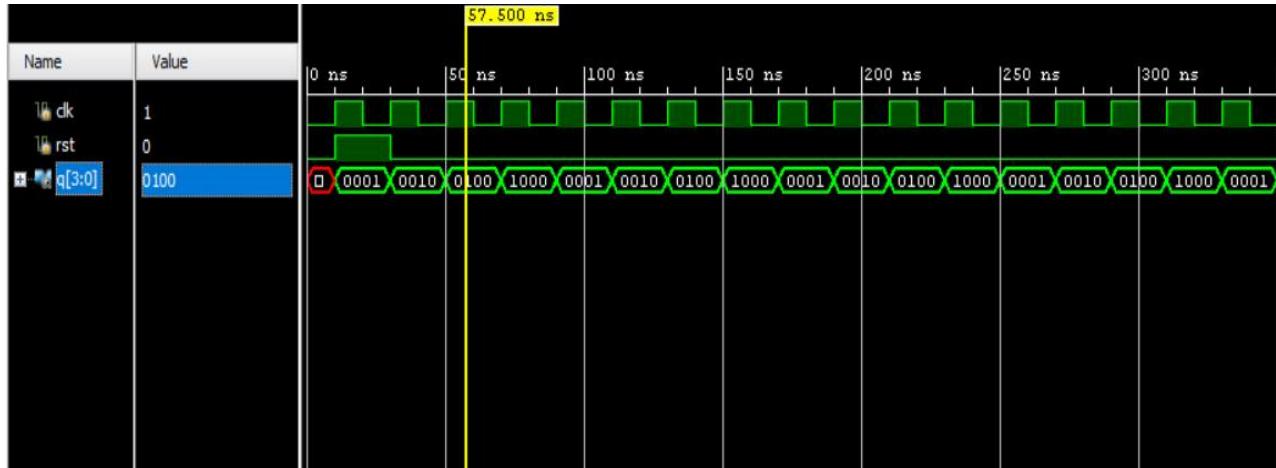
b) TESTBENCH :-

```
module ring_counter_tb(
);
reg clk;
reg rst;
wire [3:0]q;

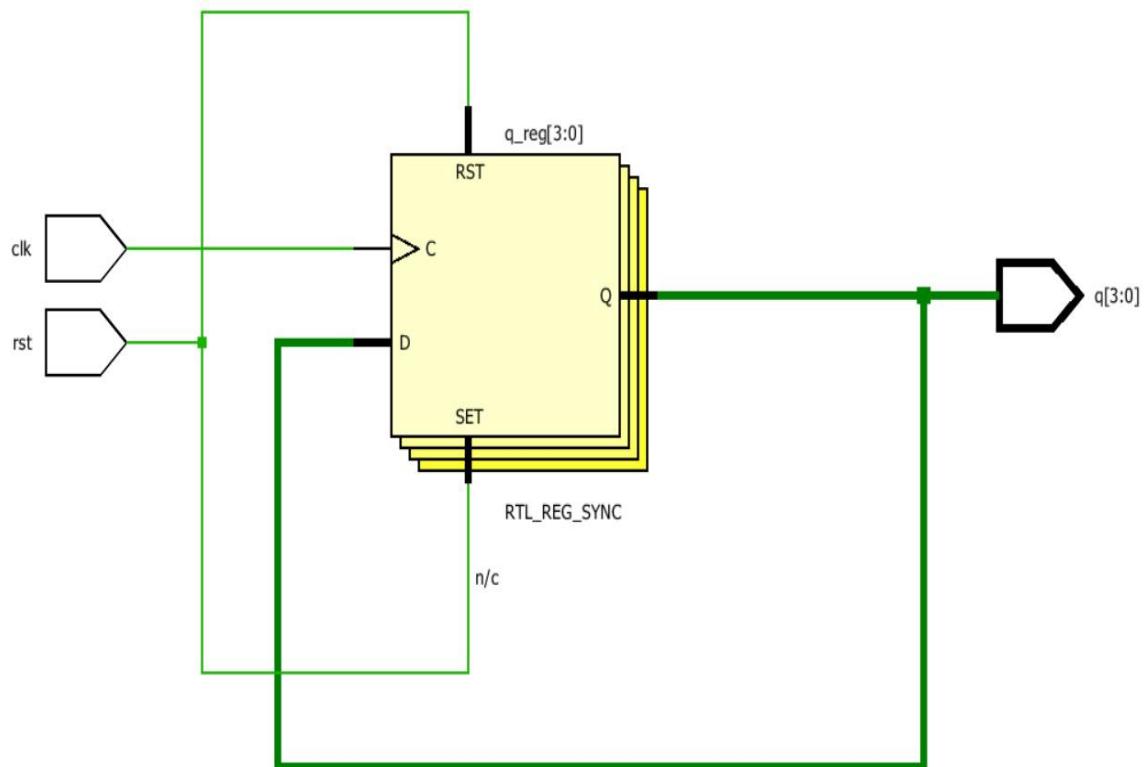
ring_counter uut(clk,rst,q);

initial begin
#0 clk=1'b0;
#0 rst = 1'b0;
end
always
#10 clk = ~clk;
initial
begin
#10 rst =1'b1;
#20 rst =1'b0;
#500 $finish;
```

```
end  
endmodule  
c) EPWAVE :-
```



d) RTL SCHEMATIC :-



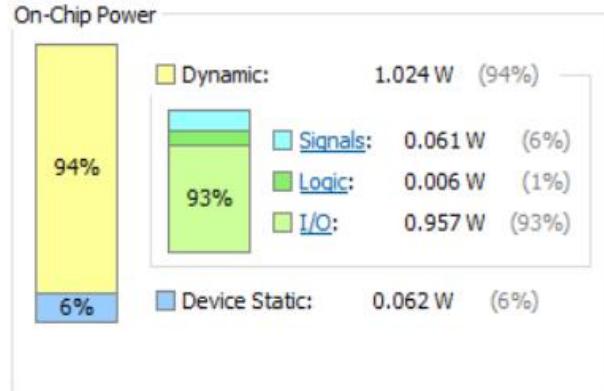
e) SYNTHESIS REPORT :-

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
++-----+  
| |BlackBox name |Instances |  
++-----+  
++-----+  
  
Report Cell Usage:  
++-----+  
| |Cell |Count |  
+-----+-----+  
|1 |BUFGE | 1|  
|2 |FDRE | 3|  
|3 |FDSE | 1|  
|4 |IBUF | 2|  
|5 |OBUF | 4|  
+-----+-----+  
  
Report Instance Areas:  
++-----+-----+-----+  
| |Instance |Module |Cells |  
+-----+-----+-----+  
|1 |top | | 11|  
+-----+-----+-----+  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:05 ; elapsed = 00:00:07 . Memory (MB): peak = 403.297 ; gain = 243.977
```

f) POWER REPORT :-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 1.086 W
Junction Temperature: 30.2 °C
Thermal Margin: 69.8 °C (14.5 W)
Effective ΔTJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



4) 5 INPUT MAJORITY CIRCUIT : -

a) VERILOG CODE: -

```
module input_majority(
    input [4:0] a,
    output reg z
);

reg [3:0]count;

always @(a) begin
    count = 3'b000;
    for (integer i = 0; i < 5; i = i + 1) begin
        if (a[i] == 1'b1)
            count = count + 1;
    end
    $display("%b",count);
    if (count >= 3'b011)
        z = 1;
    else
        z = 0;
end
endmodule
```

b) TESTBENCH : -

```
module input_majority_tb;

reg [4:0] a;
wire z;

// Instantiate the module under test
input_majority uut (
    .a(a),
    .z(z)
);
initial begin
    a = 5'b00000;
    #10 a = 5'b00001;
    #10 a = 5'b00111;
    #10 a = 5'b01111;
```

```

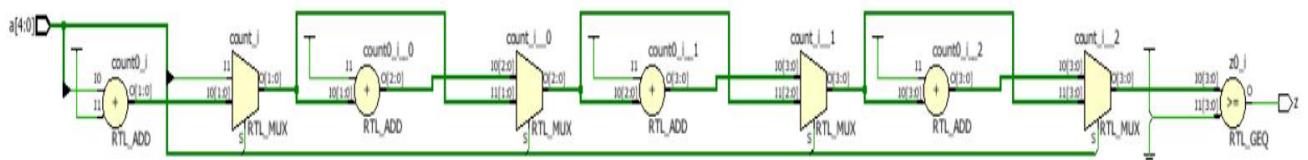
#10 a = 5'b11111;
#10 a = 5'b00011;
#10
    $finish; // Finish simulation
end
Endmodule

```

c) EPWAVE :-



d) RTL SCHEMATIC :-



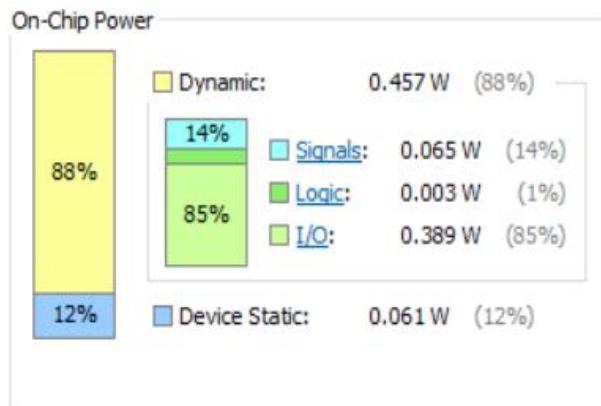
e) SYNTHESIS REPORT : -

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+-----+  
| |BlackBox name |Instances |  
+-----+  
+-----+  
  
Report Cell Usage:  
+-----+  
| |Cell |Count |  
+-----+  
|1 |LUT5 | 1|  
|2 |IBUF | 5|  
|3 |OBUF | 1|  
+-----+  
  
Report Instance Areas:  
+-----+  
| |Instance |Module |Cells |  
+-----+  
|1 |top | | 7|  
+-----+  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:05 ; elapsed = 00:00:07 . Memory (MB): peak = 410.039 ; gain = 250.438  
-----
```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.518 W
Junction Temperature: 27.5 °C
Thermal Margin: 72.5 °C (15.1 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



5) PARITY GENERATOR :-

a) VERILOG CODE:-

```
module parity_generator(
    input x,
    input y,
    input z,
    output result
);

    xor (result,x,y,z);

endmodule
```

b) TESTBENCH :-

```
module parity_generator_tb();
reg x,y,z;
wire result;

parity_generator uut(x,y,z,result);

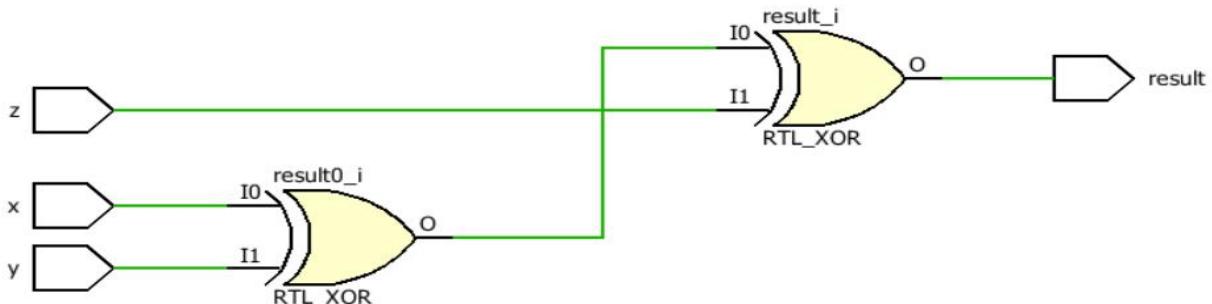
initial
begin
#00 x=0 ; y=0 ; z=0;
#100 x=0 ; y=0 ; z=1;
#100 x=0 ; y=1 ; z=0;
#100 x=0 ; y=1 ; z=1;
#100 x=1 ; y=0 ; z=0;
#100 x=1 ; y=0 ; z=1;
#100 x=1 ; y=1 ; z=0;
#100 x=1 ; y=1 ; z=1;
#100 x=0 ; y=0 ; z=0;
end

initial begin
$dumpfile("dump.vcd");
$dumpvars(0);
end
Endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



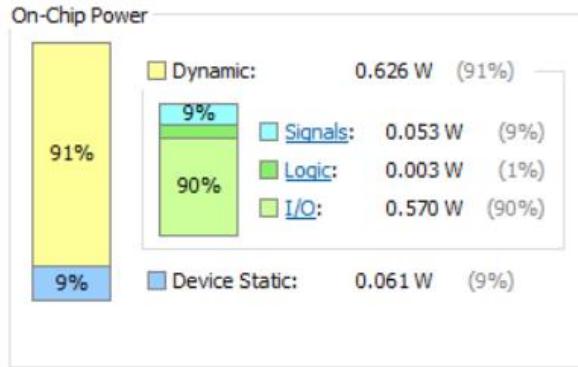
e) SYNTHESIS REPORT :-

```
Start Writing Synthesis Report
-----
Report BlackBoxes:
+-----+-----+
| |BlackBox name |Instances |
+-----+-----+
+-----+-----+
Report Cell Usage:
+-----+-----+
| |Cell |Count |
+-----+-----+
|1 |LUT3 |    1|
|2 |IBUF |     3|
|3 |OBUF |     1|
+-----+-----+
Report Instance Areas:
+-----+-----+-----+
| |Instance |Module |Cells |
+-----+-----+-----+
|1 |top      |      |    5|
+-----+-----+-----+
-----
Finished Writing Synthesis Report : Time (s): cpu = 00:00:05 ; elapsed = 00:00:06 . Memory (MB): peak = 409.969 ; gain = 250.379
```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.687 W
Junction Temperature: 28.3 °C
Thermal Margin: 71.7 °C (14.9 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



6) BINARY TO ONE HOT ENCODER :-

a) VERILOG CODE:-

```
module Binary_too_One_Hot_encoder(
    input [3:0] a,
    output [15:0] b
);

    assign b = 1'b1 << a;

endmodule
```

b) TESTBENCH :-

```
module Binary_to_One_Hot_Encoder_tb;
    reg [3:0] a;
    wire [15:0] b;

    Binary_too_One_Hot_encoder uut(a,b);

    initial begin

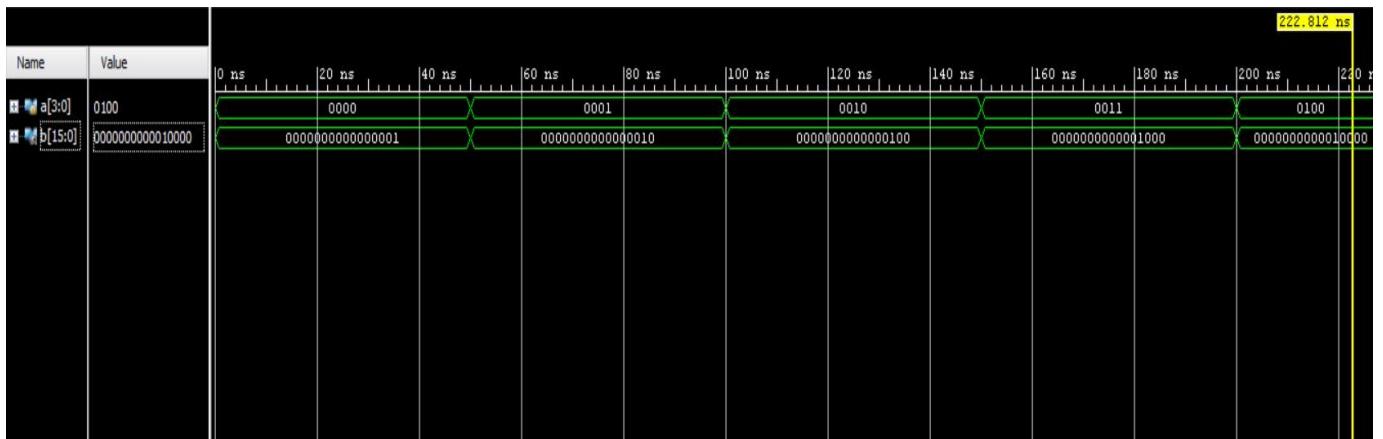
        #00 a=4'b0000;
        #50 a=4'b0001;
        #50 a=4'b0010;
        #50 a=4'b0011;
        #50 a=4'b0100;
        #50 a=4'b0101;
        #50 a=4'b0110;
        #50 a=4'b0111;
        #50 a=4'b1000;
        #50 a=4'b1001;
        #50 a=4'b1010;
        #50 a=4'b1011;
        #50 a=4'b1100;
        #50 a=4'b1101;
        #50 a=4'b1110;
        #50 a=4'b1111;
    end

    initial begin
        $dumpfile("dump.vcd");
        $dumpvars(0);
    end

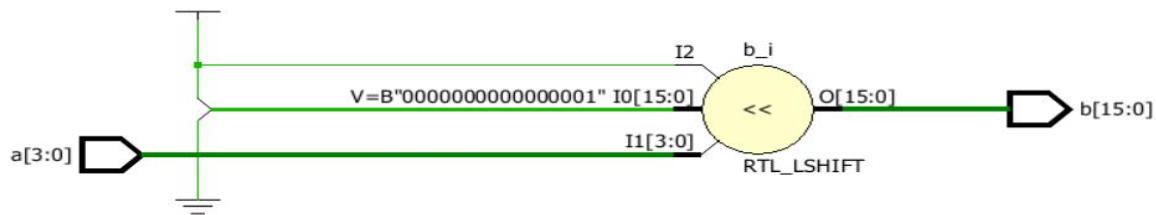
```

endmodule

c) EPWAVE :-



d) RTL SCHEMATIC :-



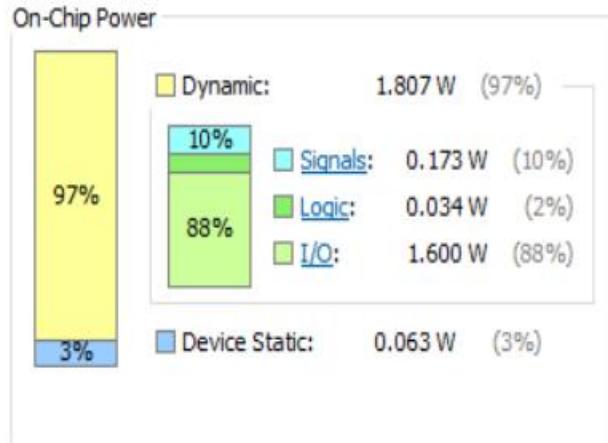
e) SYNTHESIS REPORT :-

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+---+---+  
| |BlackBox name |Instances |  
+---+---+  
+---+---+  
  
Report Cell Usage:  
+---+---+  
| |Cell |Count |  
+---+---+  
|1 |LUT4 | 16|  
|2 |IBUF | 4|  
|3 |OBUF | 16|  
+---+---+  
  
Report Instance Areas:  
+---+---+---+  
| |Instance |Module |Cells |  
+---+---+---+  
|1 |top | | 36|  
+---+---+---+  
  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:05 ; elapsed = 00:00:06 . Memory (MB): peak = 410.676 ; gain = 251.180  
-----
```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 1.87 W
Junction Temperature: 33.9 °C
Thermal Margin: 66.1 °C (13.7 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



8) 4 BIT BCD SYNCHRONOUS COUNTER :-

a) VERILOG CODE: -

```
module _4Bit_Synchronous_BCD_Counter

    input clk,
    input rst,
    output reg [3:0] count
);
reg [3:0]t;
always @ (posedge clk)
begin
if (rst)
begin
    t <= 4'b0000;
    count <= 4'b0000;
end
else
begin
    t <= t + 1;
    if (t == 4'b1001)
begin
    t <= 4'b0000;
end
    count <= t;
end
end

Endmodule
```

b) TESTBENCH : -

```
module _4Bit_Synchronous_BCD_Counter_tb();
reg clk;
reg rst;
wire [3:0]count;

_4Bit_Synchronous_BCD_Counter uut(clk,rst,count);

initial begin
    clk = 0;
    forever #5 clk = ~clk;
end
initial begin
```

```

rst = 1;
#10 rst = 0;
$monitor ("T=%0t out=%b", $time, count);
#150 rst = 1;
#10 rst = 0;
#200
$finish;
end

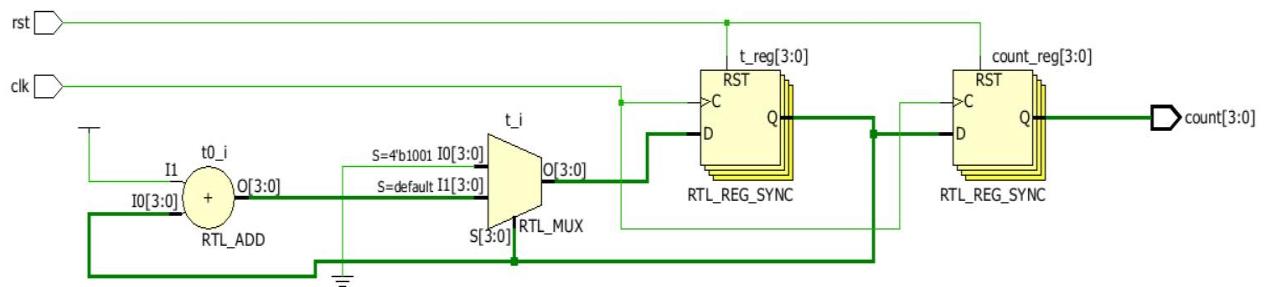
endmodule

```

c) EPWAVE :-



d) RTL SCHEMATIC :-



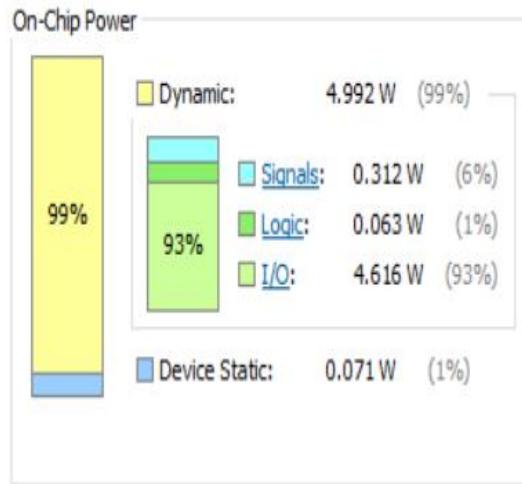
e) SYNTHESIS REPORT : -

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+---+---+  
| BlackBox name | Instances |  
+---+---+  
+---+---+  
  
Report Cell Usage:  
+---+---+  
| Cell | Count |  
+---+---+  
|1 |BUFG | 1|  
|2 |LUT1 | 1|  
|3 |LUT3 | 1|  
|4 |LUT4 | 2|  
|5 |FDRE | 8|  
|6 |IBUF | 2|  
|7 |OBUF | 4|  
+---+---+  
  
Report Instance Areas:  
+---+---+  
| Instance | Module | Cells |  
+---+---+  
|1 |top | | 19|  
+---+---+  
  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:05 ; elapsed = 00:00:07 . Memory (MB): peak = 408.035 ; gain = 248.551  
-----
```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 5.063 W
Junction Temperature: 49.2 °C
Thermal Margin: 50.8 °C (10.6 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



8) 4-BIT CARRY LOOKAHEAD ADDER :-

a) VERILOG CODE:-

```
module _4Bit_Carry_Look_Ahead_Adder(
    input [3:0] a,
    input [3:0] b,
    input cin,
    output cout,
    output [3:0] sum
);
    and (g1,a[0],b[0]);
    and (g2,a[1],b[1]);
    and (g3,a[2],b[2]);
    and (g4,a[3],b[3]);

    xor (p1,a[0],b[0]);
    xor (p2,a[1],b[1]);
    xor (p3,a[2],b[2]);
    xor (p4,a[3],b[3]);

    assign c1= cin;
    assign c2= g1 | (p1 & c1);
    assign c3= g2 | (p2 & (g1 | (p1 & c1)));
    assign c4= g3 | (p3 & (g2 | (p2 & (g1 | (p1 & c1))))));
    assign c5= g4 | (p4 & (g3 | (p3 & (g2 | (p2 & (g1 | (p1 & c1)))))));

    assign sum[0] = p1 ^ c1;
    assign sum[1] = p2 ^ c2;
    assign sum[2] = p3 ^ c3;
    assign sum[3] = p4 ^ c4;

    assign cout = c5;
endmodule
```

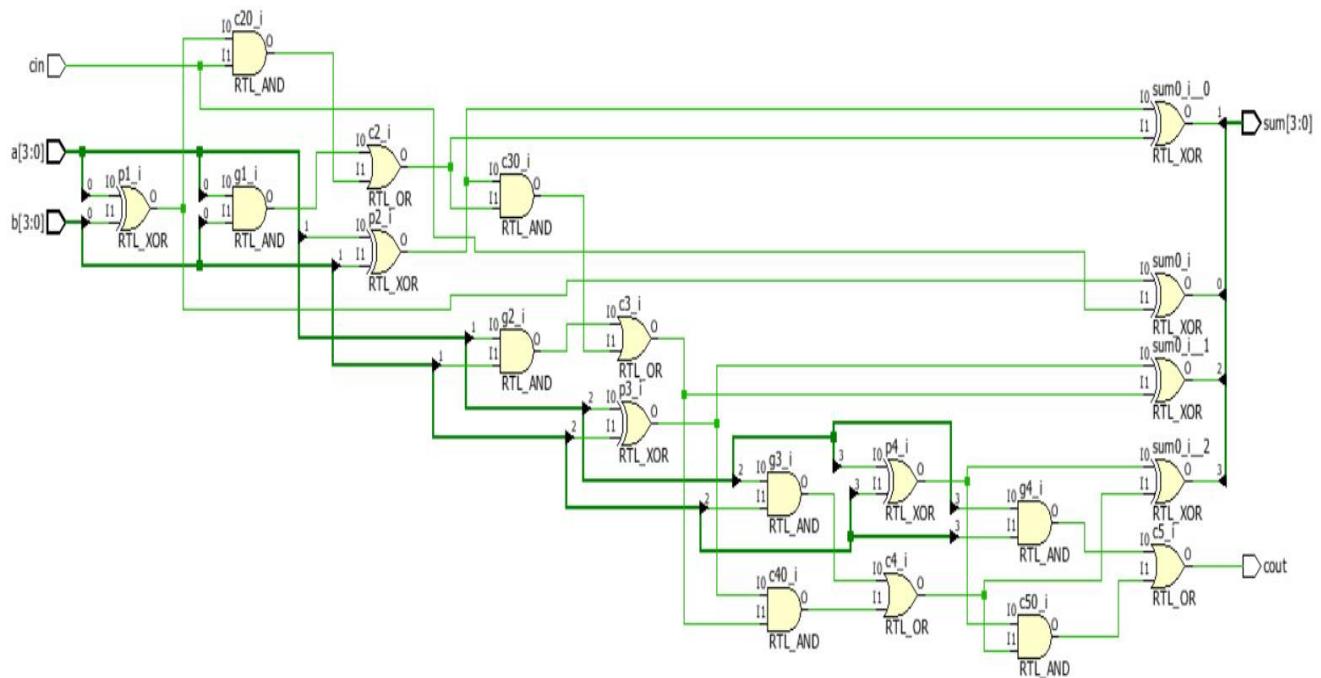
b) TESTBENCH :-

```
module _4Bit_Carry_Look_Ahead_Adder_tb(  
);  
reg [3:0]a;  
reg [3:0]b;  
reg cin;  
wire cout;  
wire [3:0]sum;  
  
_4Bit_Carry_Look_Ahead_Adder uut(a,b,cin,sum,cout);  
  
initial begin  
  
#000 a = 4'b0000 ; b = 4'b0000 ; cin = 0;  
#100 a = 4'b0001 ; b = 4'b0001 ; cin = 0;  
#100 a = 4'b0011 ; b = 4'b0011 ; cin = 0;  
#100 a = 4'b0111 ; b = 4'b0111 ; cin = 0;  
#100 a = 4'b1111 ; b = 4'b1111 ; cin = 0;  
#100 a = 4'b0000 ; b = 4'b0000 ; cin = 1;  
#100 a = 4'b0001 ; b = 4'b0001 ; cin = 1;  
#100 a = 4'b0011 ; b = 4'b0011 ; cin = 1;  
#100 a = 4'b0111 ; b = 4'b0111 ; cin = 1;  
#100 a = 4'b1111 ; b = 4'b1111 ; cin = 1;  
#100 $finish;  
  
end  
initial begin  
$dumpfile("dump.vcd");  
$dumpvars(0);  
end  
  
endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



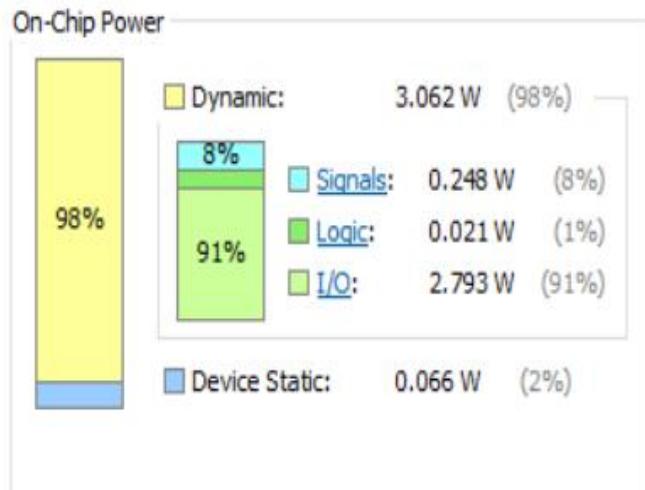
e) SYNTHESIS REPORT : -

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+-----+-----+  
| |BlackBox name |Instances |  
+-----+-----+  
+-----+-----+  
  
Report Cell Usage:  
+-----+-----+  
| |Cell |Count |  
+-----+-----+  
|1 |LUT3 | 2|  
|2 |LUT5 | 4|  
|3 |IBUF | 9|  
|4 |OBUF | 5|  
+-----+-----+  
  
Report Instance Areas:  
+-----+-----+-----+  
| |Instance |Module |Cells |  
+-----+-----+-----+  
|1 |top | | 20|  
+-----+-----+-----+  
  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:05 ; elapsed = 00:00:06 . Memory (MB): peak = 420.418 ; gain = 260.879  
-----
```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 3.128 W
Junction Temperature: 39.9 °C
Thermal Margin: 60.1 °C (12.5 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



9) N-BIT COMPARATOR :-

a) VERILOG CODE: -

```
module n_bit_comparator(
    input [n-1:0] a,
    input [n-1:0] b,
    output reg greater,
    output reg equal,
    output reg lesser
);
parameter n=3 ;
always @ (a,b)
begin

if(a>b)
begin
greater = 1;
equal = 0;
lesser = 0;
end

else if(a==b)
begin
greater = 0;
equal = 1;
lesser = 0;
end

else if(a<b)
begin
greater = 0;
equal = 0;
lesser = 1;
end

end
endmodule
```

b) TESTBENCH :-

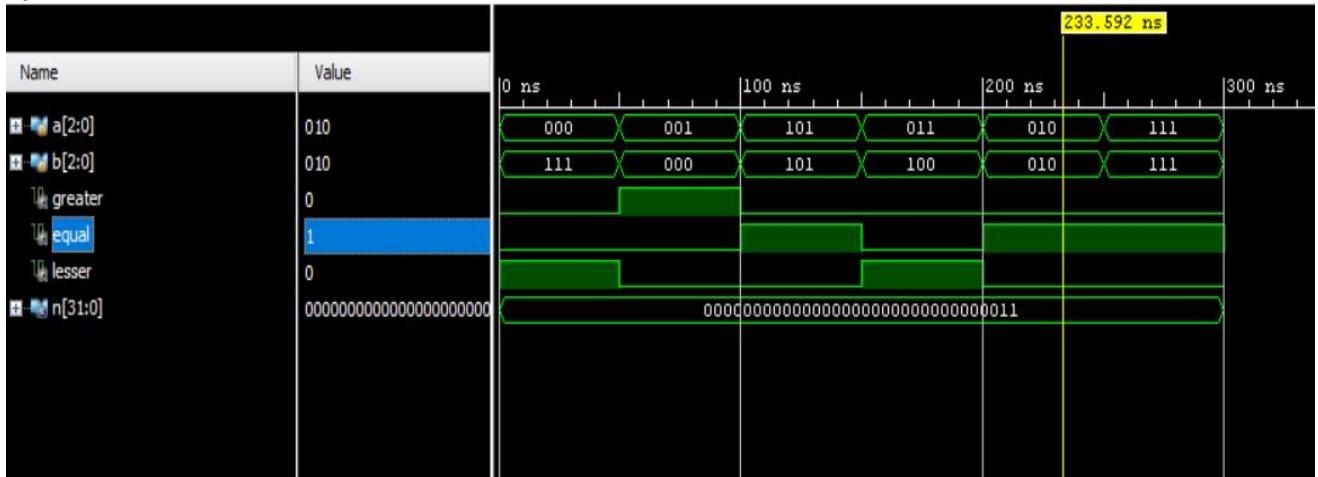
```
module n_bit_comparator_tb(
);
parameter n=3;
reg [(n-1):0]a;
reg[(n-1):0]b;
wire greater,equal,lesser;

n_bit_comparator uut(a,b,greater,equal,lesser);

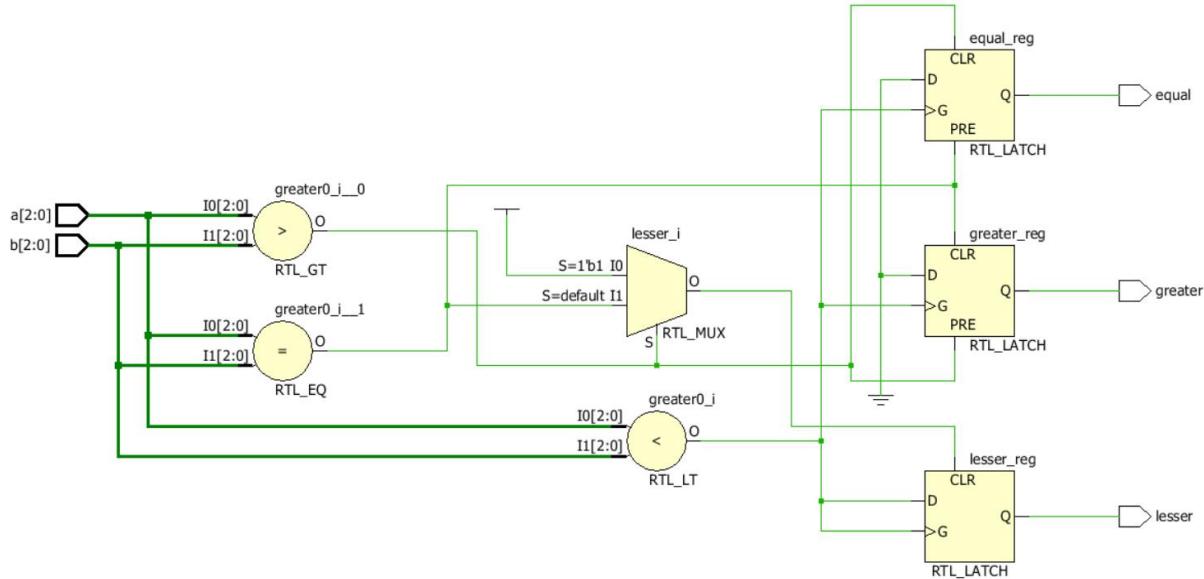
initial begin

#00 a=3'b000; b=3'b111;
#50 a=3'b001; b=3'b000;
#50 a=3'b101; b=3'b101;
#50 a=3'b011; b=3'b100;
#50 a=3'b010; b=3'b010;
#50 a=3'b111; b=3'b111;
#50 $finish;
end

initial begin
$dumpfile("dump.vcd");
$dumpvars(0);
end
endmodule
```

c) EPWAVE :-

d) RTL SCHEMATIC :-



e) SYNTHESIS REPORT : -

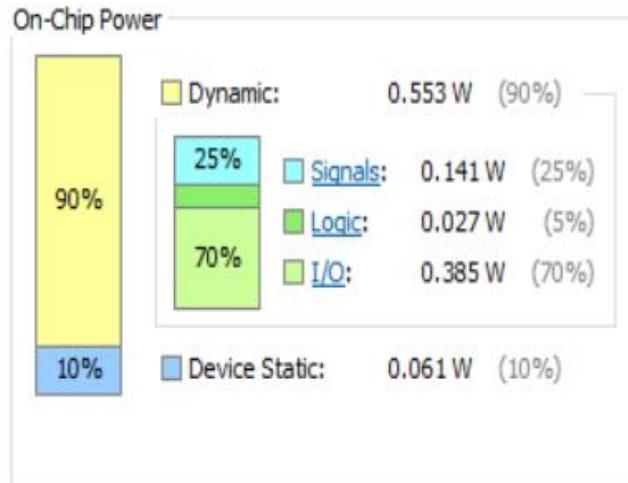
```
-----
Start Writing Synthesis Report
-----

Report BlackBoxes:
+-----+-----+
| |BlackBox name |Instances |
+-----+-----+
+-----+-----+
+-----+-----+
Report Cell Usage:
+-----+-----+
|     |Cell |Count |
+-----+-----+
|1    |LUT6 |    5|
|2    |LDC  |    1|
|3    |LDCLP |   2|
|4    |IBUF |    6|
|5    |OBUF |    3|
+-----+-----+
Report Instance Areas:
+-----+-----+-----+
|     |Instance |Module |Cells |
+-----+-----+-----+
|1    |top      |       | 17|
+-----+-----+-----+
Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:07 . Memory (MB): peak = 409.504 ; gain = 249.984
```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.614 W
Junction Temperature: 27.9 °C
Thermal Margin: 72.1 °C (15.0 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



10) SERIAL IN SERIAL OUT SHIFT REGISTER :-

a) VERILOG CODE: -

```
module siso(
    input clk,
    input rst,
    output reg [3:0] q,
    input s_in,
    output reg s_out
);

    always @ (posedge clk)
    begin
        if(rst)
            begin
                q=4'b0000;
                s_out=1'b0;
            end
        else
            begin
                q=q<<1;
                q[0]=s_in;
                s_out = q[3];
            end
    end
endmodule
```

b) TESTBENCH : -

```
module siso_tb()

);
reg clk,s_in;
reg rst;
wire [3:0]q;
wire s_out;

siso uut(clk,rst,q,s_in,s_out);

initial begin
    clk = 0;
    forever #5 clk = ~clk;
    End
```

```

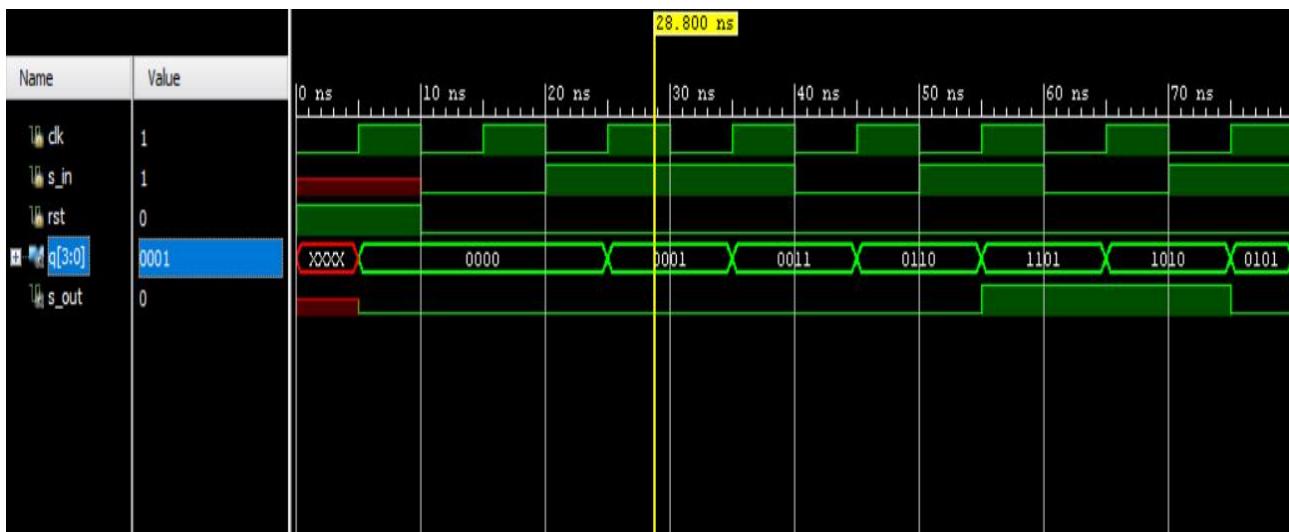
initial
begin
#00 rst = 1'b1;
#10 rst = 1'b0;
#500 $finish;

end
initial begin

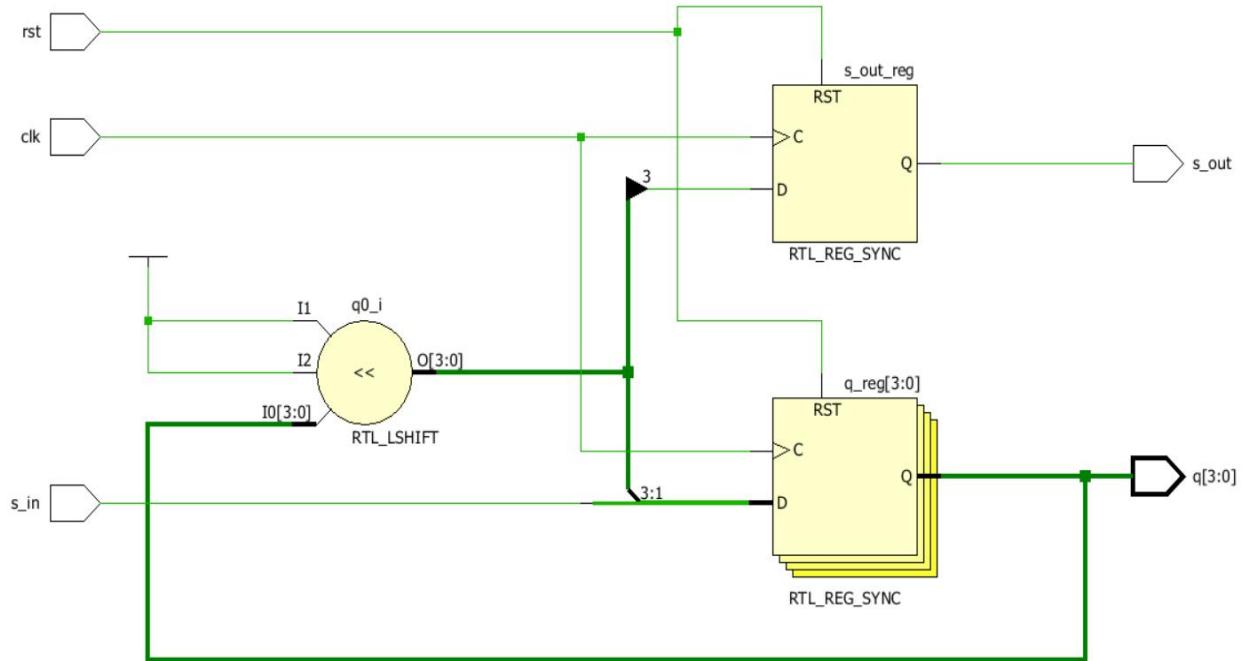
#10 s_in = 1'b0;
#10 s_in = 1'b1;
#10 s_in = 1'b1;
#10 s_in = 1'b0;
#10 s_in = 1'b1;
#10 s_in = 1'b0;
#10 s_in = 1'b1;
#10 s_in = 1'b1;
#10 $finish;
end
endmodule

```

c) EPWAVE :-



d) RTL SCHEMATIC :-



e) SYNTHESIS REPORT :-

```
Start Writing Synthesis Report
-----
Report BlackBoxes:
+-----+-----+
| BlackBox name | Instances |
+-----+-----+
+-----+-----+
Report Cell Usage:
+-----+-----+
|      |Cell |Count |
+-----+-----+
|1     |BUFG  |    1|
|2     |FDRE  |    4|
|3     |IBUF   |    3|
|4     |OBUF   |    5|
+-----+-----+
Report Instance Areas:
+-----+-----+-----+
|      |Instance |Module |Cells |
+-----+-----+-----+
|1     |top     |       |  13|
+-----+-----+-----+
-----
Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:07 . Memory (MB): peak = 400.836 ; gain = 241.180
```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 1.341 W

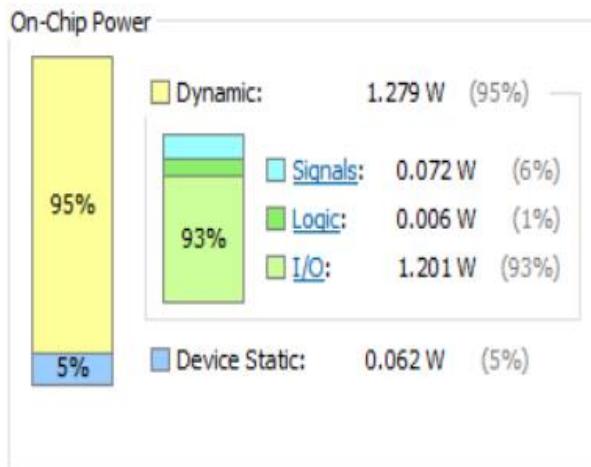
Junction Temperature: 31.4 °C

Thermal Margin: 68.6 °C (14.3 W)

Effective ΔJA: 4.8 °C/W

Power supplied to off-chip devices: 0 W

Confidence level: Low



11) SERIAL IN PARALLEL OUT SHIFT REGISTER :-

a) VERILOG CODE:-

```
module Dff(
    input clk,
    input rst,
    input d,
    output reg q
);
    always @ (posedge clk)
    begin
        if(rst)
            q=0;
        else if(clk)
            q = d ;
    end
endmodule
```

```
module siro(
    input clk,
    input rst,
    input s_in,
    output [3:0] s_out
);

Dff d1(clk,reset,s_in,s_out[0]);
Dff d2(clk,reset,s_out[0],s_out[1]);
Dff d3(clk,reset,s_out[1],s_out[2]);
Dff d4(clk,reset,s_out[2],s_out[3]);
endmodule
```

b) TESTBENCH :-

```
module sipo_tb;
reg clk,rst;
reg s_in;
wire [3:0]s_out;

sipo uut(clk,rst,s_in,s_out);

initial begin

clk = 1'b0;
forever #5 clk = ~clk;
end

initial begin
rst=1'b1;

#10 rst = 1'b0;

end

always @ (posedge clk,s_in)
begin

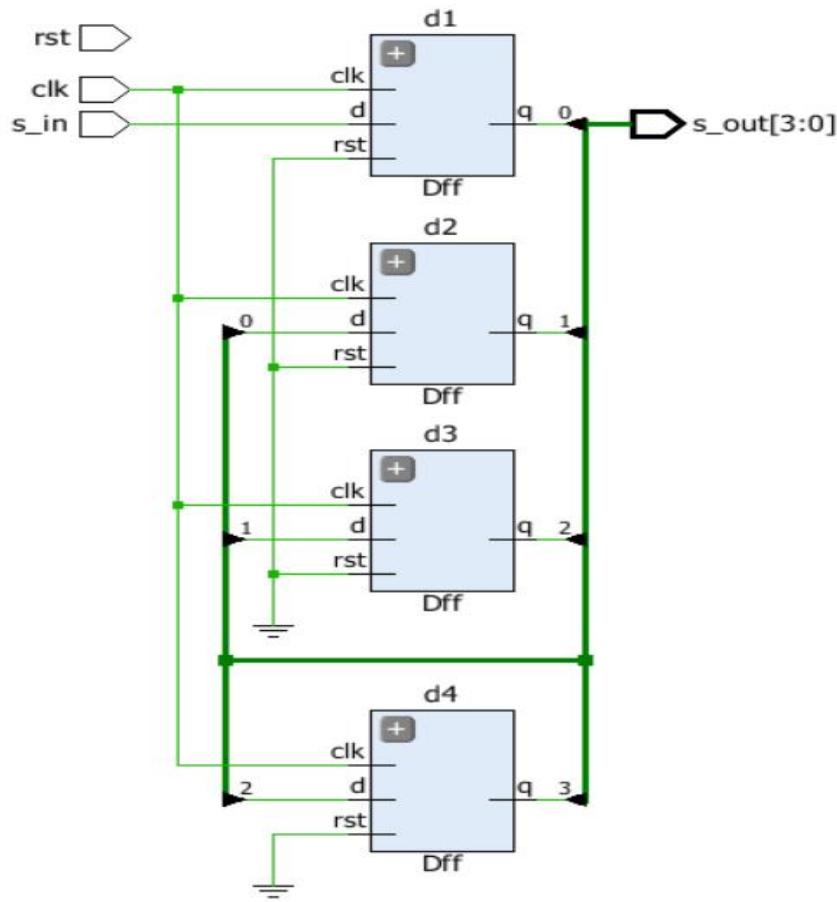
#10 s_in = 1'b0;
#10 s_in = 1'b1;
#10 s_in = 1'b1;
#10 s_in = 1'b0;
#10 s_in = 1'b1;
#10 s_in = 1'b0;
#10 s_in = 1'b1;
#10 $finish;
end

endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



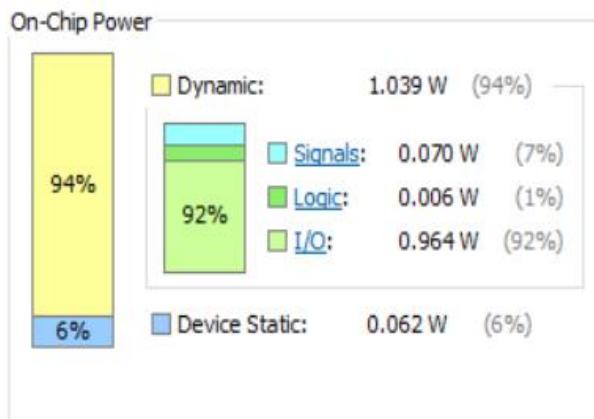
e) SYNTHESIS REPORT : -

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+-----+-----+  
| !BlackBox name |Instances |  
+-----+-----+  
+-----+-----+  
  
Report Cell Usage:  
+-----+-----+  
|     |Cell |Count |  
+-----+-----+  
|1    |BUFGE|    1|  
|2    |FDRE |    4|  
|3    |IBUF  |    2|  
|4    |OBUF  |    4|  
+-----+-----+  
  
Report Instance Areas:  
+-----+-----+-----+  
|           |Instance |Module |Cells |  
+-----+-----+-----+  
|1    |top    |       |    1|  
|2    |d1     |Dff   |    1|  
|3    |d2     |Dff_0 |    1|  
|4    |d3     |Dff_1 |    1|  
|5    |d4     |Dff_2 |    1|  
+-----+-----+-----+  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:05 ; elapsed = 00:00:07 . Memory (MB): peak = 402.305 ; gain = 242.840  
-----
```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 1.101 W
Junction Temperature: 30.3 °C
Thermal Margin: 69.7 °C (14.5 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



12) PARALLEL IN PARALLEL OUT REGISTER : -

a) VERILOG CODE: -

```
module pipo(
    input clk,
    input rst,
    input [3:0] d,
    output reg [3:0] q
);
    always @ (posedge clk,d)
    begin
        if(rst)
            q<=0000;
        else
            q<=d;

    end
endmodule
```

b) TESTBENCH : -

```
module pipo_tb;
    reg clk,rst;
    reg [3:0]d;
    wire [3:0]q;

    pipo uut(clk,rst,d,q);

    initial begin
        $monitor("%t | d = %b | q = %b",$time,d,q);
    end

    initial begin
        clk=1'b0;
        forever #5 clk=~clk;
    end

    initial begin
        rst = 1'b1;
        #10 rst = 1'b0;
    end
```

```

initial begin
#00 d=4'b0000;
#10 d=4'b1001;
#10 d=4'b1011;
#10 d=4'b1101;
#10 d=4'b0101;rst=1'b1;
#10 d=4'b1010;rst=1'b0;
#10 d=4'b1100;
#10 d=4'b1111;
#10 d=4'b0000;
#10 d=4'b0001;
#10 d=4'b0011;
#10 $finish;
end

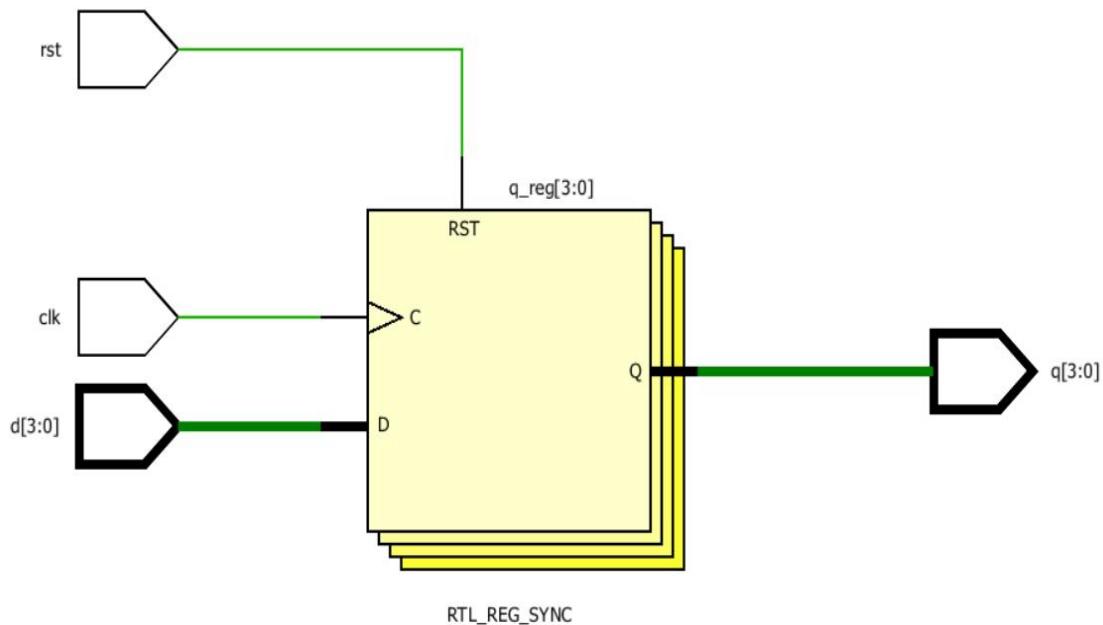
```

```
endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



e) SYNTHESIS REPORT :-

Start Writing Synthesis Report

Report BlackBoxes:

| BlackBox name | Instances |
|---------------|-----------|
| | |
| | |
| | |

Report Cell Usage:

| Cell | Count |
|------|-------|
| BUF | 1 |
| FDRE | 4 |
| IBUF | 6 |
| OBUF | 4 |

Report Instance Areas:

| Instance | Module | Cells |
|----------|--------|-------|
| top | | 15 |

Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 . Memory (MB): peak = 393.809 ; gain = 234.270

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 1.146 W

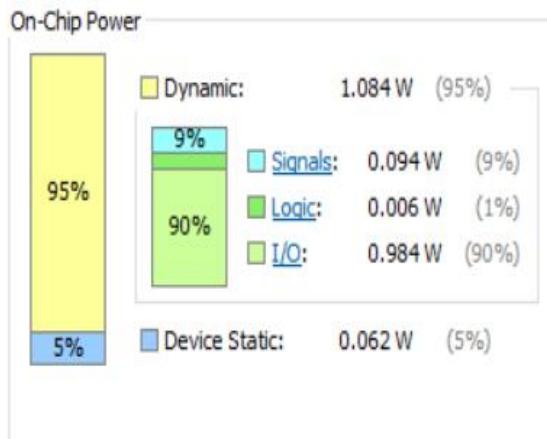
Junction Temperature: 30.5 °C

Thermal Margin: 69.5 °C (14.5 W)

Effective ΔJA: 4.8 °C/W

Power supplied to off-chip devices: 0 W

Confidence level: Low



13) PARALLEL IN SERIAL OUT REGISTER :-

a) VERILOG CODE: -

```
module Dff(
    input clk,
    input rst,
    input d,
    output reg q
);
    always @ (posedge clk)
        begin
            if(rst)
                q<=1'b0;
            else if(clk)
                q<=d;
        end
endmodule

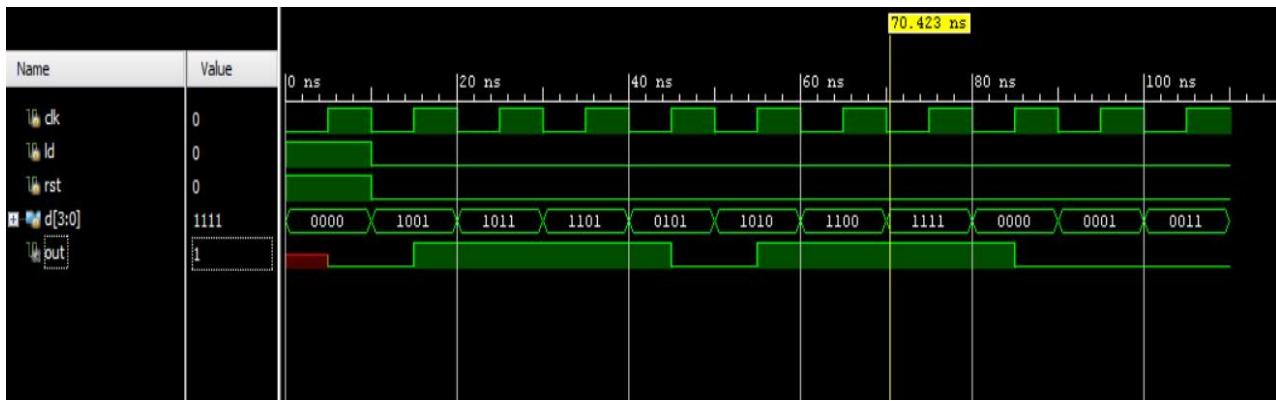
module shift_register(
    input d,
    input si,
    input ld,
    output q );
    assign q = (si & ld) | (d & ~ld);
endmodule

module piso(
    input clk,
    input ld,rst,
    input [3:0] d,
    output out );

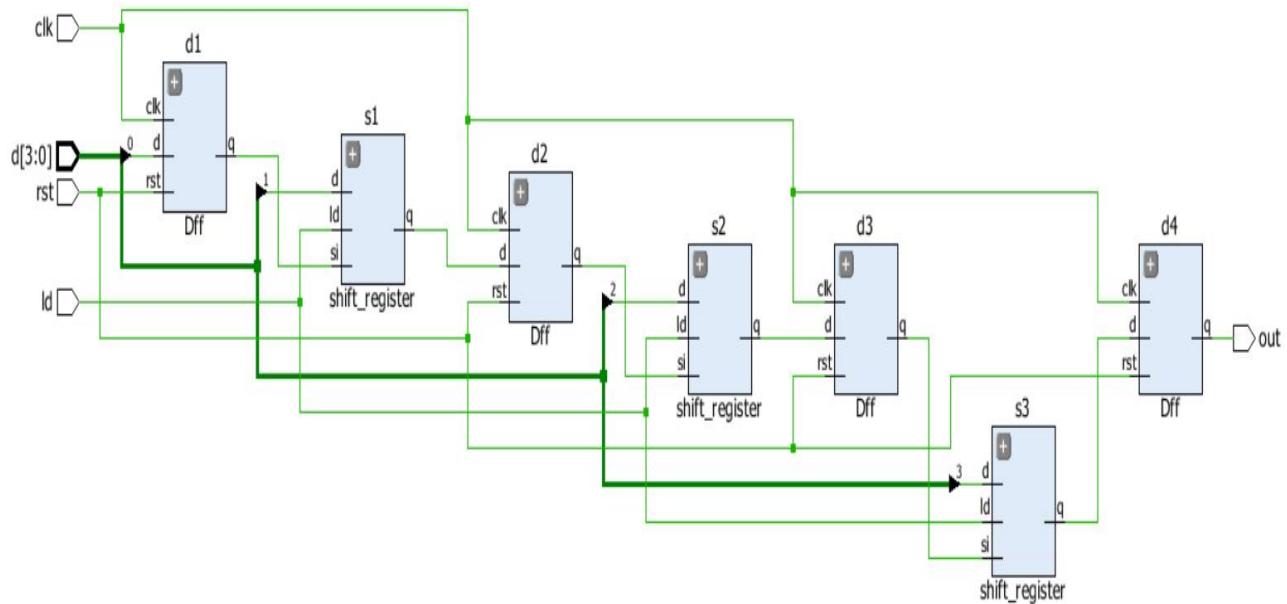
    wire w1,w2,w3;
    wire q1,q2,q3;

    Dff d1(clk,rst,d[0],w1);
        shift_register s1(d[1],w1,ld,q1);
    Dff d2(clk,rst,q1,w2);
        shift_register s2(d[2],w2,ld,q2);
    Dff d3(clk,rst,q2,w3);
        shift_register s3(d[3],w3,ld,q3);
    Dff d4(clk,rst,q3,out);
endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



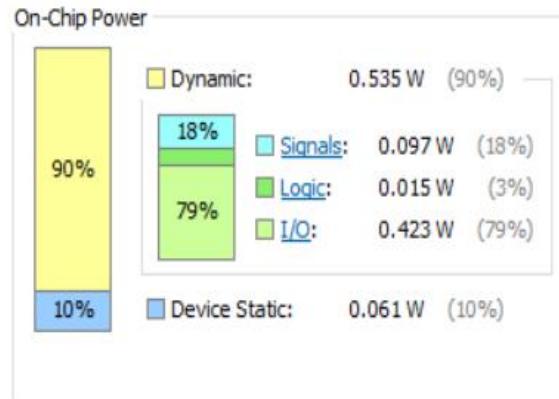
e) SYNTHESIS REPORT : -

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+---+---+  
| |BlackBox name |Instances |  
+---+---+  
+---+---+  
  
Report Cell Usage:  
+---+---+---+  
| |Cell |Count |  
+---+---+---+  
|1 |BUFGE | 1|  
|2 |LUT3 | 3|  
|3 |FDRE | 4|  
|4 |IBUF | 7|  
|5 |OBUF | 1|  
+---+---+  
  
Report Instance Areas:  
+---+---+---+  
| |Instance |Module |Cells |  
+---+---+---+  
|1 |top | 1 | 16|  
|2 | d1 | Dff | 2|  
|3 | d2 | Dff_0 | 2|  
|4 | d3 | Dff_1 | 2|  
|5 | d4 | Dff_2 | 1|  
+---+---+  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:09 ; elapsed = 00:00:21 . Memory (MB): peak = 409.051 ; gain = 249.641  
-----
```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.596 W
Junction Temperature: 27.8 °C
Thermal Margin: 72.2 °C (15.0 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



14) BIDIRECTION SHIFT REGISTER :-

a) VERILOG CODE:-

```
module bi_shift_reg(clk,rst,en,dir,d,q,out );
parameter n = 4;
input clk;
input rst;
input en;
input dir;
input d;
output reg [n-1:0]q;
output reg out;

always @ (posedge clk,en)
begin

if(rst)
    q = 4'b0000;
else if (clk)
begin
    if(en)
        begin
            case(dir)
                0 : begin q = {q[n-2:0],d}; out <= q[0]; end
                1 : begin q = {d,q[n-1:1]}; out <= q[0]; end
            endcase
        end
    else
        q <= q;
end
end
endmodule
```

b) TESTBENCH :-

```
module bi_shift_reg_tb(
);
parameter n = 4;
reg clk;
reg rst;
reg en;
reg dir;
reg d;
wire [n-1:0]q;
wire out;

bi_shift_reg uut(clk,rst,en,dir,d,q,out );

initial begin
$monitor("clk = %t | en = %b | dir = %b | d = %b | q = %b",$time,en,dir,d,q);
end

initial begin
clk = 1'b0;
forever #5 clk = ~clk;
end
initial begin
rst = 1'b1; en=1'b0;
#10 rst = 1'b0; en=1'b1;
end

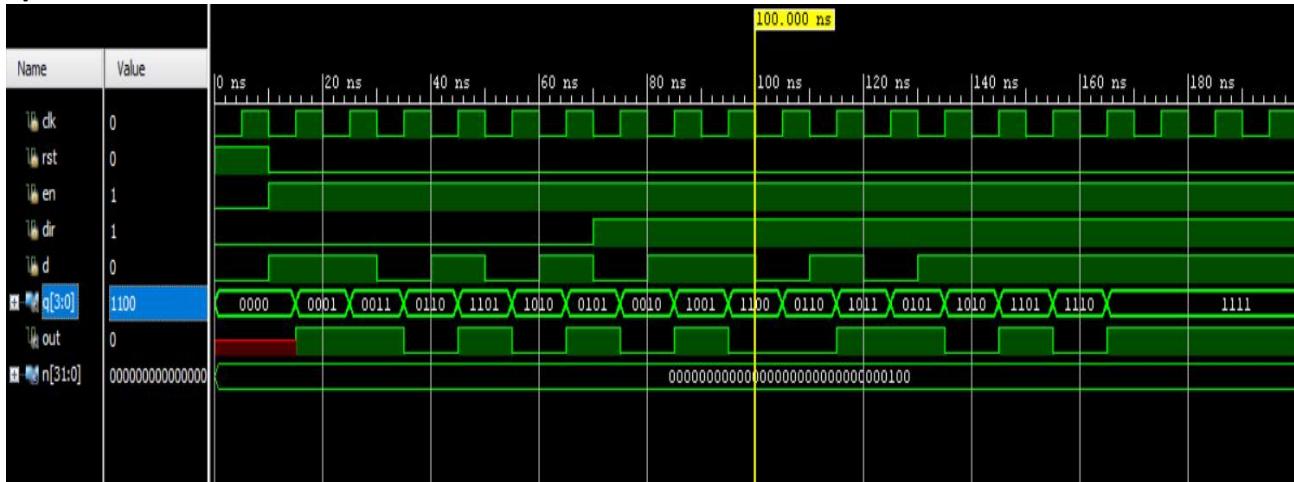
initial begin
dir = 0 ; d=1'b0;
#10 dir = 0 ; d=1'b1;
#10 dir = 0 ; d=1'b1;
#10 dir = 0 ; d=1'b0;
#10 dir = 0 ; d=1'b1;
#10 dir = 0 ; d=1'b0;
#10 dir = 1 ; d=1'b0;
#10 dir = 1 ; d=1'b1;
#10 dir = 1 ; d=1'b1;
#10 dir = 1 ; d=1'b0;
#10 dir = 1 ; d=1'b1;
```

```

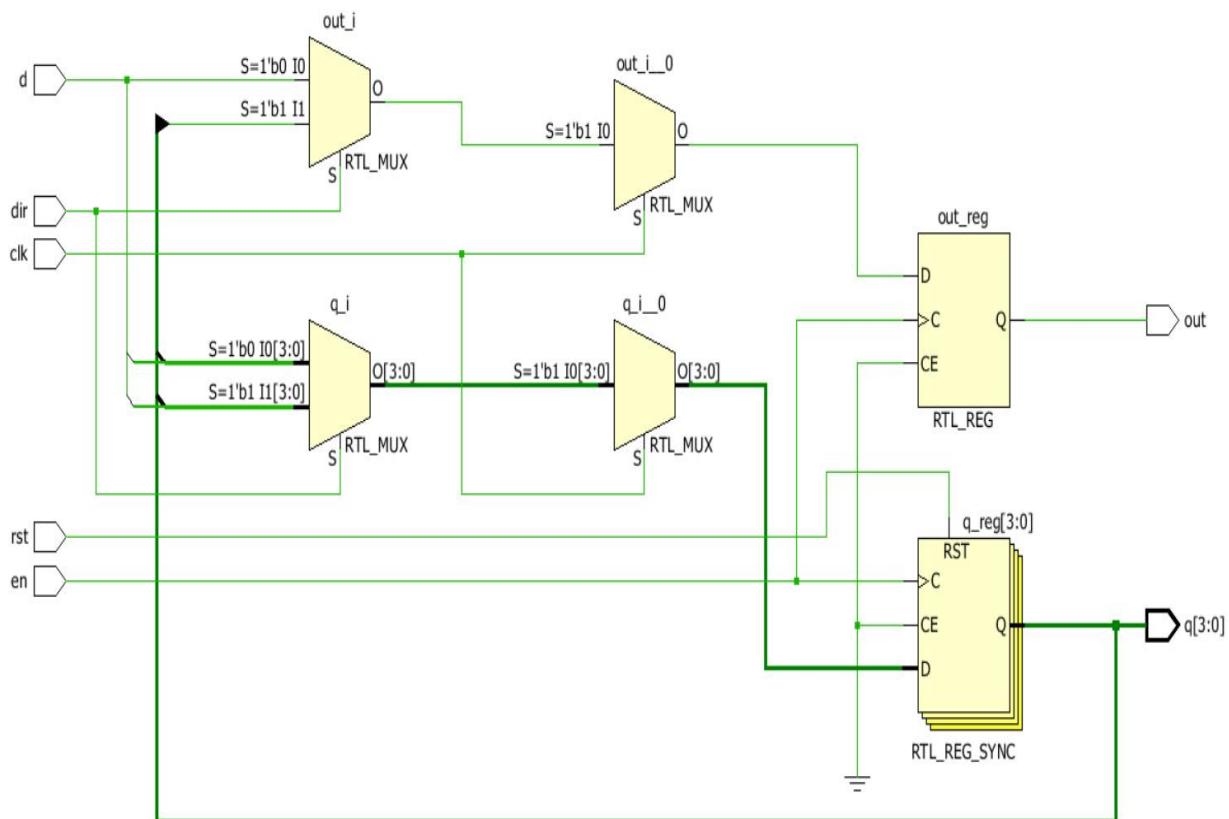
#10 dir = 1 ; d=1'b0;
#10 dir = 1 ; d=1'b1;
end
Endmodule

```

c) EPWAVE :-



d) RTL SCHEMATIC :-



e) SYNTHESIS REPORT :-

```
-----
Start Writing Synthesis Report
-----

Report BlackBoxes:
+-----+-----+
| BlackBox name | Instances |
+-----+-----+
+-----+-----+
+-----+-----+

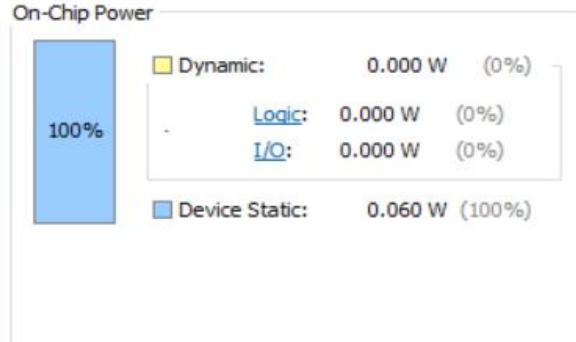
Report Cell Usage:
+-----+-----+
|     |Cell |Count |
+-----+-----+
|1    |OBUF |    5|
+-----+-----+

Report Instance Areas:
+-----+-----+-----+
|     |Instance |Module |Cells |
+-----+-----+-----+
|1    |top    |    |    5|
+-----+-----+-----+
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:09 ; elapsed = 00:00:11 . Memory (MB): peak = 403.184 ; gain = 243.828
```

f) POWER REPORT :-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.06 W
Junction Temperature: 25.3 °C
Thermal Margin: 74.7 °C (15.5 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



15) PRBS SEQUENCE GENERATOR: -

a) VERILOG CODE: -

```
module prbs(
    input clk,
    input rst,
    output out
);
reg [3:0] temp;

always @ (posedge clk or posedge rst)
begin
    if(rst)
        temp =4'b1000;
    else if(clk)
        temp <={temp[1] ^ temp[0],temp[3],temp[2],temp[1]};
    end
    assign out = temp[0];
endmodule
```

b) TESTBENCH : -

```
module prbs_tb();
    reg clk, rst;
    wire out;

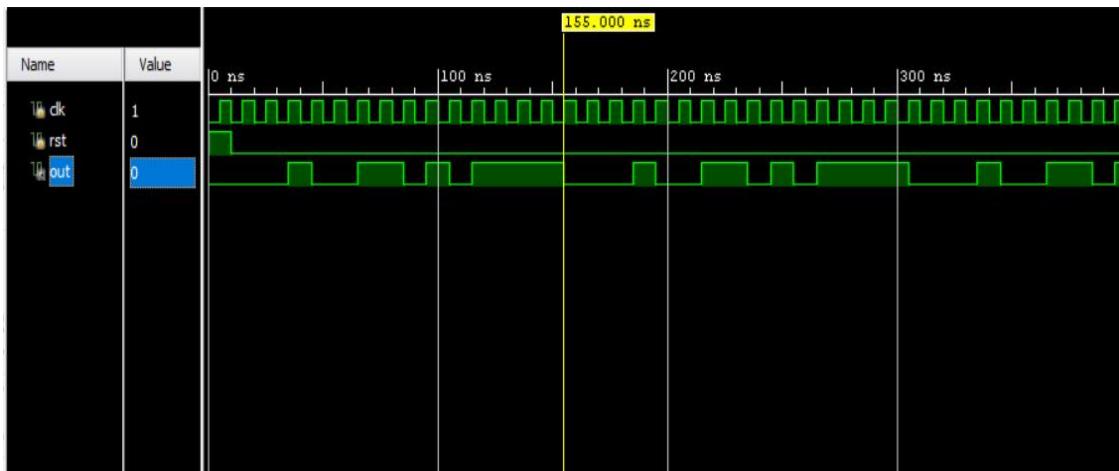
    prbs uut ( clk, rst,out);

    initial begin
        $monitor("clk = %t | rst = %b | out = %b ",$time,rst,out);
    end

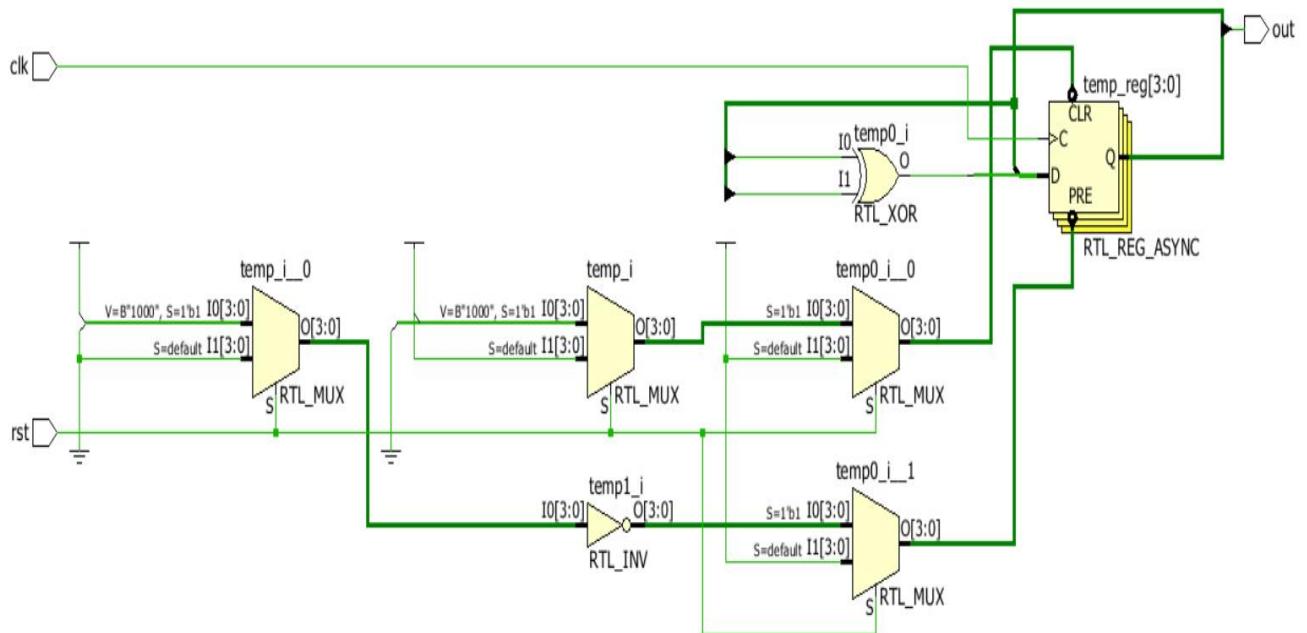
    initial begin
        clk <= 0;
    forever #5 clk <= ~clk;
    end
    initial begin
        rst = 1;
        #10 rst = 0;
        #500 $finish;
    end

endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



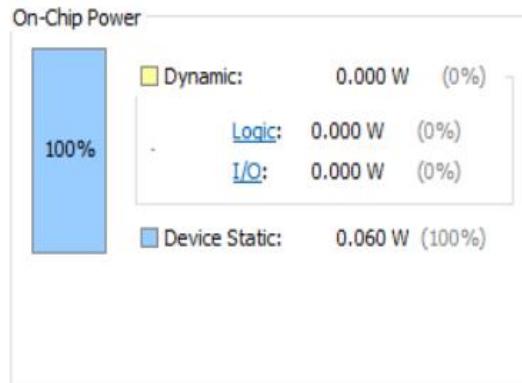
e) SYNTHESIS REPORT :-

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+-----+-----+  
| |BlackBox name |Instances |  
+-----+-----+  
+-----+-----+  
  
Report Cell Usage:  
+-----+-----+  
| |Cell |Count |  
+-----+-----+  
|1 |OBUF | 1|  
+-----+-----+  
  
Report Instance Areas:  
+-----+-----+-----+  
| |Instance |Module |Cells |  
+-----+-----+-----+  
|1 |top | | 1|  
+-----+-----+  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:07 . Memory (MB): peak = 410.449 ; gain = 251.328  
-----
```

f) POWER REPORT :-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.06 W
Junction Temperature: 25.3 °C
Thermal Margin: 74.7 °C (15.5 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: [Low](#)



16) 8-BIT SUBTRACTOR :-

a) VERILOG CODE:-

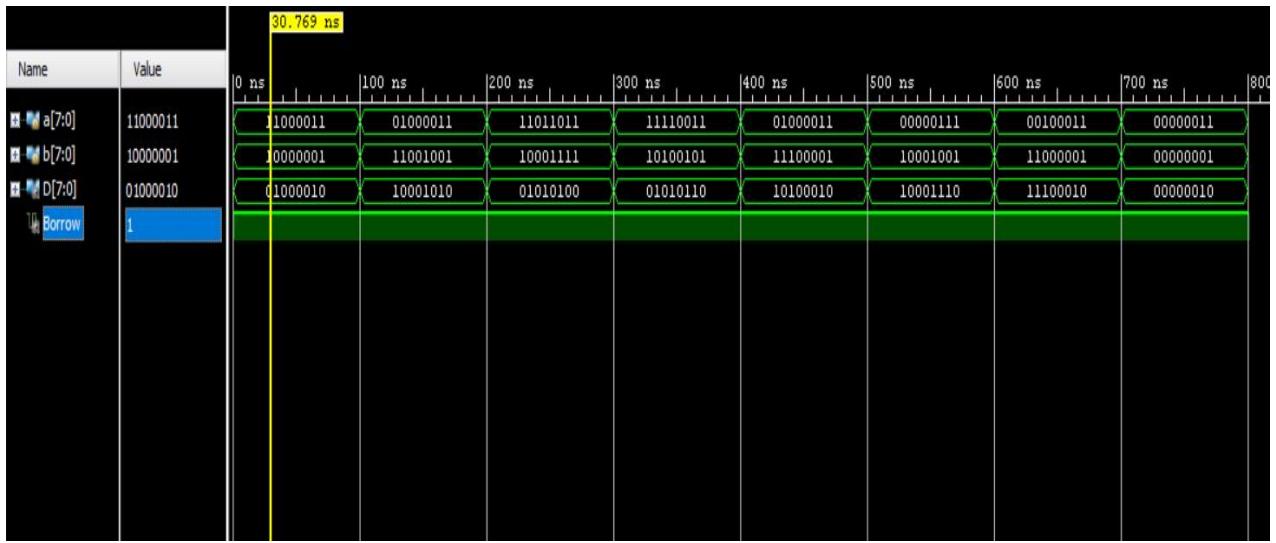
```
module full_subtractor(  
    input x,  
    input y,  
    input z,  
    output borrow,  
    output diff  
);  
  
    assign diff = x^y^z;  
    assign borrow = ~x^y | ~x^z | y^z;  
endmodule
```

```
module _8bit_subractor(  
    input [7:0] a,  
    input [7:0] b,  
    output [7:0]D,  
    output Borrow  
);  
  
    wire w1,w2,w3,w4,w5,w6,w7;  
  
    full_subtractor s1(a[0],b[0],1'b0,w1,D[0]);  
    full_subtractor s2(a[1],b[1],1'b0,w2,D[1]);  
    full_subtractor s3(a[2],b[2],1'b0,w3,D[2]);  
    full_subtractor s4(a[3],b[3],1'b0,w4,D[3]);  
    full_subtractor s5(a[4],b[4],1'b0,w5,D[4]);  
    full_subtractor s6(a[5],b[5],1'b0,w6,D[5]);  
    full_subtractor s7(a[6],b[6],1'b0,w7,D[6]);  
    full_subtractor s8(a[7],b[7],1'b0,Borrow,D[7]);  
  
endmodule
```

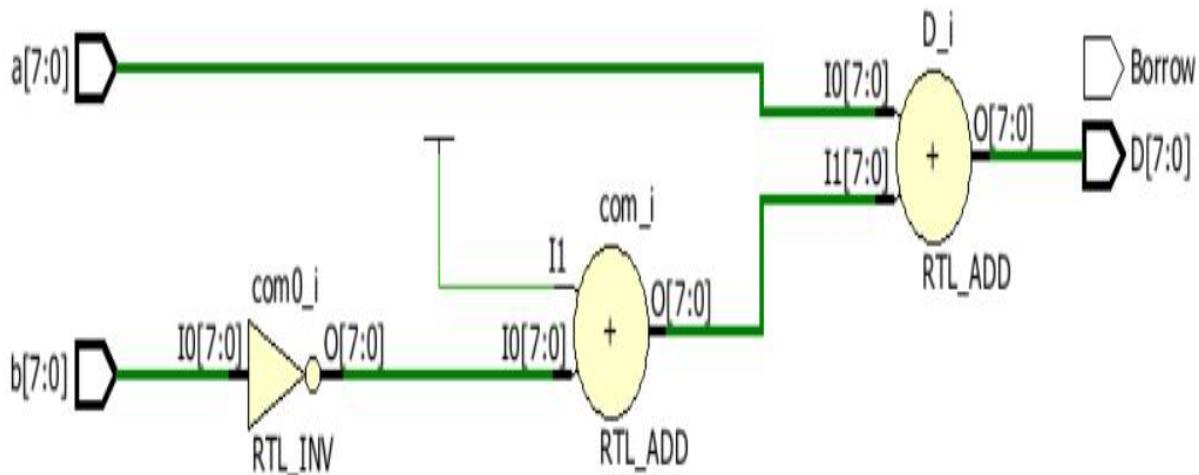
b) TESTBENCH :-

```
module _8bit_subractor_tb(  
);  
reg[7:0]a;  
reg[7:0]b;  
wire [7:0] D;  
wire Borrow;  
  
initial begin  
  
$monitor($time |" $time |a = %b | b = %b | borrow = %b | D = %b | borrow = %b,a,b,Borrow,D);  
  
end  
  
_8bit_subractor uut(a,b,D,Borrow);  
  
initial begin  
  
#000 a=8'b11000011; b=8'b10000001;  
#100 a=8'b01000011; b=8'b11001001;  
#100 a=8'b11011011; b=8'b10001111;  
#100 a=8'b11110011; b=8'b10100101;  
#100 a=8'b01000011; b=8'b11100001;  
#100 a=8'b00000111; b=8'b10001001;  
#100 a=8'b00100011; b=8'b11000001;  
#100 a=8'b00000011; b=8'b00000001;  
  
#100 $finish;  
  
end  
  
initial begin  
  
$dumpfile("dump.vcd");  
$dumpvars(0);  
  
end  
  
endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



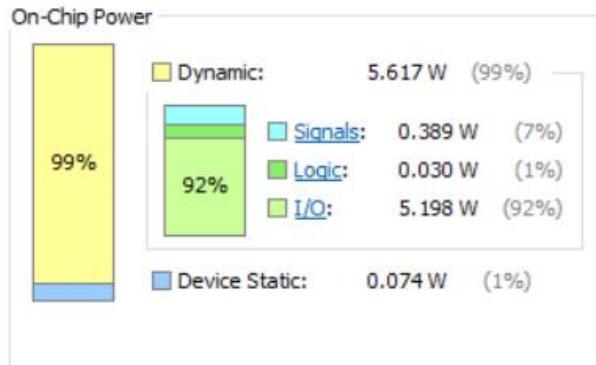
e) SYNTHESIS REPORT :-

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+---+---+  
| |BlackBox name |Instances |  
+---+---+  
+---+---+  
  
Report Cell Usage:  
+---+---+  
| |Cell |Count |  
+---+---+  
|1 |CARRY4 | 2|  
|2 |LUT2 | 8|  
|3 |IBUF | 16|  
|4 |OBUF | 8|  
|5 |OBUFT | 1|  
+---+---+  
  
Report Instance Areas:  
+---+---+---+  
| |Instance |Module |Cells |  
+---+---+---+  
|1 |top | | 35|  
+---+---+---+  
  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:07 . Memory (MB): peak = 410.813 ; gain = 251.418  
-----
```

f) POWER REPORT :-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 5.691 W
Junction Temperature: 52.2 °C
Thermal Margin: 47.8 °C (9.9 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



17) 8-BIT ADDER/SUBTRACTOR :-

a) VERILOG CODE: -

```
module _8bit_adder_sub(
    input [7:0] a,
    input [7:0] b,
    input mode,
    output reg [7:0] result,
    output reg v
);

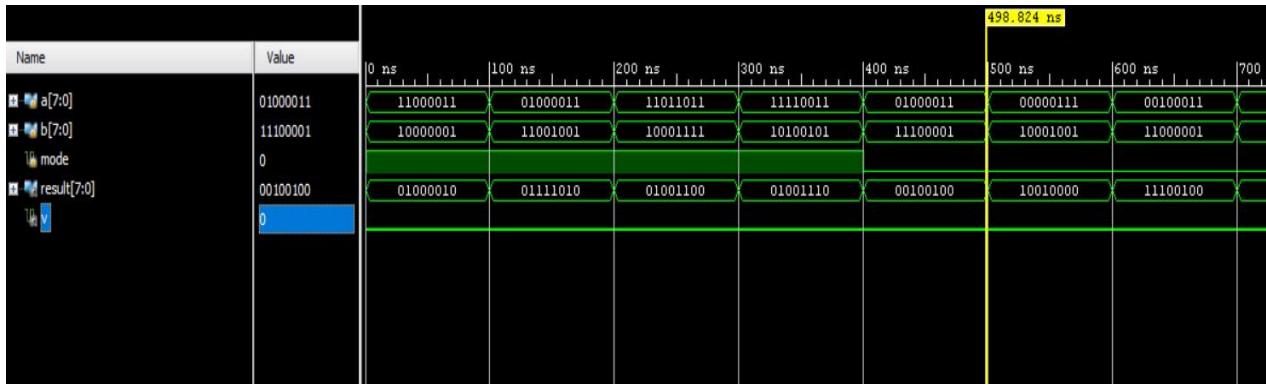
reg [7:0]com;

always @ (a,b,mode)
begin
    if(mode == 1)
        begin
            com = ~b + 1'b1;
            result = a + com;
            v = (a[7]&com[7]&~result[7]) | (~a[7]&~com[7]&result[7]);
        end
    else if(mode == 0)
        begin
            result = a + b;
            v = (a[7]&b[7]&~result[7]) | (~a[7]&~b[7]&result[7]);
        end
end
endmodule
```

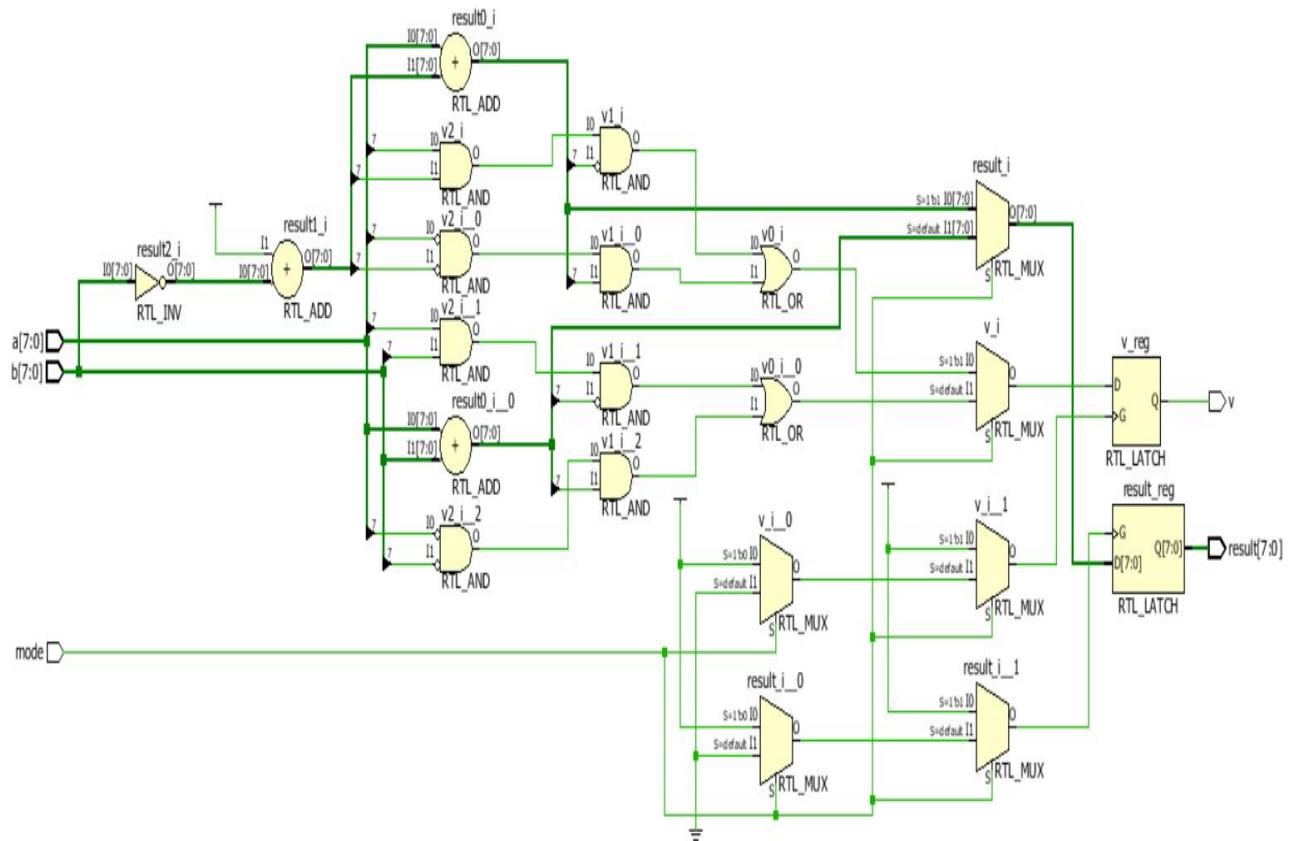
b) TESTBENCH :-

```
module _8bit_sub_add_tb(  
);  
reg [7:0] a;  
reg [7:0] b;  
reg mode;  
wire [7:0] result;  
wire v;  
  
initial begin  
  
$monitor($time |" $time |a = %b | b = %b | mode = %b | v = %b | result = %b,a,b,mode,v,result);  
  
end  
  
_8bit_adder_sub uut(a,b,mode,result,v);  
  
initial begin  
  
#000 mode = 1'b1; a=8'b11000011; b=8'b10000001;  
#100 mode = 1'b1; a=8'b01000011; b=8'b11001001;  
#100 mode = 1'b1; a=8'b11011011; b=8'b10001111;  
#100 mode = 1'b1; a=8'b11110011; b=8'b10100101;  
#100 mode = 1'b0; a=8'b01000011; b=8'b11100001;  
#100 mode = 1'b0; a=8'b00000011; b=8'b10001001;  
#100 mode = 1'b0; a=8'b00100011; b=8'b11000001;  
#100 mode = 1'b0; a=8'b00000011; b=8'b00000001;  
  
#100 $finish;  
  
end  
  
initial begin  
  
$dumpfile("dump.vcd");  
$dumpvars(0);  
  
end  
  
endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



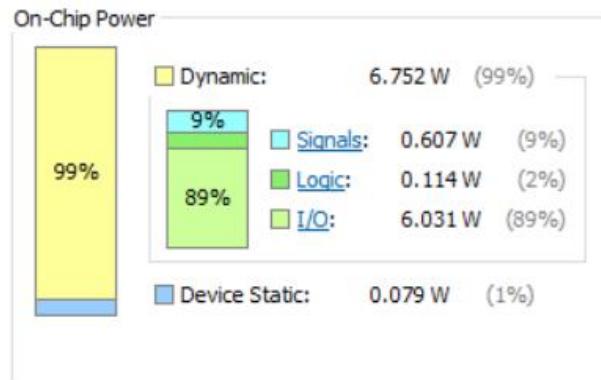
e) SYNTHESIS REPORT :-

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+---+---+  
| BlackBox name | Instances |  
+---+---+  
+---+---+  
  
Report Cell Usage:  
+---+---+  
| Cell | Count |  
+---+---+  
|1 | CARRY4 | 4|  
|2 | LUT2 | 16|  
|3 | LUT3 | 9|  
|4 | LUT6 | 2|  
|5 | IBUF | 17|  
|6 | OBUF | 9|  
+---+---+  
  
Report Instance Areas:  
+---+---+  
| Instance | Module | Cells |  
+---+---+  
|1 | top | | 57|  
+---+---+  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:07 ; elapsed = 00:00:15 . Memory (MB): peak = 421.660 ; gain = 262.137  
-----
```

f) POWER REPORT :-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 6.831 W
Junction Temperature: 57.6 °C
Thermal Margin: 42.4 °C (8.8 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



18) 4-BIT MULTIPLIER:-

a) VERILOG CODE: -

```
module _4bit_multiplier( a,b,product);

    input [3:0]a;
    input [3:0]b;
    output [7:0] product;

    wire [3:0]m0;
    wire [4:0]m1;
    wire [5:0]m2;
    wire [6:0]m3;

    wire [7:0]s0,s1,s2,s3;

    assign m0 = a[3:0] & { 4{b[0]} };
    assign m1 = a[3:0] & { 4{b[1]} };
    assign m2 = a[3:0] & { 4{b[2]} };
    assign m3 = a[3:0] & { 4{b[3]} };

    assign s0 = m0;
    assign s1 = m1<<1;
    assign s2 = m2<<2;
    assign s3 = m3<<3;

    assign product = s0 + s1 + s2 + s3;

endmodule
```

b) TESTBENCH : -

```
module _4bit_multiplier_tb();

    reg [3:0]a;
    reg [3:0]b;
    wire [7:0]product;

    _4bit_multiplier uut(a,b,product);

    initial begin
```

```

#000 a = 4'b1101 ; b = 4'b1010 ;
#100 a = 4'b0101 ; b = 4'b1001 ;
#100 a = 4'b0011 ; b = 4'b1011 ;
#100 a = 4'b0111 ; b = 4'b1111 ;
#100 a = 4'b1111 ; b = 4'b1111 ;
#100 a = 4'b0100 ; b = 4'b1000 ;
#100 a = 4'b0101 ; b = 4'b0001 ;
#100 a = 4'b1011 ; b = 4'b0011 ;
#100 a = 4'b0111 ; b = 4'b0101 ;
#100 a = 4'b1111 ; b = 4'b1101 ;
#100 $finish;

end
initial begin
  $dumpfile("dump.vcd");
  $dumpvars(0);
end

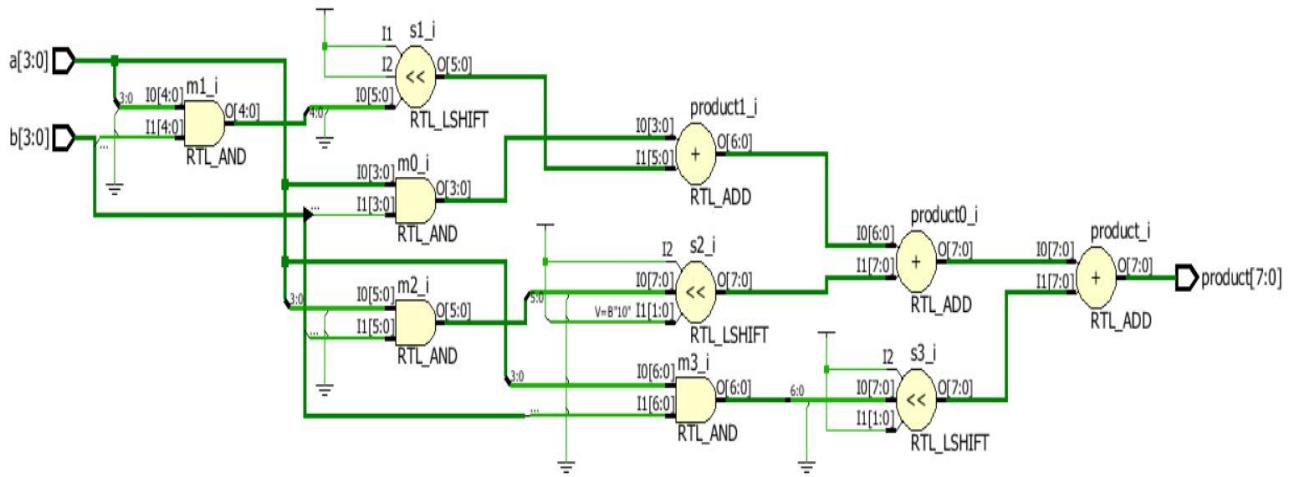
endmodule

```

c) EPWAVE :-



d) RTL SCHEMATIC :-



e) SYNTHESIS REPORT : -

```

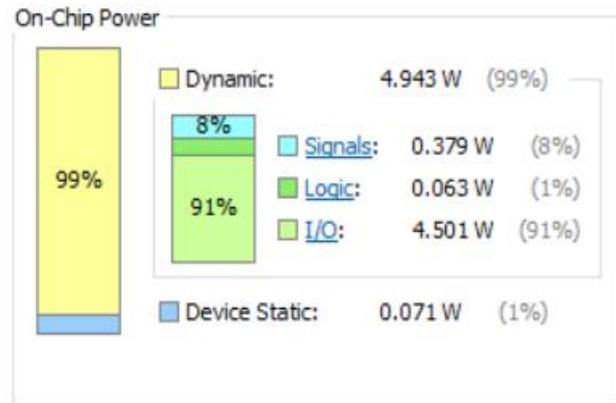
-----+
| Start Writing Synthesis Report
|
|
| Report BlackBoxes:
| +---+-----+
| | BlackBox name | Instances |
| +---+-----+
| +---+-----+
|
| Report Cell Usage:
| +---+-----+
| | Cell | Count |
| +---+-----+
| | 1 | CARRY4 | 2 |
| | 2 | LUT2 | 6 |
| | 3 | LUT3 | 2 |
| | 4 | LUT4 | 1 |
| | 5 | LUT6 | 9 |
| | 6 | IBUF | 8 |
| | 7 | OBUF | 8 |
| +---+-----+
|
| Report Instance Areas:
| +---+-----+
| | Instance | Module | Cells |
| +---+-----+
| | 1 | top | 36 |
| +---+-----+
|
| Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:07 . Memory (MB): peak = 421.020 ; gain = 261.523
-----+

```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 5.014 W
Junction Temperature: 49.0 °C
Thermal Margin: 51.0 °C (10.6 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



19) FIXED POINT DIVISION:-

a) VERILOG CODE: -

```
module divider(divisor, dividend, remainder, result);

input [7:0] divisor, dividend;
output reg [7:0] result, remainder;

integer i;
reg [7:0] divisor_copy, dividend_copy;
reg [7:0] temp;

always @(divisor or dividend)
begin
divisor_copy = divisor;
dividend_copy = dividend;
temp = 0;
for(i = 0;i < 8;i = i + 1)
begin
temp = {temp[6:0], dividend_copy[7]};
dividend_copy[7:1] = dividend_copy[6:0];

temp = temp - divisor_copy;

if(temp[7] == 1)
begin

dividend_copy[0] = 0;
temp = temp + divisor_copy;
end
else
begin

dividend_copy[0] = 1;
end
end
result = dividend_copy;
remainder = dividend - (divisor_copy*dividend_copy);
end
endmodule
```

b) TESTBENCH :-

```
module divider_tb;

// Inputs
reg [7:0] divisor;
reg [7:0] dividend;

// Outputs
wire [7:0] remainder;
wire [7:0] result;

// Instantiate the Unit Under Test (UUT)
divider uut (divisor, dividend, remainder, result);

initial begin
// Initialize Inputs
divisor = 13;
dividend = 28;

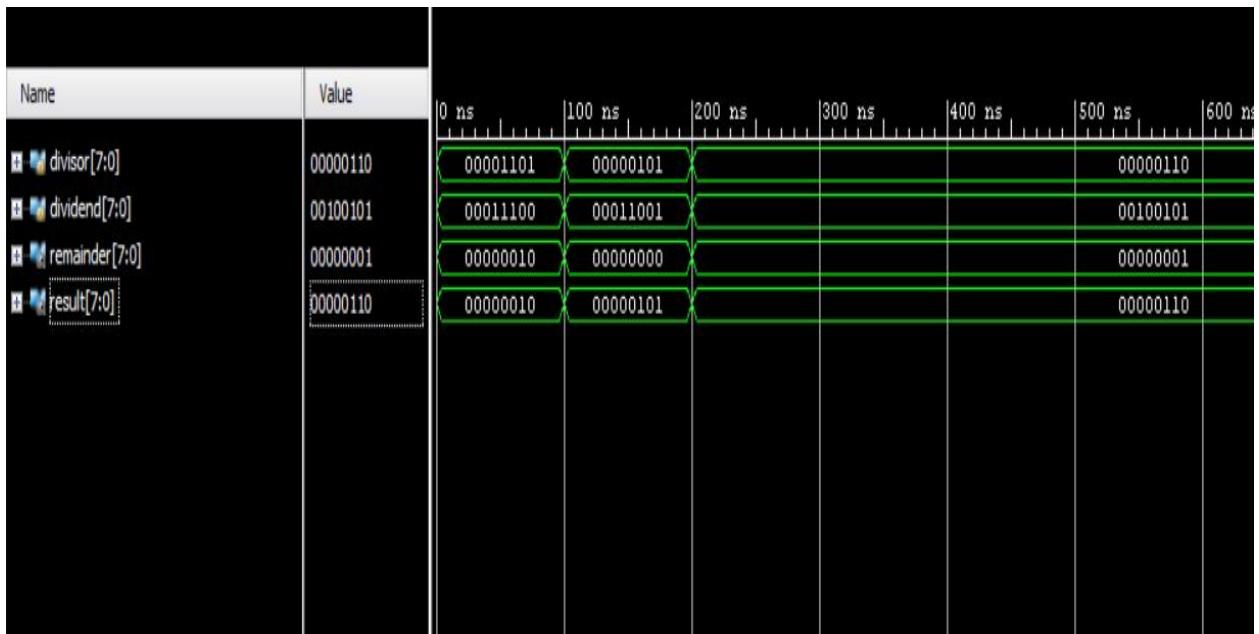
// Wait 100 ns for global reset to finish
#100;

// Add stimulus here
divisor = 5;
dividend = 25;

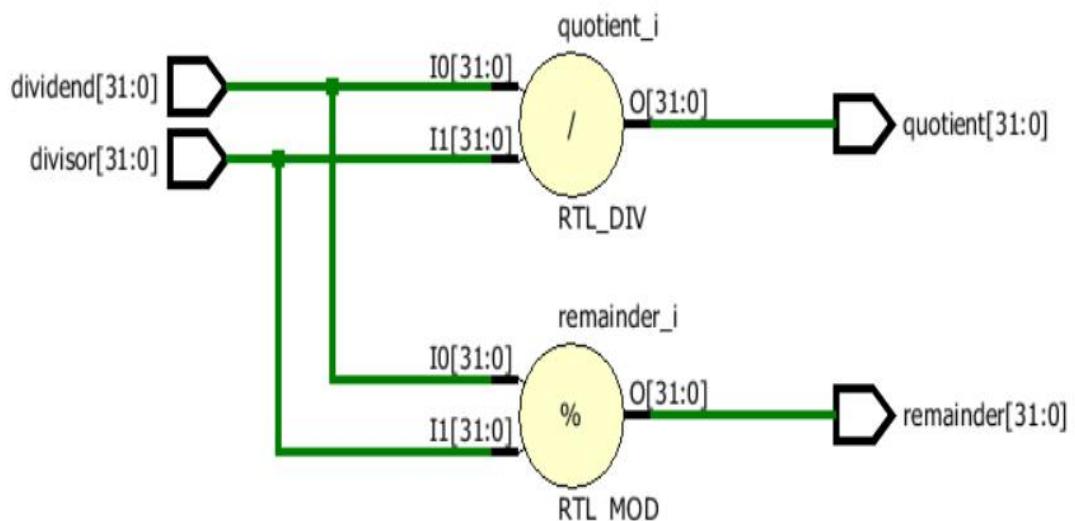
#100
divisor = 6;
dividend = 37;
end

initial begin
$monitor("Divisor: %d, Dividend: %d, Remainder: %d, Result: %d\n", divisor,
dividend,remainder, result);
end
endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



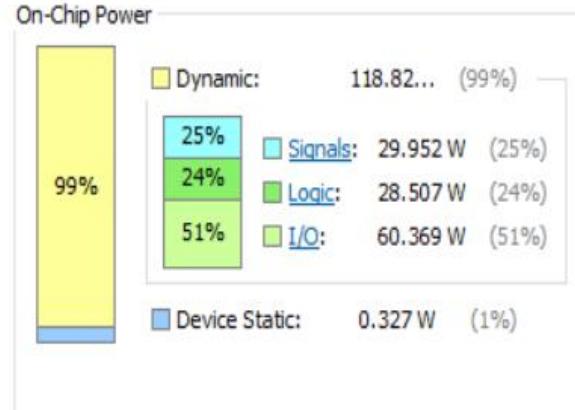
e) SYNTHESIS REPORT :-

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+---+---+  
| BlackBox name | Instances |  
+---+---+  
+---+---+  
  
Report Cell Usage:  
+---+---+  
| Cell | Count |  
+---+---+  
|1 |CARRY4 | 576|  
|2 |LUT1 | 124|  
|3 |LUT2 | 101|  
|4 |LUT3 | 1991|  
|5 |LUT4 | 29|  
|6 |LUT5 | 9|  
|7 |LUT6 | 50|  
|8 |IBUF | 64|  
|9 |OBUF | 64|  
+---+---+  
  
Report Instance Areas:  
+---+---+---+  
| Instance |Module |Cells |  
+---+---+---+  
|1 |top | 3008|  
+---+---+---+  
  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:08 ; elapsed = 00:00:08 . Memory (MB): peak = 417.785 ; gain = 258.359  
-----
```

f) POWER REPORT :-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 119.155 W
Junction Temperature: 125.0 °C
Thermal Margin: -494.4 °C (-103.3 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



20) MASTER SLAVE JK FLIP FLOP :-

a) VERILOG CODE:-

```
module jk_flipflop(
    input clk,
    input j,
    input k,
    output reg q,
    output reg qbar
);

    always @ (posedge clk)
    begin

        case ({j,k})
            2'b00 : begin q <= q; qbar<= ~q; end
            2'b01 : begin q <= 0; qbar<= 1; end
            2'b10 : begin q <= 1; qbar<= 0; end
            2'b11 : begin q <= ~q; qbar<= q; end

        endcase
    end
endmodule

module master_slave(
    input clk,

    input s,
    input r,
    output Q,
    output QBAR
);
    wire w1,w2,w3,w4;
    wire sclk;

    assign sclk = ~clk;

    jk_flipflop master(clk,s,r,w1,w2);
    jk_flipflop slave(sclk,w1,w2,Q,QBAR);

endmodule
```

b) TESTBENCH :-

```
module master_slave_tb( );
    reg clk;
    reg s;
    reg r;
    wire Q;
    wire QBAR;

    master_slave uut(clk,s,r,Q,QBAR);

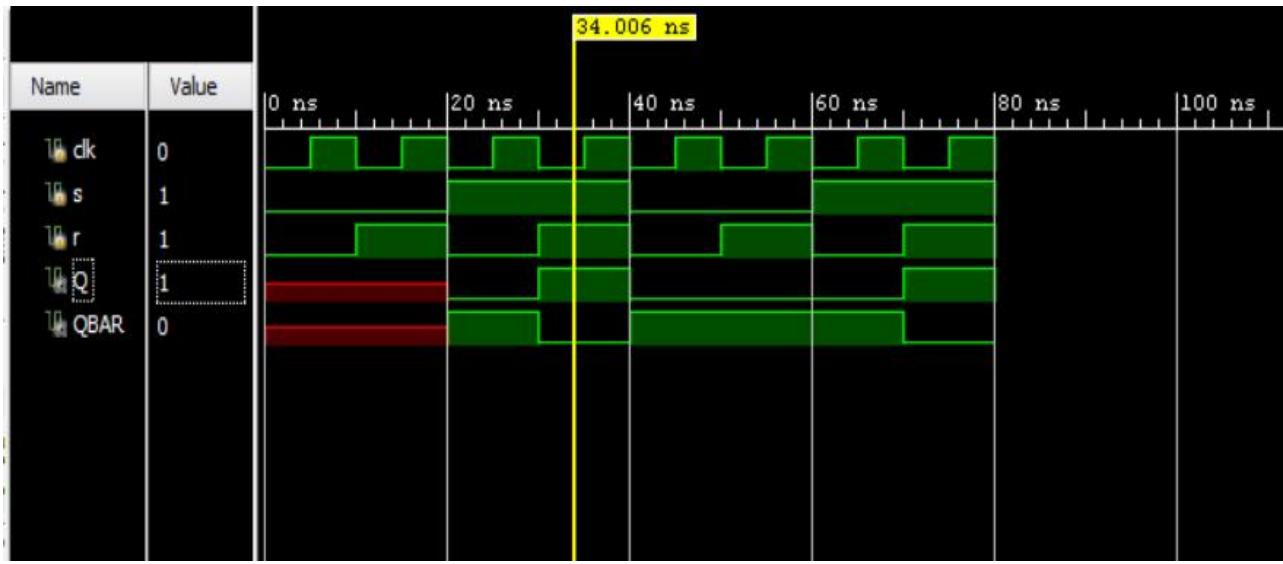
    initial begin
        $display("Time=%0t clk=%b s=%b r=%b Q=%b QBAR=%b", $time, clk, s, r, Q, QBAR);
    end

    initial begin
        clk=1'b0;
        forever #5 clk=~clk;
    end

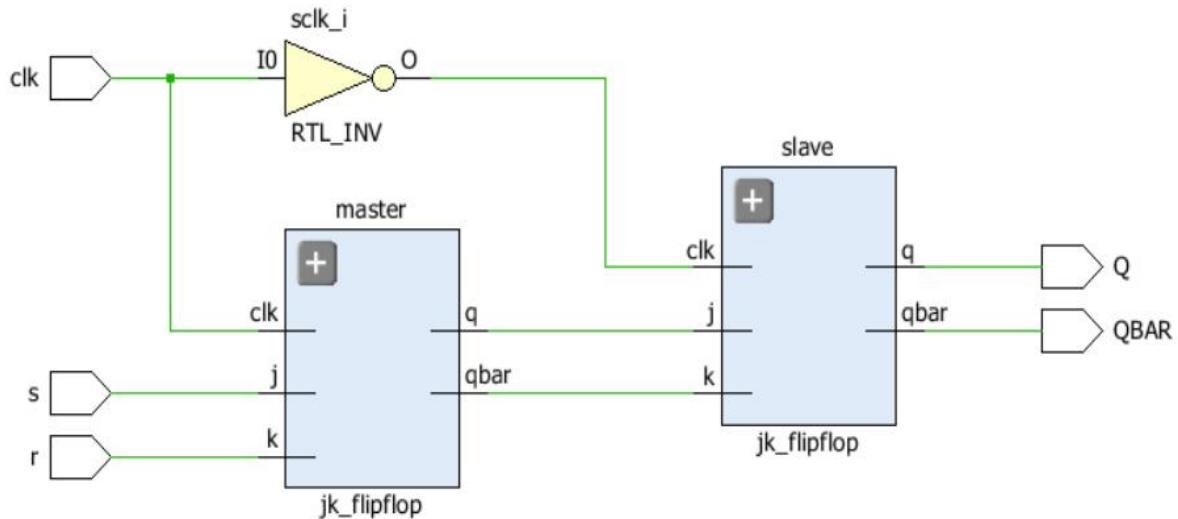
    initial begin
        s=1'b0; r=1'b0;
        #10 s=1'b0; r=1'b1;
        #10 s=1'b1; r=1'b0;
        #10 s=1'b1; r=1'b1;
        #10 s=1'b0; r=1'b0;
        #10 s=1'b0; r=1'b1;
        #10 s=1'b1; r=1'b0;
        #10 s=1'b1; r=1'b1;
        #10 $finish;
    end

endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



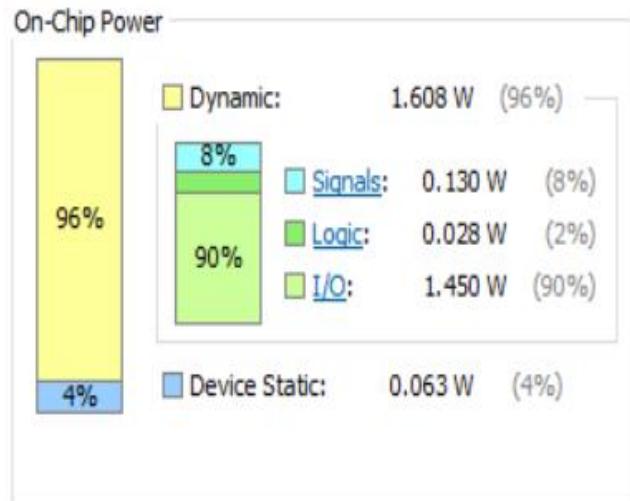
e) SYNTHESIS REPORT : -

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+-----+  
| BlackBox name | Instances |  
+-----+  
+-----+  
  
Report Cell Usage:  
+-----+-----+  
| Cell | Count |  
+-----+-----+  
| 1 | BUFG | 1 |  
| 2 | INV | 1 |  
| 3 | LUT3 | 4 |  
| 4 | FDRE | 4 |  
| 5 | IBUF | 3 |  
| 6 | OBUF | 2 |  
+-----+-----+  
  
Report Instance Areas:  
+-----+-----+-----+  
| Instance | Module | Cells |  
+-----+-----+-----+  
| 1 | top | | 15 |  
| 2 | master | jk_flipflop | 6 |  
| 3 | slave | jk_flipflop_0 | 2 |  
+-----+-----+-----+  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:05 ; elapsed = 00:00:08 . Memory (MB): peak = 409.574 ; gain = 249.809
```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 1.67 W
Junction Temperature: 33.0 °C
Thermal Margin: 67.0 °C (13.9 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



21) POSITIVE EDGE DETECTOR:-

a) VERILOG CODE: -

```
module pos_edge_det (
    input sig,
    input clk,
    output pe
);

reg sig_dly;

always @ (posedge clk) begin
    sig_dly <= sig;
end

assign pe = sig & ~sig_dly;
endmodule
```

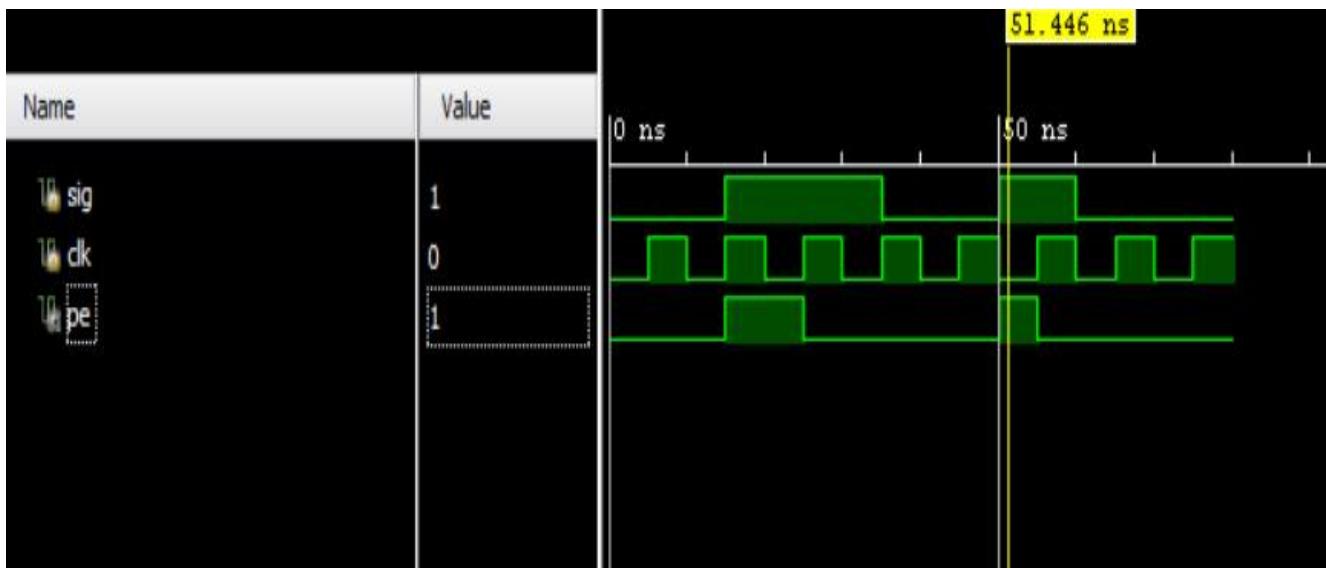
b) TESTBENCH : -

```
module pos_edge_det_tb;
reg sig;
reg clk;
wire pe;
pos_edge_det uut (sig,clk, pe);

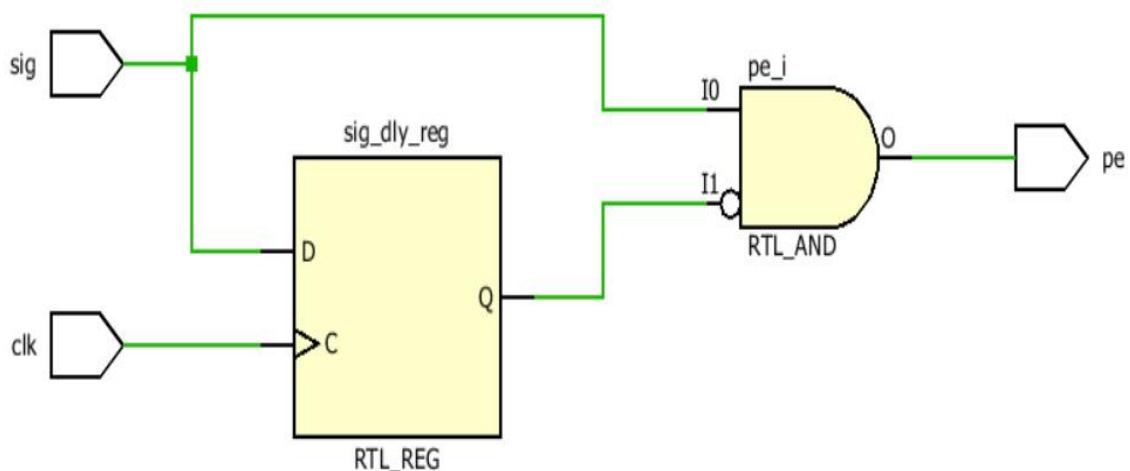
always #5 clk = ~clk;
initial begin
clk <= 0;
sig <= 0;
#15 sig <= 1;
#20 sig <= 0;
#15 sig <= 1;
#10 sig <= 0;
#20 $finish;
end

initial begin
$dumpvars;
$dumpfile("dump.vcd");
end
endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



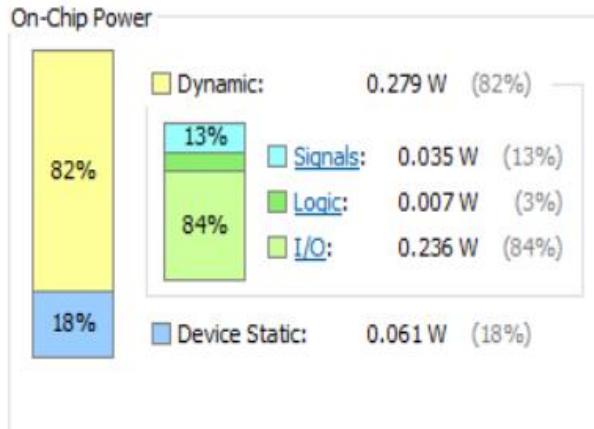
e) SYNTHESIS REPORT : -

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+-----+-----+  
| |BlackBox name |Instances |  
+-----+-----+  
+-----+-----+  
  
Report Cell Usage:  
+-----+-----+  
| |Cell |Count |  
+-----+-----+  
|1 |BUFG | 1|  
|2 |LUT2 | 1|  
|3 |FDRE | 1|  
|4 |IBUF | 2|  
|5 |OBUF | 1|  
+-----+-----+  
  
Report Instance Areas:  
+-----+-----+-----+  
| |Instance |Module |Cells |  
+-----+-----+-----+  
|1 |top | | 6|  
+-----+-----+  
  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:07 . Memory (MB): peak = 410.668 ; gain = 250.883  
-----
```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.34 W
Junction Temperature: 26.6 °C
Thermal Margin: 73.4 °C (15.3 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



22) BCD ADDER:-

a) VERILOG CODE: -

```
module full_adder(
    input a,
    input b,
    input c_in,
    output sum,
    output c_out
);
    assign sum = a ^ b ^ c_in;
    assign c_out = a&b | a&c_in | b&c_in;

endmodule

module _4_bit_adder(
    input [3:0]a,
    input [3:0]b,
    input c_in,
    output [3:0]sum,
    output c_out
);
    wire w1,w2,w3;

    full_adder fa1(a[0],b[0],c_in,sum[0],w1);
    full_adder fa2(a[1],b[1],w1,sum[1],w2);
    full_adder fa3(a[2],b[2],w2,sum[2],w3);
    full_adder fa4(a[3],b[3],w3,sum[3],c_out);

endmodule

module bcd_adder(
    input [3:0]a,
    input [3:0]b,
    input c_in,
    output c_out,
    output [3:0]sum
);
    wire w1,w2,p1,p2,c0;
    wire [3:0]data,z;
```

```

and (p1,z[3],z[2]);
and (p2,z[3],z[1]);
or (c_out,p1,p2,w1);
xor (c0,c_out,c_out);

//assign data ={ 1'b0,c_out,c_out,1'b0};
assign data[0]=c0;
assign data[1]=c_out;
assign data[2]=c_out;
assign data[3]=c0;

_4_bit_adder a1(a,b,c_in,z,w1);
_4_bit_adder a2(data,z,c_in,sum,w2);
endmodule

```

b) TESTBENCH :-

```

module bcd_adder_tb();
reg [3:0]a;
reg [3:0]b;
reg c_in;
wire c_out;
wire [3:0]sum;

bcd_adder uut(a,b,c_in,c_out,sum);

initial begin
#000 a = 4'b0101 ; b = 4'b0110 ; c_in = 0;
#100 a = 4'b0011 ; b = 4'b0001 ; c_in = 0;
#100 a = 4'b0011 ; b = 4'b1001 ; c_in = 0;
#100 a = 4'b0110 ; b = 4'b0111 ; c_in = 0;
#100 a = 4'b1000 ; b = 4'b0001 ; c_in = 0;
#100 a = 4'b0000 ; b = 4'b0000 ; c_in = 0;
#100 a = 4'b0001 ; b = 4'b0001 ; c_in = 0;
#100 a = 4'b0011 ; b = 4'b0011 ; c_in = 0;
#100 a = 4'b0111 ; b = 4'b1001 ; c_in = 0;
#100 a = 4'b0111 ; b = 4'b0111 ; c_in = 0;
#100 $finish;
end

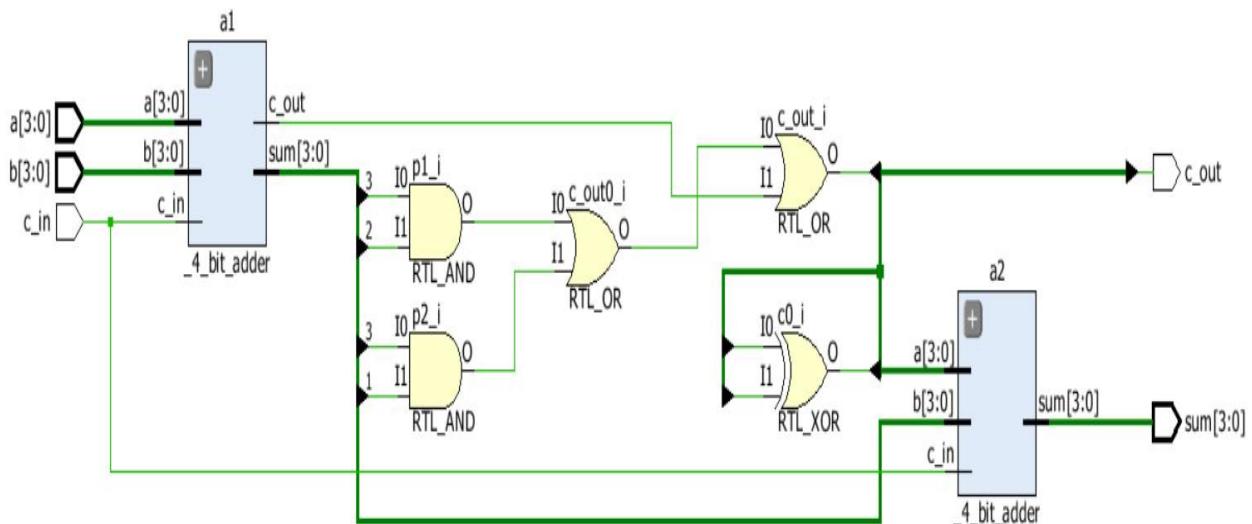
initial begin
$dumpfile("dump.vcd");
$dumpvars(0);
end
endmodule

```

c) EPWAVE :-



d) RTL SCHEMATIC :-



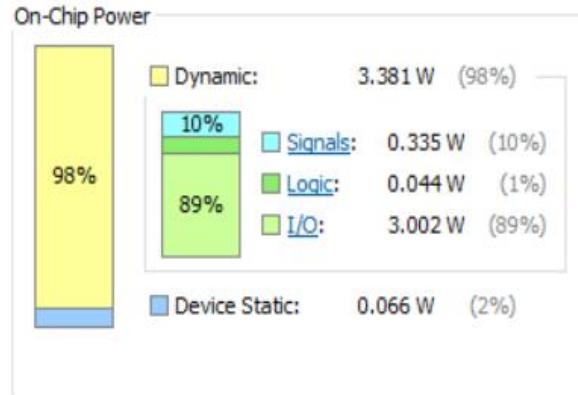
e) SYNTHESIS REPORT :-

```
Start Writing Synthesis Report
-----
Report BlackBoxes:
+---+---+
| |BlackBox name |Instances |
+---+---+
+---+---+
Report Cell Usage:
+---+---+
| |Cell |Count |
+---+---+
|1 |LUT2 | 1|
|2 |LUT3 | 3|
|3 |LUT5 | 2|
|4 |LUT6 | 4|
|5 |IBUF | 9|
|6 |OBUF | 5|
+---+---+
Report Instance Areas:
+---+---+
| |Instance |Module |Cells |
+---+---+
|1 |top |  | 24|
+---+---+
Finished Writing Synthesis Report : Time (s): cpu = 00:00:05 ; elapsed = 00:00:07 . Memory (MB): peak = 421.852 ; gain = 262.324
```

f) POWER REPORT :-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 3.448 W
Junction Temperature: 41.5 °C
Thermal Margin: 58.5 °C (12.2 W)
Effective δ JA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



23) 4-BIT CARRY SELECT ADDER:-

a) VERILOG CODE: -

```
module FA(
    input a,
    input b,
    input c_in,
    input sum,
    input c_out
);

    assign sum = a^b^c_in;
    assign c_out = a&b | b&c_in | a&c_in;
endmodule

module mux_21(
    input x,
    input y,
    input sel,
    output reg out
);

    always @ (*)
    begin
        case(sel)
            1'b0 : out = x;
            1'b1 : out = y;
        endcase
    end

    module _4bit_carry_select_adder(
        input [3:0] a,
        input [3:0] b,
        input c_in,
        output [3:0]sum,
        output c_out
    );
        wire [3:0] s1;
        wire [3:0] s2;
        reg d1=1'b0,d2=1'b1;
```

```
wire c1,c2;

FA f1(a[0],b[0],d1,s1[0],w1);
FA f2(a[1],b[1],w1,s1[1],w2);
FA f3(a[2],b[2],w2,s1[2],w3);
FA f4(a[3],b[3],w3,s1[3],c_out);

FA f5(a[0],b[0],d2,s2[0],w4);
FA f6(a[1],b[1],w4,s2[1],w5);
FA f7(a[2],b[2],w5,s2[2],w6);
FA f8(a[3],b[3],w6,s2[3],c_out);

mux_21 m1(s1[0],s2[0],c_in,sum[0]);
mux_21 m2(s1[1],s2[1],c_in,sum[1]);
mux_21 m3(s1[2],s2[2],c_in,sum[2]);
mux_21 m4(s1[3],s2[3],c_in,sum[3]);

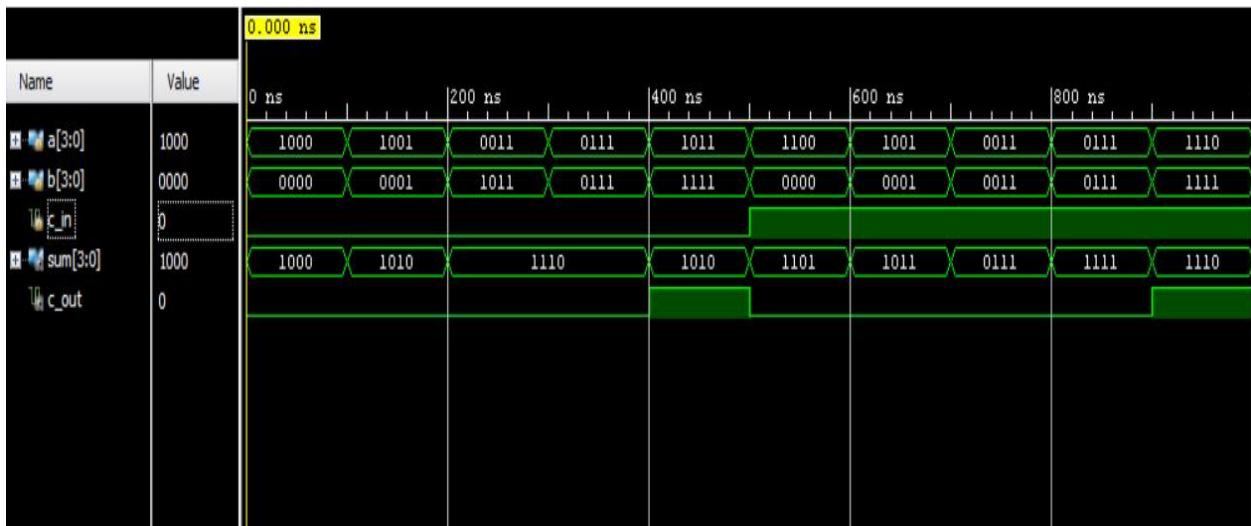
mux_21 m5(c1,c2,c_in,c_out);

endmodule
```

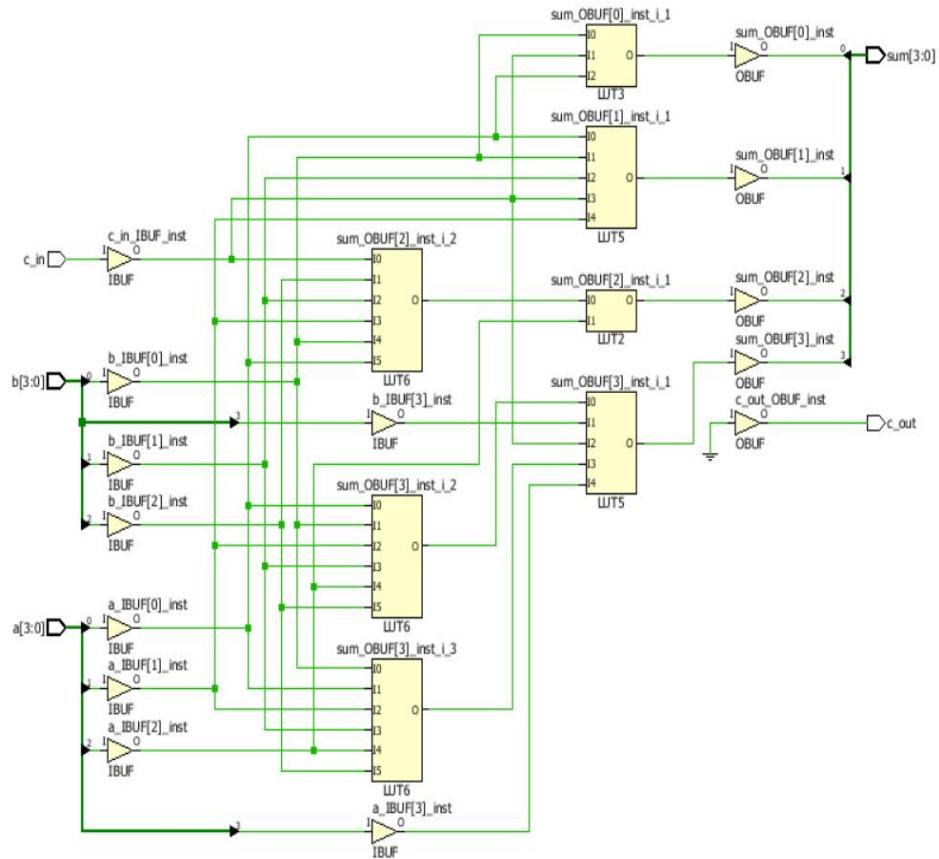
b) TESTBENCH :-

```
module _4bit_carry_select_adder_tb(  
);  
reg [3:0]a;  
reg [3:0]b;  
reg c_in;  
wire [3:0]sum;  
wire c_out;  
  
_4bit_carry_select_adder uut(a,b,c_in,sum,c_out);  
  
initial begin  
  
#000 a = 4'b1000 ; b = 4'b0000 ; c_in = 0;  
#100 a = 4'b1001 ; b = 4'b0001 ; c_in = 0;  
#100 a = 4'b0011 ; b = 4'b1011 ; c_in = 0;  
#100 a = 4'b0111 ; b = 4'b0111 ; c_in = 0;  
#100 a = 4'b1011 ; b = 4'b1111 ; c_in = 0;  
#100 a = 4'b1100 ; b = 4'b0000 ; c_in = 1;  
#100 a = 4'b1001 ; b = 4'b0001 ; c_in = 1;  
#100 a = 4'b0011 ; b = 4'b0011 ; c_in = 1;  
#100 a = 4'b0111 ; b = 4'b0111 ; c_in = 1;  
#100 a = 4'b1110 ; b = 4'b1111 ; c_in = 1;  
#100 $finish;  
  
end  
initial begin  
$dumpfile("dump.vcd");  
$dumpvars(0);  
end  
endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



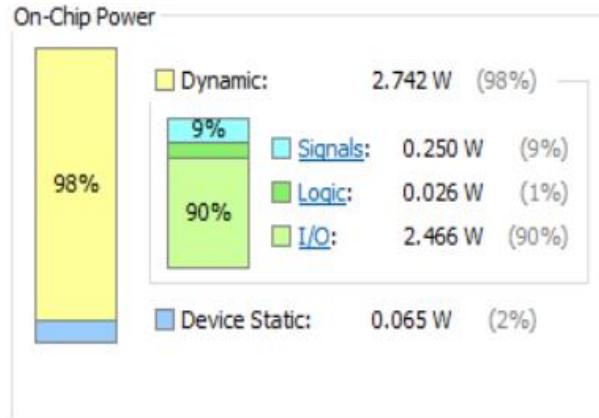
e) SYNTHESIS REPORT : -

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+-----+-----+  
| |BlackBox name |Instances |  
+-----+-----+  
+-----+-----+  
  
Report Cell Usage:  
+-----+-----+  
| |Cell |Count |  
+-----+-----+  
|1 |LUT2 | 1|  
|2 |LUT3 | 1|  
|3 |LUT5 | 2|  
|4 |LUT6 | 3|  
|5 |IBUF | 9|  
|6 |OBUF | 5|  
+-----+-----+  
  
Report Instance Areas:  
+-----+-----+-----+  
| |Instance |Module |Cells |  
+-----+-----+-----+  
|1 |top | | 21|  
+-----+-----+  
  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:07 . Memory (MB): peak = 420.801 ; gain = 261.102  
-----
```

f) POWER REPORT : -

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 2.807 W
Junction Temperature: 38.4 °C
Thermal Margin: 61.6 °C (12.8 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



24) MOORE FSM 1010 SEQUENCE DETECTOR:-

a) VERILOG CODE: -

```
module fsm_moore_1010(
    input clk,
    input rst,
    input in,
    output reg out
);
reg [2:0]state,next_state;
parameter s0 = 3'b001;
parameter s1 = 3'b010;
parameter s2 = 3'b011;
parameter s3 = 3'b100;
parameter s4 = 3'b101;

always @ (state or in)
begin
    case (state)
        s0: if (in == 1'b1)
            begin
                next_state = s1;
                out=1'b0;
            end
        else
            begin
                next_state = s0;
                out=1'b0;
            end
        s1: if (in == 1'b0)
            begin
                next_state = s2;
                out=1'b0;
            end
        else
            begin
                next_state = s1;
                out=1'b0;
            end
        s2: if (in == 1'b1)
            begin
```

```

    next_state = s3;
    out=1'b0;
  end
else
begin
  next_state = s0;
  out=1'b0;
end

s3: if (in == 1'b0)
begin
  next_state = s4;
  out=1'b0;
end
else
begin
  next_state = s1;
  out=1'b0;
end

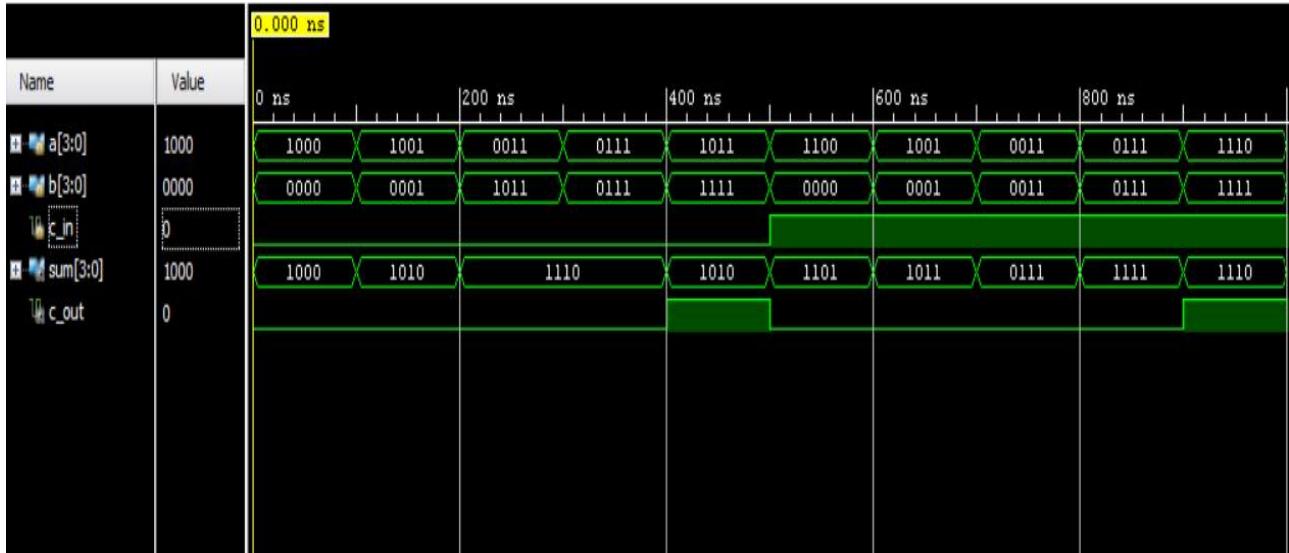
s4: if (in == 1'b0)
begin
  next_state = s0;
  out=1'b1;
end
else
begin
  next_state = s1;
  out=1'b1;
end
default: next_state = s0;
endcase
end

always@(posedge clk)
begin
  if (rst)
    state <= s0;
  else
    state <= next_state;
end
endmodule

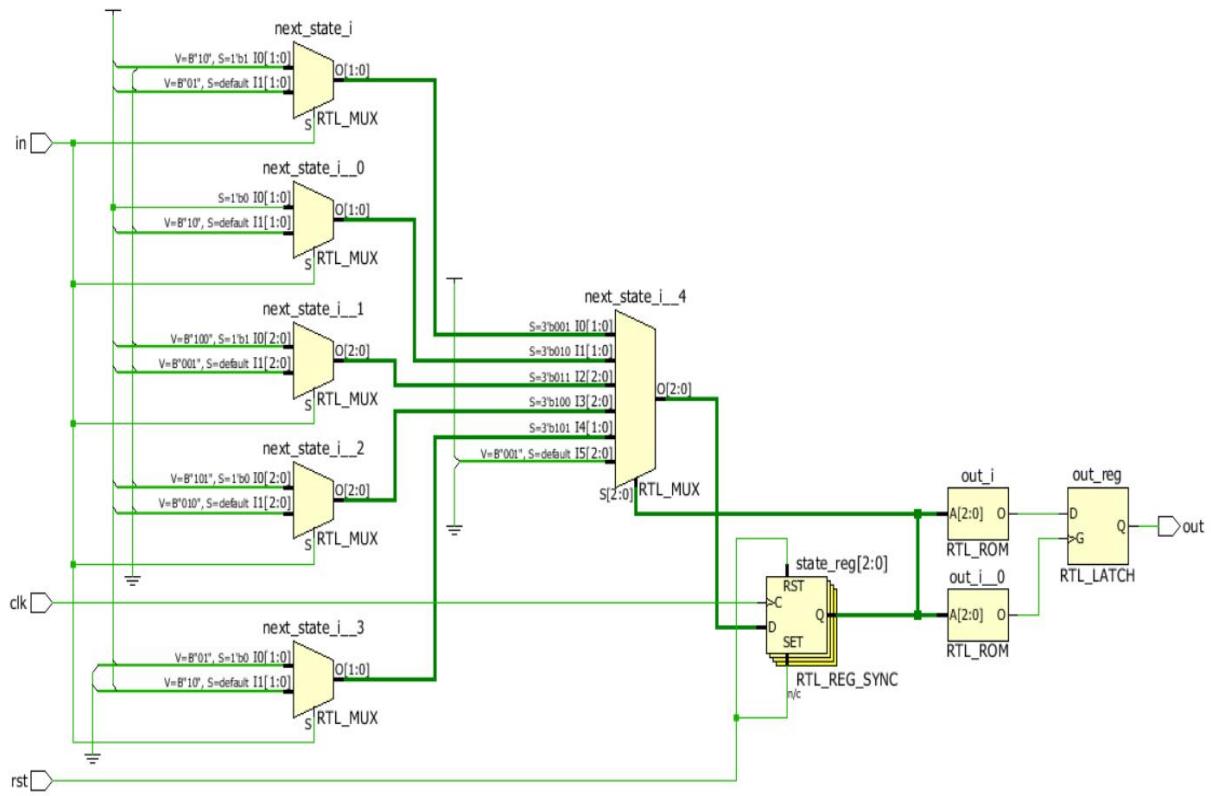
```

b) TESTBENCH :-

c) EPWAVE :-



d) RTL SCHEMATIC :-



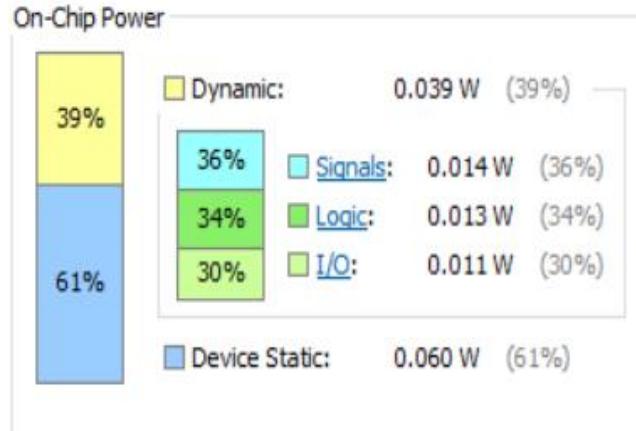
e) SYNTHESIS REPORT :-

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+---+---+  
| |BlackBox name |Instances |  
+---+---+  
+---+---+  
  
Report Cell Usage:  
+---+---+  
| |Cell |Count |  
+---+---+  
|1 |BUFG | 1|  
|2 |LUT3 | 2|  
|3 |LUT5 | 3|  
|4 |FDRE | 3|  
|5 |LD | 1|  
|6 |IBUF | 3|  
|7 |OBUF | 1|  
+---+---+  
  
Report Instance Areas:  
+---+---+---+  
| |Instance |Module |Cells |  
+---+---+---+  
|1 |top | | 14|  
+---+---+---+  
  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:04 ; elapsed = 00:00:09 . Memory (MB): peak = 407.980 ; gain = 248.656  
-----
```

f) POWER REPORT :-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 0.099 W
Junction Temperature: 25.5 °C
Thermal Margin: 74.5 °C (15.5 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



25) N:1 MUX:-

a) VERILOG CODE: -

```
module N_1_Multiplexer(  
    input [15:0] in,  
    input [3:0] sel,  
    output reg  out  
)
```

```
always @(*)  
begin  
case(select)  
    4'b0000: out = in[0];  
    4'b0001: out = in[1];  
    4'b0010: out = in[2];  
    4'b0011: out = in[3];  
    4'b0100: out = in[4];  
    4'b0101: out = in[5];  
    4'b0110: out = in[6];  
    4'b0111: out = in[7];  
    4'b1000: out = in[8];  
    4'b1001: out = in[9];  
    4'b1010: out = in[10];  
    4'b1011: out = in[11];  
    4'b1100: out = in[12];  
    4'b1101: out = in[13];  
    4'b1110: out = in[14];  
    4'b1111: out = in[15];  
    default: out = 16'b0;  
endcase  
end
```

```
endmodule
```

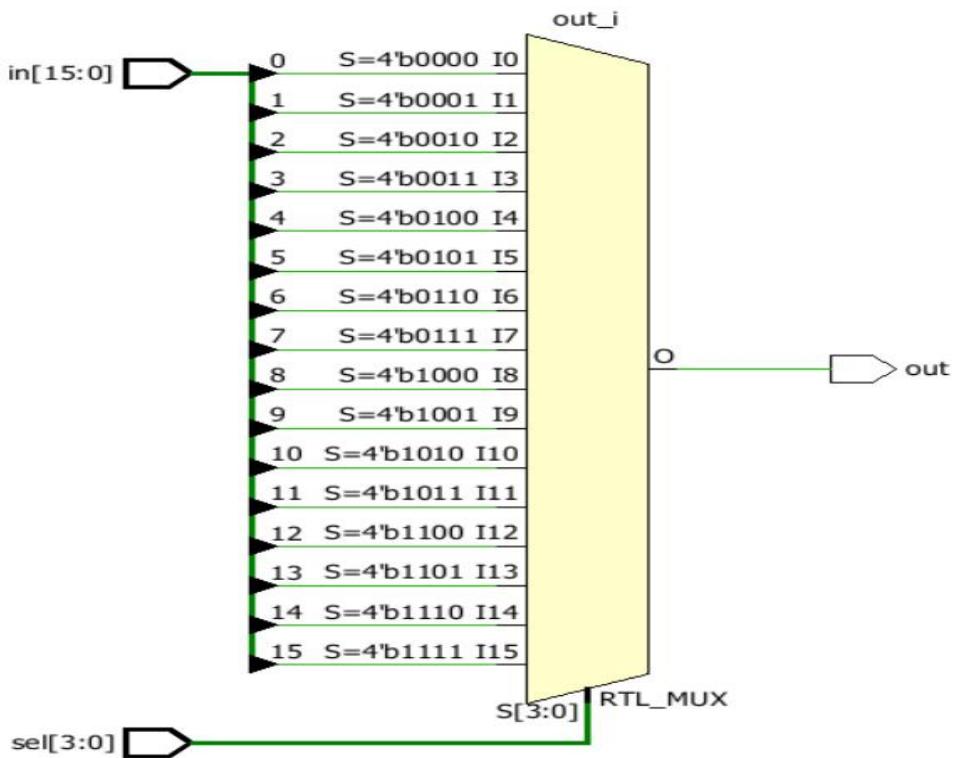
b) TESTBENCH :-

```
module N_1_multiplex_tb(  
);  
  
reg [15:0] in;  
reg [3:0] sel;  
wire out;  
  
N_1_Multiplexer uut (in,sel,out);  
  
reg clock = 0;  
always #5 clock = ~clock;  
  
initial begin  
    $dumpfile("mux_16x1_waveform.vcd");  
    $dumpvars(0, N_1_multiplex_tb);  
  
    in = 16'b1010101010101010;  
    sel = 4'b0000;  
  
    #10;  
    in = 16'b1100110011001100;  
    sel = 4'b0111;  
  
    #10;  
    in = 16'b1111000011110000;  
    sel = 4'b1111;  
    #10;  
  
    $finish;  
end  
  
endmodule
```

c) EPWAVE :-



d) RTL SCHEMATIC :-



e) SYNTHESIS REPORT :-

```
Start Writing Synthesis Report

Report BlackBoxes:
+---+-----+
| |BlackBox name |Instances |
+---+-----+
+---+-----+
+---+-----+

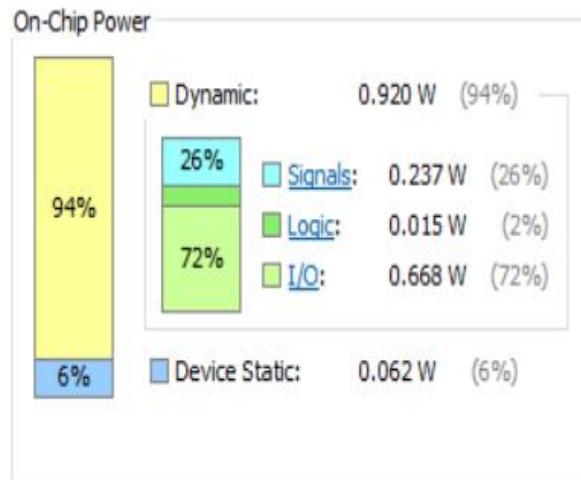
Report Cell Usage:
+-----+-----+
|     |Cell   |Count  |
+-----+-----+
|1    |LUT6   |      4|
|2    |MUXF7  |      2|
|3    |MUXF8  |      1|
|4    |IBUF   |     20|
|5    |OBUF   |      1|
+-----+-----+

Report Instance Areas:
+-----+-----+-----+
|     |Instance |Module |Cells  |
+-----+-----+-----+
|1    |top     |       |  28|
+-----+-----+-----+
Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:07 . Memory (MB): peak = 413.047 ; gain = 253.766
```

f) POWER REPORT :-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.982 W
Junction Temperature: 29.7 °C
Thermal Margin: 70.3 °C (14.6 W)
Effective ΔJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low



END

