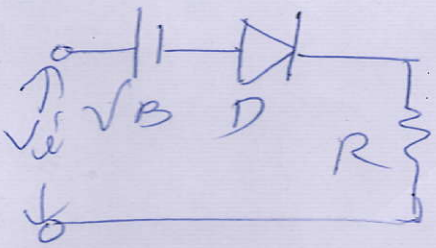
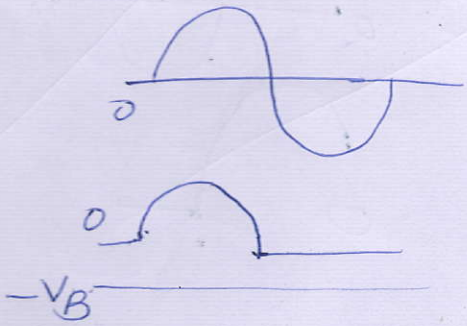
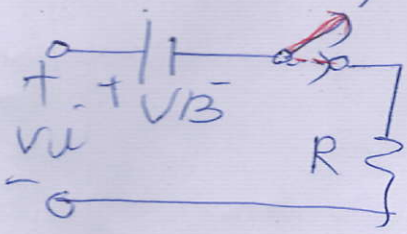
LECTURE 14/10/2020

(17) BIASED SERIES NEGATIVE CLIPPER

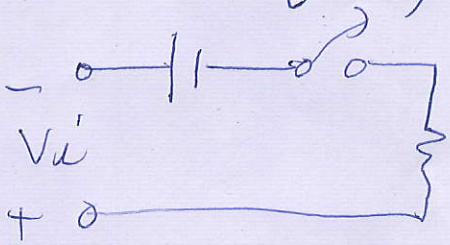




+ve half cycle



-ve half cycle



(a) $|V_i| \leq |V_B|$

D is reverse biased

$V_O = 0$

(b) $|V_i| > |V_B|$

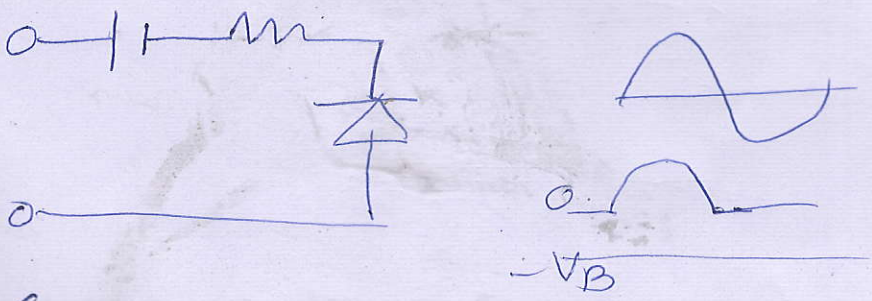
D is forward biased

$V_O = V_i - V_B$

D is reverse biased for entire cycle

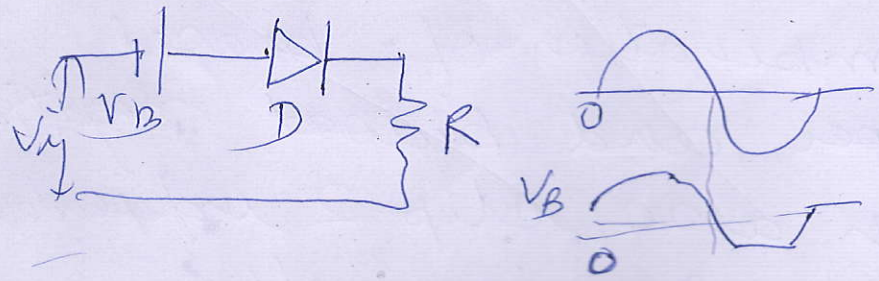
$\therefore V_O = 0$.

(18) BIASED SHUNT NEGATIVE CLIPPER

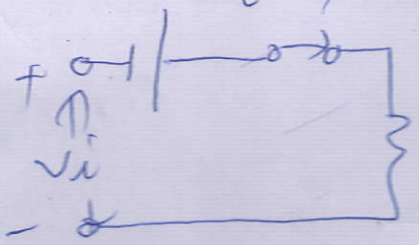


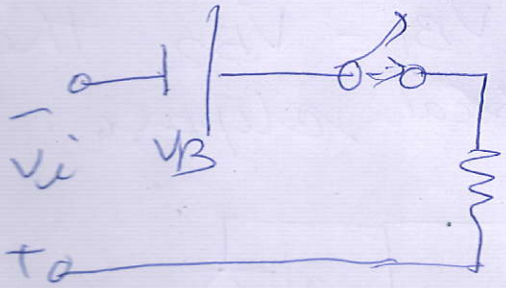
(The analysis same as circuit no.17, biasing of diodes change).

(19) BIASED SERIES NEGATIVE CLIPPER



+ve half cycle





D is forward biased for entire half cycle

$V_O = V_i + V_B$

(a) Till $V_i \leq V_B$

D is forward biased

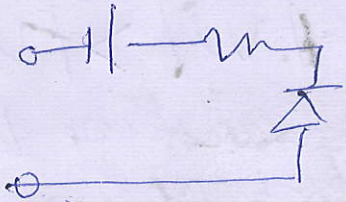
$V_O = -(V_i - V_B)$

(b) $V_i > V_B$

D is reverse biased

$V_O = 0$

(20) BIASED SHUNT NEGATIVE CLIPPER

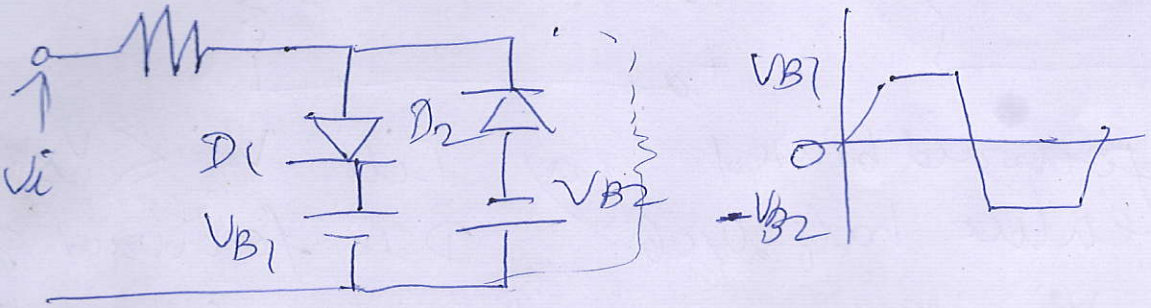


(Output waveform same as circuit 19, biasing of diodes reversed)

(21) COMBINATION CLIPPER

It is a combination of biased positive clipper and biased negative clipper. It can also clip 2 independent levels depending on bias voltages.

If $V_{B1} = V_{B2}$ the circuit is called symmetrical clipper.



+ve half cycle

(a) $V_i < V_{B1}$

D_1 & D_2 reverse biased

$V_o = V_i$

(b) $V_i > V_{B1}$

D_1 is forward biased & D_2 is reverse biased

$V_o = V_{B1}$

-ve half cycle

(a) $|V_i| \leq |V_{B2}|$

D_1 & D_2 reverse biased

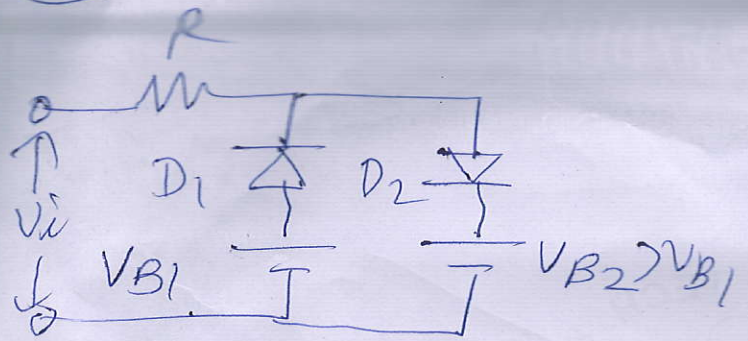
$V_o = V_i$

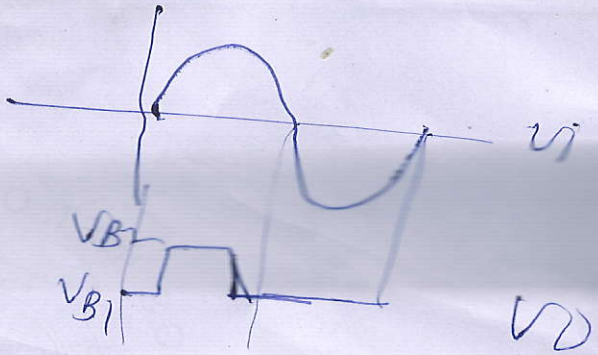
(b) $|V_i| > |V_{B2}|$

D_1 reverse biased & D_2 forward biased

$V_o = -V_{B2}$

(22) TWO LEVEL SLICER





Input V_i	Output V_O	Diode states
$V_i \leq V_{B1}$	$V_O = V_{B1}$	D_1 F. Biased D_2 Reverse biased
$V_{B1} < V_i < V_{B2}$	$V_O = V_i$	D_1 Reverse biased D_2 Reverse biased
$V_i \geq V_{B2}$	$V_O = V_{B2}$	D_1 Reverse biased D_2 forward biased

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CLAMPERS (Circuits using diodes)

The circuit with which the waveform can be shifted in such a way that a particular part of it say +ve or -ve peak is maintained at a specified voltage level is called a clamping circuit or simply clamper.

A clamping circuit introduces or restores a d.c. level to an a.c. signal, it is called as d.c. restorer. (5)

It is used in T.V. receivers to restore the d.c. reference to the video signals. The d.c. reference level corresponding to the brightness level of the picture is not transmitted with video signal.

It is also called as shunt rectifier as it provides unidirectional output.

Essential components of clamper are (1) Capacitor (2) Diode (3) Resistor

Optional component is d.c. supply to introduce additional shift.

Note: The magnitude of R & C must be chosen such that $T = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is not conducting

Assumptions

(1) First consider the condition under which the diode becomes foward biased

(2) The voltage swing of the input and output waveforms is the same

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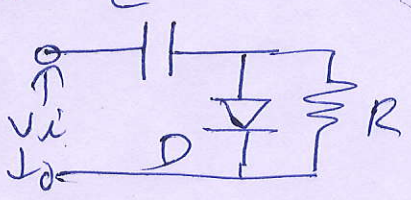
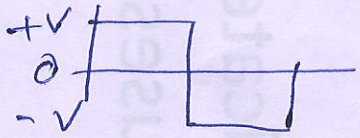
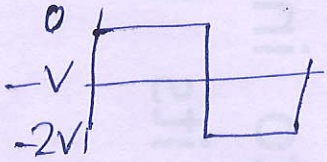
(1) NEGATIVE CLAMPER.

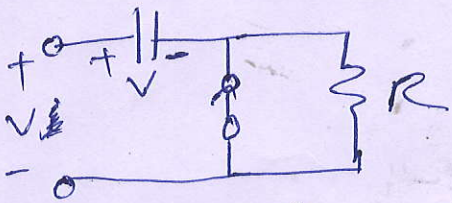






As the diode is foward biased in positive half cycle, consider positive half cycle first.

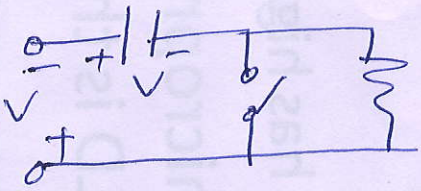
+ve half cycle



Diode is foward biased

$\therefore V_O = D$

-ve half cycle.



Diode is reverse biased

$V_O = -(V+V) = -2V$

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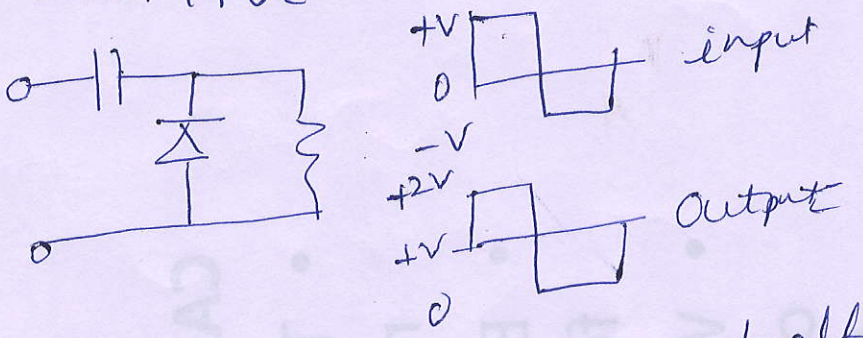
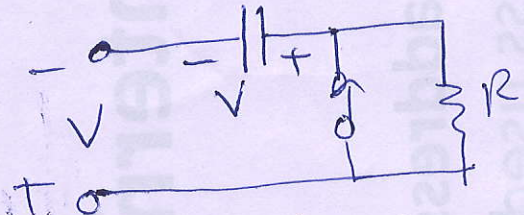
(2) ~~POSITIVE CLAMPER~~

(2) POSITIVE CLAMPER



Here consider -ve half cycle first as the diode is forward biased in -ve half cycle

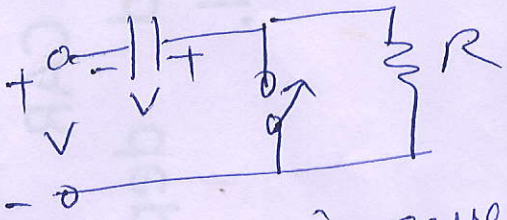
-ve half cycle



Diode is forward biased

$V_0 = 0$

+ve half cycle



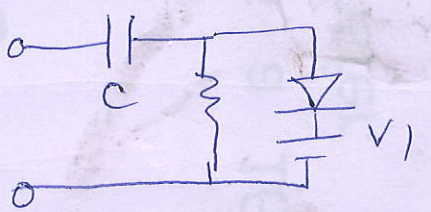
Diode is reverse biased

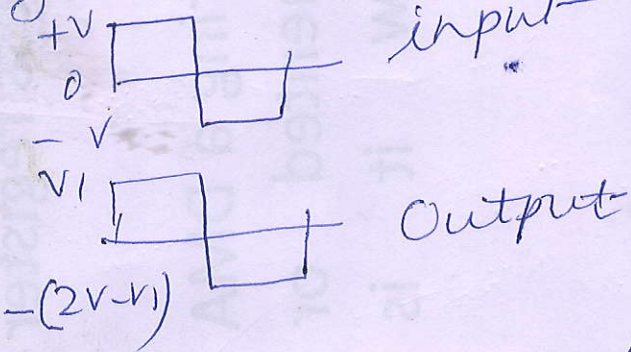
$V_0 = +(V+V) = 2V$

BIASED CLAMPERS

A biased clamper means that the ~~clamp~~ clamping can be done at any voltage level other than zero.

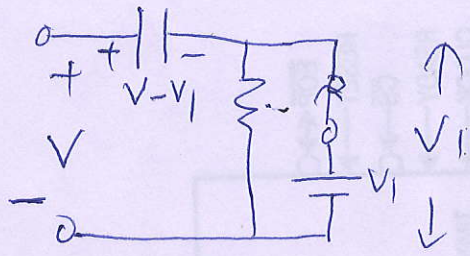
(3)





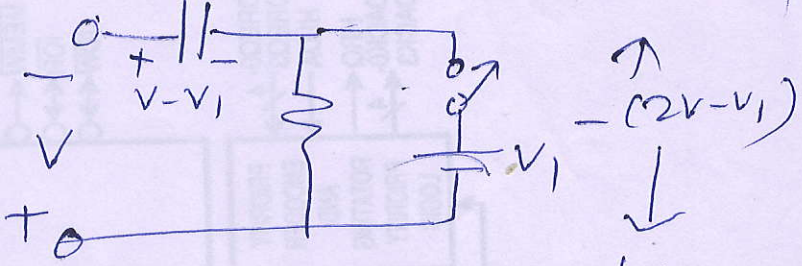
Here consider +ve half cycle first as the Diode is forward biased in positive half cycle.

+ve half cycle



D is forward biased and
$V_0 = V_1$

-ve half cycle



D is reverse biased

$V_0 = -(V+V-V_1)$

$= -(2V-V_1)$

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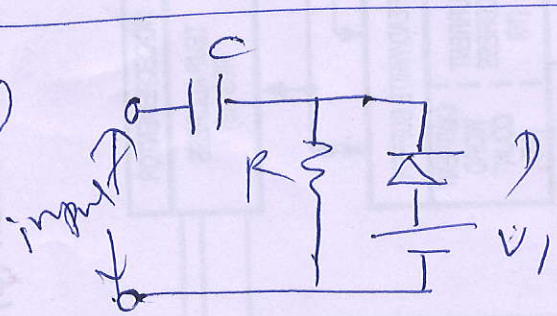
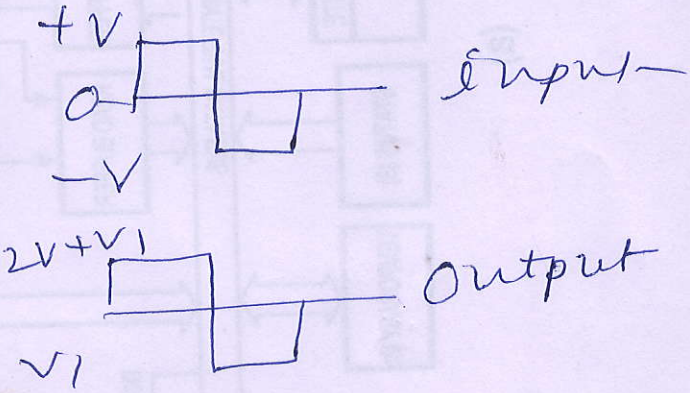
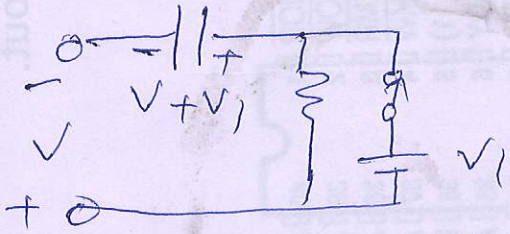
(4)





First consider -ve half cycle as diode is forward biased in -ve half cycle.

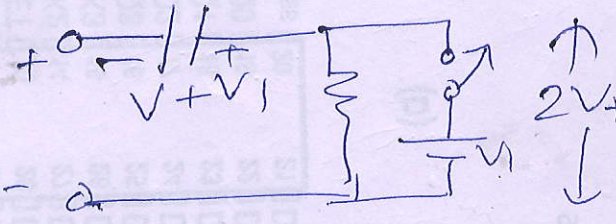
-ve half cycle



D is forward biased

$V_0 = V_1$

+ve half cycle

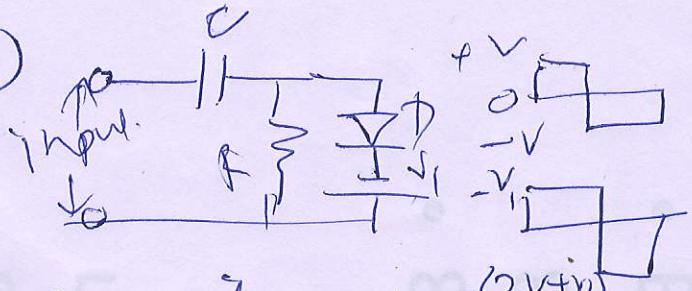


D is reverse biased

$V_0 = V+V+V_1$

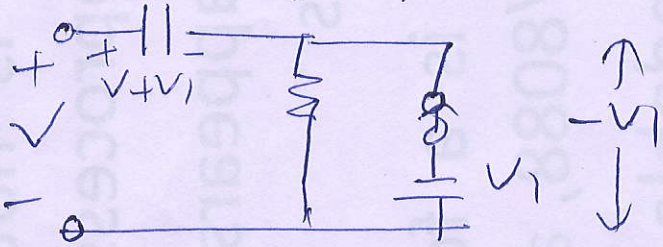
$= 2V+V_1$

(5)



Consider +ve half cycle first

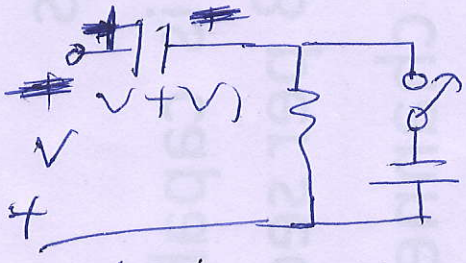
+ve half cycle



D is forward biased

$V_0 = -V_1$

-ve half cycle

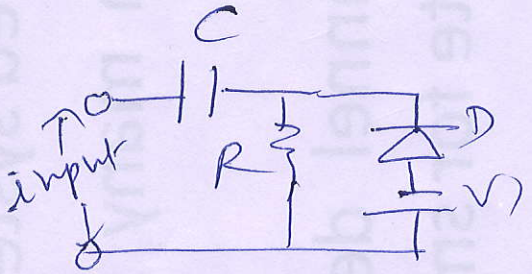


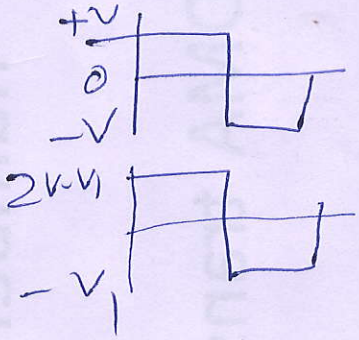
D is reverse biased

$V_0 = -(V+V+V_1)$

$= -(2V+V_1)$

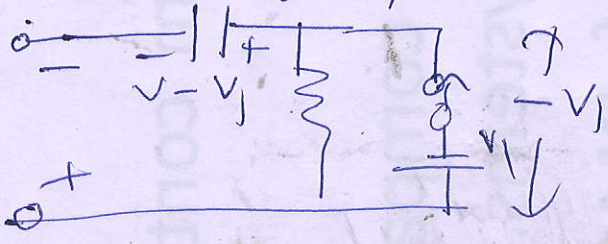
(6)





Consider -ve half cycle first

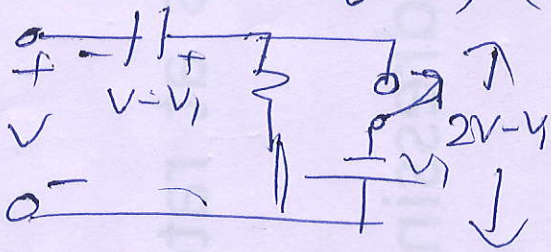
-ve half cycle



D is forward biased

$V_0 = -V_1$

+ve half cycle



D is reverse biased

$V_0 = V+V-V_1$

$= 2V-V_1$