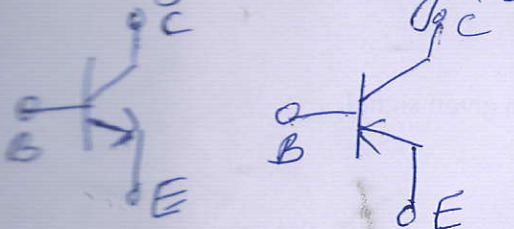
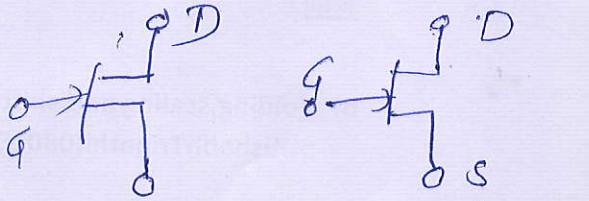
MODULE IV

Field Effect transistor (FET) is an another semiconductor device like BJT which can be used as an amplifier or switch. FET is also 3 terminal device but its principle of operation is completely different from BJT.

COMPARISON BETWEEN FET AND BJT

	FET	BJT
1.	Unipolar device i.e. current carried by either holes or electrons	Bipolar device i.e. current carried by both electrons & holes
2.	Voltage controlled device i.e voltage at the Gate or Drain terminal controls the amount of current flowing through it	Current controlled device i.e. current I_B controls I_C
3.	 Symbols	 Symbols
4.	Input resistance is very high i.e. several mega ohms	Input resistance is very low i.e. few kΩ.
5.	Negative temp. coefficient at high current levels i.e. current decreases as temperature increases	Positive temp. coefficient at high current levels i.e. current increases as temp. increases

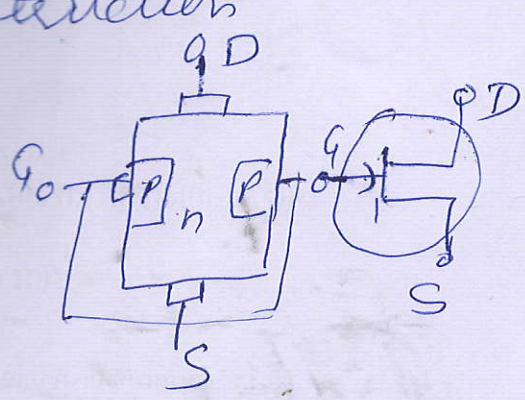
FET	BJT
This characteristic prevents FET from break down.	This characteristic leads BJT to thermal breakdown.
(E) It does not suffer from minority carrier storage effects and therefore has higher switching speeds & cut-off frequencies	It suffers from minority carrier storage effects and therefore has lower switching speed and cut-off freqs than FETs
(F) Less noisy therefore used as input amplifier for low level signals	More noisy
(G) Simple to fabricate as an integrated circuit and occupies less space	Comparatively difficult to fabricate as an IC & occupies more space on IC chip
(H) Low gain-bandwidth product	High Gain Bandwidth product.
(I) High power gain	Less than FET

FET

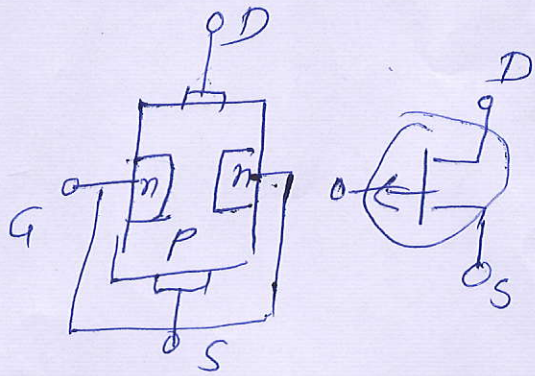
- JFET (Junction Field Effect)
  - p-channel
  - n-channel
- MOSFET (Metal Oxide Semiconductor FET) or IGFET (Insulated gate FET)
  - DEMOSFET
    - DEPLETION
      - p-channel
      - n-channel
    - ENHANCEMENT
      - p-channel
      - n-channel
  - ENHANCEMENT ONLY
    - p-channel
    - n-channel

JUNCTION FIELD EFFECT TRANSISTOR (JFET)

Construction



N channel JFET



P-channel JFET

N channel JFET (construction)

It consists of an N type semiconductor bar with 2 P type heavily doped regions diffused on opposite sides of its middle portion. The P type regions form 2 P-N junctions. The space

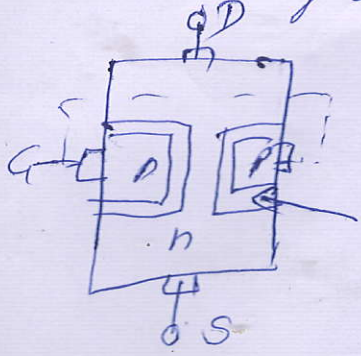
between the junctions i.e. N region is called channel. Both the p regions are connected internally and a single wire is taken out in the form of terminal called Gate (G). The electrical connections (ohmic contacts) are made to both ends of the N type semiconductor and are taken out in the form of 2 terminals called drain (D) and source (S). Source is the terminal through which electrons enter the semiconductor bar and Drain is the terminal through which electrons leave the semiconductor bar.

Electrons are charge carriers in n channel JFET.

In p channel JFET holes are the charge carriers.

Unbiased JFET

In the absence of any applied voltage, JFET has gate channel junctions under no bias conditions. The result is depletion region. which has no carriers and hence no conduction



Operation of N channel JFET

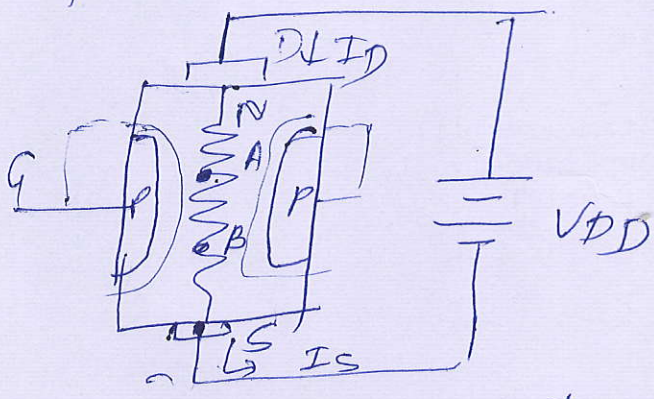


Fig (a) V_{DD} connected & ~~V_{GS}~~ Gate open

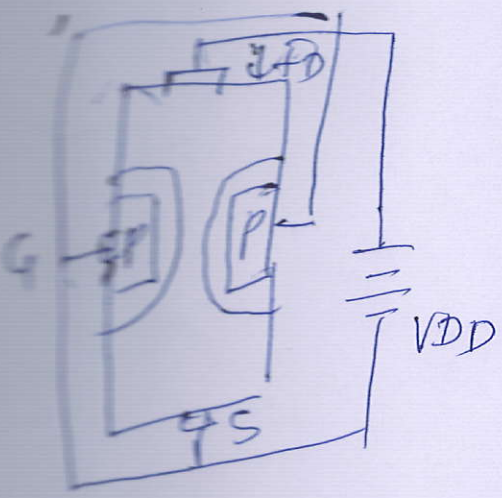
(a) The voltage V_{DD} is dropped across the N channel resistance (R_{DS}) giving rise to drain current $I_D = \frac{V_{DD}}{R_{DS}}$, Due to this current flow there will be a uniform voltage drop while going from drain to source.

Consider two points A and B in N channel. Let V_A and V_B be potential drops at these points. $V_A > V_B$ therefore due to the progressive voltage drop along the length of the channel, the reverse biasing effect on P-N junction is stronger near drain than near source. Due to this reason, the penetration of depletion region at A is more than at B. This explains why the depletion regions extends more near drain than source when both V_{DD} and V_{GG} are applied

(b) $V_{GS} = 0$, V_{DD} applied.

Let no potential be applied between Gate and source ($V_{GS} = 0$) and a potential V_D

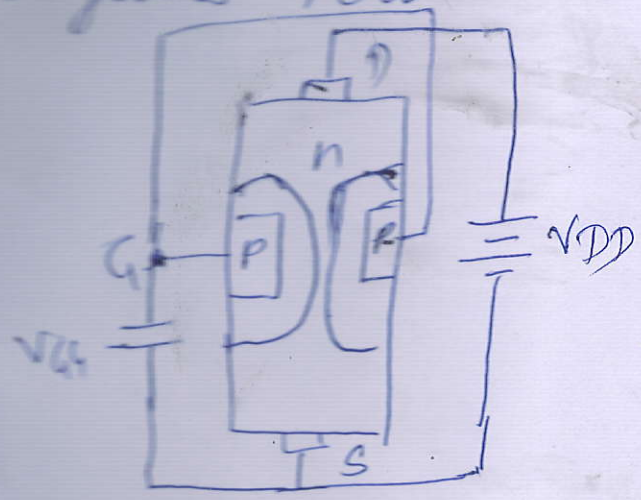
applied between D and S. Current I_D (0)
flows from drain to S which is maximum
because the channel is widest.



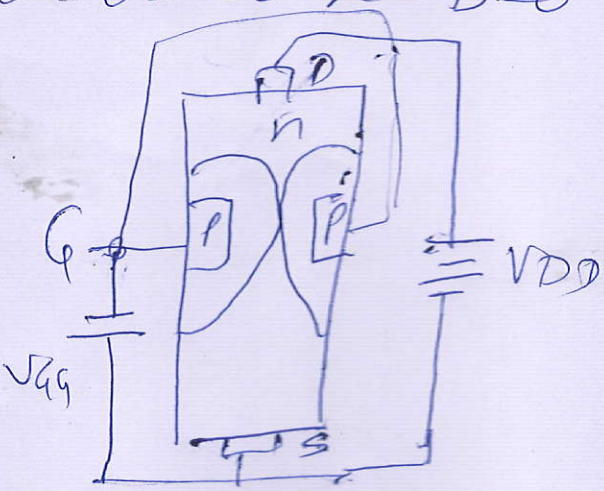
(b)

cc) $V_{GG} > 0$, V_{DD} applied

Let the G be reverse biased by applying a voltage V_{GG} between G and S. The G bias increases the depletion regions and thereby decreases the cross-section of N channel., I_D decreases (d) when V_{GG} is increased further, a stage is reached when two depletion regions touch each other & $I_D = 0$



(c)

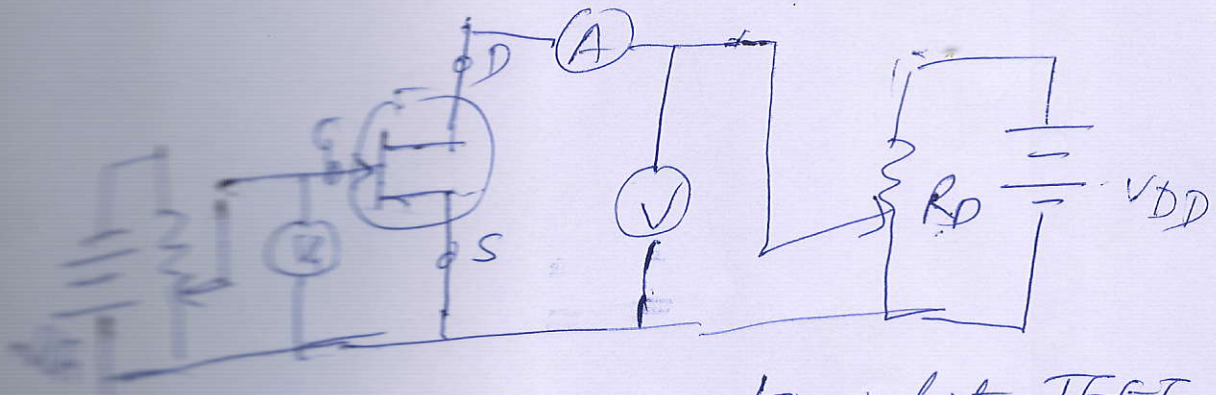


(d)

V-I CHARACTERISTICS OF JFET

(1) DRAIN CHARACTERISTIC

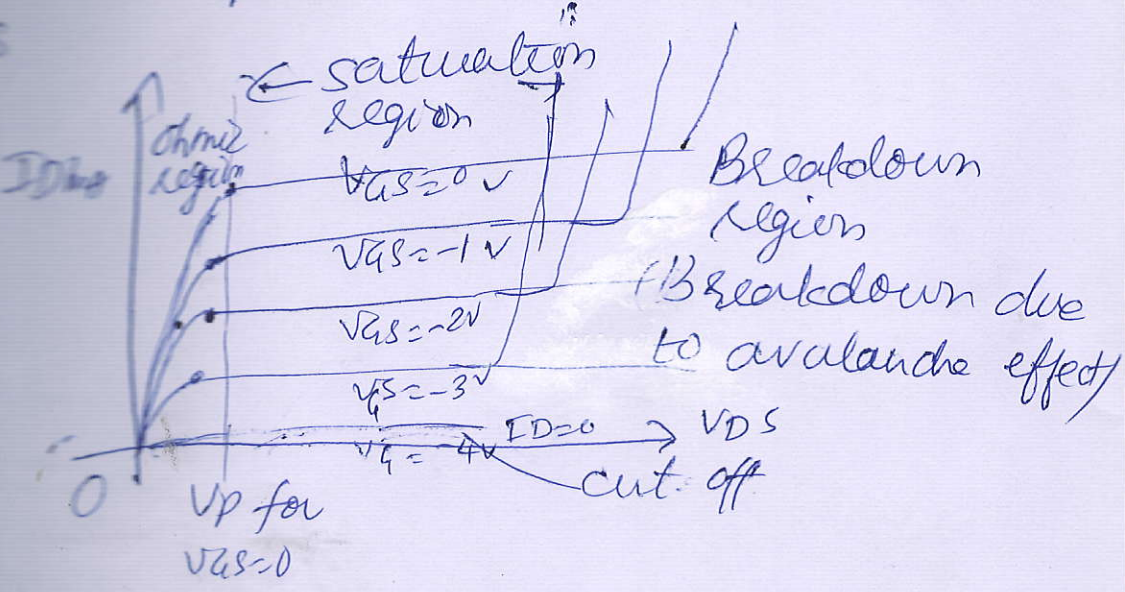
(2) TRANSFER CHARACTERISTIC



Experimental set up to plot JFET characteristics.

(a) DRAIN V-I CHARACTERISTIC FOR N CHANNEL JFET

I_D Between and V_{DS} for different V_{GS}



(i) V_{GS} and V_{DS} both = 0

When $V_{GS}=0$, the channel is entirely open. But $V_{DS}=0$, there is no attraction force for majority carriers and hence I_D does not exist.

(ii) When $V_{GS}=0$

At $V_{GS}=0$, in response to a small

voltage is reached at lower I_D than when $V_{GS} = 0$.

If V_{GS} is increased in steps -2, -3 ... etc, the pinch off voltage is reached at lesser values of I_D.

(iv) Breakdown region:

If V_{DS} is increased beyond pinch-off voltage V_p, the I_D remains constant upto a certain value of V_{DS}. If V_{DS} is increased further, a voltage will be reached at which gate channel junction breaks down due to avalanche effect. At this point I_D increases very rapidly and the device may be destroyed

(v) Ohmic region - Here I_D varies with V_{DS}. JFET behaves as voltage variable resistance.

(vi) saturation region - I_D remains fairly constant and does not vary with V_{DS}. FET as an amplifier operates in saturation region

(vii) cut-off: More negative V_{GS} causes I_D to reduce and pinch-off voltage reaches at lower I_D. When V_{GS} is made sufficiently negative I_D is reduced to zero. Depletion region completely closes the channel. This value of V_{GS} is designated as $V_{GS(off)}$

applied voltage V_{DS}, n type bar acts as a simple semiconductor resistor and current I_D increases linearly with V_{DS}. As V_{DS} increases the voltage drop along the channel also increases. This increase in voltage drop increases the reverse bias on G-S junction and causes the depletion regions to penetrate into the channel reducing channel width. The effect of reduction in channel width provides more opposition to increase in I_D. Thus rate of increase in I_D (w.r.t. V_{DS} is now reduced (curved shape)

At some value of V_{DS}, I_D cannot be increased further, due to reduction in channel width. I_D approaches a constant saturation value (I_{DSS}) The voltage at which the current I_D reaches its constant saturation level is called 'pinch-off voltage' V_P.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Schelkay's equation.

when $V_{GS} = 0$, $I_D = I_{DSS}$

(iii) V_{GS} with negative bias

When $V_{GS} = -1V$, gate channel junctions are further reverse biased, reducing the effective width of the channel available for the conduction. Because of this I_D reduces and pinch-off

NOTE: Do not confuse cut-off and pinch-off.

(i) Pinch off voltage V_p is the value of V_{DS} at which I_D reaches a constant value for given value of V_{GS}.

(ii) Cut-off voltage $V_{GS(off)}$ is the value of V_{GS} at which $I_D = 0$.

I_D becomes 0 only when $V_{GS} \geq V_p$

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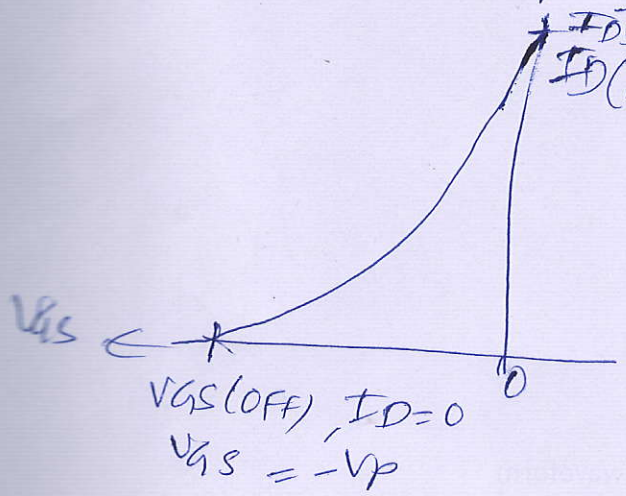
(2) TRANSFER CHARACTERISTICS OF n-channel JFET. (Between I_D & V_{GS})



(i) The relationship between I_D & V_{GS} is non-linear and is given by Schokley's equation $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

(ii) $I_D = 0$ when $V_{GS} = V_{GS(off)}$

$I_D = I_{DSS}$ when $V_{GS} = 0$.