

JFET PARAMETERS

The main parameters of a JFET when connected in common source configuration

(1) D.C. drain resistance: This is the static or ohmic resistance of the channel. It is given by

$$R_{DS} = \left[\frac{V_{DS}}{I_D} \right]$$

(2) A.c. drain resistance:

$$r_d = \left[\frac{\Delta V_{DS}}{\Delta I_D} \right] / V_{GS} \text{ held constant}$$

It is the a.c. resistance between D and S terminal when JFET is operated in the pinch-off or saturation region.

(3) Transconductance (g_m)

g_m is also called forward transconductance / forward transmittance.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} / \text{constant } V_{DS}$$

= siemens/mhos

(4) Amplification factor (μ)

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} / \text{constant } I_D$$

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

= $r_d \times g_m$

(5) Input resistance (R_i)

G-S junction is reverse biased. As G-S junction is used as input therefore the input resistance of a JFET is very high. $R_i = \frac{V_{AS}}{I_{GSS}}$ (I_{GSS} = Gate reverse current in mA)

(6) Power ~~gain~~ dissipation: (P_D)

$$P_D = I_D \times V_{DS}$$

JFET APPLICATIONS:

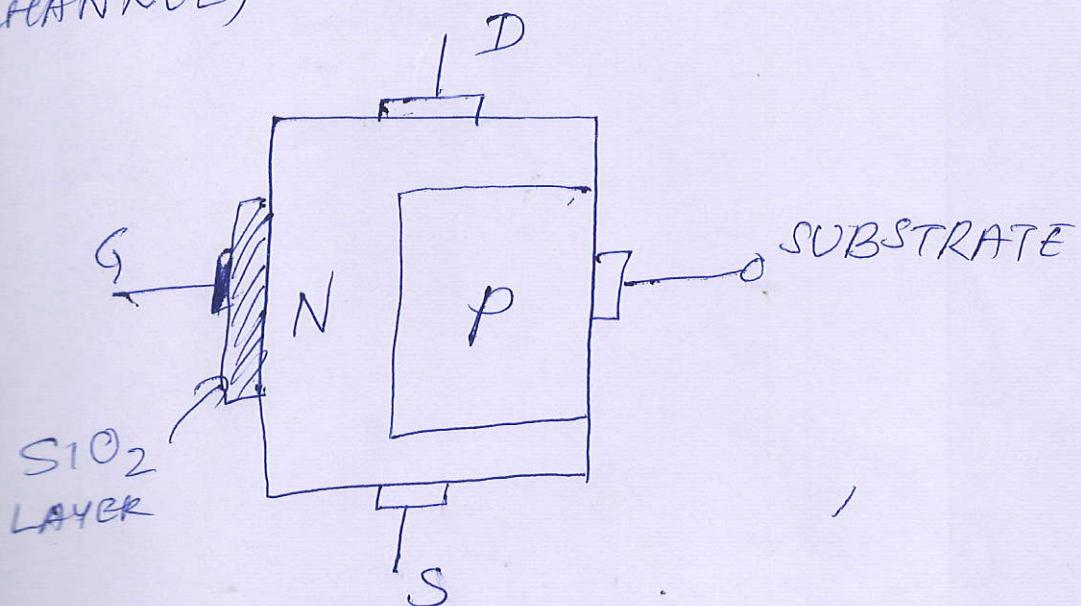
- (1) Used in switch, digital and linear amplifier applications.
- (2) Since JFET has high input impedance and low output impedance they are used as buffer in measuring instruments.
- (3) Because of low noise, they are used in RF amplifiers in FM tuners and in communication equipments.
- (4) Used in mixer circuits in FM and TV receivers because it reduces intermodulation distortion.
- (5) They are used in low freq. amplifiers.

MOSFETS

G of MOSFET is insulated from the channel therefore it is also called as Insulated Gate field effect transistor.

- (1) Depletion & enhancement MOSFET
- (2) Enhancement only MOSFET

- (1) DEPLETION- ENHANCEMENT MOSFET
(N CHANNEL)



construction:

It consists of a conducting bar of N type material with an insulated gate on the left and P region on the right. Free electrons can flow from S to D through N type material. The P region is called the substrate or body.

(that is why it has 4th terminal substrate) It physically reduces the conducting path to a narrow channel. A thin layer of SiO₂ is deposited on the left side of the channel.

This layer insulates the gate from the channel. Because of this negligible current flows even when the gate voltage is zero. In MOSFET there is no p junction.

Note: The basic construction of a DE MOSFET type p channel MOSFET is similar to that of N channel except that the conducting bar is of P type material and the substrate is of N type material.

WORKING OF DE MOSFET

It can be operated in 2 different modes. Visualize the entire structure of MOSFET as a parallel plate capacitor. One of the plates is formed by the G and the other by the semiconductor channel. The plates are separated by a dielectric (SiO_2 layer). If one plate of capacitor is made negative it induces a positive charge on the opposite plate and vice versa. This principle is used in DE MOSFET (by Depletion mode).

G is maintained at negative potential while the D is maintained at positive potential.

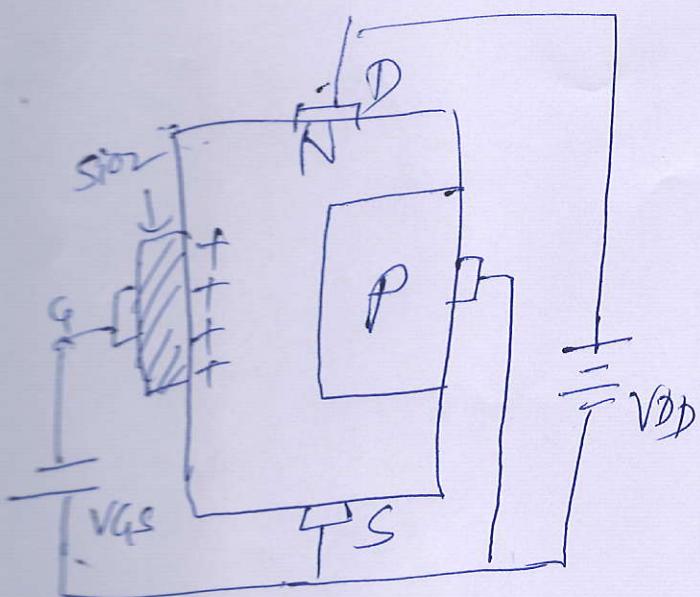
When $V_{DS}=0$ i.e. G, S and substrate terminals are connected to ground, a

significant current flows for a given V_{DS} . As depletion MOSFET can conduct even if the V_{GS} is zero it is called NORMALLY ON MOSFET. The reason is that due to the +ve voltage applied to the drain, the free electrons from the channel are attracted.

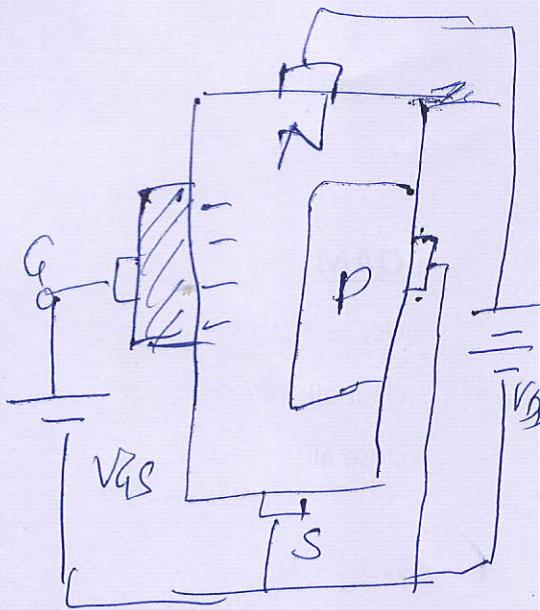
Let a negative potential is applied at the G. Positive charges are induced in the N channel. The G will repel the free electrons towards P type substrate and attract the holes from the substrate. The holes & electrons will now combine. This serves to deplete the channel of majority carriers (electrons) so the conductivity decreases. Greater is the negative voltage on the G, greater is the reduction in number of electrons in the channel and consequently lesser is its conductivity.

As the value of negative V_{GS} is increased (at $V_{GS} = 0$), the channel is totally depleted of free electrons and I_D reduces to zero.

As the negative G voltage depletes the channel of free electrons, this mode is called depletion mode.



(a) DEPLETION MODE



(b) ENHANCEMENT MODE

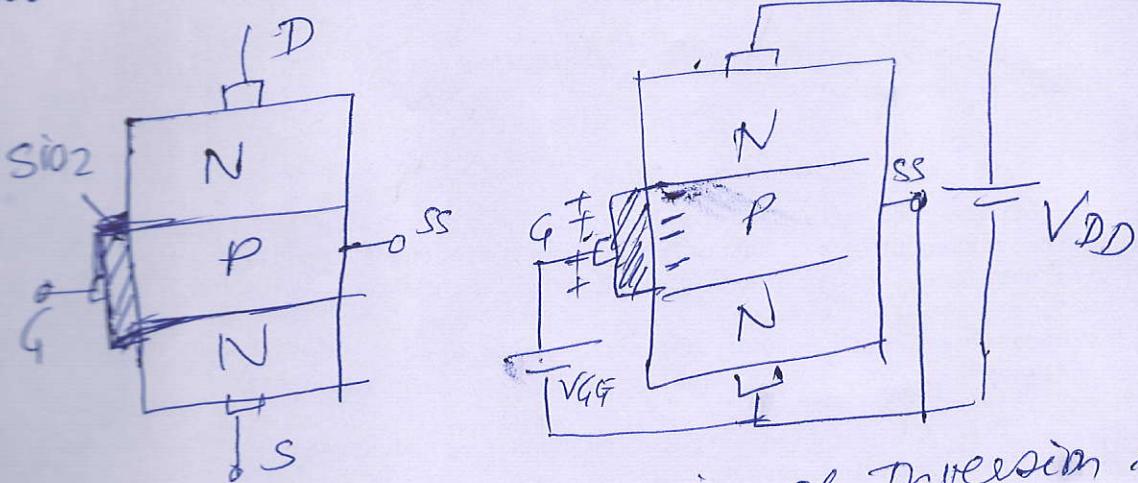
(c) ENHANCEMENT MODE

A positive voltage is applied at the G. The positive potential at G terminal will repel the holes present in P type substrate while attracting the minority carriers electrons towards the G terminal. The electrons are gathered near surface of SiO_2 .

The number of ^{gathered} electrons increase to such an extent that an induced N channel is developed which connects N type doped regions.

Hence I_D starts flowing through the induced channel. The particular value of V_{GS} at which conduction starts is called as threshold voltage or $V_{GS(th)}$.

(2) ENHANCEMENT ONLY MOSFET
 It has no depletion mode. It has no physical channel. P type substrate extends into the SiO_2 layer completely.



Formation of Inversion layer
 When $V_{GS} = 0$, the V_{DD} supply tries to force free electrons from S to D. But the presence of P region does not permit the electrons to pass through it. Thus there is no I_D for $V_{GS} = 0$: the enhancement type MOSFET is also called NORMALLY OFF MOSFET.

When $V_{GS} > 0$ it induces a negative charge in the P type substrate just adjacent to the SiO_2 layer. The induced negative charge is produced by attracting free electrons from the source.

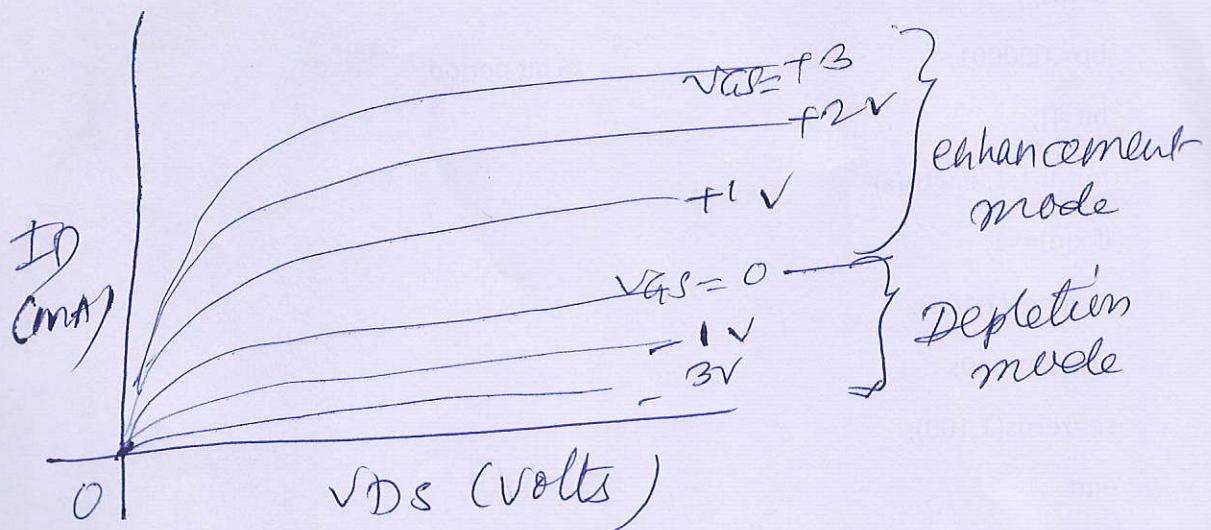
When G is positive enough it can attract a no. of free electrons. This form a thin layer of electrons which stretch from S to D. This effect is equivalent to producing a thin layer of N type channel.

Drain characteristics of DEMOSFET.

This is I_D & V_{DS} characteristic for common Source configuration.

(i) Depletion mode $V_{GS} \leq 0$

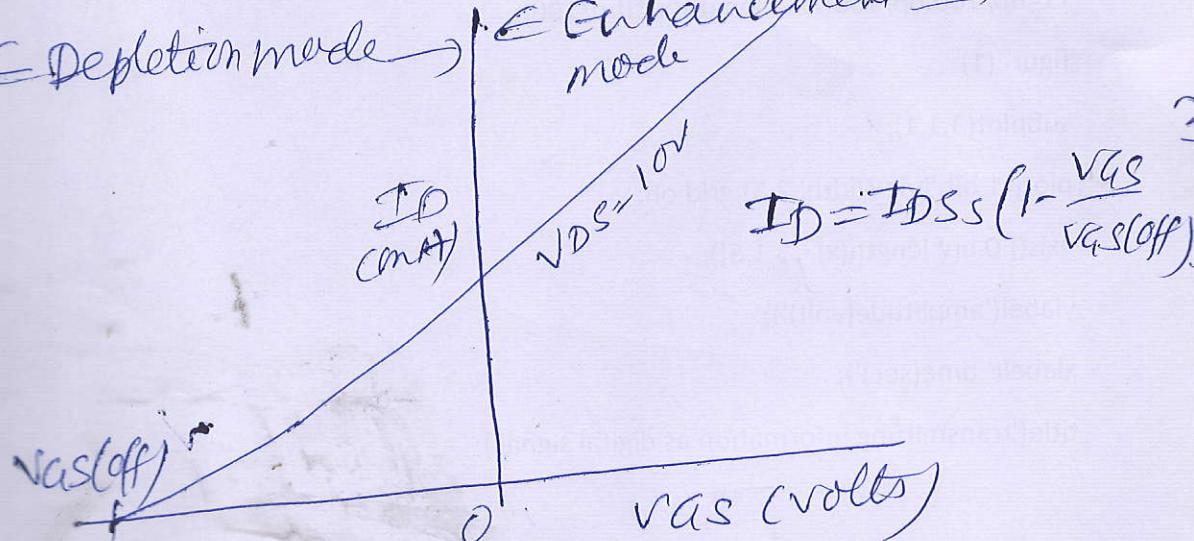
(ii) Enhancement mode $V_{GS} \geq 0$



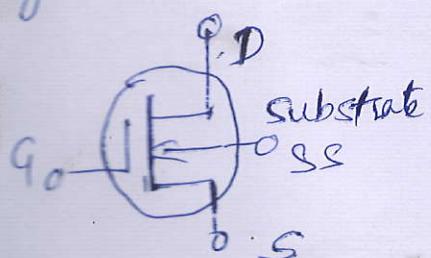
Transfer characteristics of DEMOSFET

I_D vs V_{GS} (Transconductance char)

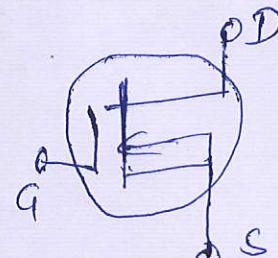
Depletion mode → Enhancement mode



Symbols for DEMOSFET (n channel)



when substrate is
4th terminal



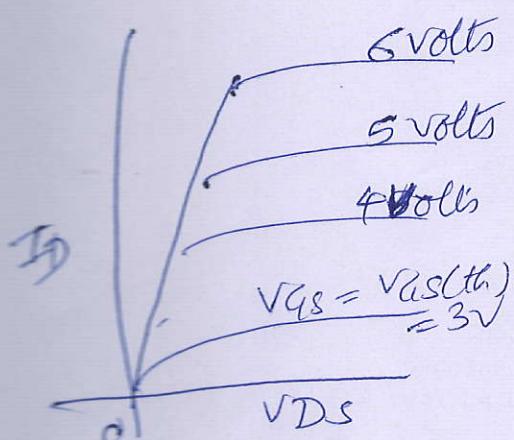
When substrate
is connected to
source

in P type substrate. This layer of free electrons is called N type inversion layer.

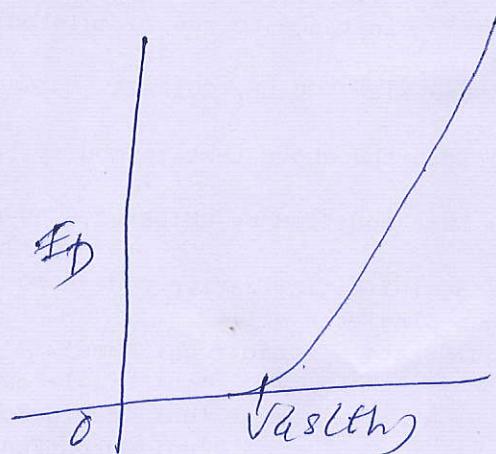
$V_{GS(th)}$ = The min V_{GS} which produce inversion layer is called threshold voltage.

When $V_{GS} < V_{GS(th)}$ no I_D flows from D to S.

CHARACTERISTICS CURVES FOR ENHANCEMENT ONLY MOSFET



(a) DRAIN CHARACTERISTICS



(b) TRANSFER CHARA.

(a) Drain characteristics

When $V_{GS} < V_{GS(th)}$: There is no I_D through the MOSFET. ~~due to~~ Actually an extremely small I_D flows through the MOSFET due to presence of thermally generated electrons in the p type substrate.

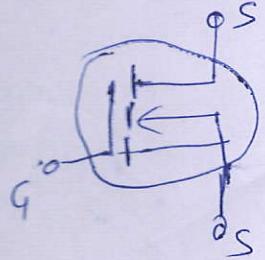
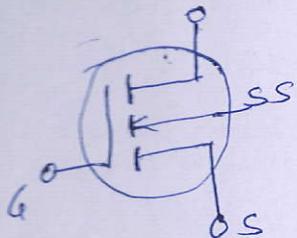
I_D increases with increase in V_{GS} the width of the inversion layer widen for increased value of V_{GS} and therefore allows more no. of free electrons to pass through it. I_D reaches its saturation value at a certain value of V_{GS} .

(b) TRANSFER CHARACTERISTICS

There is no I_D when $V_{GS} = 0$. If $V_{GS} > V_{GS(th)}$, I_D increases rapidly. If at any point along the curve is given by the relation.

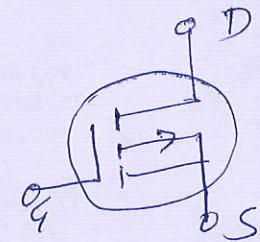
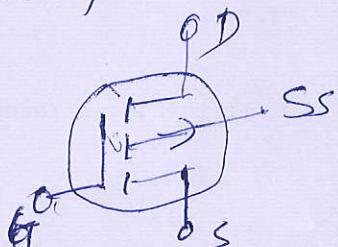
$$I_D = K [V_{GS} - V_{GS(th)}]^2$$

where K is constant whose value depends on the type of MOSFET.



(i) symbols for
n channel Enhancement-
only MOSFET

Broken lines indicate that there is no conducting channel between D and S.



(ii) symbols for
p channel type
enhancement only
MOSFET.

MOS CAPACITOR

Mos structure is essentially a capacitor. Metal acts as one plate of a capacitor, SiO_2 acts as a dielectric and semiconductor layer which may be p or n type acts as another plate.

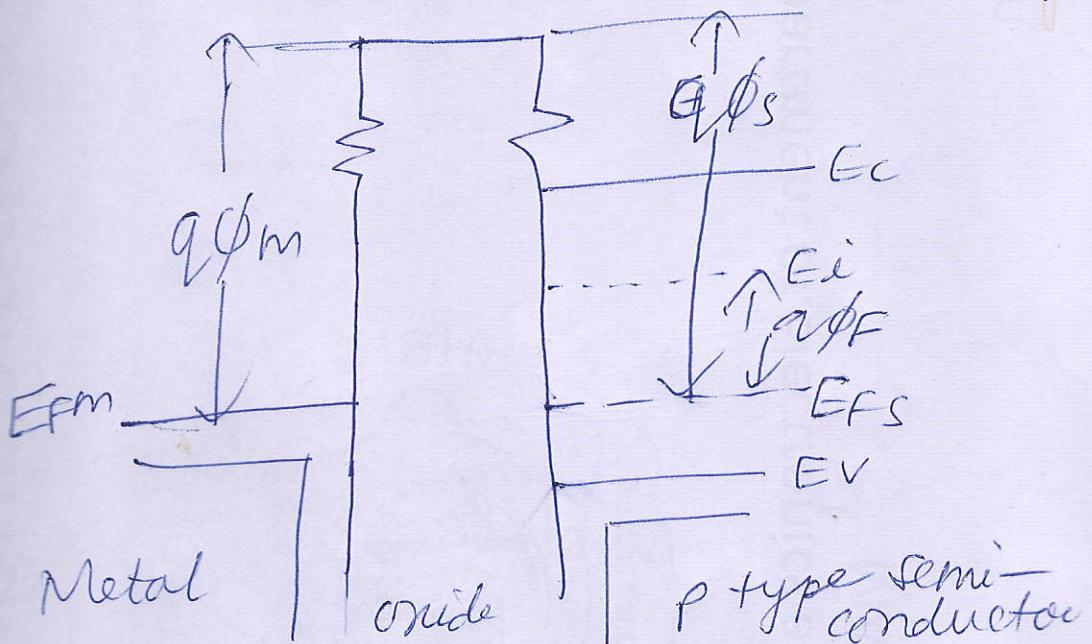


Fig: Band diagram of Ideal MOS structure at equilibrium.

(i) $q\phi_m$: work function of metal
It is the energy required to move an electron from the Fermi-level to outside the metal.

(ii) $q\phi_s$: work function of semiconductor
It is the energy required to move an electron from the Fermi-level to outside the semiconductor.

(iii) $q\phi_F$: Measures the position of EF below the intrinsic level E_i for semiconductor. This quantity indicates

how strongly P type the semiconductor is. Assume for ideal MOS capacitor $\phi_m = \phi_s$, so there is no difference in the 2 work functions.

(a) Effect of -ve voltage between Metal and semiconductor:

If -ve voltage is applied between the metal and semiconductor, effectively a negative charge is deposited on the metal. In response an equal net positive charge accumulates on the surface of the semiconductor. In case of P substrate this occurs by hole accumulation on semiconductor-moxide ~~surface~~ interface.

Since applied -ve voltage decreases the electrostatic potential of the metal relative to the semiconductor, the electron energies are raised in the ~~semiconductor~~ metal. As a result, Fermi level for the metal E_{fm} lies above its equilibrium position by qV where V is the applied voltage.

Since $q\phi_m$ & $q\phi_s$ do not change with applied voltage, moving E_{fm} up in the energy relative to E_{fs} causes tilt in the oxide conduction band. Such a tilt cause a ~~tilt~~ gradient in E_i , E_v & E_f .

An increase in hole concentration implies an increase in $E_i - E_f$ at the

semiconductor surface.

Since no current passes through MOS structure, there can be no variation in Fermi-level within the semiconductor. Therefore if $E_F - E_F$ is to increase it must occur by E_F moving up in energy near the surface. The result is bending of semiconductor bands near the interface.

Fermi-level near the interface lies closer to the valence band, indicating a larger hole concentration than that arising from the doping of the p type semiconductor.



Fig (a) Effect of -ve voltage.

(b) Effect of +ve voltage between Metal and Semiconductor

If a +ve voltage is applied between metal and semiconductor it raises the potential of the metal lowering

metal Fermi level by φ_V relative to its equilibrium position. As a result the oxide conduction band is again tilted.

The positive voltage deposits positive charge on the metal and -ve charge at the surface of the ^{semi}conductor. Such a negative charge in 'p' material arises from depletion of holes from the region near the surface, leaving behind uncompensated ionized acceptors.

In the depleted region, the hole concentration decreases, moving E_i closer to E_F and bending the band down near the semiconductor.

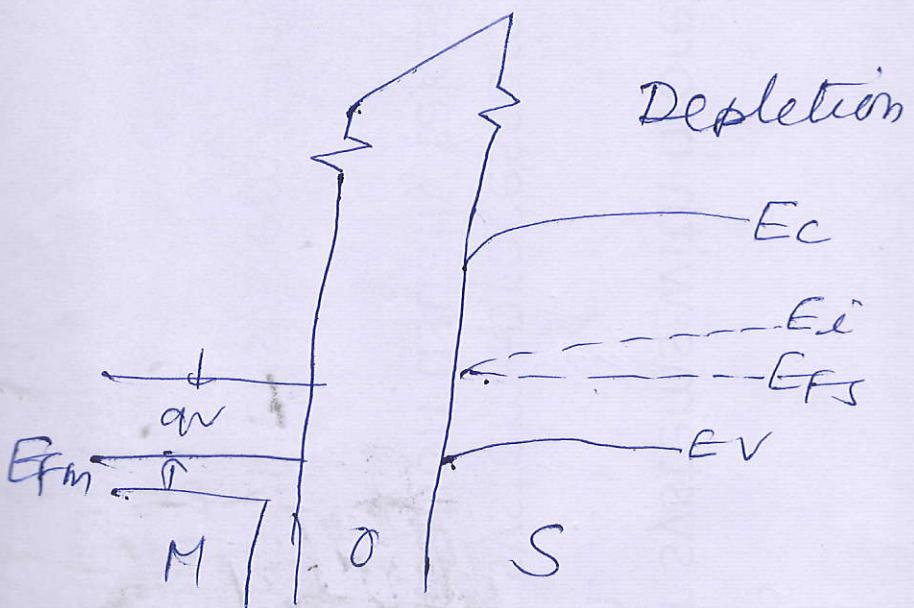


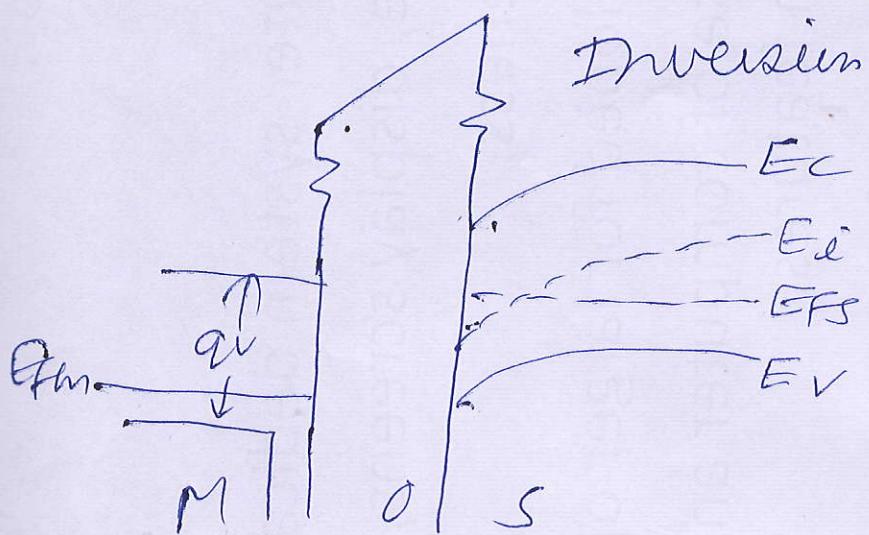
Fig (b) Effect of +ve voltage

(c) Effect of more + voltage between metal and semiconductor:

If more +ve voltage is applied, the bands at the semiconductor surface bend down more strongly. A sufficiently

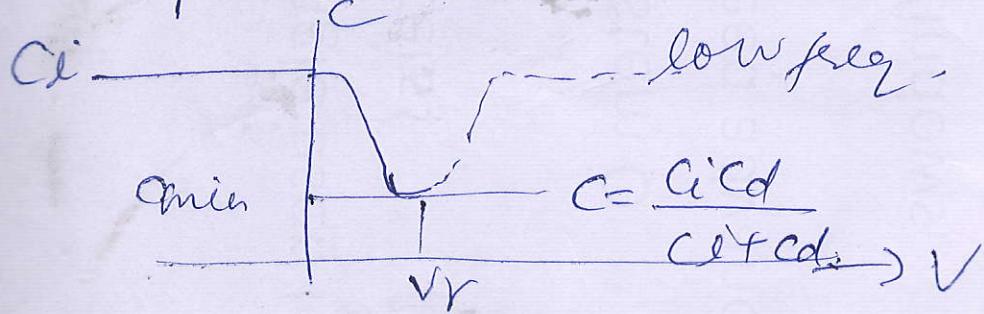
large voltage can bend E_F below E_F^* . $E_F > E_F^*$ implies a large electron concentration in the conduction band.

The region near the semiconductor surface has conduction properties typical of n type material. This n type surface layer is formed not by doping but by inversion of original p type semiconductor due to the applied voltage. The inversion region becomes conducting channel in FET.



c) Effect of more +ve voltage

C-V characteristics of P substrate MOS capacitor.



(i) For -ve voltage: Holes are accumulative at the surface. As a result, the MOS structure appears almost like a parallel plate capacitor dominated by the insulator properties. $C_i = \frac{\epsilon_i}{d}$

(ii) For + voltage: The semiconductor surface is depleted. Thus a depletion layer capacitance C_d is added in series with C_i . $C_d = \frac{\epsilon_s}{w}$

(ϵ_s = Semiconductor permittivity
 w = width of depletion layer)

\therefore Total capacitance $C = \frac{C_i C_d}{C_i + C_d}$.

With +ve voltage, the capacitance decreases as w grows until finally inversion is reached at V_r . With inversion there is no further charge in C_d since the depletion width has reached its maximum. (W_m)

(iii) For $V > V_r$; For the measurement at very low frequency ($\approx 10\text{Hz}$), the MOS capacitor in inversion resembles the parallel plate capacitor C_i again.

This effect can be induced at higher measurement frequencies by speeding up the carrier generation rate (e.g. by shining light on the sample)