

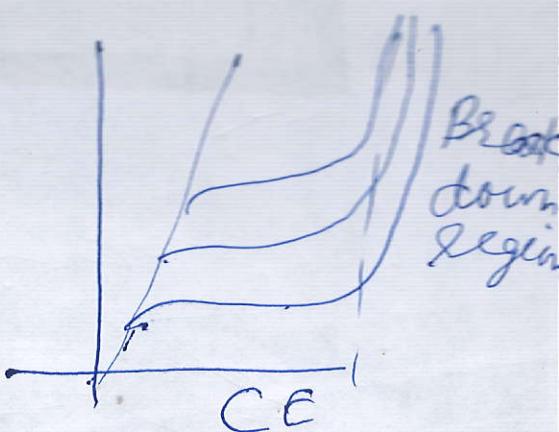
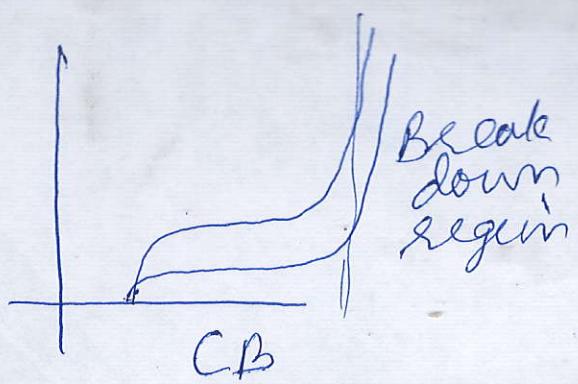
- (2) As V_{CE} is increased above zero, I_C increases rapidly to a saturation value depending on the value of I_B .
- (3) When V_{CE} is increased further, I_C slightly increases. This increase in I_C is due to the fact that increased value of V_{CE} reduces I_B and hence I_C increases because of Early effect.
- (4) When $I_B = 0$, a small I_C exists. This is leakage current. Under this condition the Transistor is said to be cut-off.

- (5) It determines a.c. input resistance. Its value is given by the ratio of a change in V_{CE} (ΔV_{CE}) to change in I_C (ΔI_C) for a constant base current.

$$R_o = \frac{\Delta V_{CE}}{\Delta I_C} / \text{constant } I_B$$

R_o ranges from $10\text{ k}\Omega$ to $50\text{ k}\Omega$

- (6) It determines B_o (a.c. current gain of CE configuration)
- $$B_o = \frac{\Delta I_C}{\Delta I_B}$$



LECTURE 28/10/2020 (2nd Lecture) (11)

EBER-MOLL MODEL

A transistor consists of 2 coupled P-N junctions. The B region is common to both junctions and forms a coupling between them. Since the transistors are constructed with a very narrow base regions therefore a significant electrical interaction exists between the junctions. This interaction is called transistor action.

The relationship between transistor currents and transistor junction voltages is given by

$$I_C = -\alpha_N I_E - I_{C0} \left(e^{\frac{V_C}{V_T}} - 1 \right). \quad (1)$$

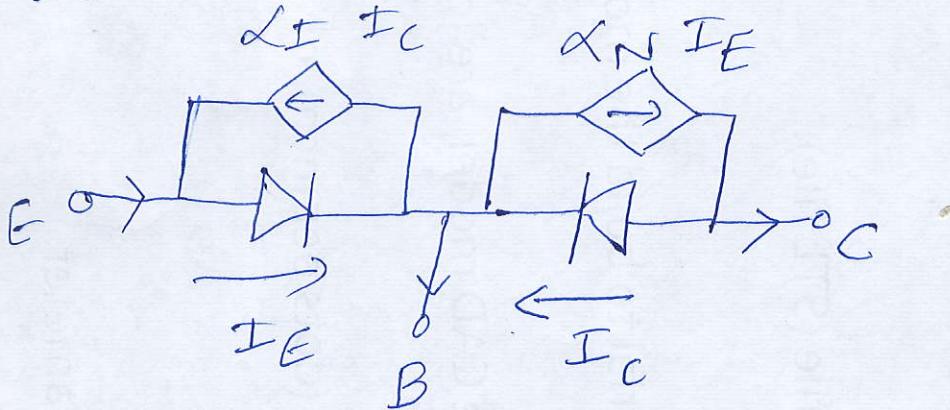
$N \rightarrow$ means the transistor is used in normal manner. ($E \rightarrow$ input, $C \rightarrow$ output)

If the role of E and C are interchanged, the transistor operates in inverted fashion.

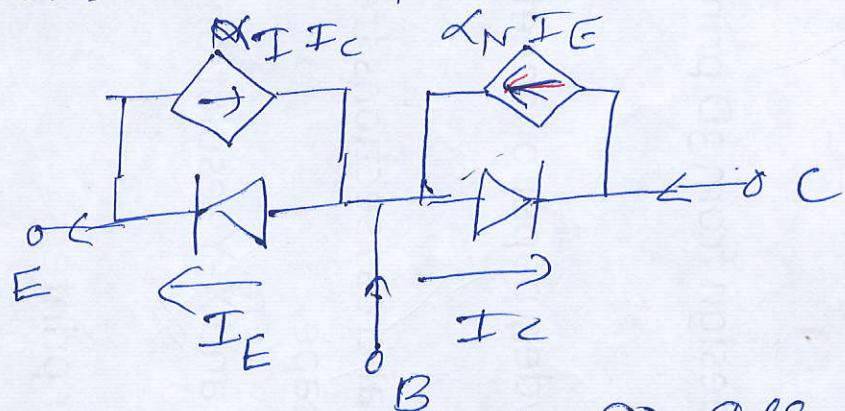
$$I_E = -\alpha_I I_C - I_{E0} \left(e^{\frac{V_E}{V_T}} - 1 \right). \quad (2)$$

where $I_{E0} \times I_{C0}$ are reverse saturation currents, α_I = reverse alpha
 α_N = forward alpha.
 $V_E \times V_C$ are voltages at junctions.

Ebel's Mole P-N-P model



Ebel's Mole N-P-N model



Equations ① and ② are valid for P-N-P model. For N-P-N model the signs will change for all currents and voltages.

BJT BIASING AND STABILIZATION

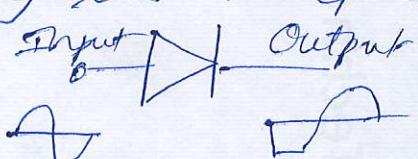
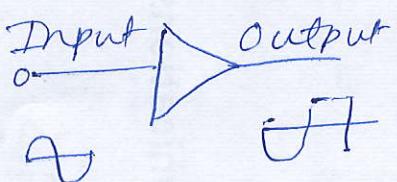
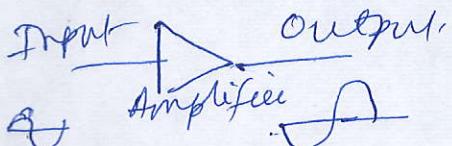
BJTs are used in large variety of applications. To use a transistor in any application, it is necessary first to bias the transistor.

Biasing turns the device ON and place it in a region where it operates linearly and provide a constant voltage gain.

The biasing deals with setting a fixed level of current which should flow

through the transistor with a desired fixed voltage drop across the transistor junction (13)

Usually I_C , I_B , V_{CE} and V_{BE} are the currents and voltages which are required to be set by the biasing circuit. The proper value of these currents and voltages allow a transistor to amplify the weak signals faithfully. It means that the transistor must increase the magnitude of the signal without changing its shape.



(a) Amplifier linear operation (Properly biased)

(b) Amplifier driven into cut-off

(c) Amplifier driven into saturation

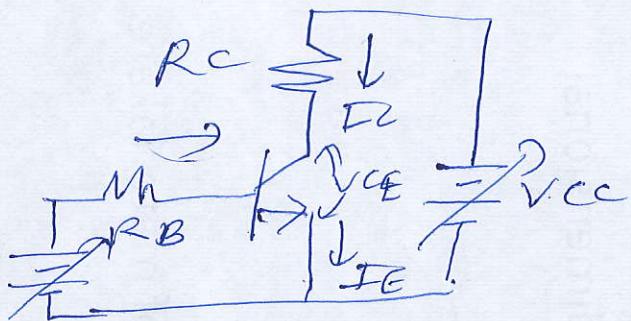
THE D.C. OPERATING POINT AND LOAD LINE

A fixed level of certain voltages and currents define the operating point at which the transistor operates. It is also known as quiescent point or simply Q point.

Since the level of currents and voltages are fixed, therefore the operating point is also called d.c. operating point.

D.C. LOAD LING

Consider the transistor biased with two d.c. supplies V_{CC} and V_{BB} to obtain the fixed values of I_C , I_B and V_{CE} .



$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \quad \dots \textcircled{1}$$

As V_{CE} is very small at saturation point compared to V_{CE} $\therefore V_{CE}$ is neglected.

$$\therefore I_C = \frac{V_{CC}}{R_C}$$

$$I_C (\text{sat}) = \frac{V_{CC}}{R_C} \quad \dots \textcircled{2}$$

Putting $I_C = 0$ in equation ① At cut-off point $I_C = 0$

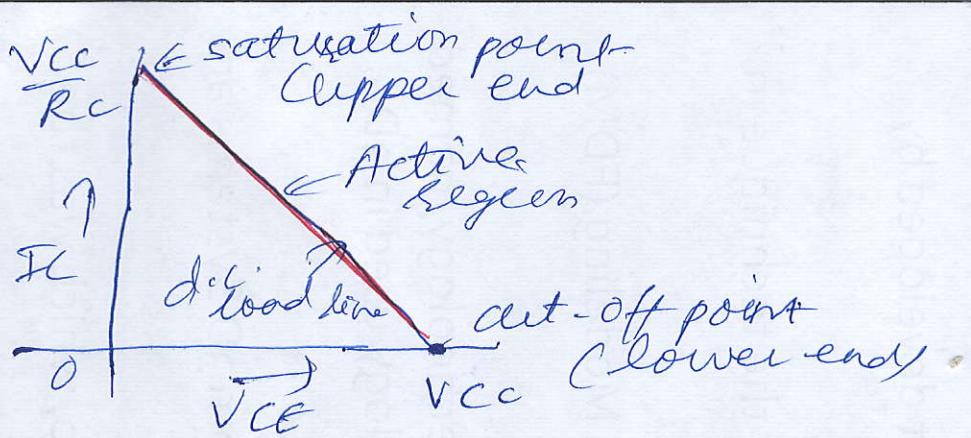
$$0 = \frac{V_{CC} - V_{CE}}{R_C}$$

$$\therefore V_{CC} = V_{CE} \text{ (cut off)} \quad \dots \textcircled{3}$$

The region lying between saturation and cut-off points of the load line is active region of the transistor operation. As long as the transistor is operating in this active region, the output voltage is linear reproduction of the input.

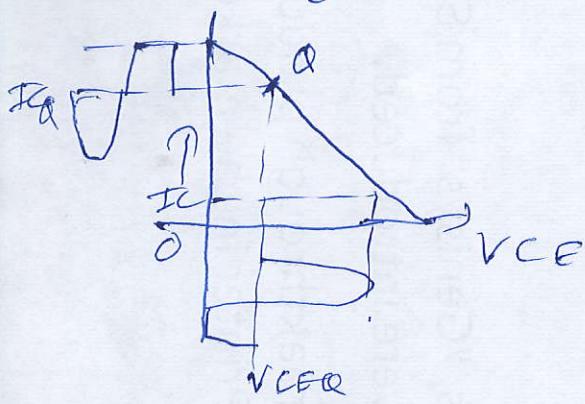
The line joining the cut-off point and saturation point is called d.c. load line.

For normal operation Q point of the transistor is selected midway between the saturation and cut-off point i.e. V_{CE} is $\frac{1}{2} V_{CC}$.

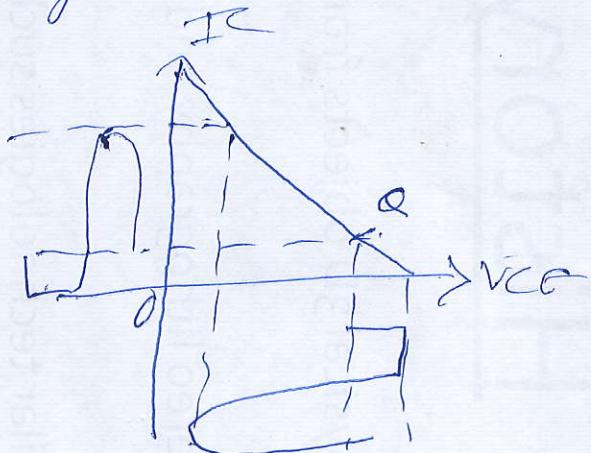


Q POINT AND MAXIMUM UNDISTORTED OUTPUT

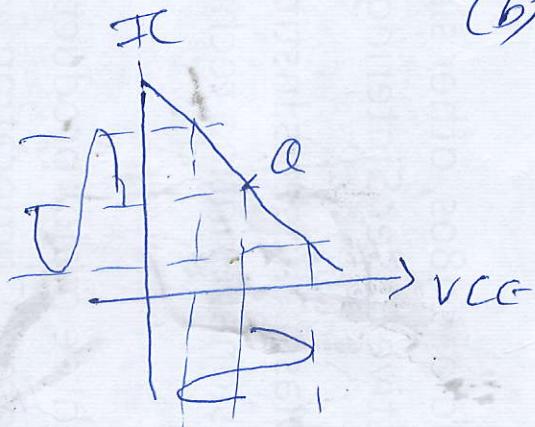
(a) Q point near saturation point
During -ve half cycle of the input, the transistor is driven into saturation. As a result of this, the negative peak of the input signal is clipped at the out



(a)



(b)



(c)

(b) Q point located near cut-off point
The transistor is driven into cut-off. Therefore the positive peak of the input

signal is clipped at the output (16)

c) Q point located at the centre of load line:

Here there is an undistorted signal at the output

FACTORS AFFECTING STABILITY OF Q POINT

Even after the suitable selection of Q point, it tends to shift from its position.

This happens because of two factors

(1) Inherent variations of transistor parameters

For CE configuration

$$I_C = \beta I_B + (1+\beta) I_{C0}$$

All the 3 variables β , I_B and I_{C0} are strongly dependent on temperature. As the temperature increases, all the 3 variables also increase which results in increase in I_C . This causes the operating point to shift towards the saturation point, resulting in clipping and bad distortion of the output. In some cases the transistor may even burn out because of excessive I_C .

(2) Variation in parameter values of the same type

In spite of advance technology, transistors of the same type are manufactured with large variation in parameters i.e. minimum, maximum and typical values of parameters.

are mentioned by manufacturer's data sheet. This gives instability of the Q point.

PRINCIPLE (Designing biasing circuit)

If the temperature increases, I_{C0} also increases. This causes I_C to increase by a factor of $(1+B)$. However by some means, if the I_B is made to decrease with increase in temperature the I_C will decrease by a factor of B . This will compensate for the increase in $(1+B) I_{C0}$ and hence I_C will remain nearly constant.

This principle is used to provide stabilization of I_C by designing it as biasing circuit of different types.

STABILITY FACTOR

It is defined as the rate of change of collector current (dI_C) w.r.t. the I_{C0} (dI_{C0}) keeping B and I_B constant.

$$S = \frac{dI_C}{dI_{C0}} \quad | B, I_B \text{ constant}$$

The stability factor is a measure of bias stability of a transistor circuit. A higher value of stability factor indicates poor stability whereas a lower value indicates good stability.

The stability factor may also be expressed using the relationship between I_B , I_C and I_{CO} .

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$$I_C = B I_B + (1+B) I_{CO}$$

differentiating w.r.t. I_C

$$1 = \frac{dBI_B}{dI_C} + \frac{d(1+B)I_{CO}}{dI_C}$$

$$= B \frac{dI_B}{dI_C} + (1+B) \frac{dI_{CO}}{dI_C}$$

$$1 = B \frac{dI_B}{dI_C} + (1+B) \times \frac{1}{S} \quad \text{as } S = \frac{dI_C}{dI_B}$$

$$\cancel{1 - (1+B) \frac{1}{S}} = \cancel{B \frac{dI_B}{dI_C}}$$

$$1 - B \frac{dI_B}{dI_C} = (1+B) \times \frac{1}{S}$$

$$\therefore S = \frac{1+B}{1 - B \frac{dI_B}{dI_C}} \quad \dots \textcircled{1}$$

The above expression is very useful in determining the stability factor S of any biasing circuit.

Stability factor of CB circuit

For CB configuration

$$I_C = \alpha I_E + I_{CO} \quad \text{(2)}$$

Differentiating (2) w.r.t. I_{CO} .

$$\frac{dI_C}{dI_{CO}} = \alpha + 1$$

α, I_E
are constant

$$\therefore S = 1$$

It indicates that CB circuits are highly stable.

therefore there is no need of bias stabilization
in CB circuits

(19)

Stability factor of CE circuit

For CE configuration

$$I_C = B I_B + (1+B) I_{C0} \quad (3)$$

Differentiating (3) w.r.t. I_{C0}

$$\frac{dI_C}{dI_{C0}} = 0 + (1+B)$$

$$S = 1+B$$

In a CE circuit, I_C is highly dependent on I_{C0} and hence upon the temperature. Thus there is a strong need to provide bias stabilization in CE circuits to improve the stabilization factor.

CONDITIONS FOR PROPER BIASING OF A TRANSISTOR

1. Proper d.c. value of I_C
2. Proper value of $V_{BE} \geq 0.7V$ for Si and $0.3V$ for Ge at any instant.
3. Proper value of $V_{CE} \leq 1V$ for Si & $0.5V$ for Ge at any instant.

* ~~NOTE~~ Conditions ① and ② make sure that

B-E junction of a transistor shall remain forward biased during all parts of signal

Condition ③ makes sure that C-B junction of transistor shall remain reverse biased at all instants.

REQUIREMENTS OF A BIASING CIRCUIT.

1. Establish an operating point in the center of active region
2. Stabilize I_C against temperature variation
3. Make the Q point independent of the transistor parameters so that it does not shift when the transistor is replaced by another of the same type in the circuit