

(1)

Module V

Till now we have considered discrete circuits where separately manufactured components like diodes, transistors resistors, capacitors etc. are joined by wires or assembled on printed circuit boards.

2 main disadvantages are (i) they occupy large space (ii) less reliability as hundred of components die to be soldered.

To meet these problems of space conservation and reliability, a new branch of electronics known as microelectronics was developed in 1950's. It deals with micro circuits. One type of such circuit is integrated circuit (IC).

An integrated circuit is one in which the active components (transistors, diodes etc.) and passive components (resistors, capacitors etc.) are automatically a part of semiconductor chip.

Advantages of ICs.

(1) Extremely small physical size - size is thousand of times smaller than a discrete circuit. The various components and their interconnections are distinguishable only under powerful microscope.

(2) Very small weight!

Since the size of chip is small and circuit is miniaturised, weight is very small.

3. Reduced cost:

This is because large number of circuit components are produced simultaneously on a small semi-conductor wafer (batch fabrication).

4. Extremely high Reliability:

This is due to absence of soldered joints and need for few interconnections. Therefore Ics will work for longer periods without giving any trouble.

5. Decreased response time and speed:

As various components are located close to each other, the time delay of signals is reduced. Because of short distances the chance of stray, electrical pickup is practically nil. Hence it makes them very suitable for small signal and high frequency operation. Response time or operating speed is increased.

6. Low power consumption:

Because of small size, they have low power consumption.

7. Easy replacement:

Ics are not repaired but replaced.

8. Higher yield:

Yield means % of usable devices. Because of batch fabrication, yield is very high.

Q. Temperature differences between parts of a circuit are small.

Limitations of ICs

1. Coils or inductors cannot be fabricated.
2. Capacitors and resistors are limited in maximum value.
3. It is not possible to produce high power ICs (greater than 10W).
4. Low noise and high voltage operation are not easily obtained.
5. High frequency response is limited.
6. If any component of IC goes out of order the whole IC has to be replaced by new one.
7. They are quite delicate and cannot withstand rough handling or excessive heat.

SCALE OF INTEGRATION

The number of electronic circuits or components that can be fitted into a standard size ICs is drastically increasing with each passing year.

① SSI	Small Scale Integration	Components / chip
② MSI	Medium Scale Integration	< 12
③ LSI	Large - II - II	12 - 99
④ VLSI	Very Large - II - II	100 - 9999
⑤ ULSI	Ultra Large - II - II	100000 - 999999
⑥ GSI	Giga Scale Integration	1,000,000

IC CLASSIFICATIONS

(4)

- (a) Fabrication technique
- (b) Functionality
- (c) Size
- (d) Devices employed in IC.

(a) Fabrication technique:

- (i) Monolithic ICs
- (ii) Hybrid ICs

- (iii) Thin and thick film ICs.

(i) Monolithic (mono-single, litho-stone)
here the active and passive elements
and their interconnections are formed upon
or within a single piece of silicon crystalline
material. ^{called wafer.} Most commonly used e.g. Amplifiers,
Voltage regulators, TV circuits etc.

Drawbacks of monolithic ICs.

(1) Isolation between the components is
not good

(2) Inductor cannot be fabricated.

(3) very low power rating.

(4) For making any change in circuit
, a new set of masks is required.
Hence less flexible in circuit design.

(ii) hybrid ICs / Multichip ICs.

The circuits are formed either by
interconnecting a number of individual
chips or by a combination of film and
monolithic IC techniques.

Active components are first formed
within a silicon wafer (using monolithic
which is subsequently covered ~~by~~ with

insulating layer such as Si_3N_4 (5)
Film techniques are then employed
to form passive components on the Si_3N_4
surface. Connections are made from the
film to the monolithic structure through
windows cut in the Si_3N_4 layer.

They are used in high power audio
amplifiers. More expensive but have
better performance than monolithic ICs.

(ii) Thin and thick film ICs

Both these techniques have similar
appearance, properties and general
characteristics. They differ not in their
relative thickness but in the method
of depositing the film. Only passive
components are formed through thick
or thin film techniques on the insulating
surface. The active elements are added
externally as discrete elements to complete
the functional ~~unit~~ circuit. The discrete
active components are produced using
the monolithic process.

(a) Thin film ICs:

Such circuits are constructed by depositing
films such (typically 0.1 to 0.5 mm)
of conducting material through a mask
on the surface of a substrate made of
glass or ceramic.

(a) Resistors & conductors - formed by
varying the width and thickness of the

film and by using materials of different resistivity

(i) capacitors : produced by sandwiching an insulating oxide film between two conducting films.

(ii) small inductors - made by depositing a spiral formator of film.

The active components like transistors and diodes are externally added & interconnected by wire bonds.

Methods of producing thin films

(i) vacuum evaporation : Here vapourised material is deposited through a set of masks on the glass or ceramic substrate contained in vacuum.

(ii) cathode sputtering : Here atoms from a cathode made of the desired film material are deposited on the substrate which is located between the cathode and anode.

Thick film ICs :

They are sometimes referred as printed thin-film circuits. They are so called because silk-screen printing techniques are employed to create the desired circuit pattern on the surface of the substrate. The screens are made of fine stainless steel wire mesh and the inks are pastes (of pulvressed glass and aluminium) which have

conductive, resistive or dielectric properties. After printing, the circuits are high-temp fired in a furnace to fuse the films to the insulating substrate. Active elements are added externally as discrete components.

IC family Properties	Monolithic	Thick thin film	Hybrid
Substrate	Silicon	Glass, ceramic	(i) Glass ceramic (ii) Silicon
Structure	Active & passive devices alongwith interconnection on a single chip.	Passive components (say Passive device & interconnection) are fabricated on a substrate and then prefabricated active components are added along with interconnection.	(a) Passive device & interconnection on one insulating substrate with active devices wire wound (b) Active device on a single chip while passive devices alongwith interconnections on thick-thin film
Active devices	BJT, MOSFET	MOSFET	BJT MOSFET.
Passive devices	(i) Diffused resistors, oxide capacitor. (ii) MOS resistor, oxide capacitor.	Metal film resistor, oxide capacitor	Metal films resistor, oxide capacitor.
Application	Linear & digital ICs	Digital ICs	Linear & digital ICs.

(B) on the basis of functionality (8)

(i) Linear ICs (Analog ICs)

Their inputs and outputs can take on a continuous range of values and the outputs are generally proportional to the inputs. They are quickly replacing their discrete circuit counterparts in many applications as their cost becomes competitive. They are highly reliable. Find use in military & industrial applications e.g. amplifiers, voltage regulators, multipliers etc.

(ii) Digital ICs:

They contain circuits whose input and output voltages are limited to two possible levels low and high (ON or OFF states). They find application in computer and logic circuits e.g. logic gates, FFs, counters, clock chips, calculator chips, memory chips microprocessors etc.

(C) On the basis of size:

Number of gates or circuits per chip SSI, MSI, LSI, VLSI etc.

(D) On the basis of device implemented

(i) Bipolar ICs - use BJT

(ii) Unipolar ICs - use FET

SEMICONDUCTORS USED IN FABRICATION OF IC'S AND DEVICES.

Germanium	Silicon.
① Unsuitable for certain application due to high junction leakage currents as it has relatively narrow energy band gap (0.7 eV)	Comparatively suitable for all applications as junction leakage currents are negligible as the energy band gap is 1.1 eV.
② Ge devices can be operated upto 100°	Si devices can be operated upto 200°
③ Ge Oxide is unsuitable for certain device applications	SiO ₂ is required for the planar processes as it has superb insulating properties
④ The intrinsic resistivity of Ge is 47Ω.cm. Hence not suitable for high voltage rectifying devices	The intrinsic resistivity is 230,000Ω.cm. hence most suitable for high voltage rectifying devices as well as infrared sensing devices
⑤ Costlier	Cheaper because available in abundance as sand.

(10)

GaAs

Advantages

- (1) Attractive electrical properties
- (2) Has an electron velocity that is larger than Si's. GaAs devices are faster than Si devices.
- (3) Lower saturation electric field therefore devices have lower power delay product.
- (4) Devices have lower parasitic capacitances hence high speed.
- (5) It has direct band gap and therefore emits light.

Disadvantages

- Crystals have a high density defects which limit the performance of devices made from it.
- (2) Very difficult to grow in single crystal form.

GaAs, GaP & GaN → used in high speed devices and devices requiring emission and absorption of light such as lasers and LEDs.

ZnS → As fluorescent material used in TV screens.

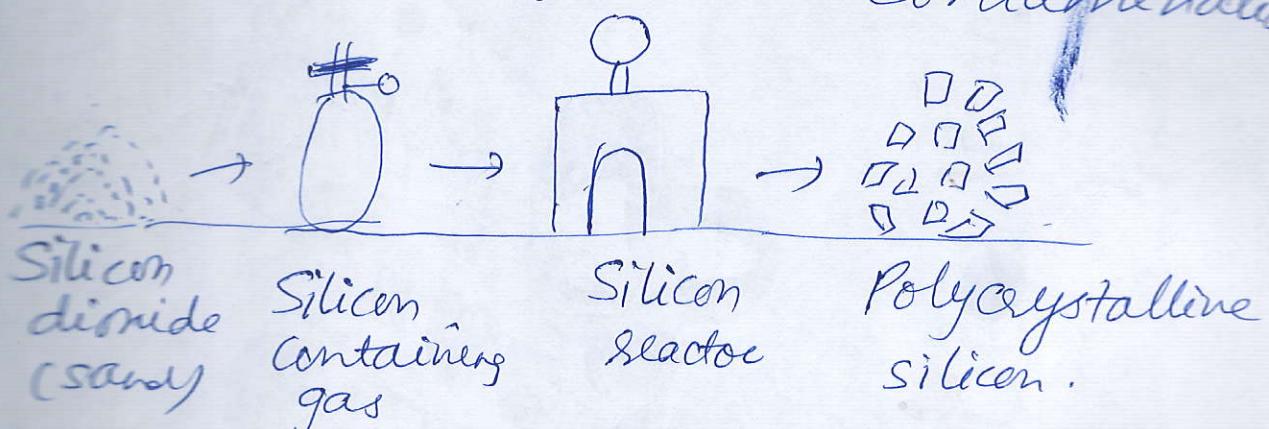
InSb, CdSe → used as light detectors

PROCESSES INVOLVED IN IC FABRICATION

① Material preparation

(1)

Si is found in nature in the form of silica and silicates. SiO_2 constitutes almost 20% of earth's crust. The sand can be converted into pure Si through number of processes. For the fabrication of ICs, Si must be in crystalline form which is pure Si with no defects or contamination.



The sand is allowed to react with a gas produced from the burning of carbon (coal, coke & wood chips). This produces Si with 98% purity. Next Si is further purified in a reactor to produce electronic grade polycrystalline Si.

② Crystal growth & Wafer preparation

The polycrystalline Si is composed of many small crystals having random orientation and containing many defects.

For Si to be used for fabrication of ICs, it should be ~~not~~ nearly perfect and crystalline in nature. This is done by crystal growth.

2 methods are used.

(i) Czochralski process (ii) flat zone

Flat zone method is used to prepare crystals for fabricating high power, high voltage semiconductor devices.

(i) Czochralski process - In practice all the Si required is prepared using this process. In general a phase change from solid, liquid or gas phases to crystalline solid phase is nothing but growing crystal.

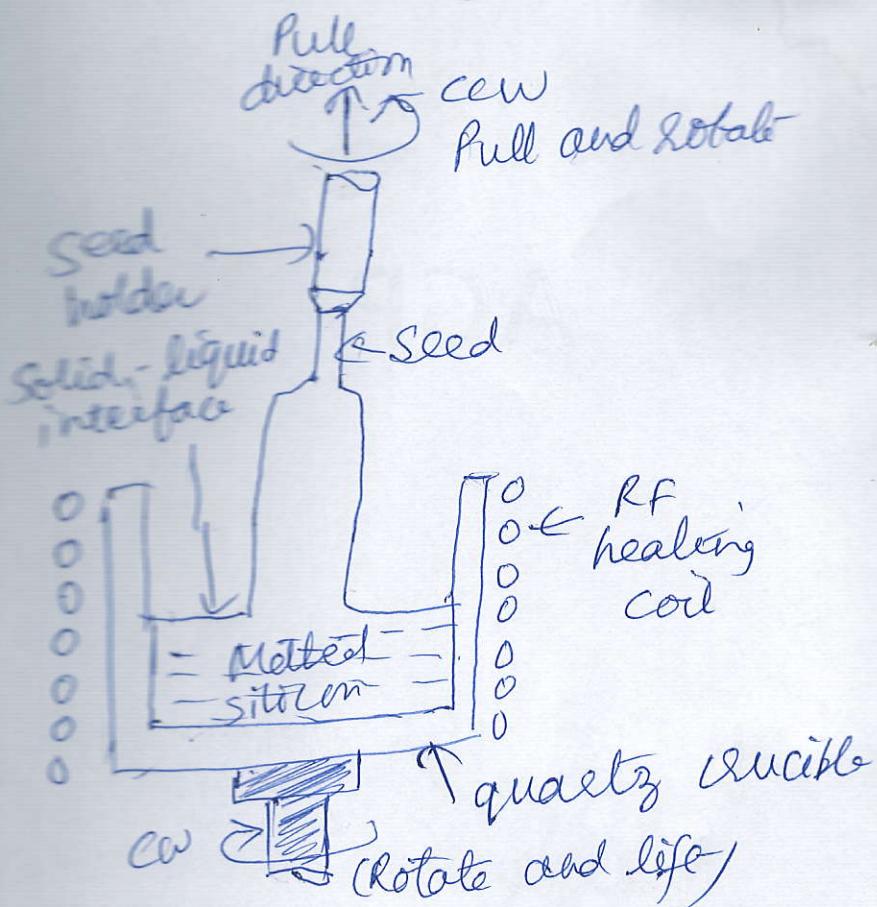
This process consists of 4 important subsystems

(i) a furnace which includes quartz crucible, a rotation mechanism (clockwise and a radio frequency (RF) heating element

(ii) a crystal pulling mechanism which includes a seed holder and a counter clockwise rotation mechanism.

(iii) an ambient control which includes an argon gas source, a flow control and exhaust system.

(iv) Computer system to control process parameters such as temperature, crystal diameter, pull rate & rotation speed.



The polycrystalline silicon is placed in fused silica crucible. The furnace is heated to a temperature of 1690K which is slightly greater than the melting point (1085K) of silicon. A precisely controlled amount of dopant (trivalent or pentavalent) is added to make it P or N type. A suitable seed crystal is suspended over the crucible in seed holder. The seed is inserted into the melt and a small portion of it is allowed to melt. The seed is rotated and pulled up very slowly while at the same time, the crucible is rotated in the opposite direction. The molten silicon attaches itself to the seed and becomes identical to the seed in structure and orientation.

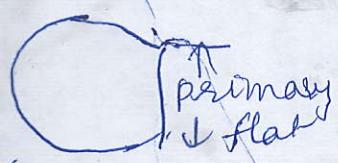
As the seed is pulled up, the material

that is attached to the seed solidifies. The crystal structure becomes the same as that of the seed and a larger crystal is formed. Thus using this method cylindrical single crystal bars (called ingots) of Si are produced.

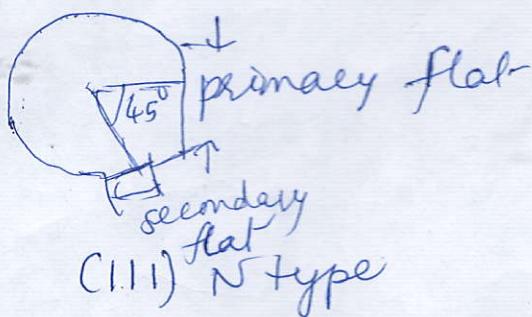
The desired diameter of silicon ingot is obtained by controlling both the temp. and the pulling speed. In the final step, when bulk of the melt has been grown, the crystal diameter is decreased until there is a point contact with the melt. The resulting ingot is cooled and removed to be made into thin discs called wafers.

WAFER PREPARATION

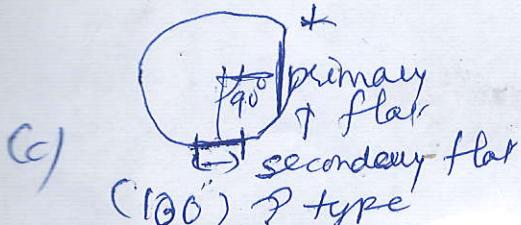
In this stage the ingot surface is ~~grounded~~ ground throughout to an exact diameter and the top & bottom portions are cut-off. After that one or more flat regions are ground along the length of the ingot. These flat regions mark the specific crystal orientation of the ingot and conductivity type (P or N) of Si material.



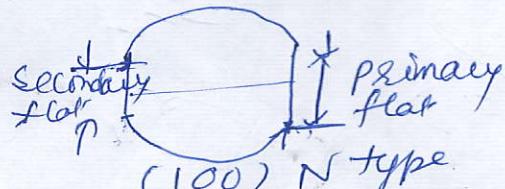
(a) (111) P type



(111) N type



(100) P type



(100) N type

The semiconductor industry uses (111) (P) wafers for fabricating IC with bipolar transistor technology and (100) wafers for MOS circuits.

Once the orientation is done the ingot is sliced into wafers by a high speed diamond saw. Thickness of wafer is 0.4 to 1.0 mm.

If the sliced wafers are to be used for VLSI application, 2 sided mechanical lapping process is carried out (Lapping is a machining process in which 2 surfaces are rubbed together with an abrasive between them). Using this process wafers with uniform flatness are achieved which are required for photolithography.

Due to trimming, grinding & slicing the surface & edges of the wafers get contaminated & even damaged. Chemical etching / alkaline etching is done to remove contamination.

After etching the wafer is polished to a mirror like finish.

Finally the wafers are cleaned, rinsed and dried for use in fabrication of ICs

Wafer fabrication

- Following processes are used in the fabrication of ICs.
- (1) Oxidation (2) Etching (3) diffusion
 - (4) Ion-implantation (5) Photolithography
 - (6) Epitaxy (7) Metallization and interconnections

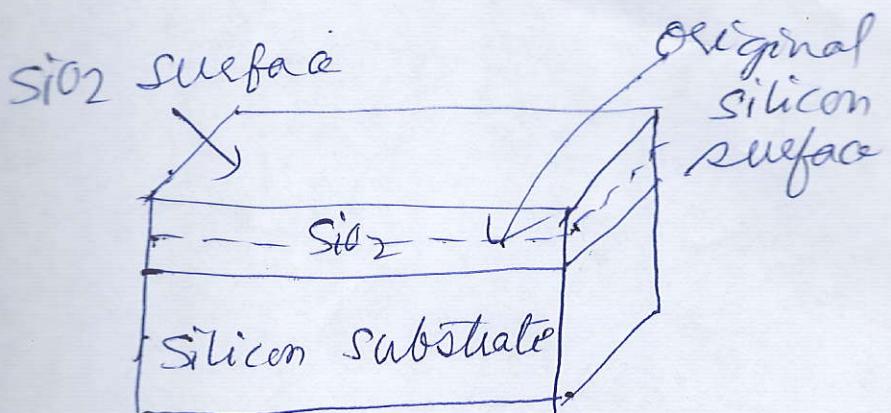
(1) OXIDATION:

The process in which a thin layer of SiO_2 is formed on the surface of silicon wafer using thermal growth technique is called oxidation.

In the planar process i.e. a process in which the introduction of impurities and metallic interconnections is carried out from the top of the wafer, it is essential to protect certain regions of surface of the wafer so that dopant atoms may be driven into other selective regions during the processes such as diffusion or ion-implantation. For such a shielding ~~process~~ purpose, SiO_2 is best suited.

SiO_2 has several uses

- (i) To serve as a mask against implant or diffusion of dopant into silicon.
- (ii) To provide surface passivation to isolate one device from another.
- (iii) To act as a component in MOS structure.



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Figure shows oxide layer grown on the surface of Si substrate. The commonly used silicon dopants such as Boron, P, As and Antimony have very low diffusion coefficient (i.e. they diffuse with great difficulty) in SiO_2 . Because of this reason, SiO_2 is used as a shield against infiltration of these dopants. These dopants diffuse easily if the surface is silicon.

Different techniques developed for forming oxide layers are

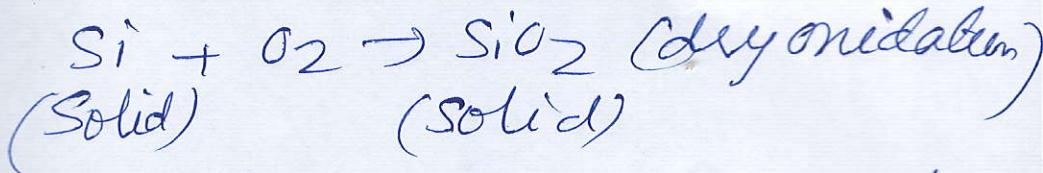
- (A) Thermal oxidation (a) Dry oxidation
- (B) Wet anodization / oxidation
- (C) Vapour phase technique
- (D) Plasma anodization or oxidation

Thermal Oxidation is most commonly used technique in IC fabrication.

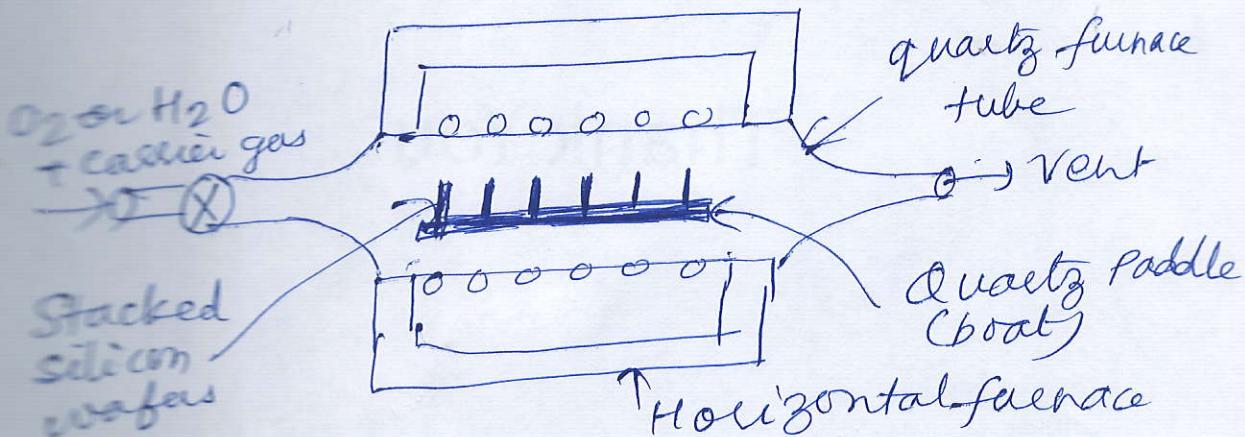
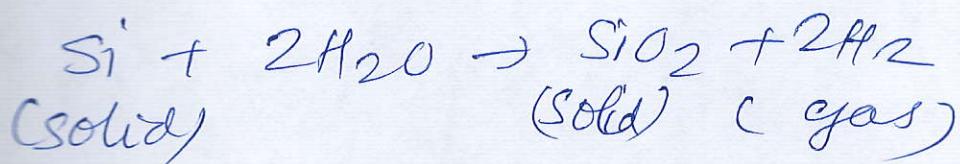
(A) THERMAL OXIDATION :

It is called thermal oxidation because to grow oxide layer, the temp. is maintained high. The selection of the oxidation technique depends upon the thickness and oxide properties required.

(a) For thin oxides with low charge density at interface, the oxides are grown in dry oxygen and is called dry oxidation.



(b) For thick layers of oxides, steam or water vapour is used at high pressure for oxidation. This is called wet oxidation.



Here the wafers are stacked vertically in a slotted paddle or boat which is open ended. It is made up of quartz and is placed in quartz tube. The quartz tube is slowly passed through resistance heated horizontal furnace. Temp. is maintained at 700°C to 1200°C .

A computer controls the whole operation which includes regulating the

The gas flow sequence, automatic insertion and removal of wafers and the furnace temp.

Once the SiO_2 layer has been formed on the surface of the wafer, it is selectively removed (etched) from those surfaces where impurities are to be introduced and kept as a shield for underlying Si surface whose dopants are to be allowed.

(B) Vapour phase / chemical vapour deposition (CVD) - It is used when the oxide layer is required on the top of a metal layer such as in multi level metallization structure.

(C) Plasma nitridation - It is a low temp. vacuum process carried out in a pure oxygen discharge. This process allows to grow high quality oxides on the surface of Si wafer compared to other techniques.

(2) ETCHING :

It is a process in which the material which is not masked by lithographic process is removed uniformly or selectively.

(A) Wet Etching : the unmasked region on the wafer are etched using wet etchants (i.e. chemicals) such as nitric