EI-27003: Electronics Devices and Circuits
Lecture - 12

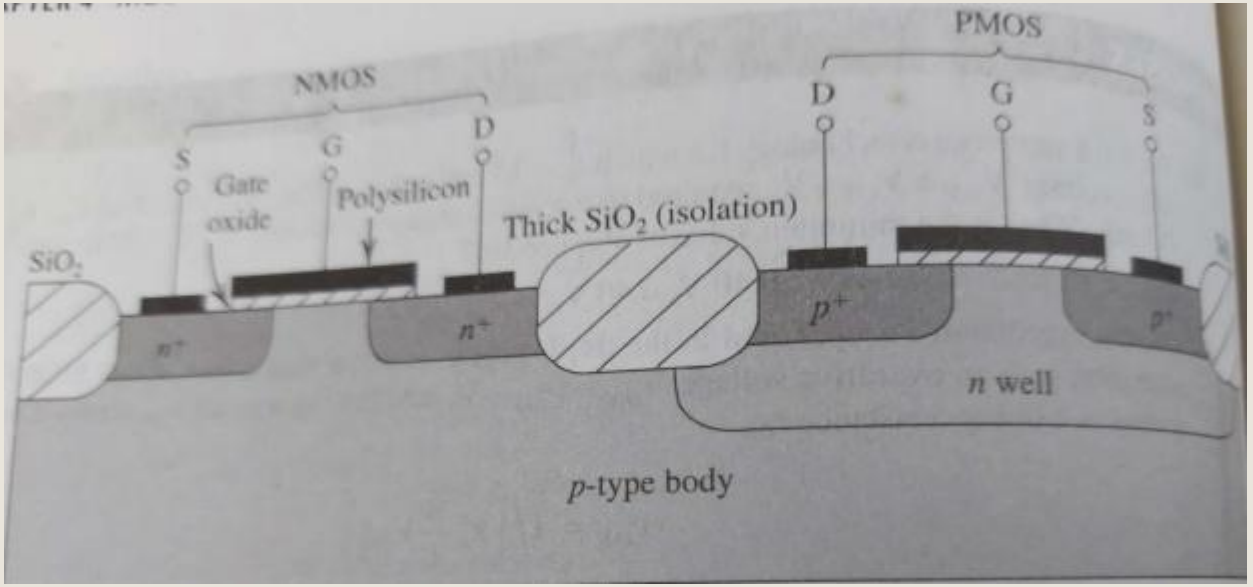
Subject Incharge: Mr. Rajesh Khatri
Associate Professor

LECTURE - 12

Year: 2020-21

MOS Transistor Applications

- MOS transistors are of two types: NMOS and PMOS.
- If we fabricate a transistor with NMOS and PMOS on same wafer, then we have CMOS (Complementary MOS).
- CMOS have many applications in electronics, specially VLSI industry.



MOS Transistor Applications

- VLSI (Very Large Scale Integration), as name suggest, large or very large number of transistors are integrated (accommodated) on a single chip.

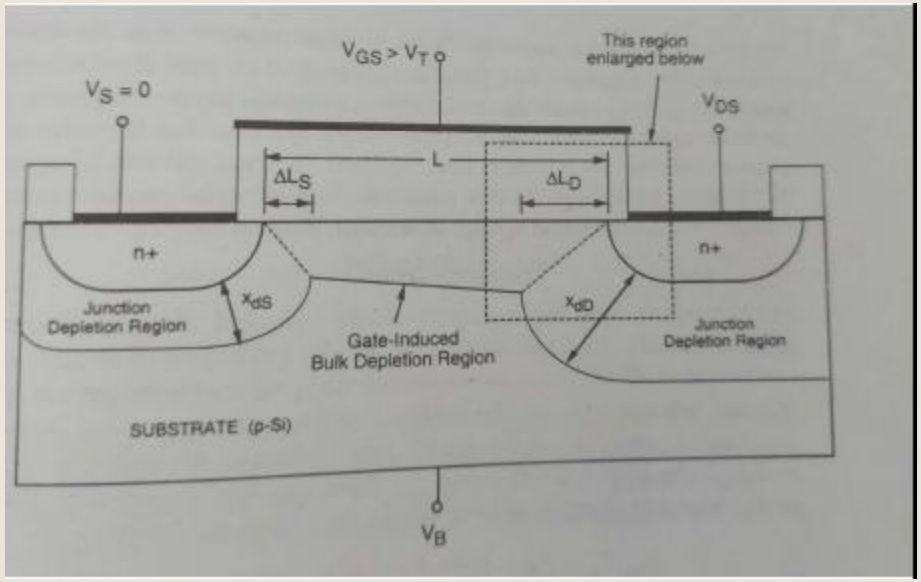
- To integrate very large (Millions/Billions) of transistors on very small may be of few mm^2 of area, it is required to reduce the physical dimensions (length, Width) of transistors.

- If we reduce channel length(distance between drain and source), the width has to be reduce accordingly for proper operation of transistor.

Short Channel Effects

- What do you mean by Short Channel in MOS?

A MOS transistor is called as short channel if its channel length is on the same order of magnitude as the depletion region thicknesses of the source and drain junctions.



i.e. if $L = X_{dS} + X_{dD}$

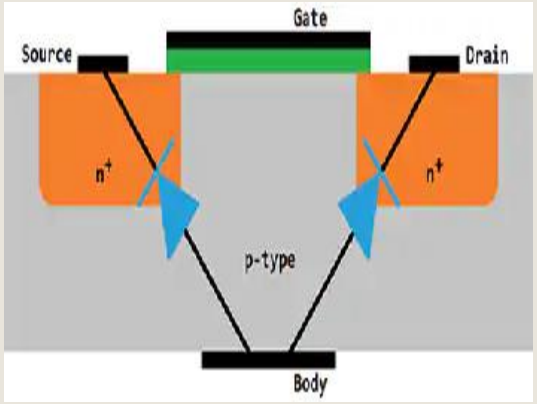
Short Channel Effects

- Although, by reducing the channel length (dimensions) of MOS, we can integrate very large number of MOS transistors on single chip. But this short channel creates lots of undesirable effects which should be taken care of before designing.

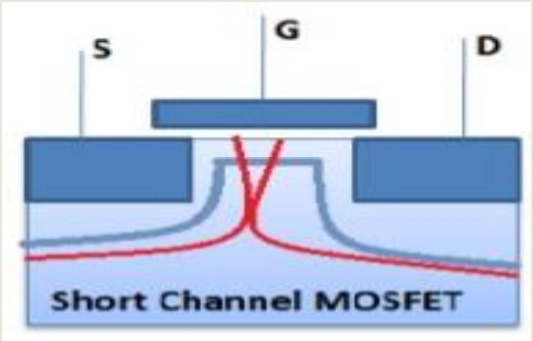
- Various short channel effects are:
  1. Drain Punch through
  2. Drain Induced Barrier Lowering (DIBL)
  3. Hot electron effect
  4. Velocity Saturation effect
  5. Impact Ionization

1. Drain Punch Through

- In NMOS; there are two PN junction diodes.
- One is between drain and body and other is between source and body.
- These both diodes are reverse biased, if we apply V_{DS}.



- As both diodes are reverse biased, if we increase V_{DS}, the depletion layers of both drain and source diodes will increase.

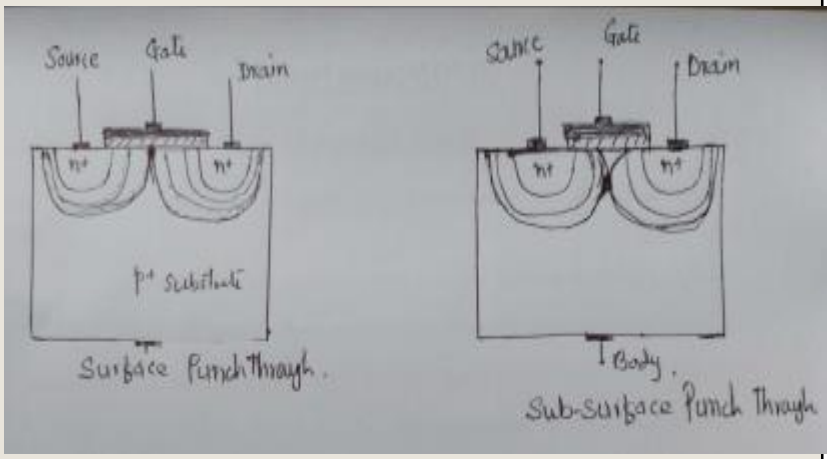


- But since drain is more reverse bias compare to source, the drain depletion layer will increase more faster than source depletion layer, if V_{DS} goes on increasing.

- If VDS is still increased, drain depletion layer will enter(Punch through) the source, hence called as Drain Punch Through.
- This effect is undesirable.

1. Drain Punch Through

- Drain Punch Through are of two types:
  1. Surface Punch Through
  2. Sub Surface Punch Through.



- Surface Punch Through: If the drain depletion layer enters source at surface (just below oxide), then it is called surface punch through.

- Sub surface Punch Through: If the drain depletion layer touches source depletion layer deep inside substrate, then it is called as sub Surface punch through.

2. Drain Induced Barrier Lowering(DIBL)

- In NMOS the drain current flows through only when $V_{GS}>V_t$ and V_{DS} is applied.
- If gate voltage is not sufficient to invert the surface i.e. $V_{GS}<V_t$, the electrons in channel face a potential barrier that blocks the flow.
- Increasing the gate voltage reduces the potential barrier and eventually, allows flow of electrons under influence of V_{GS}.
- But now in short channel MOS this becomes complicated.
- Because in short channel MOS as channel L is very small, the potential barrier is controlled by both V_{GS} and V_{DS}.
- Now if drain voltage is increased, the potential barrier in channel reduces called as Drain induced barrier lowering (DIBL), this reduction in barrier eventually allows drain current to flow, even if the $V_{GS}<V_t$.
- Thus in short channel MOS drain current flows even if $V_{GS}<V_t$ due to lowering of Barrier due to drain voltage (DIBL effect)

Its Quiz Time

https://forms.gle/LemqzZJse2zjmR217