

(1) Electron beam lithography (31)  
Used for feature size less than 1 μm.  
offers high resolution but exposure  
time is more and equipment cost  
is high.

### (6) EPI TAXY

Epitaxy means "arranged upon".  
It is the process of controlled growth  
of a crystalline doped layer of Si on  
a single crystal substrate. This method  
produces a layer of lower concentration  
than the existing one whereas diffusion  
and ion-implantation produce a layer  
at the surface that is of higher density  
than that which existed before the  
dopant was added.

The epitaxial layer formed on  
the substrate may be either n doped,  
p doped or intrinsic. P type doping  
uses bi-borane ( $B_2H_6$ ) and n type  
doping uses phosphine ( $PH_3$ ) with the  
steam of silicon tetrachloride gas  
+ Hydrogen gas.



There are 2 types of epitaxy

Homoepitaxy: Here epitaxial layer  
and the substrate are of same material  
e.g. Si formed grown on Si substrate

(2) Heteroepitaxy - When epitaxial layer and substrate are not of same material then process is called hetero-epitaxy. But the materials should have same crystalline structure.

The main epitaxial processes are

(1) Chemical vapour deposition (CVD)

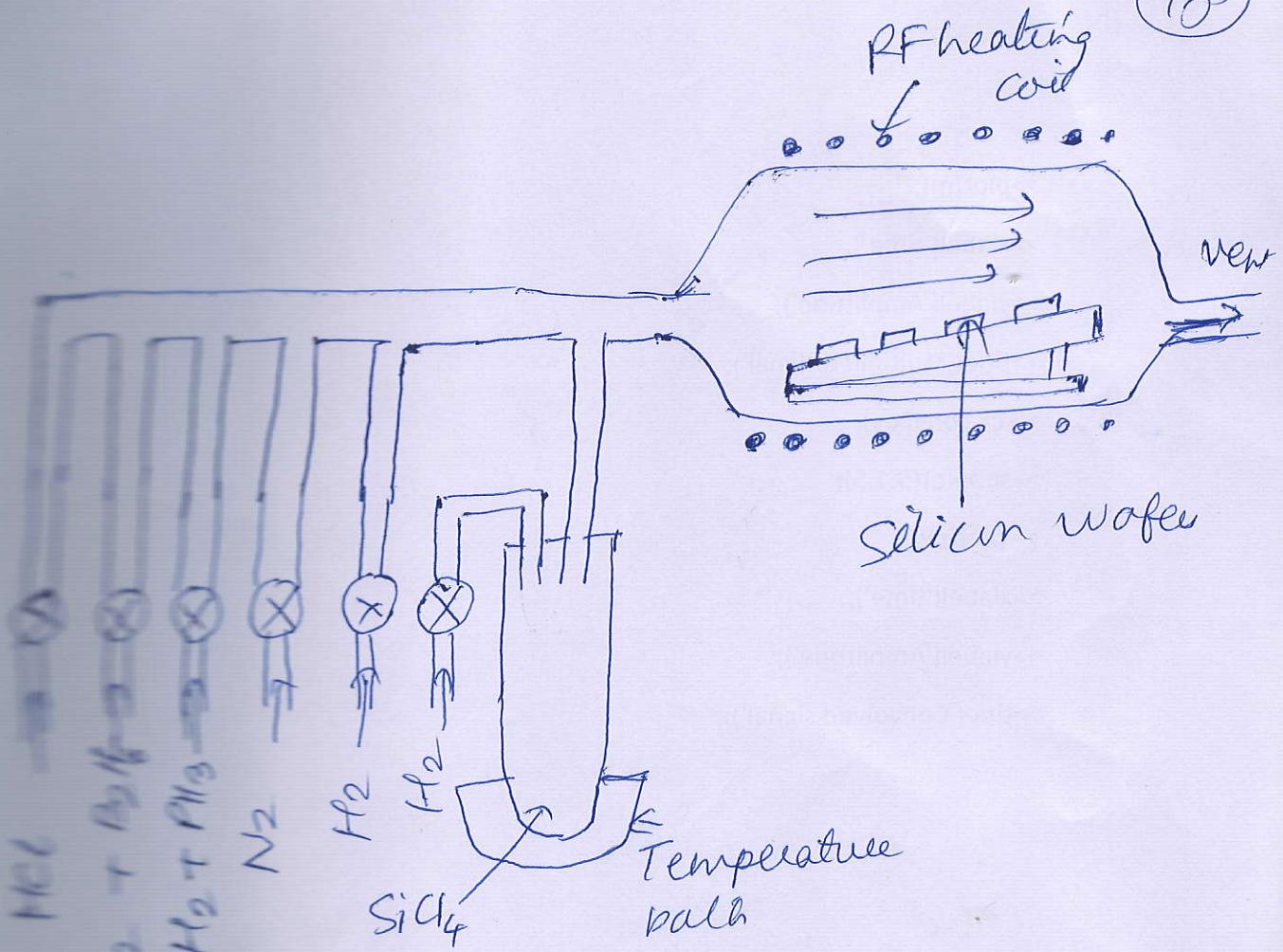
(2) Molecular beam epitaxy.

(1) Chemical vapour deposition / Vapour phase epitaxy.

In this method, the film is formed on the surface of the substrate by thermal decomposition and/or the reaction of various gaseous compounds.

In this system, Si wafers are placed in a long crucible made of graphite. The crucible is placed in a long cylindrical quartz tube, which has inlet and outlets for the gases. The tube is heated by ~~the~~ induction using the heating coils wound around the tube. Reactions are carried out at a temp. of approx.  $1200^{\circ}\text{C}$ . The high temp. is necessary so that the dopant atoms can acquire a sufficient amount of energy to allow them to move into the crystal to form covalent bonds and become extension of a single crystal.

(B3)



## (ii) MOLECULAR BEAM EPITAXY:

It is based on evaporation. The film is evaporated and deposited one layer at a time. Evaporation of silicon and other dopant is carried out under ultra high vacuum (UHV) pressures. Throughput and growth rates are very slow. Temperature is between 600°C to 900°C. It is an expensive process.

## G) Metallization and Interconnections. (34)

After all the fabrication steps of an IC are completed, it is necessary to provide metallic interconnections for the IC and external connections to the IC.

~~Interconnection~~ should have low resistance to minimize both the voltage drops on the lines as well as the capacitance between the lines so as to reduce delay times. The connection must also make ohmic contacts to semiconductors in the devices such as P and N regions of a P-N junction diode. An ohmic contact is one that exhibits a very low resistance allowing currents to pass easily in both direction through the contact.

Aluminium is used because:

- (i) it is a good conductor.
- (ii) it can form mechanical bonds with silicon.
- (iii) it can form low resistance ohmic contacts with heavily doped n type and p type silicon.
- (iv) it can be easily etched.
- (v) not expensive.
- (vi) it is easy to evaporate.

~~Metallization~~: is a process in which

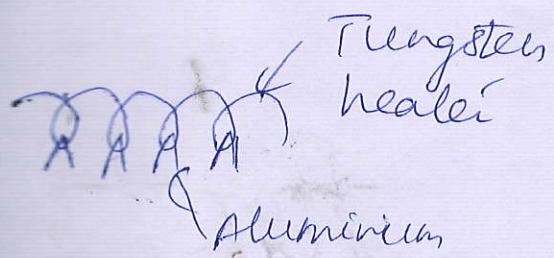
thin layer of metal is formed.

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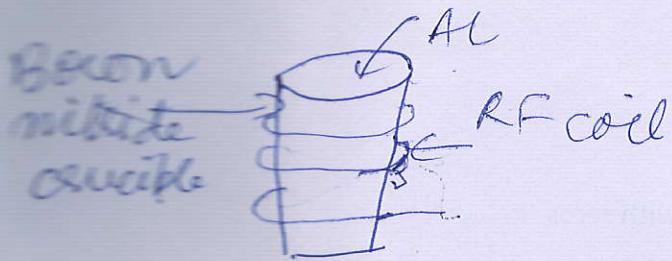
Process for depositing aluminium  
on Si substrates

### RESISTANCE HEATING

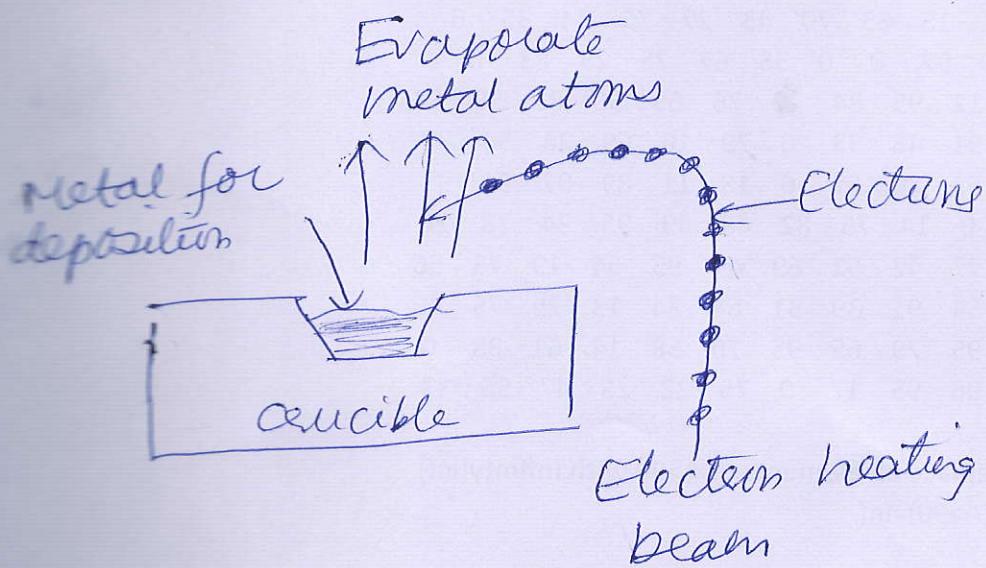
In this process, the source of heated element and the silicon substrate are located in an evacuated chamber. The source is a small piece of aluminium, attached to a coil of tungsten. The heated element with a high melting point remains solid while the aluminium is vaporized. The aluminium atoms travel to the substrate where they condense, depositing an aluminium layer on the surface of the Si. A photolithographic masking and etching method is used to remove the metal from the regions where it is not wanted ...



(ii) In another method, the evaporation source is kept in a boron nitride crucible is heated by radio frequency induction. High deposition rates are possible but crucible may contaminate the metal.



## (B) Electron Beam heating



In this process, aluminium in a crucible is placed into a vacuum chamber together with the substrate. The aluminium is subjected to a high intensity electron beam formed by an electron gun, which vaporizes the aluminium. This causes aluminium to travel to the wafer. By the use of mask and photolithography the aluminium is deposited on the identified regions on the Wafer surface.

## (c) Sputtering:

In this process the material to be deposited is placed in a container maintained at low pressure in the vicinity of the substrate. The material to be

deposited is labelled as cathode or target while the anode is the substrate. A DC or a radiofrequency high voltage is applied between anode & cathode. The high voltage ionizes the inert gas in the chamber. The ions are accelerated to the cathode, (the anode is usually grounded) where by impact with aluminium target, atoms of aluminium are vaporized. A gas of aluminium atoms is generated and deposited on the surface of the wafer.

Following the deposition of aluminium, the silicon wafers are placed in a furnace to solidify the connections so that low resistance metallic contacts are made.

(2) Interconnections: between the elements of an ICs are made by aluminium lines having a thickness of about  $0.5\mu m$ . They are laid on top of  $SiO_2$  layer which covers the surface of the wafer. By using photolithography, openings are made in  $SiO_2$  so that the aluminium layer is connected to the Si or to the ohmic contact on the Si. The interconnecting lines terminate at aluminium pads (bonding pads) from which connections to the outside are made.

## Testing:

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After the wafer of monolithic circuits has been processed and the final metallization pattern defined, it is placed in a holder under microscope and is aligned for testing called multiple point probe. The probe contacts the various pads on an individual circuit and a series of tests are made to verify the electrical properties of the device in a very short time. After all the circuits are tested the wafer is removed ~~and~~ from the testing machine sawed between the circuits and broken apart. Then each die that passed the test is picked up and placed in the package.

## Bonding:

- (i) In first step the back of the die is mechanically attached to an appropriate mount mechanism such as ceramic substrate, multilayer ceramic package or metal lead frame.
- (ii) In the second step the bond pads on the circuit side of the die are connected by wires to the package

## Packaging:

(39)

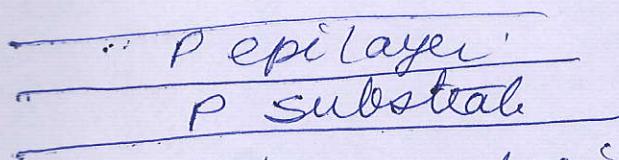
The device is packed in a suitable medium that can protect it from moisture and contamination. Bonds and other elements must be protected from corrosion and mechanical shocks.

The ICs are mounted in a package with many output leads. The package is formed by applying a ceramic or plastic case.

## DUAL WELL / TWIN TUB PROCESS (40)

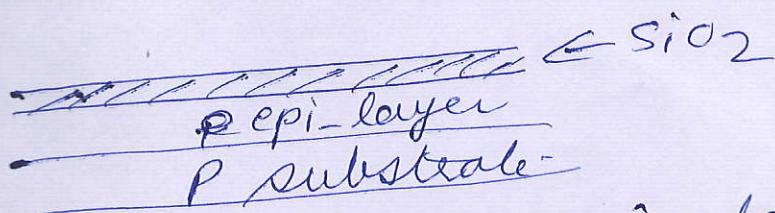
Here both p well and n well for NMOS & PMOS transistors respectively are formed on the same substrate.

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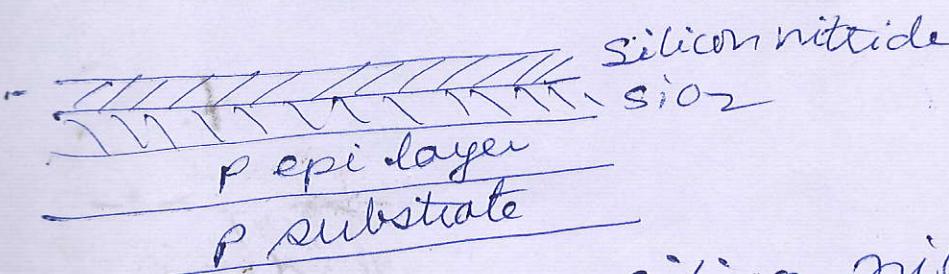
The starting material for the process is  $p^+$  substrate with epitaxially grown p layer which is also called epi layer.

Step 1



A thin layer of  $\text{SiO}_2$  is deposited which will serve as pad oxide. (pad oxide - is used as a buffer layer for reducing stress)

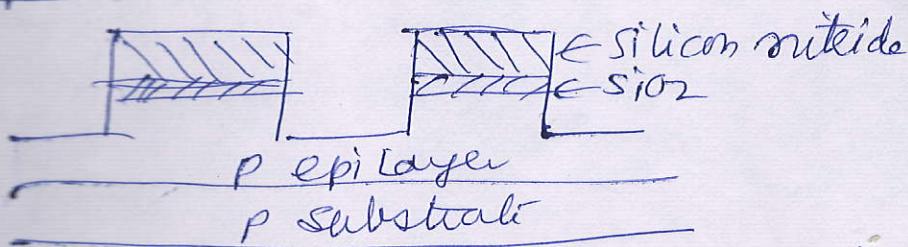
Step 2



A thicker sacrificial silicon nitride layer is deposited ~~which acts~~ by chemical vapour deposition (sacrificial - acts as a buffer layer which can be later removed)

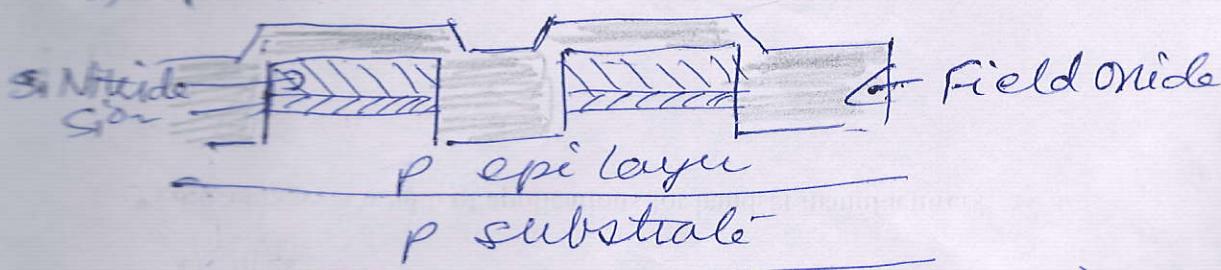
### (3) Step 3

(4)



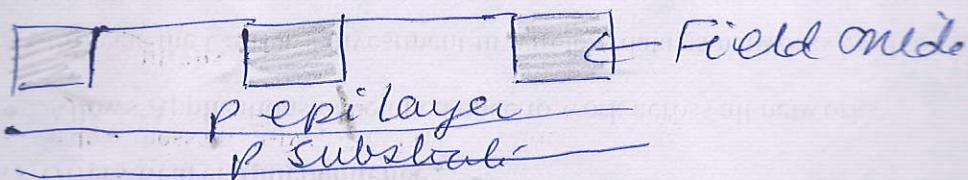
A plasma etching process is used to create trenches used for insulating devices.

### (4) Step 4



The trenches are filled with SiO<sub>2</sub> which is called field oxide (field oxide is formed to passivate and protect semiconductor surface)

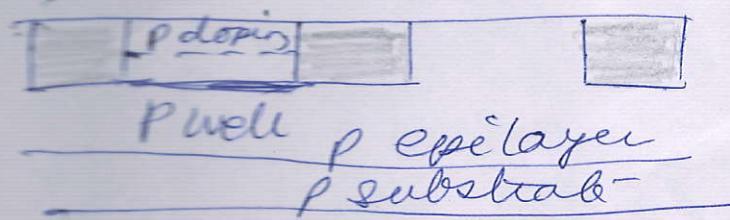
### (5) Step 5



To provide flat surface chemical mechanical planarization is performed and sacrificial nitride and pad oxide is removed (planarization - increasing flatness)

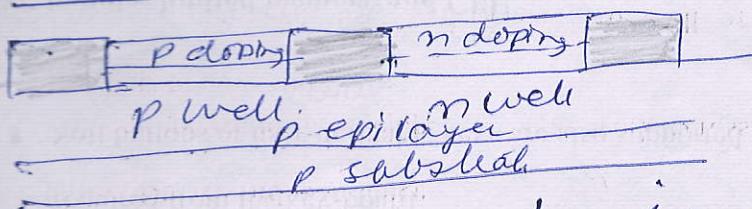
## Q. Step 6

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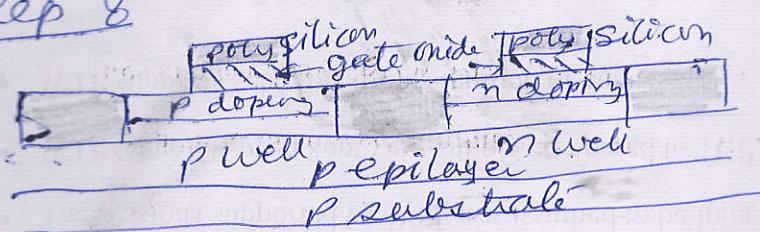
The p well mask is used to expose only the p well areas. After this implant an annealing sequence is applied to adjust well doping. This is followed by second implant to adjust threshold voltage of NMOS transistor.  
(annealing - heat treatment)

## Q. step 7



The n well mask is used to expose only n well areas. After this implant an annealing sequence is applied to adjust well doping. This is followed by second implant to adjust threshold voltage of PMOS transistor.

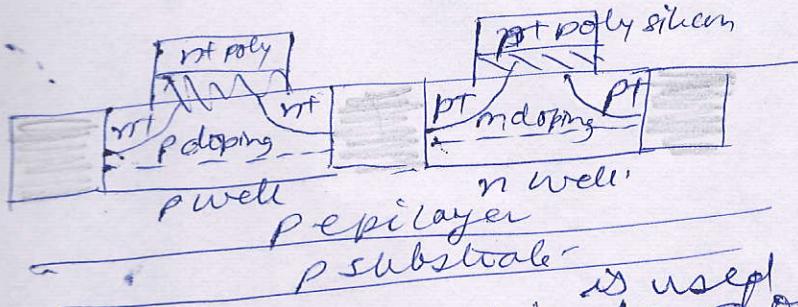
## Q. Step 8



A thin layer of gate oxide and polysilicon is chemically deposited and patterned with the help of polysilicon mask.

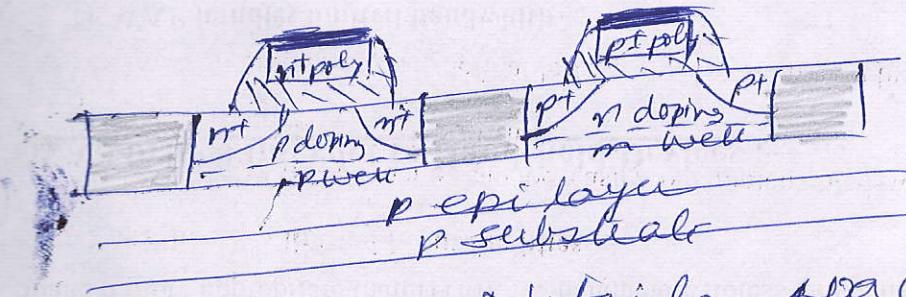
### (9) Step 9

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Ion implantation is used to dope the source and drain regions of PMOS (p<sup>+</sup>) and NMOS (n<sup>+</sup>) transistors. This will also form n<sup>+</sup> polysilicon gate and p<sup>+</sup> polysilicon gate for NMOS and PMOS transistors respectively.

### (10) Step 10



Nitride or Nitride spaces are formed by chemical vapour deposition (Spacers) to protect the gate & underlying gate-oxide from subsequent processing.

### (11) Step 11

In this step contact or holes are etched, the metal is deposited and patterned. After the deposition of last metal layer final passivation or overglass is deposited.

Coverglass is protective coating over the entire chip.)

## DETAILED SYLLABUS      Module -5

Introduction, Advantages and limitations of IC, IC classification:

- (i) Fabrication Techniques- Monolithic, Hybrid and thin and thick film ICs and their comparison.
- (ii) Functionality- Linear and Digital ICS.
- (iii) On the basis of size : SSI, MSI, LSI, VLSI, ULSI etc.
- (iv) On the basis of device implemented Bipolar and Unipolar.  
Semiconductors used in fabrication of ICs and devices Ge, Si, GaAs etc. Processes involved in IC fabrication
  - Material preparation, crystal growth and wafer preparation
  - Czochralski process.
  - Processes in wafer fabrication –
- (i) Oxidation – thermal oxidation, vapour phase or chemical vapour deposition (CVD), plasma oxidation.
- (ii) Etching – Wet etching, reactive plasma etching, reactive ion etching .
- (iii) Diffusion - Preposition and drive in
- (iv) Ion implantation – advantages and disadvantages over diffusion.
- (v) Photolithography – Photo- mask generation, lithography, x-ray lithography, Electron beam lithography.
- (vi) Epitaxy – Homoepitaxy, Hetroepitaxy, chemical vapour deposition, vapour phase epitaxy and molecular beam epitaxy.
- (vii) Metallization and interconnections – Advantages of Aluminium and ways of depositing aluminium on substrate – resistance heating, electron beam heating, sputtering.  
Testing, bonding, packing, Dual well or twin tube process.