



Shri G. S. Institute of Technology and Science, Indore

END-SEMESTER EXAMINATION DECEMBER 2020

B.E./ B.Tech./B. Pharm/M.Pharma/M.E./ M.Tech/M.C.A./ M.B.A./M.Sc.

(For use in all exams as First page of Answer sheets. All entries must be filled. See www.sgsits.ac.in for instructions.)

Enrolment No.

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Branch: Electronics Telecomm. Engg Email: gs0801ec191010@sgsitsindore.in

Subject Code EC25016

Date: 08-01-2021

Subject Nomenclature Electronic devices

Total Number of Pages
(fill this at the end of exam)

25

I have read all the instructions given in website and provided by Exam office for online examination and accept.

Name with surname: Anant Dev Srivastava

Anant Dev

Signature (as per Institute's record)

Instructions : (read detailed instructions from Institute's website <http://www.sgsits.ac.in>)

30 min before Examination

1. This page must be duly filled with correct entries using Blue/Black pen only. Overwriting is not allowed.
2. Print required number of A4 size blank pages. EACH PAGE MUST BE NUMBERED at bottom right corner of all pages. Also write Enrollment number and put signature on all pages..

10-15 min before Examination

1. Login with your email id gsxxxxxx@sgsitsindore.in
2. Enter the classroom through meet link.
3. Download the question paper (For MCQ type wait for the start of exam).

During Examination

1. The password for the question paper will be disclosed 2 minutes before the start of examination
2. In case of any doubts you may talk to the invigilator via Google Meet. Switch ON mic and CAMERA before raising any questions.

End of Examination

1. Arrange all papers in series with front page at top. Scan the front page first and then all written material in serial order. Use any PDF file generation facility, including "document scanner" etc.
2. RENAME PDF file as "enrollment number-subject code". (example 0801EC12345-MT12001.PDF)
3. Students are required to read all instructions and guideline published in institute's web site for the use of G-Suite

IMPORTANT after Examination

1. After scanning the answer sheet, staple all original pages at the three marked locations with front page at the top. Keep the answer sheet in safe location or in an envelope.
2. Once all exams are over, dispatch all original answer sheets in a single envelope by registered post to the following address within 24hrs from your last exam: To, Exam Office, Shri G.S. Institute of Technology & Science, 23 Sir M. Visvesvaraya Marg, Indore, Madhya Pradesh 452003. The envelope shall be superscribed with "Dec. 2020 Exam: Enrolment No. _____".
3. Keep softcopies of answer sheets as PDF file at safe place for 2 months from the date of exam.



Q1 (a) The minimum Energy required to excite an electron from the ground state of an atom to any excited state is called excitation energy.
Exciting an electron in an atom from its ground state (i.e. $n=1$ state) to infinite state (i.e. $n=\infty$ state) is called ionization.

(b). Mobility is the measure of how quickly an electron can move through a metal or semi-conductor in presence of electrical field.

Mobility describes the relation between drift velocity of electron or holes and an applied electric field in a solid.

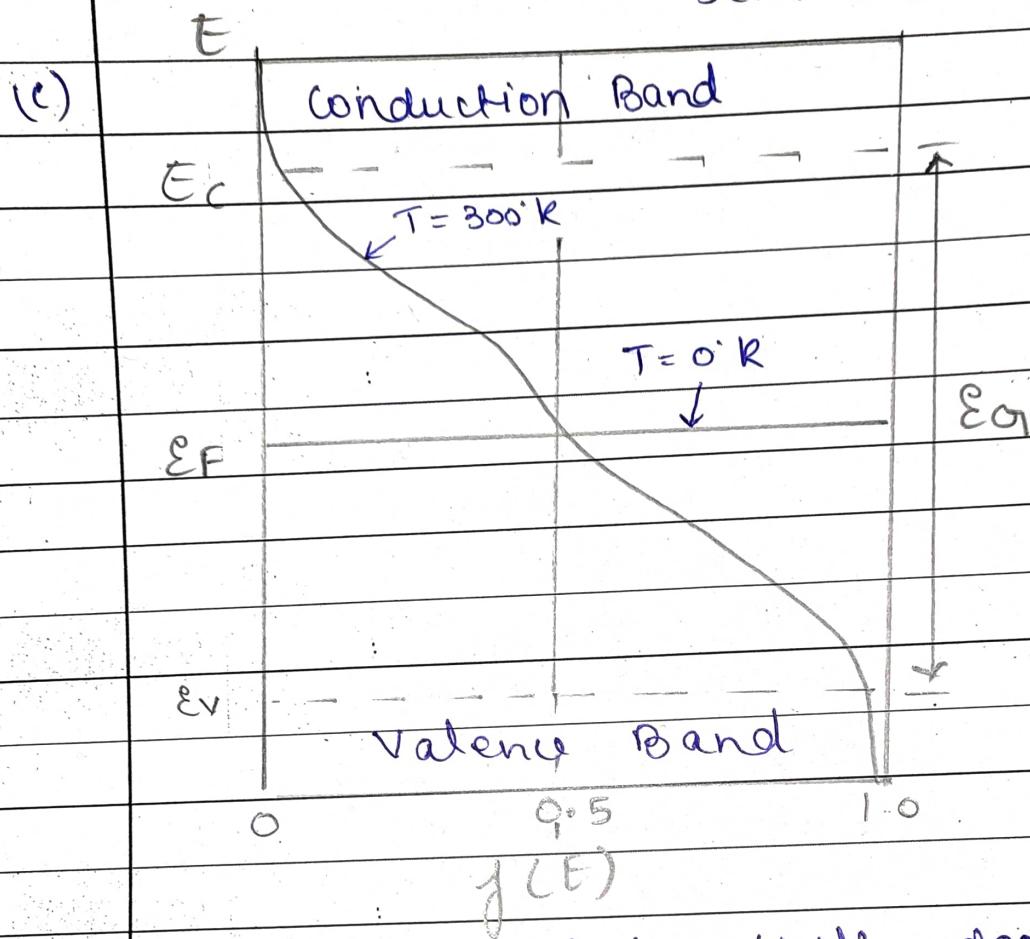
$$V_d = \mu \mathcal{E}$$

V_d = drift velocity, \mathcal{E} = electric field
 μ = denotes mobility tensor.

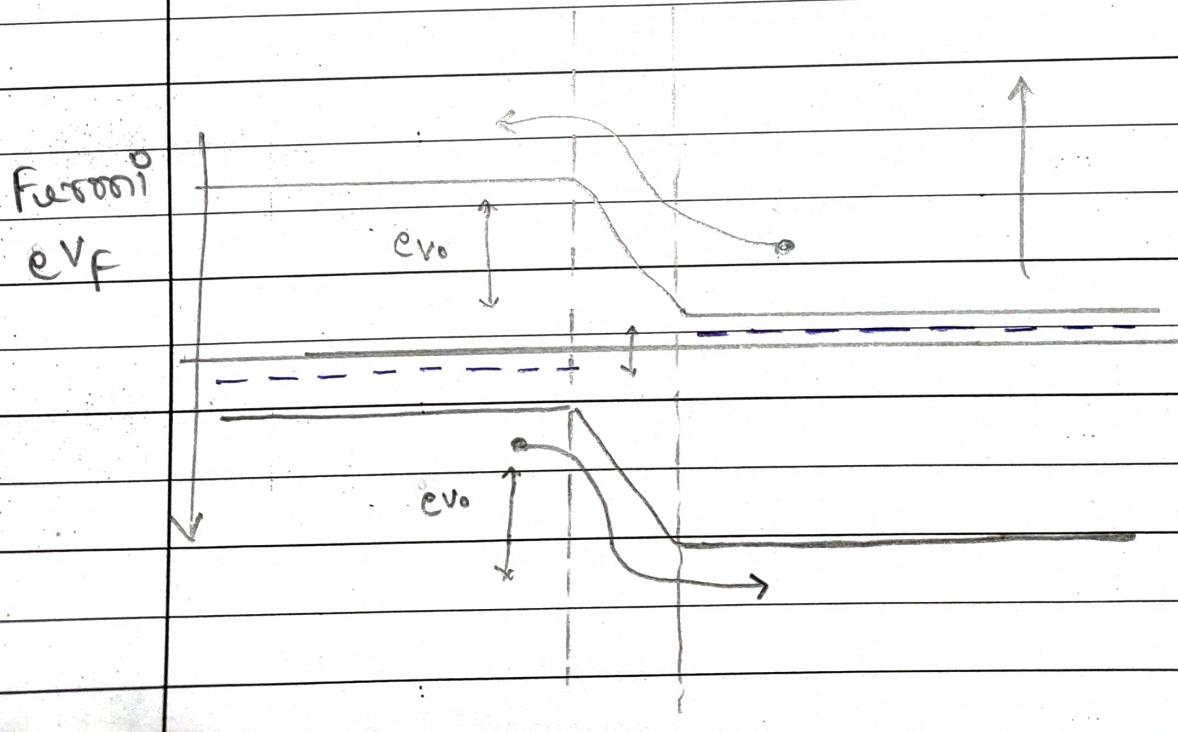


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→ Fermi level in intrinsic semi-conductor.

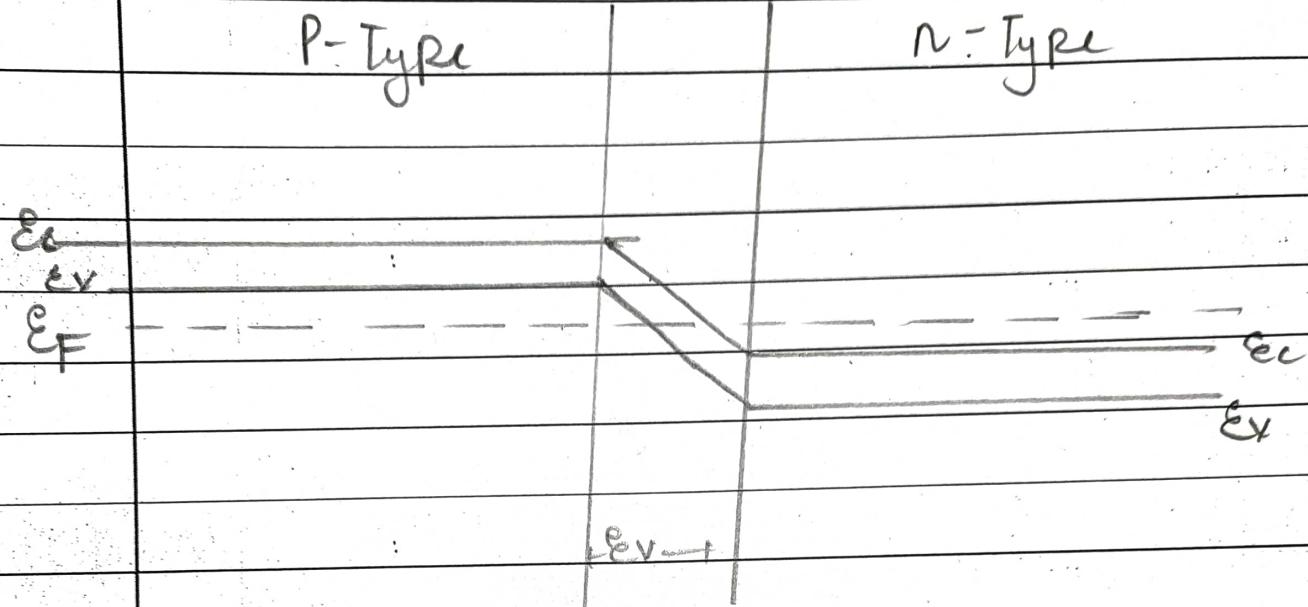


→ Fermi level in lightly doped.



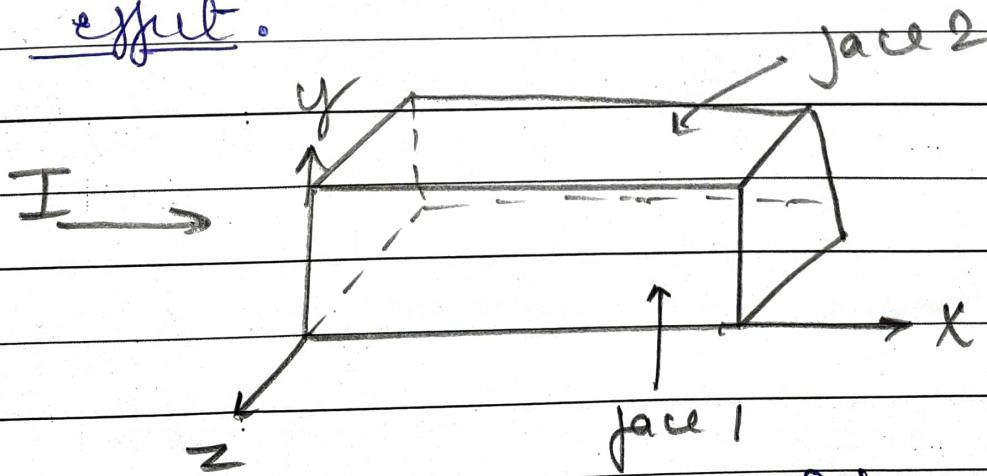


Fermi level for heavily doped



Hall effect

- (d). When a specimen of metal or semiconductor carrying a current 'I' is placed in a transverse magnetic field B , then an electric field is introduced in the direction perpendicular to both I and B. This Phenomenon is called Hall effect.





In equilibrium state, the electric field intensity E due to Hall effect must exert a force on the carrier which just balances the magnetic force.

$$ce = Bev$$

v = drift velocity

$$Te = Bv \quad \text{--- (1)}$$

c = charge on hole

E = Electric field intensity

B = Magnetic field intensity

Let V_H = hall voltage

$$E = \frac{V_H}{d}; V_H = Ed$$

Putting ' E ' from eq (1)

$$\boxed{V_H = Bvd} \quad \text{--- (2)}$$

d = distance between

face 1 and 2.

w = width of element.

current density $J = \frac{I}{A}$

$$J = \frac{I}{wd} = J = \rho v \Rightarrow \rho v = \frac{I}{wd}$$

$$\boxed{v = \frac{I}{\rho wd}} \quad \text{--- (3)}$$

ρ = charge density.



from ② and ③,

$$V_H = \frac{BI}{SW} \quad \boxed{④}$$

now, R_H = hall coefficient

$$R_H = \frac{1}{\Phi} ; \quad \boxed{R_H = \frac{V_H W}{B T}}$$

Application :-

- ① To determine whether semiconductor is p-type or n-type
- ② parameter like electron or hole concentration and mobility can be measured.
- ③ used to measure the flux density.



Q2. (a) The resistance offered by a p-n junction diode when it's connected to a DC circuit static resistance.

$$R_f = \frac{\text{DC voltage}}{\text{DC current}}$$

The dynamic resistance is the resistance offered by the p-n junction diode when AC voltage is applied.

$$r_f = \frac{\text{change in Voltage}}{\text{change in current}}$$

(b). In a forward Biased diode, the transition capacitance exist.

$$C_T = dQ/dV$$

C_T = Transition capacitance

dQ = change in electric charge

dV = change in voltage

Also, Diffusion capacitance occur in forward Biased pn.



$$C_D = dQ/dV$$

C_D = diffusion capacitance

dQ = Change in number of minority carriers stored outside depletion region.

dV = change in voltage applied across diode.

(c) Expression for Barrier Potential

* Expression for potential diff. in diode $\Rightarrow V_{B1} = V_T \ln \frac{P_1}{P_2}$

Let V_B = Barrier Potential at the junction there is an ~~abrupt~~ abrupt change in concentration of holes from P_p to P_n .

$$\text{So, } P_1 = P_p = N_A \quad \& \quad P_2 = P_n$$

$$\therefore V_B = V_T \ln \left(\frac{N_A}{P_n} \right)$$

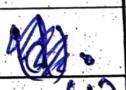
$$\text{But } P_n = \frac{n_i^2}{n_n}$$



$$V_B = V_T \ln \left(\frac{N_A}{n_i^2 / n_n} \right)$$

but $n_n = N_D$

$$\therefore V_B = \left\{ \ln \frac{N_A \times N_D}{n_i^2} \right\} V_T$$

(e)  → clipper circuits :-

(1)

The circuit with which the waveform is shaped by removing or clipping a certain portion of the input signal voltage above or below a certain level.

uses :- Digital computer, radar.

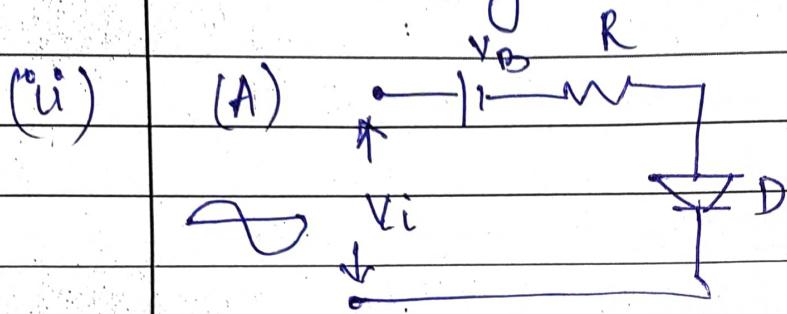
Two types.  series clipper
shunt clipper.

→ Clampers :-

The circuit with which the waveform can be shifted in such a way that a particular part of it



say positive or negative peak is shifted voltage level is called clamping circuit or simply clamp.



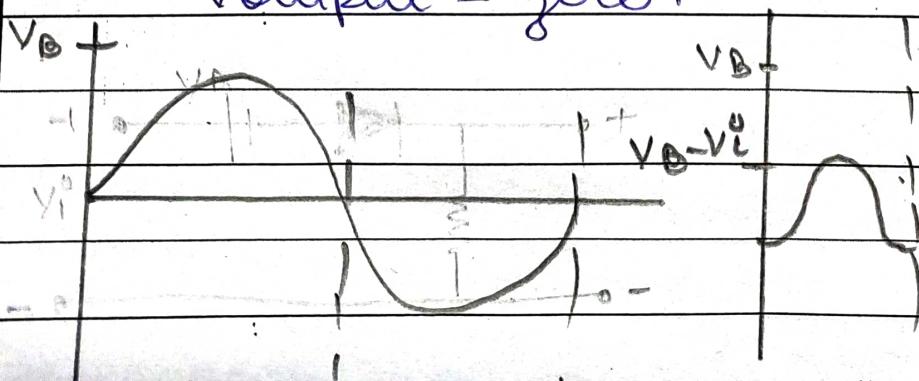
for the first positive half cycle

case(1) when $V_B > V_i$ the diode is open so, the output is zero.

case(2) when $V_i > V_B$ diode is short circuit
 $V_0 = V_i - V_B$

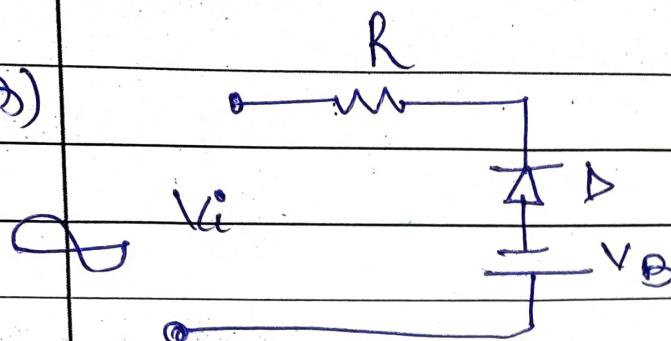
→ for negative half cycle diode is always reverse biased, hence the circuit will be open circuit

$$V_{\text{output}} = \text{zero.}$$





(B)



for positive half cycle diode is always reverse Bias

$$V_O = V_i^o$$

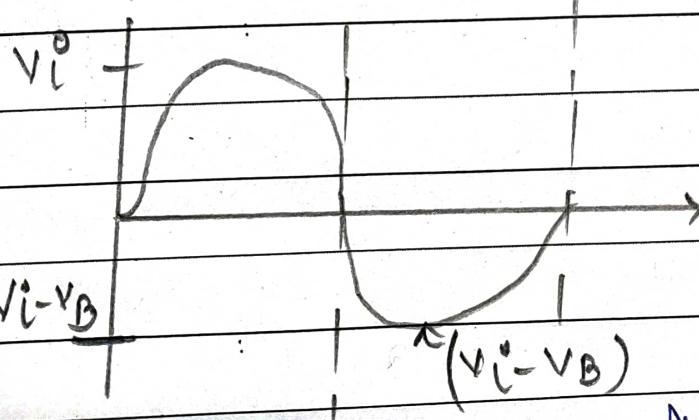
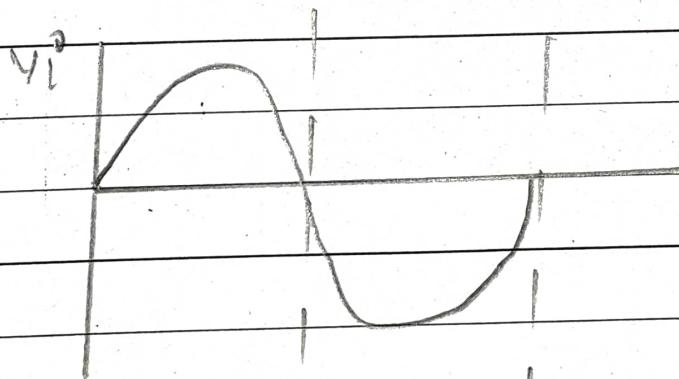
① for negative half cycle

$V_B > V_i^o$ - open circuit

$$V_O = V_B$$

② when $V_i^o > V_B$ - forward Bias
~~short circuit~~ short circuit

$$V_O = V_i^o - V_B$$





Q3(a)

- i) Collector is more wider than emitter and base because it has to handle more power than both and large surface area is required for heat dissipation.
- ii) Base is made thin, so that maximum current can flow from emitter to collector with recombination of holes.
- iii) Depletion layer width is more at collector junction because there it is lightly doped than emitter.
- iv) Collector current is slightly less than emitter current because some of the electron combines with hole in base region.



(b)

$$I_{CBO} = 0.2 \mu A$$

$$I_{CEO} = 18 \mu A$$

~~Working of Transistor~~

$$\text{Now; } I_{CEO} = (1 + \beta) I_{CBO}$$

$$I_{CEO} = I_{CBO} + \beta (I_{CBO})$$

$$\beta = \frac{I_{CEO} - 1}{I_{CBO}}$$

$$\beta = \frac{18 - 1}{0.2} = 89$$

$$\text{Now, } I_{CEO} = (1 + \beta) I_{CBO}$$

$$= \frac{I_{CBO}}{1 - \alpha}$$

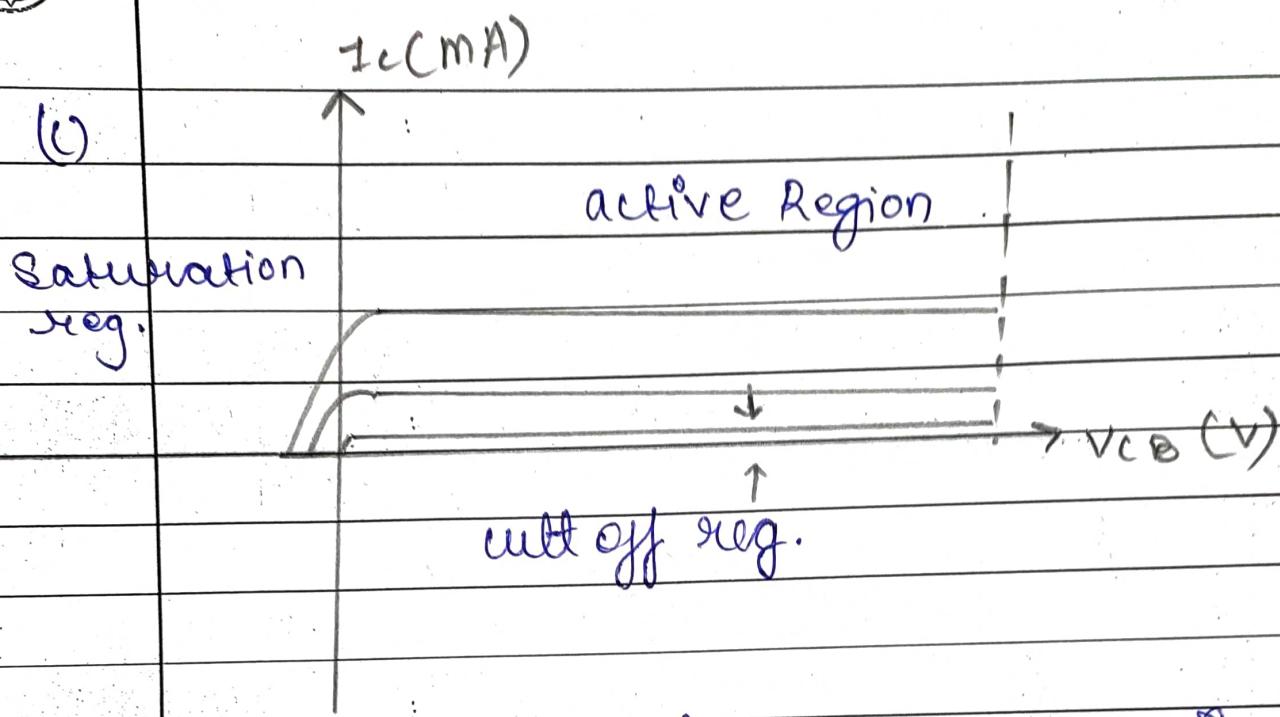
$$\alpha = \frac{1 - I_{CBO}}{I_{CEO}} = \frac{1 - 0.2 \times 10^{-6}}{18 \times 10^{-6}}$$
$$= 0.988$$

\rightarrow ~~Given~~ $\alpha = 0.988$ and $\beta = 89$

(c) PTO.



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Emitter current can be obtained from given graph

$$I_c = \alpha I_e + I_{cbo}$$

I_{cbo} very small

$$I_c \approx \alpha I_e$$

$$(\alpha = 0.95 - 0.98)$$

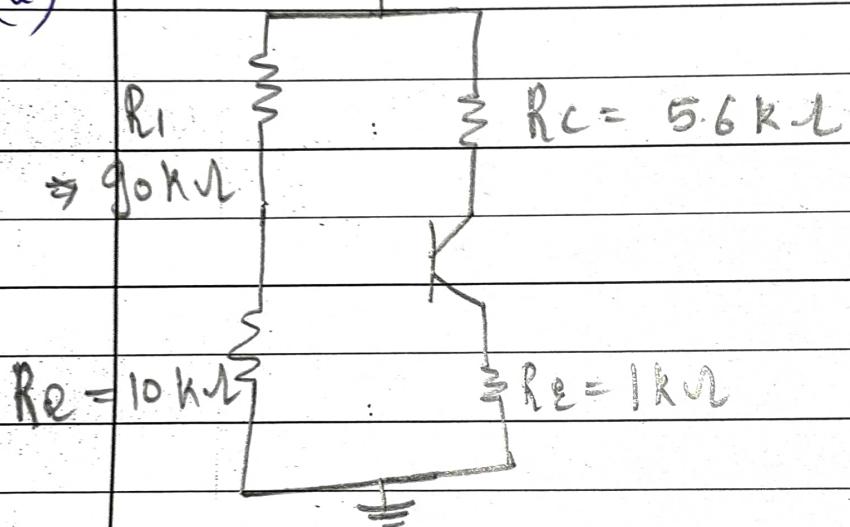
so; $I_c \approx I_e$

(d) \rightarrow PTO
(e)



(e). i) The self destruction of unstabilized transistor due to excess power dissipation in form of heat energy is called thermal runaway.

(ii)



$$R_{TH} = \frac{R_1(R_2)}{R_1 + R_2} = \frac{90 \times 10}{100} = 9 \text{ k}\Omega$$

$$V_{TH} = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{22.5 \times 10 \times 10^3}{100 \times 10^3}$$

$$\boxed{V_{TH} = 2.25 \text{ V.}}$$

$$I_C = \frac{B(V_{TH} - V_{BE})}{R_{TH} + (B+1) R_E}$$

$$= \frac{55(2.25 - 0.7)}{9 \times 10^3 + 56 \times 1 \times 10^3}$$

$$I_C = \frac{55 \times 1.55}{65 \times 10^3} = 1.311 \text{ mA} = I_C$$

$$I_B = \frac{I_C}{B} = \frac{1.311}{55} = 0.023 \text{ mA}$$

$$I_B = 23.8 \mu A$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$22.5 - 1.311 \times 10^{-3} (5.6 + 1) \times 10^3$$

$$V_{CE} = 13.84 \text{ V}$$

$$\text{stability factor} = \frac{(B+1)(R_{TH} + R_E)}{R_{TH} + (B+1) R_E}$$

$$= \frac{55(10) \times 10^3}{65 \times 10^3} \Rightarrow [S = 8.46]$$



Q4 (a) On increasing V_{dd} or V_{ds} depletion layer increases, if V_{ds} is increased to a level where it appears to touch each other, this condition is called pinch off, this particular voltage is called pinch off voltage.

The ~~cut off~~ cut off voltage to turn a transistor off is applied to the gate source region of FET Transistor. It is the particular gate source voltage where the JFET acts like.

(b)

JFET

MOSFET

- ① it only operates in the depletion mode
- ② it has less impedance than MOSFET
- ① it operates in both depletion and enhancement
- ② it offers higher input impedance than

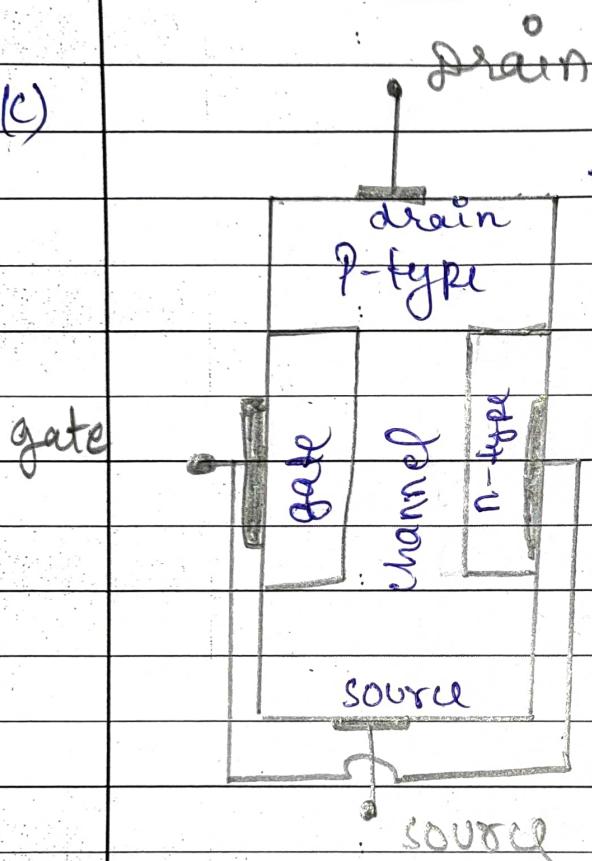
Front Dev. FET.



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- ⑤ It is mainly used in low noise application. Used in high noise application.

(c)



→ A JFET consists of a p-type silicon base/ channel, containing two heavily doped n-region, which form the PN junction.

→ P channel JFET :-

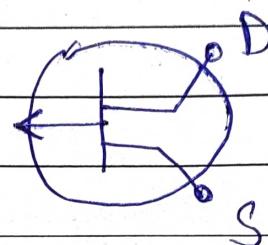
Both the N region are connected internally and a single wire is taken out in the form of terminal called gate (G). The electrical connections are made to both



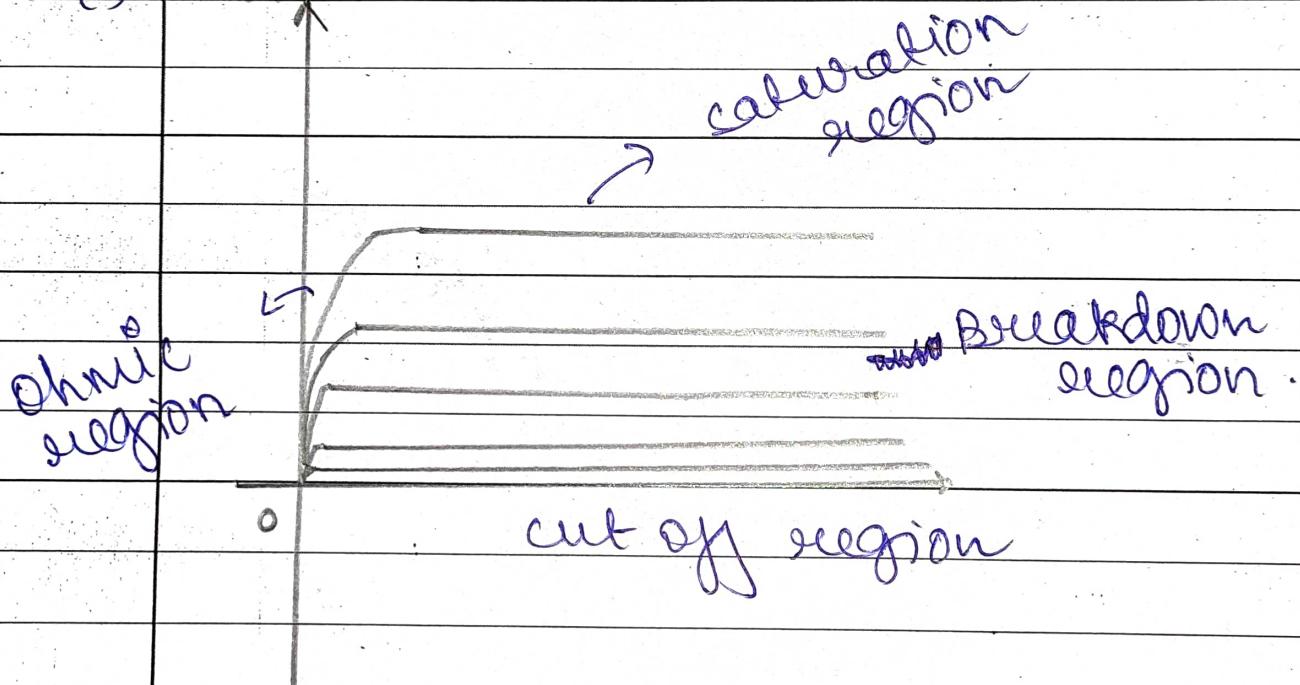
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ends of the p type semiconductor
and are taken out in the
form of 2 terminal called drain (D)
and source (S)

Symbol -



(d) (i) I_D (mA)



① Ohmic Region = The region where I_D and V_{DS} are proportional. I_{DS} increases with an increase in the value of V_{DS} .



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(2)

Cut off region = The region in which the MOSFET will be off as there will be no current flow through it when the MOSFET behaves like open switch.

(3)

Saturation region = The MOSFET have their I_D constant inspite of an increase in V_{DS} and once V_{DS} exceeds the value of pinch off voltage V_p .

(4)

Breakdown Reg = Region where V_{DS} increase excessively, & hence I_D goes beyond breakdown value.

(5)

$$I_{DSS} = 8.4 \text{ mA}$$

$$V_p = -3 \text{ V}, V_{GS} = -1.5 \text{ V}$$

$$J_D = ?$$

$$J_D = J_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

$$J_D = 8.4 \text{ mA} \left(1 - \frac{-1.5}{-3} \right)^2$$

$$J_D = 8.4 \left(1 - 0.5 \right)^2 = 2.1 \text{ mA}$$

$$J_D = 2.1 \text{ mA}$$



$$g_m = \left| \frac{\partial I_p}{\partial V_{DS}} \right| \Rightarrow \frac{I_p}{V_{DS}} = \frac{2 \cdot 1mA}{-1.5}$$

$$g_m = 1.4 \times 10^{-3} \text{ mho.}$$

(a) i) It is used for surface passivation which is nothing but creating protective SiO_2 layer on the wafer surface, it protects the junction from moisture and other atmospheric contaminations.

ii) SiO_2 acts as the active gate electrode in MOS device.

iii) it provides electrical isolation of multi-level metallization in VLSI.

(b) In a diffusion process the mask has to withstand high temperature, however ion implantation process the wafer is not intentionally heated.



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for moderate doses, the temperature of the wafer would not increase substantially above room temperature. So, it is possible to use resist to mask ion implantation.

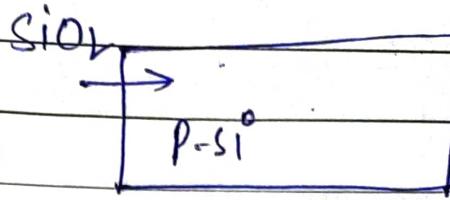
(C). Lithography:- It is the process

in which the pattern generated on the photomask is transferred or imaged on the wafer covered photoresist.

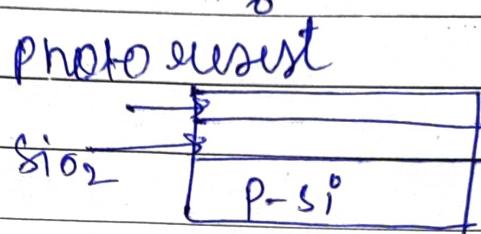
To transfer the pattern the wafer is ~~not~~ coated with light sensitive material called photoresist.

diagram - (PTO)

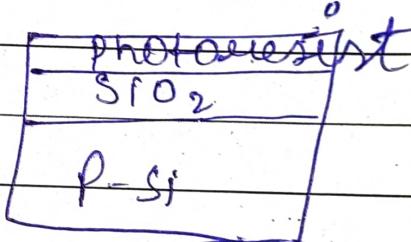
(a) Psi substrate
oxide film



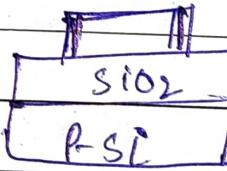
(b) Photoresist applied



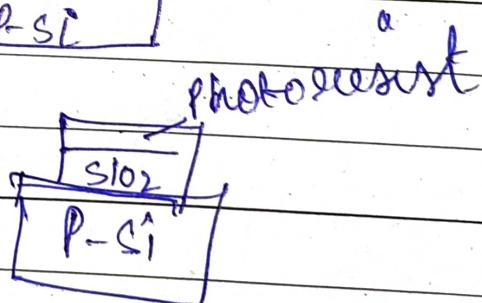
(c) Mask placed



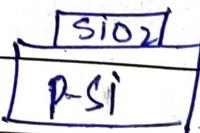
(d) Photoresist etched away.



(e) SiO2 etched away



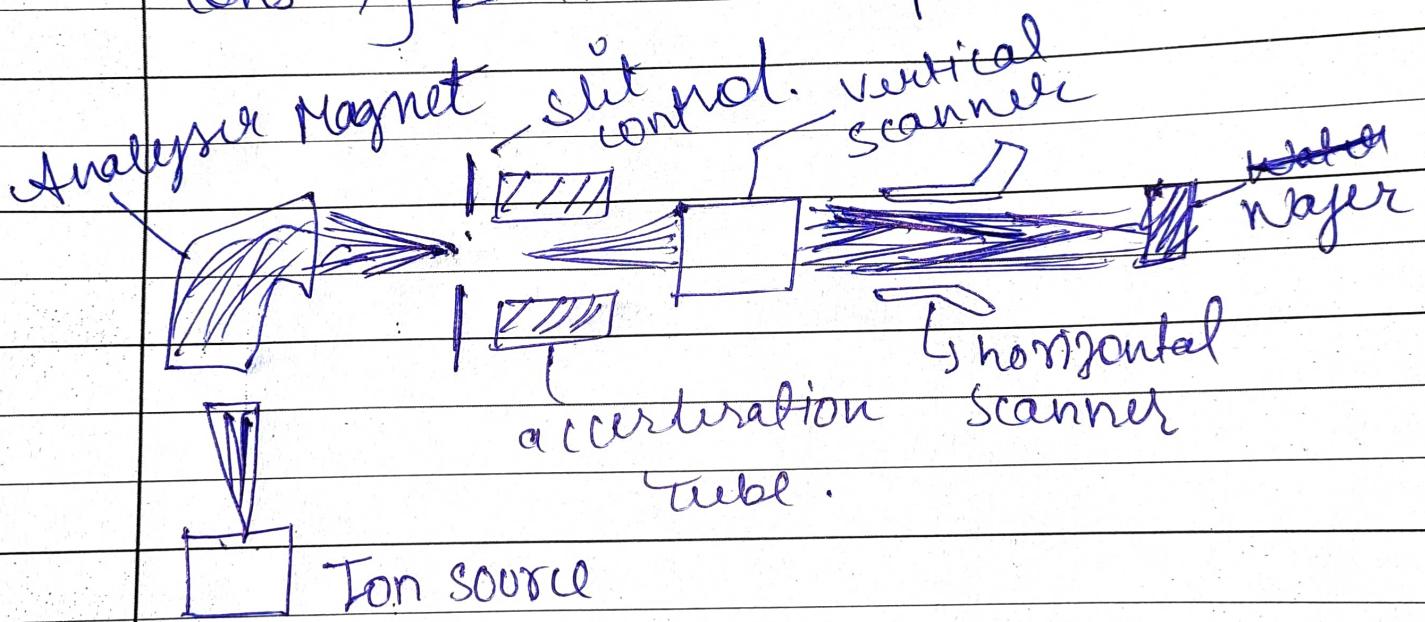
(f) remaining photoresist etched away.



(d)

Ion-Implantation

→ This is a process of introducing dopants into selected areas by the surface of wafer by the bombarding the surface with high energy ions of particular dopant.



Ion-Implanter

A gas source delivers a small amount of gas into ion source. The gas used is BF_3 . The molecules break into charged particles, due to heating.



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The ion source contains desired ions alongwith charged particles, due to high voltage about 20kV the charged ions are pulled out of the ion source into the magnet analysis. Thus the desired ion's only can travel through analyser

In the acceleration tube, the ion's are accelerated from KV to ~~MV~~ MV.