

Roman Dobrodly

Sheet: /

File: loran\_c\_proc\_board.sch

**Title: Processor board**

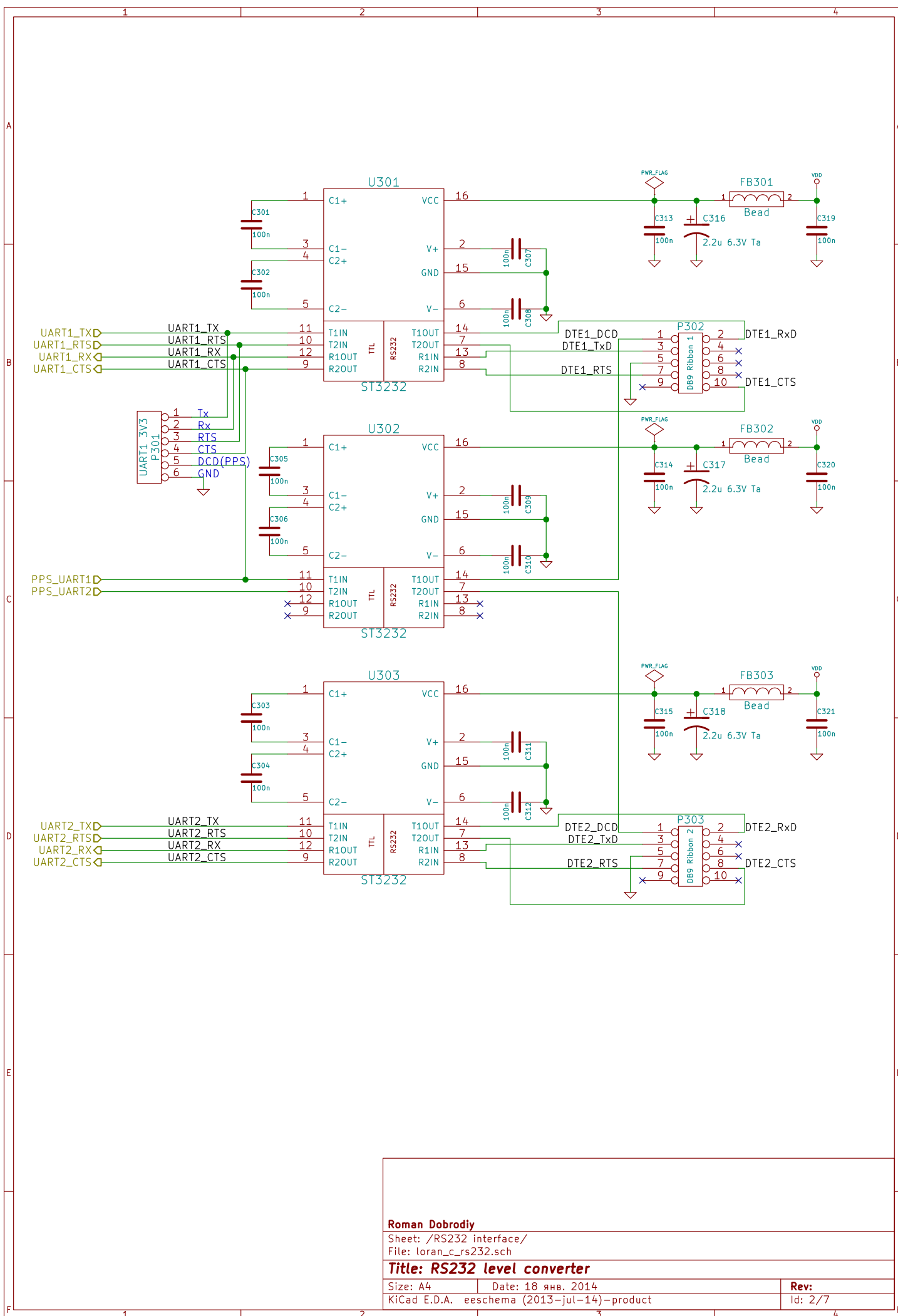
Size: A4

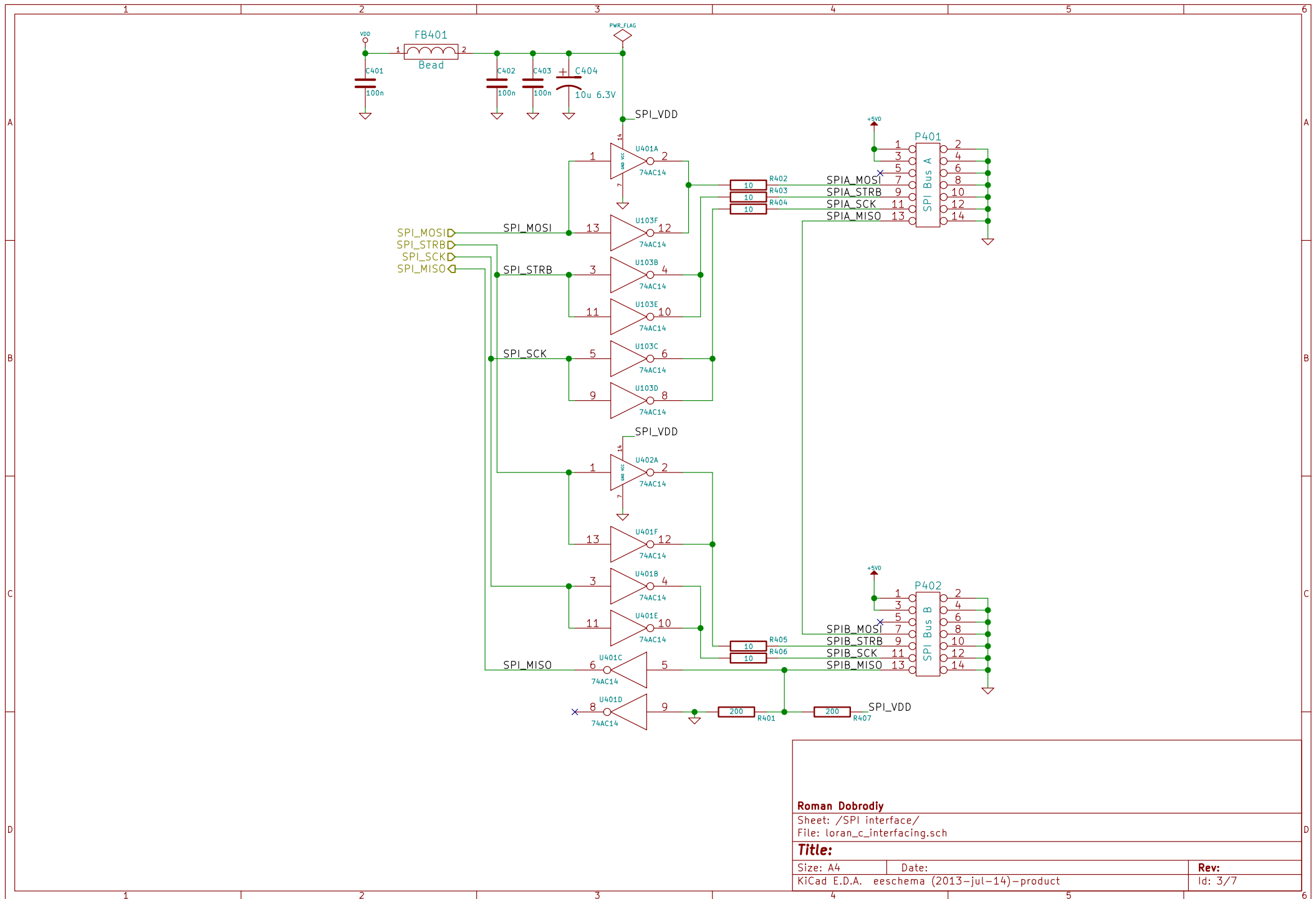
Date: 15 янв. 2014

Rev:

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Sheet: /SPI interface/

File: loran\_c\_interfacing.sch

**Title:**

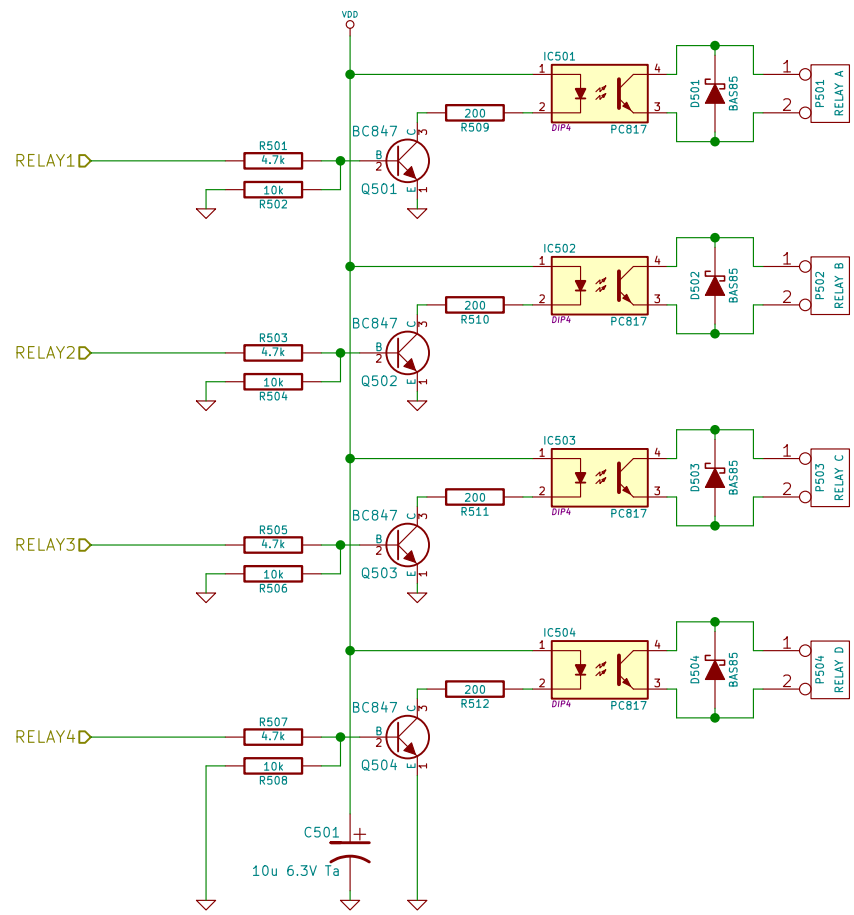
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Date:

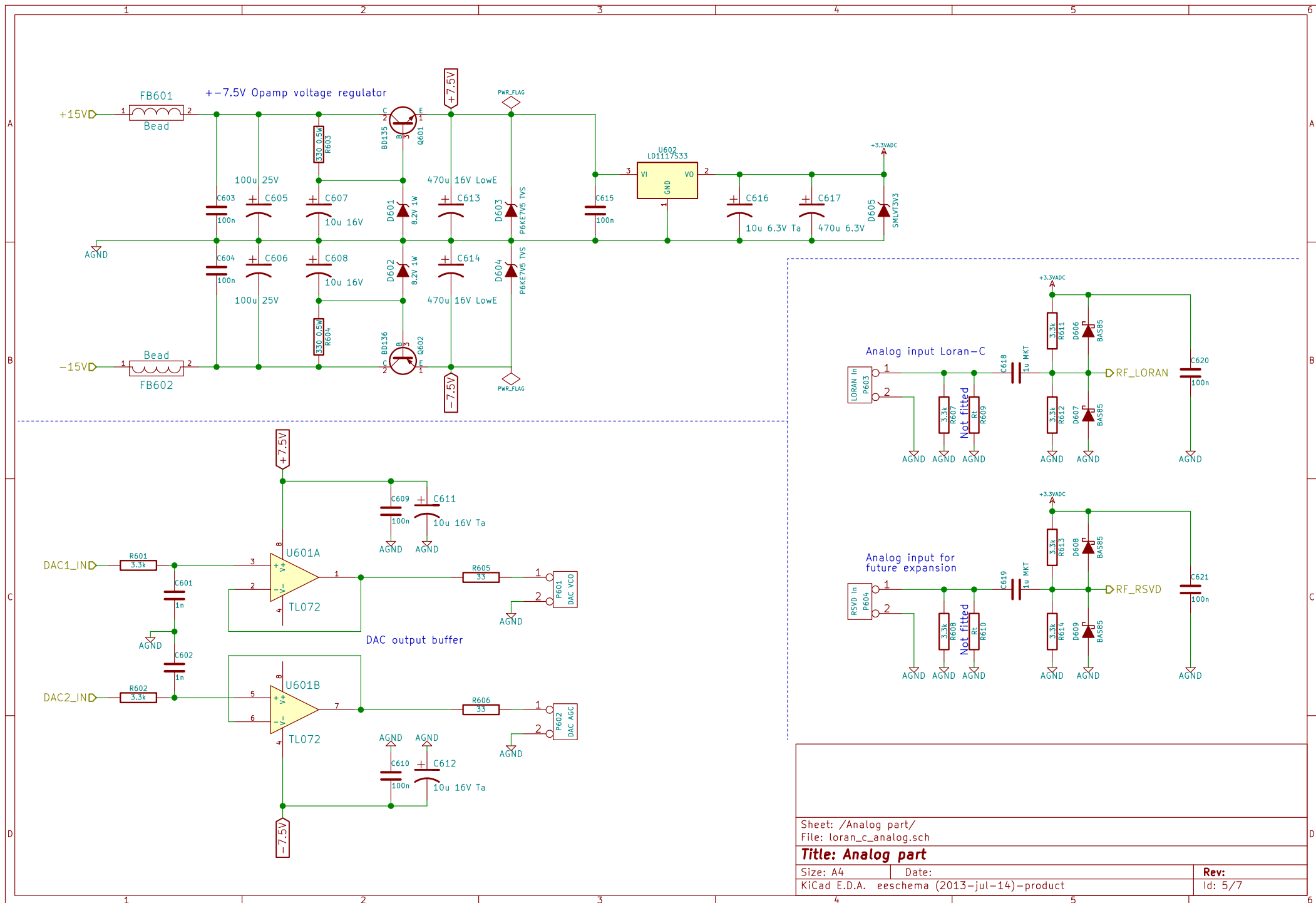
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Sheet: /Relay optoisolation/ File: loran_c_relay.sch		
<b>Title:</b>		
Size: A4	Date:	Rev:
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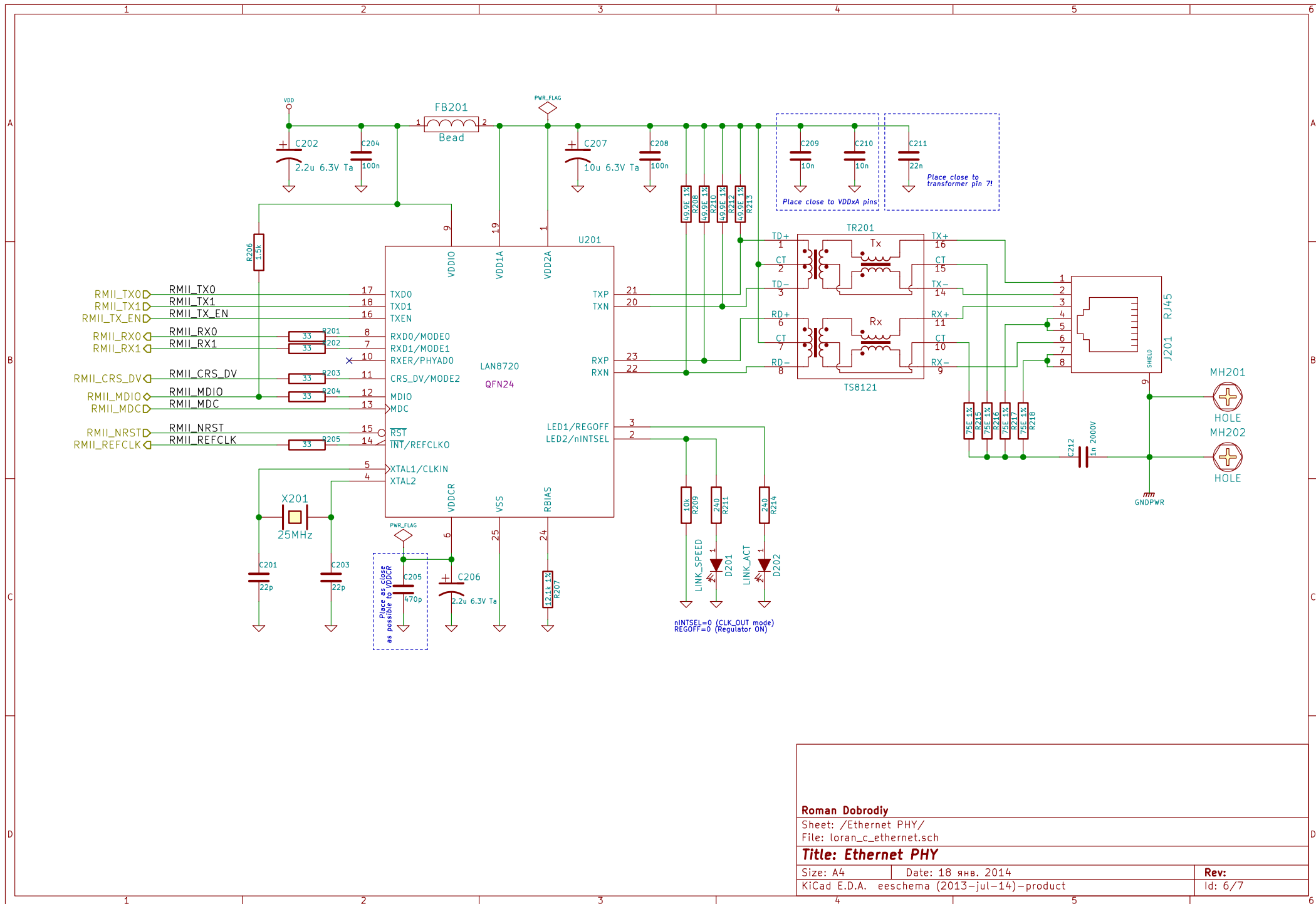


Sheet: /Analog part/  
File: loran\_c\_analog.sch

# **Title: Analog part**

Size: A4 Date:  
KiCad E.D.A. eeschema (2013-jul-14)-product

Rev:  
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**Roman Dobrodiy**

Sheet: /Ethernet PHY/

File: loran\_c\_ethernet.sch

**Title: Ethernet PHY**

Size: A4 Date: 18 янв. 2014

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**Rev:**

Id: 6/7

