# BIPOLAR TRANSISTOR

# Bibliography:


- ***H. Mathieu***, « Physique des semi-conducteurs et des composants électroniques », 4° édition, Masson 1998.
- ***D.A. Neamen***, « semiconductor physics and devices », McGraw-Hill, Inc 2003.
- ***P. Leturcq et G.Rey***, « Physique des composants actifs à semi-conducteurs », Dunod Université, 1985.
- ***J. Singh***, « semiconductors devices :an introduction », McGraw-Hill, Inc 1994.
- ***Y. Taur et T.H. Ning***, « Fundamentals of Modern VLSI devices », Cambridge University Press, 1998.
- ***K.K. Ng***, « complete guide to semiconductor devices », McGraw-Hill, Inc 1995.
- ***D.J. Roulston***, « Bipolar semiconductor devices », McGraw-Hill, Inc 1990.

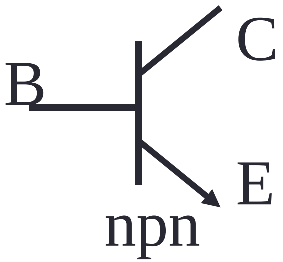
# Plan

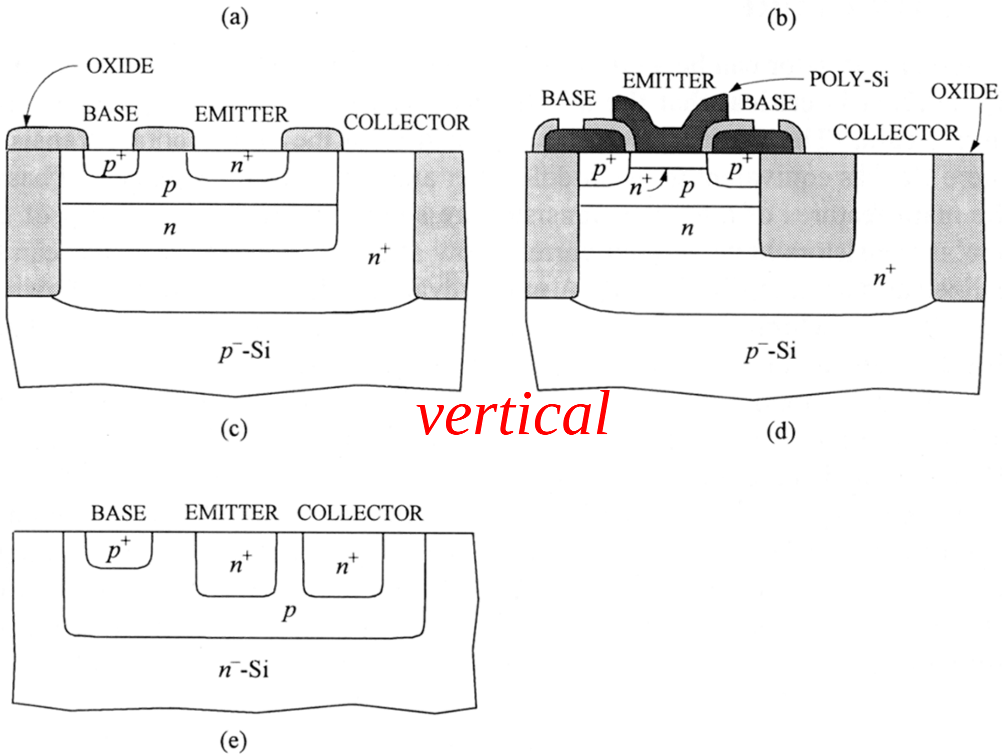
- Geometry
- Principle of operating
- Static characteristics
- Ebers-Moll Equations
- Static parameters ( gain…)
- Second order effects
- Switching performances
- Transistor in HF domain
- Hetero-junction Bipolar Transistor (HBT or TBH)

# Geometry

- Geometry:
  - Lateral
  - Vertical

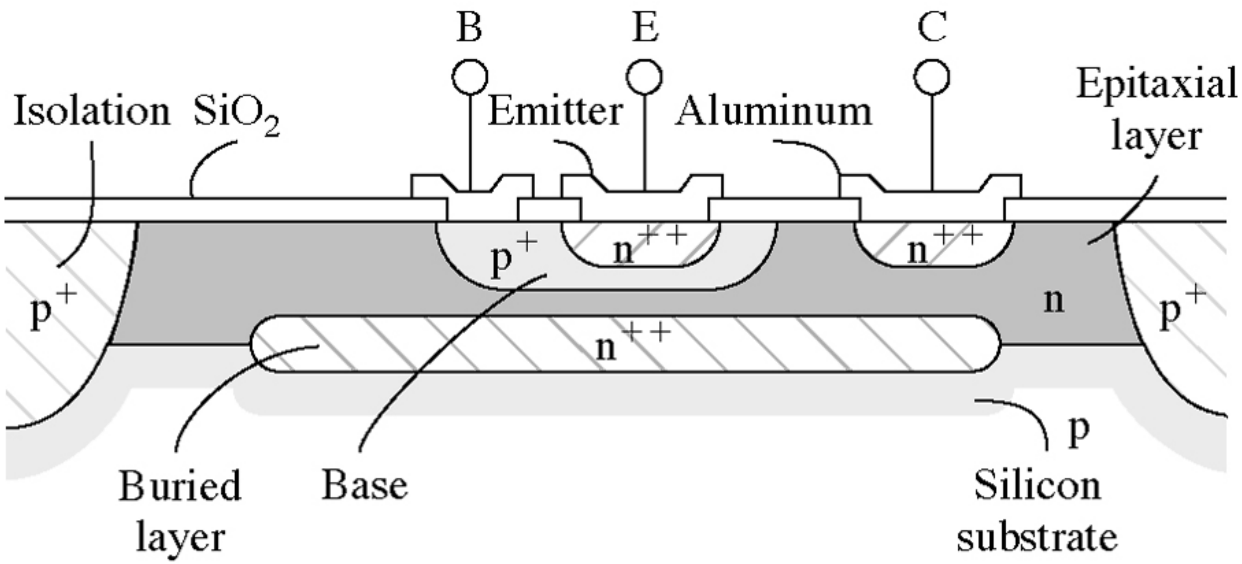
- For digital circuits, *vertical design*




lateral

# Geometry for IC

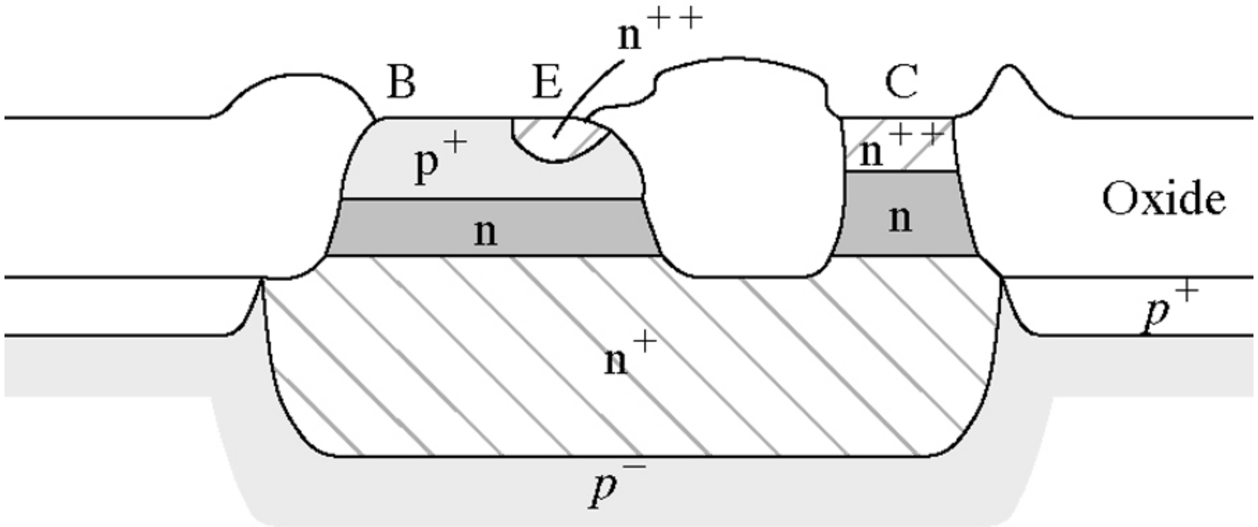



Conventional npn transistor

(a)

Muller et Kamins, « device electronics for IC »,2nd Ed., Wiley, 1986

# Geometry with insulating oxide




(b)

Muller et Kamins, « device electronics for IC »,2nd Ed., Wiley, 1986

# BJT always present: why?

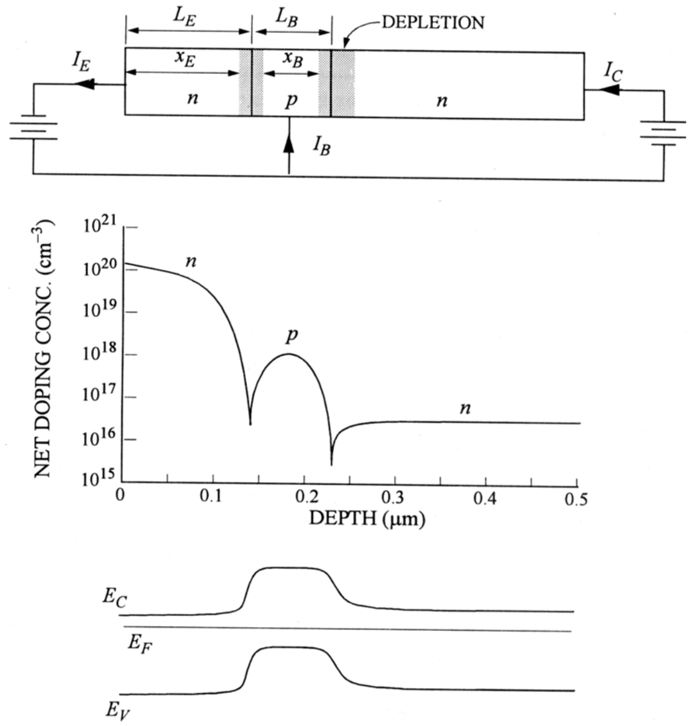
- speed
- Low noise
- High gain
- Low output resistance

Analogue amplifier

- Still present in mobile phone ( analog part)
- Low density, mainly in power stage
- BiCMOS

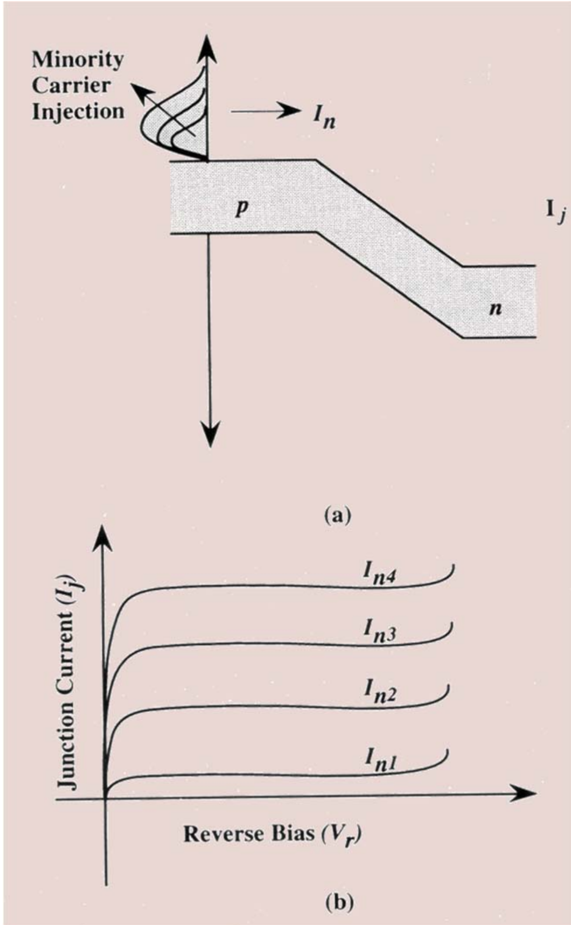
# Working principle

- 2 PN Junctions with one common region (base)
  - The first Junction (EB) will inject carriers
  - The second one (CB) will collect carriers
- The base must be thin (lower than diffusion )length



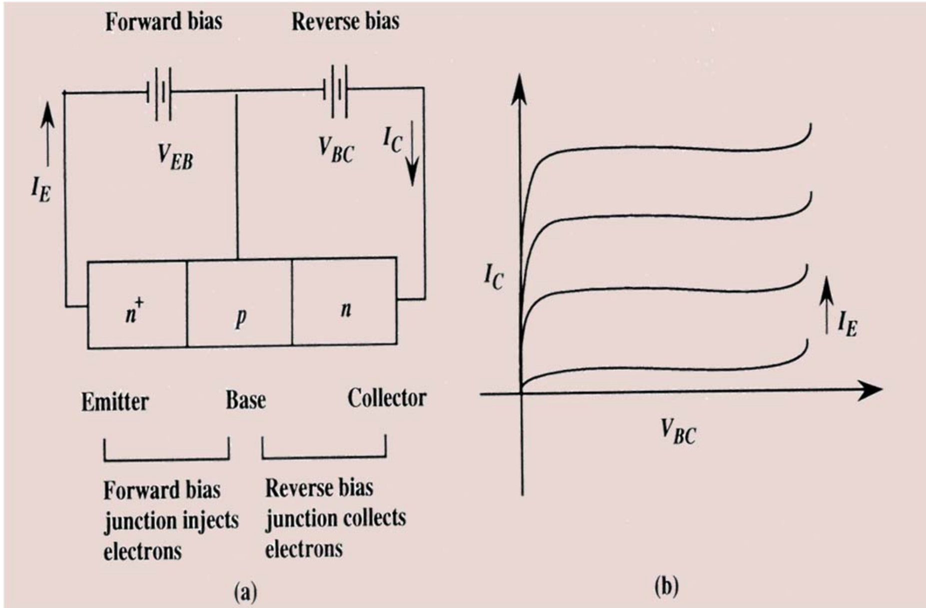
# Working principle

- Reverse biased Junction:
  - Low current due to empty « tank »
  - En modulant le remplissage du réservoir, modulation du courant inverse collecté (collecteur)
  - On remplit le réservoir (la base) en polarisant en direct la jonction EB

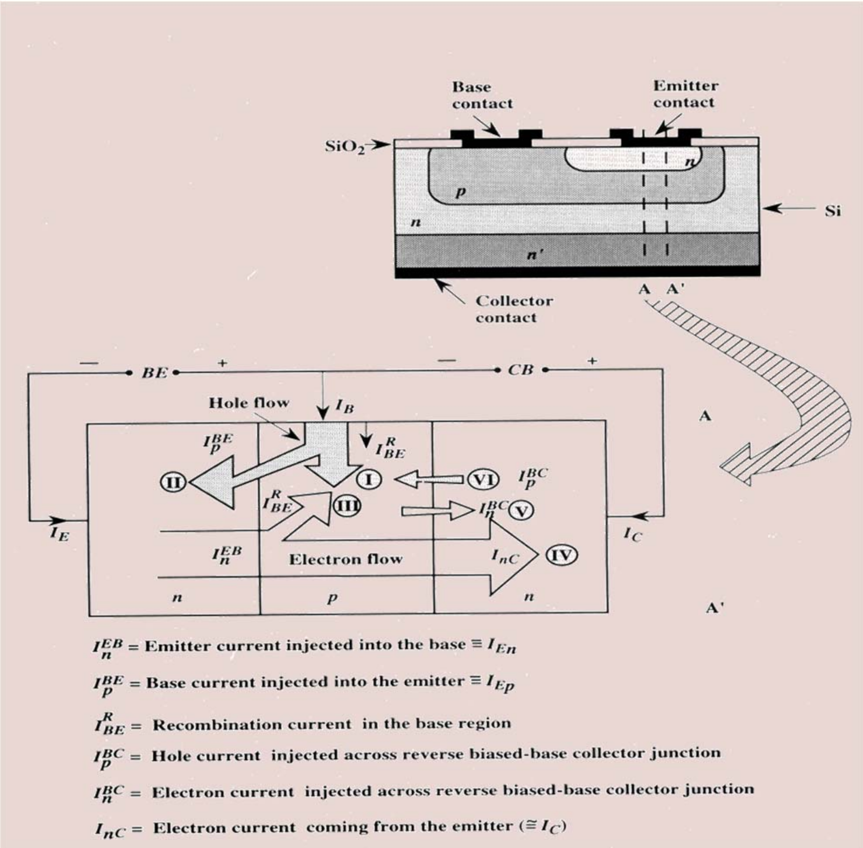


# Working principle

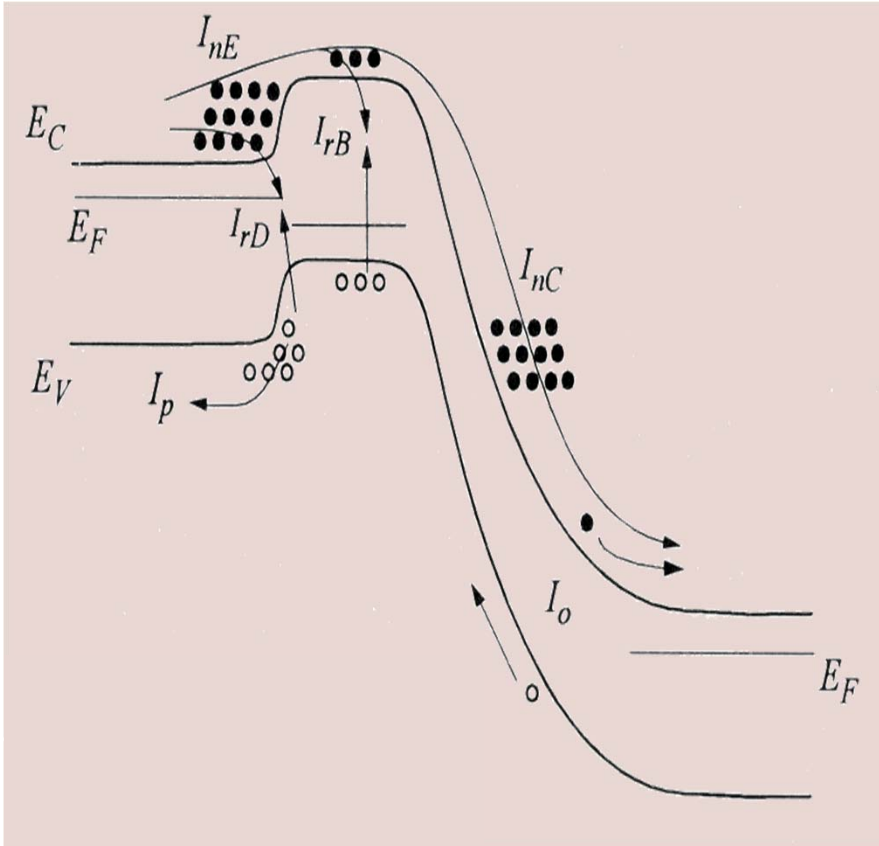
- The reverve biasing CB junction creates a favorable electric field for the collect
- Conditions:
  - Thin base:
    - Avoid recombination effects
  - Ligthly doped base compared to emitter
    - favors one type of injected carriers (better injection efficiency)



# Statics characteristics

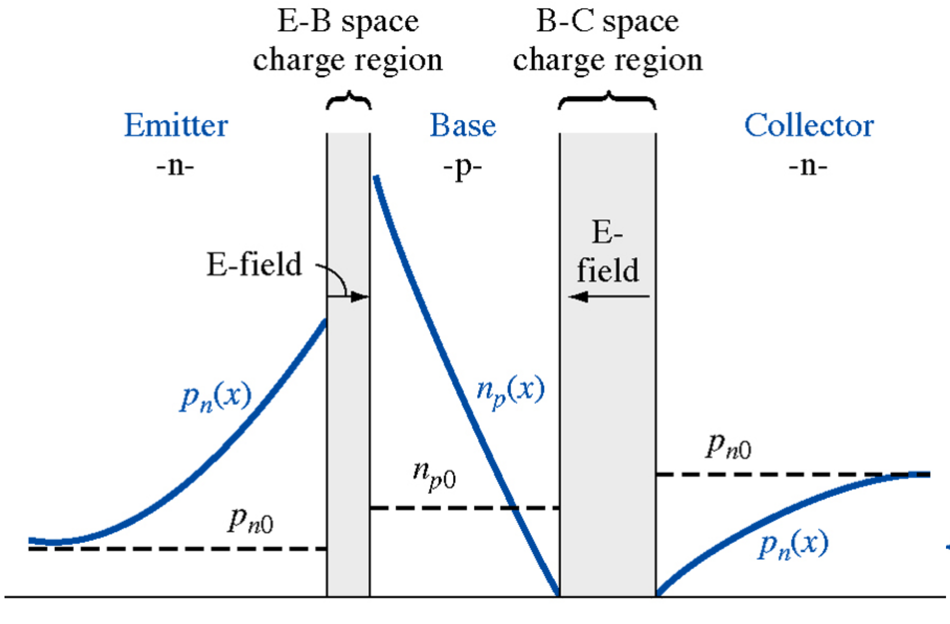



*NPN Transistor*




*NPN Transistor*

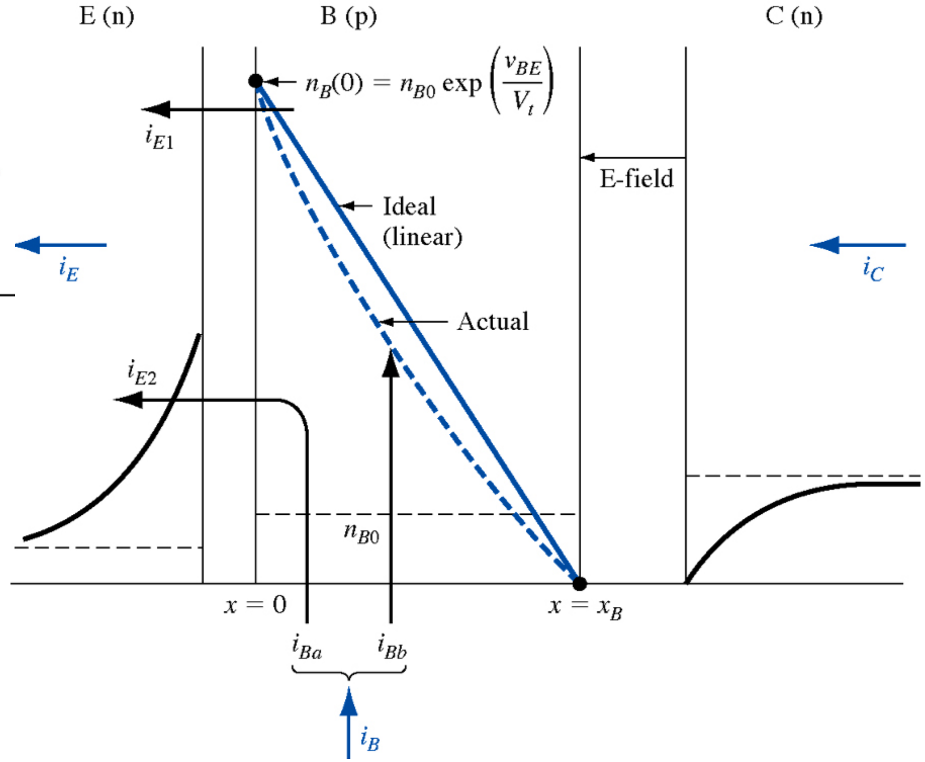
# Minority carrier distribution in a forward biased npn transistor




(b)

ideal

With recombination



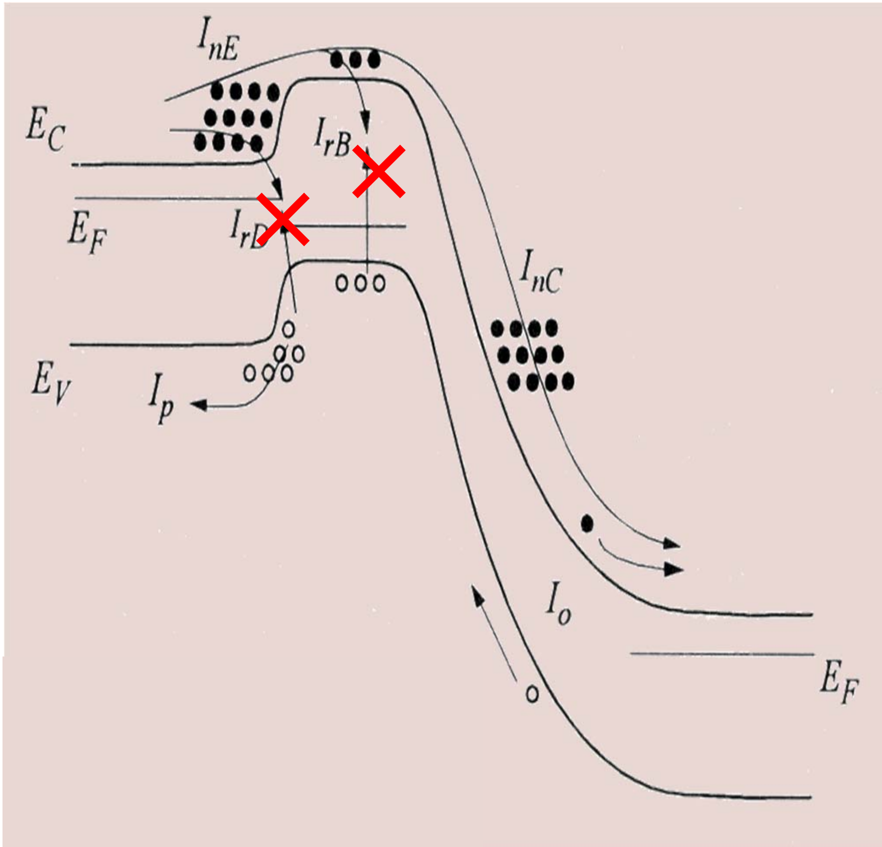
# Statics characteristics + simplifying hypotheses

No recombination in the Base ! ( ✕ )

1D Approximation

Homogeneous doping in the Base

Low Injection




PNP Transistor

# Current components in the NPN Transistor

- In the neutral Base region:
  - Continuity equation

$$\boxed{p\frac{J_n}{eD_n} - n\frac{J_p}{eD_p} = \frac{d(p.n)}{dx}}$$

  - and $J_n >> J_p \quad , \quad n << p$

$$\Rightarrow \quad \boxed{p\frac{J_n}{eD_n} = \frac{d(p.n)}{dx}}$$

  - Integrating from E-B to C-B:

$$\boxed{J_n = -eD_{nb} n_{iB}^2 \frac{\left[\exp(\frac{eV_{BE}}{kT}) - \exp(\frac{eV_{BC}}{kT})\right]}{\int_{E'}^{C'} p(x)dx}}$$

- finally:

$$\boxed{J_n = -eD_{nb} n_{iB}^2 \frac{\left[(e^{\frac{eV_{BE}}{kT}} - 1) - (e^{\frac{eV_{BC}}{kT}} - 1)\right]}{\int_{E'}^{C'} p(x)dx}}$$

- In forward active regime, $J_n$ is negative ( $e^-$ vers $x$<0)

# Current components in the NPN Transistor

$$J_n = -eD_{nb}n_{iB}^2 \frac{\left[(e^{\frac{eV_{BE}}{kT}}-1)-(e^{\frac{eV_{BC}}{kT}}-1)\right]}{\int_{E'}^{C'} p(x)dx} = -\left[\frac{eD_{nb}n_{iB}^2}{\int_{E'}^{C'} p(x)dx}(e^{\frac{eV_{BE}}{kT}}-1)-\frac{eD_{nb}n_{iB}^2}{\int_{E'}^{C'} p(x)dx}(e^{\frac{eV_{BC}}{kT}}-1)\right]$$

and: $$\int_{E'}^{C'} p(x)dx = N_{A_B} \times W_{Beff}$$

So: $$I_n = -A_E\left[\frac{en_{iB}^2 D_{nb}}{N_{A_B}W_{Beff}}(e^{\frac{eV_{BE}}{kT}}-1)-\frac{en_{iB}^2 D_{nb}}{N_{A_B}W_{Beff}}(e^{\frac{eV_{BC}}{kT}}-1)\right] = -I_{Sn}\left[(e^{\frac{eV_{BE}}{kT}}-1)-(e^{\frac{eV_{BC}}{kT}}-1)\right]$$

with : $$I_{Sn} = A_E\frac{en_{iB}^2 D_{nb}}{N_{A_B}W_{Beff}} = A_E\frac{en_i^2}{G_B}$$

Saturation current of electrons in the PN narrow junction ( or without recombination in the Base).

$$G_B = \frac{n_i^2}{n_{iB}^2}\frac{N_{A_B}}{D_{nb}}W_{Beff} = \frac{n_i^2}{n_{iB}^2}\frac{p}{D_{nb}}W_{Beff}$$

Gummel number in the Base ($s/cm^4$)

# Current components in the NPN Transistor

- Emitter current
- Collector current

$$J_{pE} = -J_{spE}\left(\exp\left(\frac{eV_{BE}}{kT}\right) - 1\right)$$

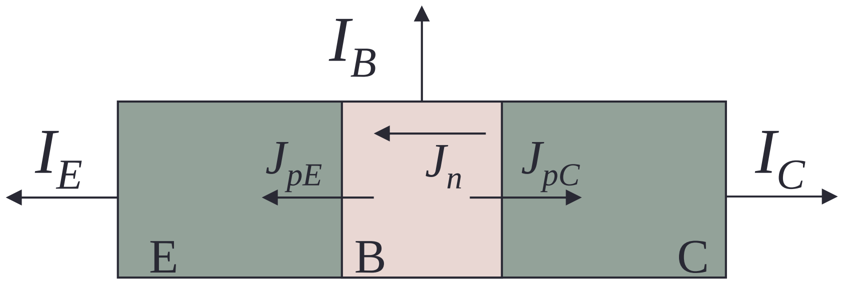
$$J_{pC} = J_{spC}\left(\exp\left(\frac{eV_{BC}}{kT}\right) - 1\right)$$

- finally

$$I_E = I_{pE} + I_n$$

$$I_C = +I_{pC} - I_n$$

$$I_B = -I_C - I_E = -I_{pE} - I_{pC}$$




*NPN*

# Current components in the NPN Transistor

- And (!) :

$$I_E = I_n + I_{pE} = -[\frac{Aen_i^2 D_{nb}}{\int_{E'}^{C'} p(x)dx} + I_{spE}](\exp\frac{eV_{BE}}{kT} - 1) + \frac{Aen_i^2 D_{nb}}{\int_{E'}^{C'} p(x)dx}(\exp\frac{eV_{BC}}{kT} - 1)$$

$$I_{sn}$$

$$I_C = -I_n - I_{pC} = +\frac{Aen_i^2 D_{nb}}{\int_{E'}^{C'} p(x)dx}(\exp\frac{eV_{BE}}{kT} - 1) - [\frac{Aen_i^2 D_{nb}}{\int_{E'}^{C'} p(x)dx} + I_{spC}](\exp\frac{eV_{BC}}{kT} - 1)$$

$$I_B = -I_E - I_C = -I_{pE} - I_{pC} = +I_{spE}\left(\exp(\frac{eV_{BE}}{kT}) - 1\right) - I_{spC}\left(\exp(\frac{eV_{BC}}{kT}) - 1\right)$$

# Statics characteristics

- Forward active region:
  - E-B (forward) and C-B (reverse)

$$I_E = -\left(\frac{Ae^2 n_i^2 D_{nB}}{Q_B + Q_S} + I_{SpE}\right)\exp\frac{eV_{BE}}{kT} = -(I_{Sn} + I_{SpE})\exp\frac{eV_{BE}}{kT}$$

$$I_C = +\left(\frac{Ae^2 n_i^2 D_{nB}}{Q_B + Q_S}\right)\exp\frac{eV_{BE}}{kT} = I_{Sn}\exp\frac{eV_{BE}}{kT}$$

$$I_B^* = -I_E - I_C = -I_{SpE}\exp\frac{eV_{BE}}{kT}$$

# Statics characteristics

- Emitter injection efficiency:

$$\gamma_E = \frac{I_n}{I_{Ep}}$$

- DC common base current gain:

$$\alpha = \frac{I_C}{I_E} = \frac{1}{1 + \frac{J_{Sp}.(Q_B + Q_S)}{e^2 n_i^2 D_{nB}}} = \frac{I_{Sn}}{I_{Sn} + I_{Sp}}$$

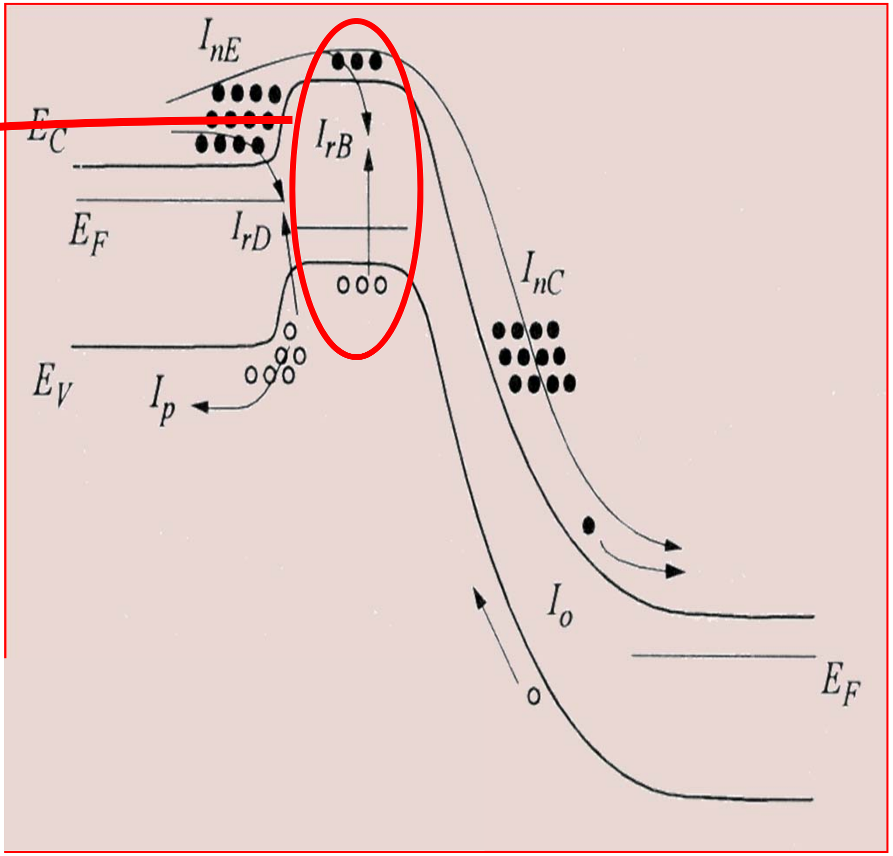
- DC common emitter current gain :

$$\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$$

NB:if we neglect recombination process $\beta$ and $\gamma_E$ are equivalent

# Statics characteristics

- Base transport factor:
  - Take into account recombination in neutral base region




$$I_{rB} = \frac{Q_s}{\tau_n} \approx \frac{AeX_{B_{eff}}(n_p(0) - n_p)/2}{\tau_n}$$

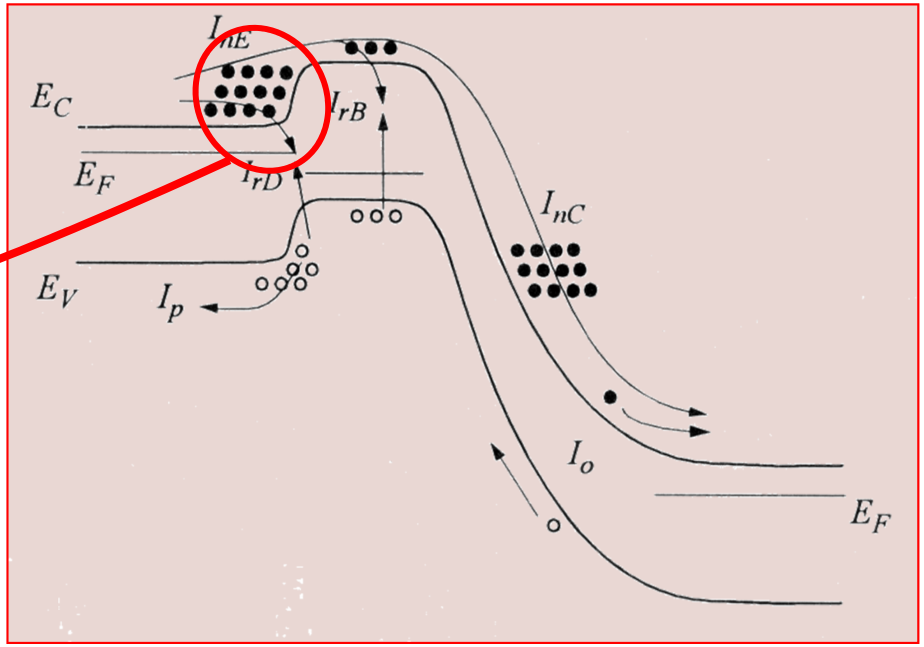
$$I_C = Q_s / \tau_t$$

$$\delta = \frac{I_C}{I_{rB}} = \frac{\tau_n}{\tau_t} = \frac{2L_n^2}{X_{B_{eff}}^2} > 1$$

# Statics characteristics

- Recombination factor:
  - Take into account recombination in depleted base region

$$I_{rD} = \frac{Aen_i}{2\tau} W_T \exp\left(\frac{eV_{BE}}{2kT}\right)$$




with $W_T$, width of E-B space charges.

When we add up all the contribution to the base current we get:

$$I_B = I_B^* + I_{rB} + I_{rD}$$

# Statics characteristics

- The common emitter gain can be expressed as:

$$\frac{1}{\beta} = \frac{I_B}{I_C} = \frac{I_B^* + I_{rB} + I_{rD}}{I_C} = \frac{1}{\gamma_E} + \frac{1}{\delta} + \frac{I_{rD}}{I_C}$$

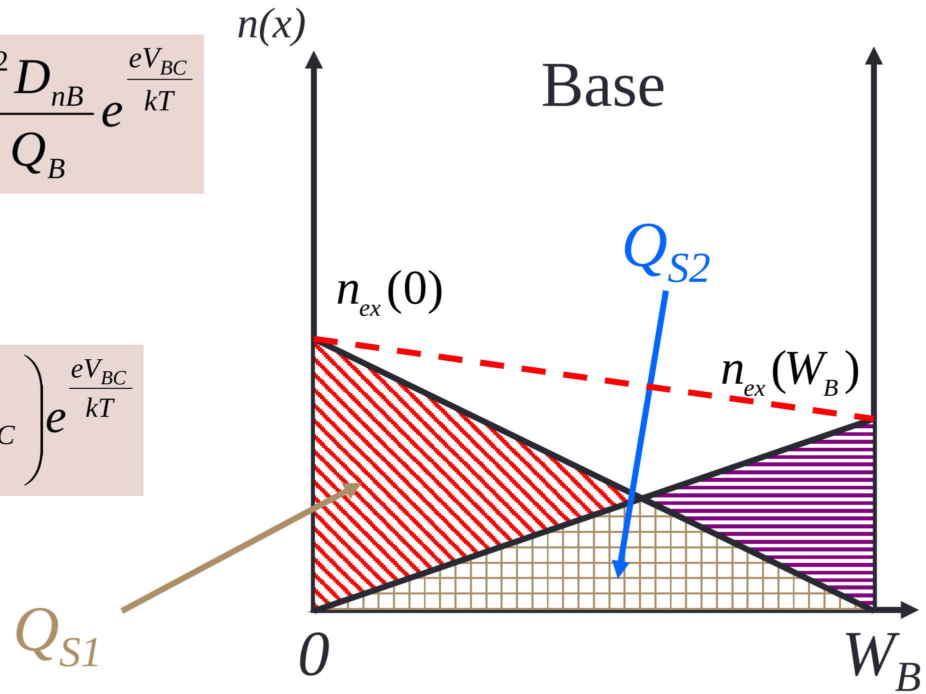
- $I_B^*$ intriseque base current (no recombination)
- $I_{rB}$ recombination current in the neutral base region
- $I_{rD}$ recombination current in the depletion zone of EB junction

# Other modes of operation

- Saturation mode (regime):
  - The two junctions are forward biased.

$$I_E \cong -\left(\frac{Ae^2 n_i^2 D_{nB}}{Q_S + Q_B} + I_{spE}\right) e^{\frac{eV_{BE}}{kT}} + \frac{Ae^2 n_i^2 D_{nB}}{Q_S + Q_B} e^{\frac{eV_{BC}}{kT}}$$

$$I_C \cong \frac{Ae^2 n_i^2 D_{nB}}{Q_S + Q_B} e^{\frac{eV_{BE}}{kT}} - \left(\frac{Ae^2 n_i^2 D_{nB}}{Q_S + Q_B} + I_{spC}\right) e^{\frac{eV_{BC}}{kT}}$$



# Saturation mode

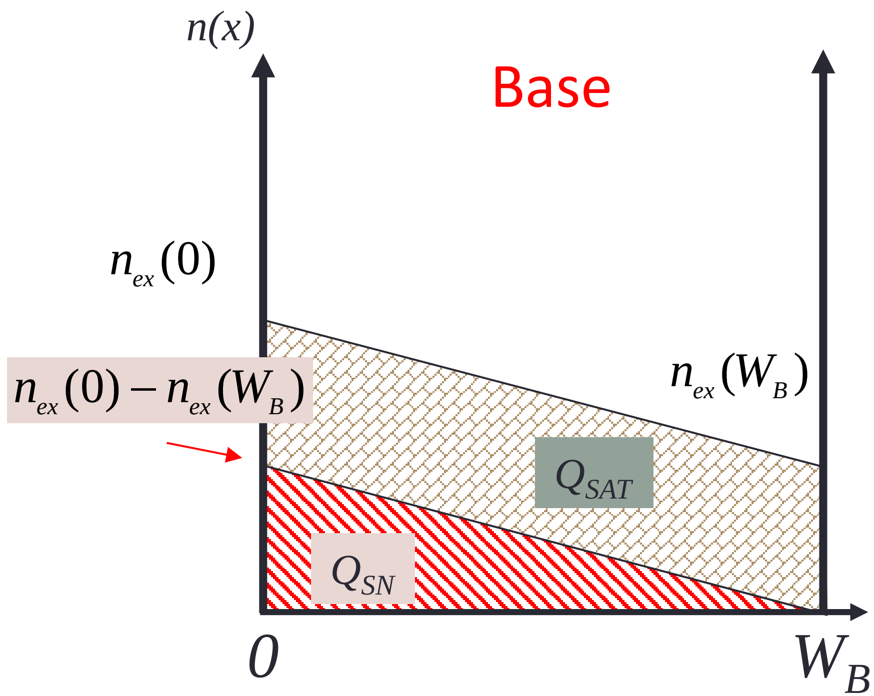
- Low injection : ($Q_S$<<$Q_B$):
  - Current is due to saturation charge injected into the base, *ie* $Q_{ST} = Q_{S1} + Q_{S2}$
  - If we deal with « narrow » junction, this charge is simply given by the surface of ½ trapeze (linear decay)

$$Q_{S1} = -\frac{1}{2}W_B en(x=0) = -\frac{1}{2}W_B \frac{n_i^2}{N_A} e^{\frac{eV_{BE}}{kT}} = -\tau_t J_{sn} e^{\frac{eV_{BE}}{kT}}$$

$$Q_{S2} = -\frac{1}{2}W_B en(x=W_B) = -\frac{1}{2}W_B \frac{n_i^2}{N_A} e^{\frac{eV_{BC}}{kT}} = -\tau_t J_{sn} e^{\frac{eV_{BC}}{kT}}$$

# Saturation mode

- Low injection: ($Q_S$<<$Q_B$):
  - An other « view » of saturation charge (from *Ablard*):
    - We consider transistor in active mode with a charge $Q_{SN}$ and a charge $Q_{SAT}$ (we have to determine) which supply the same saturation current $I_{csat}$.




$Q_{ST} = Q_{SN}+Q_{SAT}$

We get :

Responsible for the degradation of dynamic performance

# Saturation mode

- High injection level
  - In this case, injected electron density reaches holes density into the base ( $n \approx p$ )
  - Equivalent study leads to the following result :

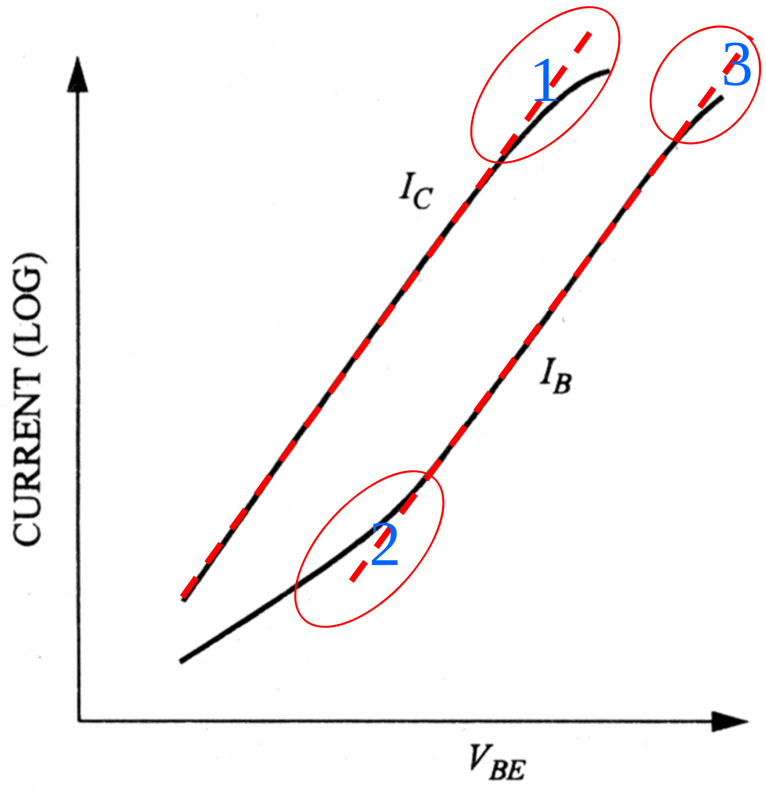
$$\boxed{Q_S = -\frac{1}{2} e n_i \left(e^{\frac{eV_{BE}}{2kT}} + e^{\frac{eV_{BC}}{2kT}}\right) W_B}$$

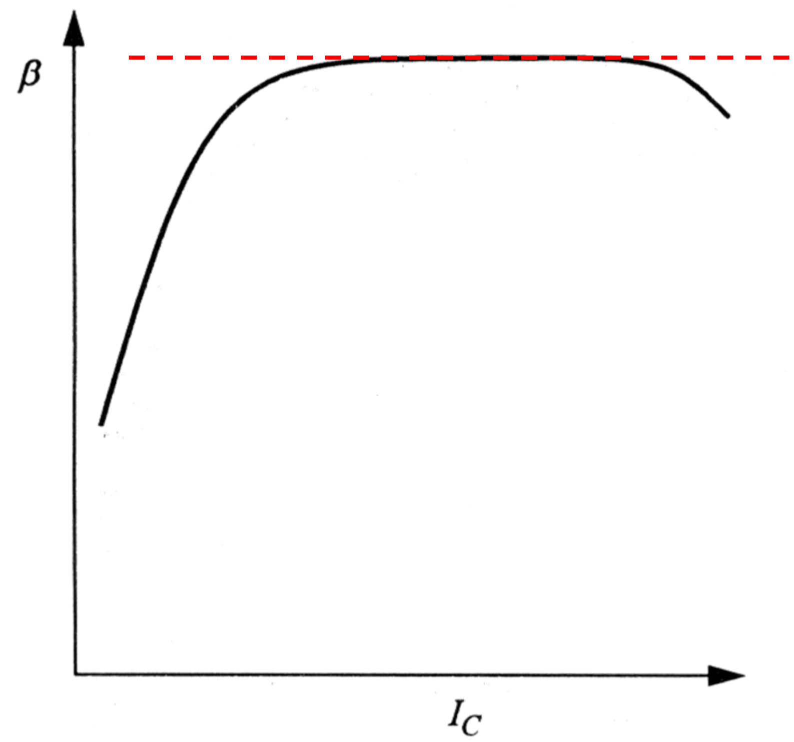
$$\boxed{J_n = -\frac{2eD_{nB}}{W_B} n_i e^{\frac{eV_{BE}}{2kT}} - \frac{2eD_{nB}}{W_B} n_i e^{\frac{eV_{BC}}{2kT}}}$$

  - .

# Nonideal Effects

- *« Gummel plot »:*
  - Graph of $I_C$ and $I_B$ versus $V_{BE}$



# Nonideal Effects

- Early effect / collector punchthrough
- Base – collector junction breakdown
- Emitter and Base serie resistance
- $I_c$ « collapse » fort high current
- « crowding effect »

# Early effect / collector punchthrough

- At "first glance" Ic is independent of $V_{CB}$

$$I_C = -\left(\frac{Ae^2 n_i^2 D_{nB}}{Q_B + Q_S}\right)\exp\frac{eV_{BE}}{kT}$$

- In fact we have the modulation of the width of the neutral region in the base, so in the same way $Q_B$+$Q_S$ , and so $I_c$ !

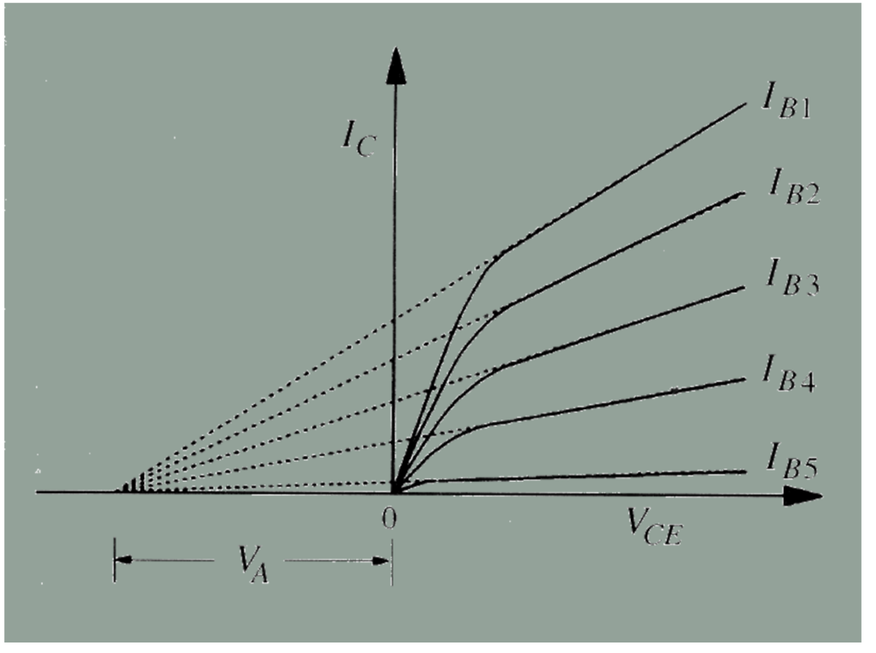
$\Rightarrow$ if $V_{BC} \uparrow$ $\quad$ ZCE B-C $\uparrow$ $\quad$ $W_B \downarrow$ $\quad$ $Q_B+Q_S \downarrow$

$\Rightarrow$ $I_c \uparrow$

# Early effect / collector punchthrough

- At the limit:
  - The space charge BC « depletes » totaly the neutral base
  - collector injects directly current into the emitter.
  - Current only limited by serie resistance $R_{serie}$ form E and C

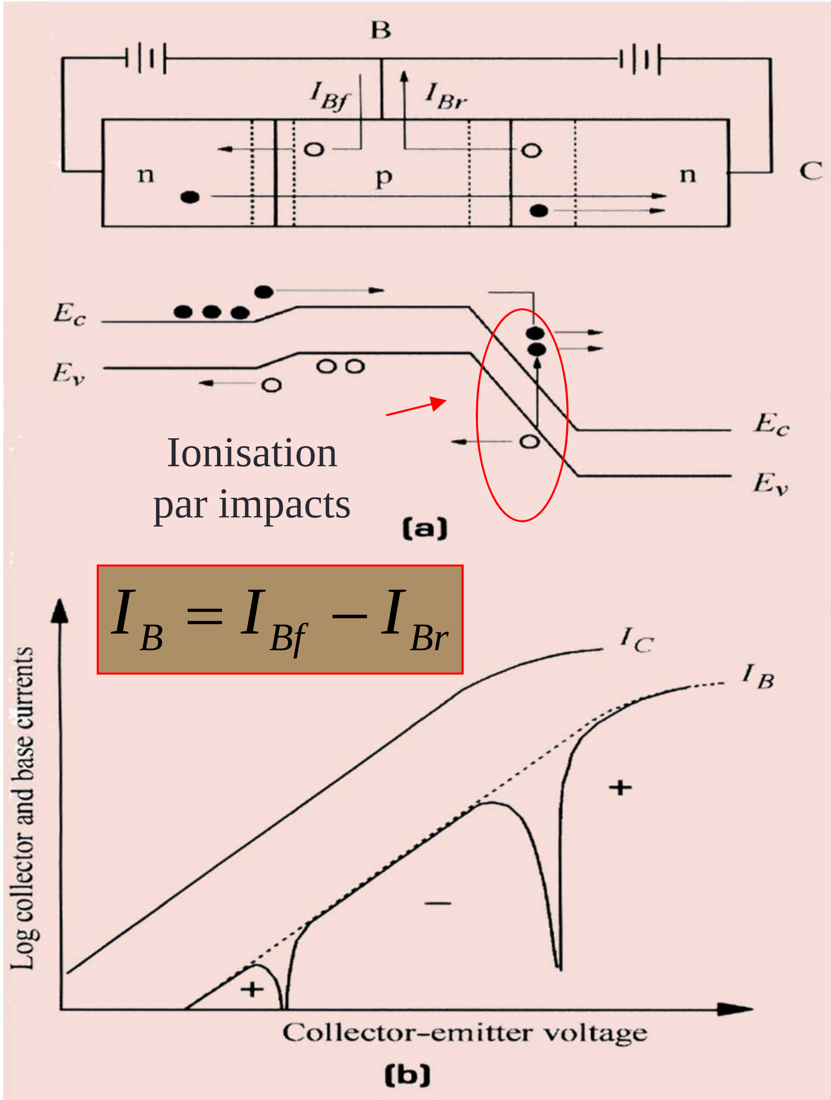
$$|V_A| \approx \frac{Q_{pB}}{C_{dBC}} = \frac{eN_B W_B}{\varepsilon_{SC} / W_{ZCE_{BC}}}$$




$$V_{pt} = \frac{eW_B^2 N_{A_B}(N_{A_B} + N_{D_C})}{2\varepsilon_{SC} N_{D_C}}$$

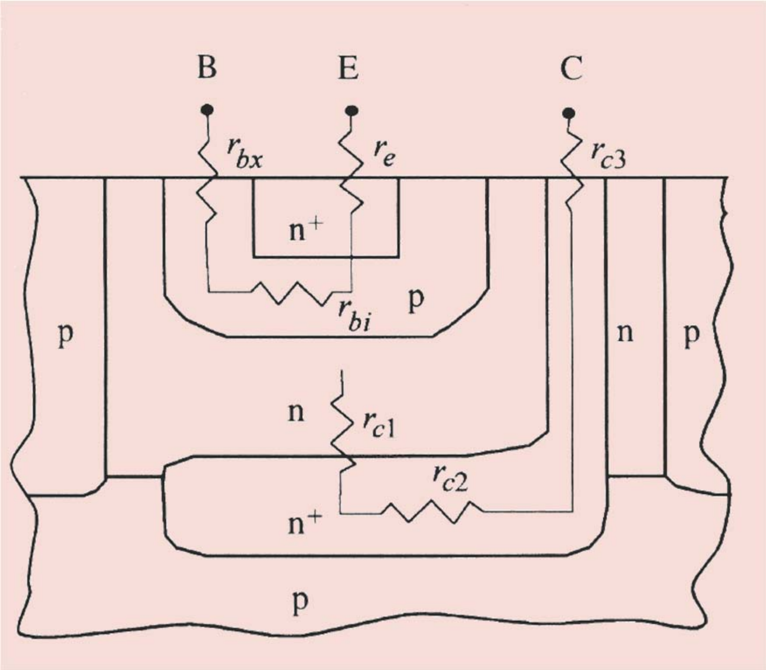
# Base - Collector junction breakdown

- Avalanche of BC:
  - Often occurs before punchthrough
  - How to prevent it?
    - Lowering the electric field:
      - Reduce the doping gradient in the collector
      - Lightly doped layer between base and collector



# Emitter and Base resistance (effet 3)

- At low current negligeable effects
- In high speed circuits, B-C allways reverse biased ($r_{c2}$ *and* $r_{c3}$ as low as possible)
  - Resistances $r_c$ have no effects on current flow
- only $r_e$ and $r_b$ play a major role .
  - IR drop Voltage




$$\Delta V_{BE} = -r_e I_E + I_B r_b = r_e I_C + I_B (r_e + r_b)$$

$$V'_{BE} = V_{BE} - \Delta V_{BE}$$

$$I_C + I_E + I_B = 0$$

$$I'_B = I_B \exp(-\frac{e\Delta V_{BE}}{kT})$$

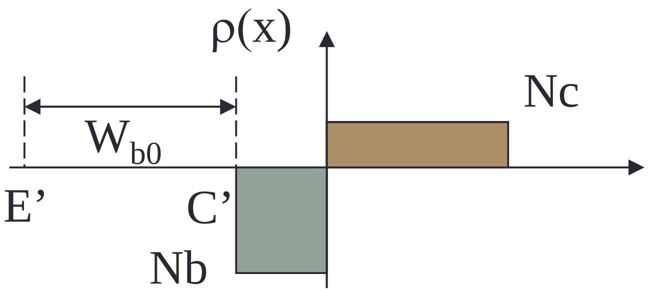
Measured current: $I_{B'}$

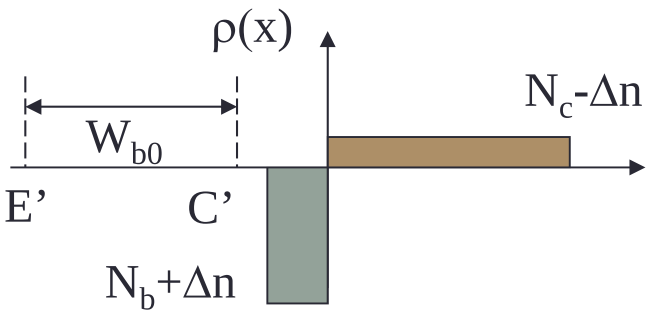
## Collector « collapse » for high injection level (effect 1)

- Numbers of physical mechanisms can cause this falloff of $I_{C0}$:
  - Increase of the charge (holes) into the base (maintain neutrality)
  - Increase the width of the quasineutral base layer (push of the space charge into the collector): *Kirk effect*

$$\left|I_C\right| = A_E J_{C0} \exp\frac{eV_{BE}}{kT}$$

$$\left|I_C\right| = A_E \frac{eD_{nB} n_{ieB}^2}{\int_{E'}^{C'} p_p(x)\,dx} \exp\frac{eV_{BE}}{kT}$$



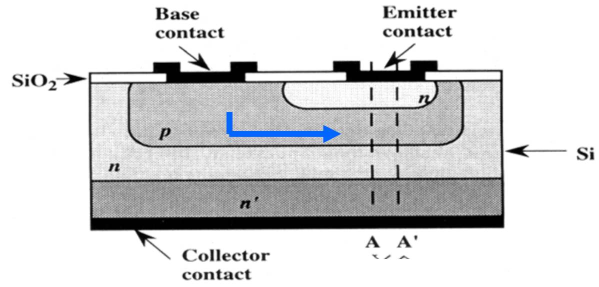



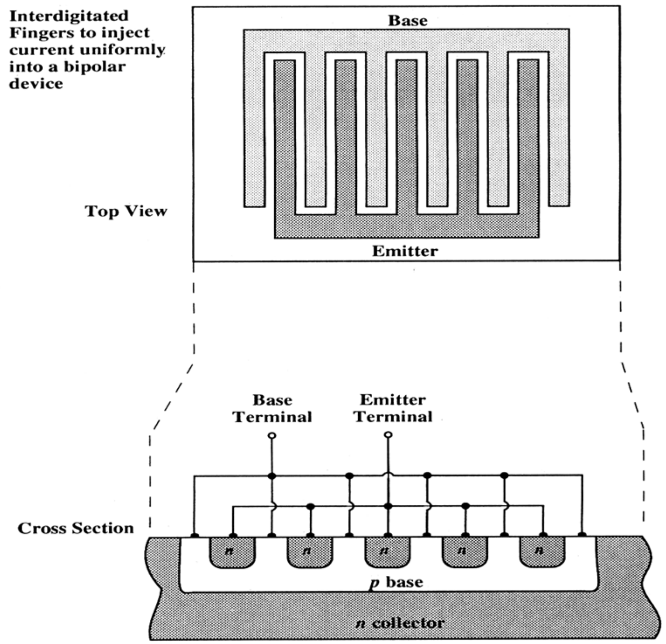
*And the effect #2 ????????????????*

# « crowding effect »

- The view of a 1D devices is an approximation
- Drop voltage IR in the base.
- The edge of the emitter contact is more biased than the core
- Favour a high density of current essentially along the edges
- Not a good thing for high power devices

- *Solutions: interdigitated approach*

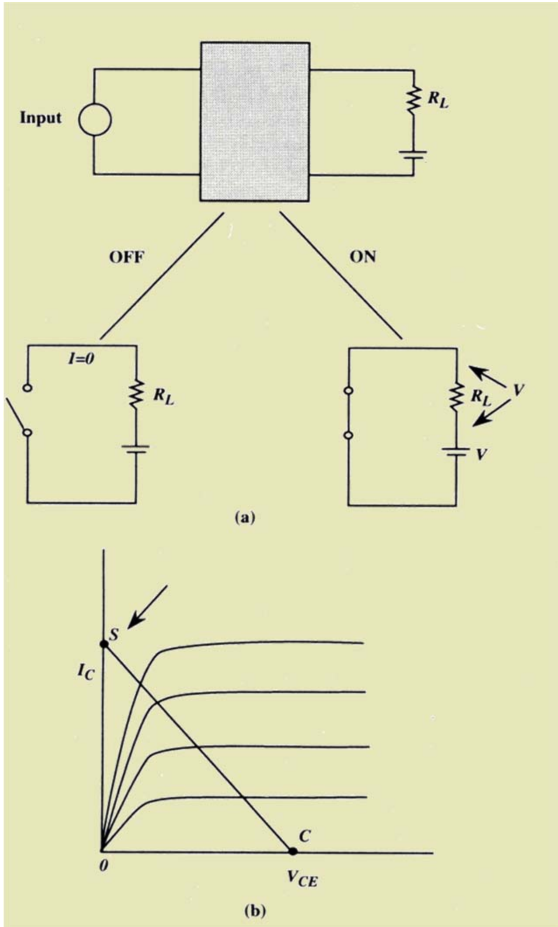


# Bipolar Transistor: a switch ?

ON state: the switch is closed (saturation mode)

OFF state: the switch is open (cutoff mode)

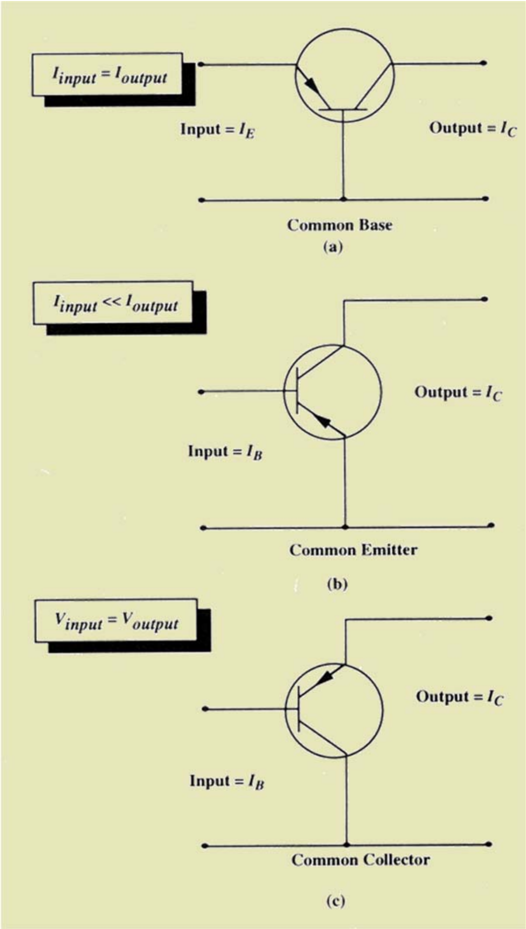


# Bipolar Transistor: a switch ?

Input signal as low as possible

input power as low as possible

***common emitter***



# Bipolar Transistor: a switch ?

- Switching velocity?
- Limiting factors?

- Turn on transient:
  - Continuity equation fir the charge:

$$I_n = \frac{dQ_B}{dt} + \frac{Q_B}{\tau_n}$$

- Base charge can be written:

$$Q_B(t) = I_B \tau_n [1 - \exp(-\frac{t}{\tau_n})]$$

- Collector current is given by:

$$I_C(t) = \frac{Q_B(t)}{\tau_t}$$

*transit time*

*in the base (narrow)*

$$\frac{Q_B(t)}{\tau_t} = I_c = I_B \frac{\tau_n}{\tau_t} [1 - \exp(-\frac{t}{\tau_n})]$$

# Bipolar Transistor: a switch ?

- Turn on:
  - $I_C$ increases until the saturation regime is reached:

$$I_{C_{sat}} \approx \frac{V_{DD}}{R_C}$$

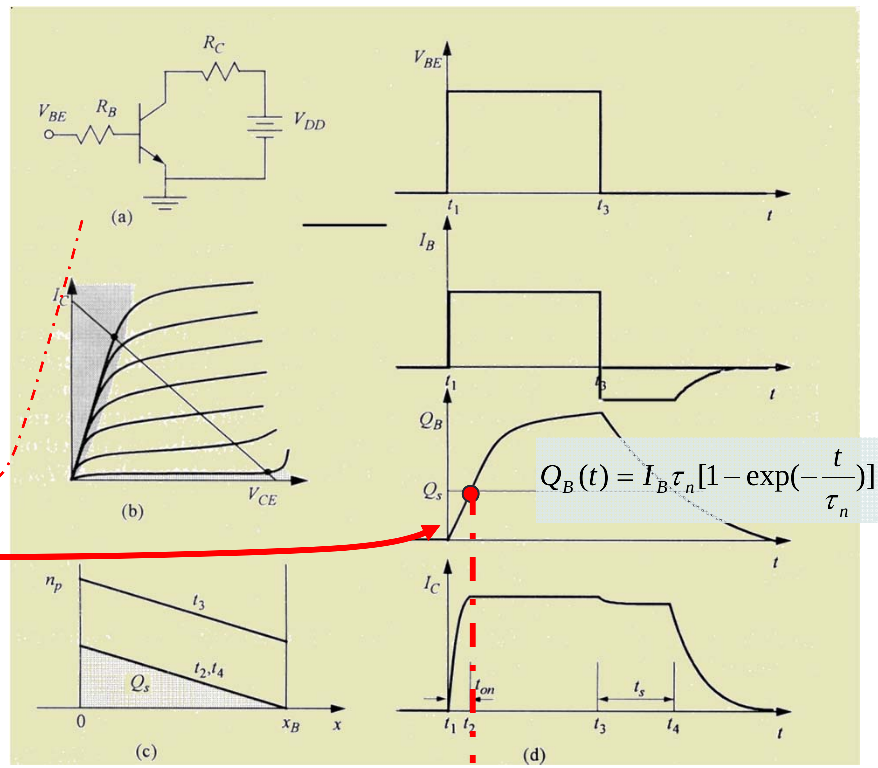
(we neglect $V_{CEsat}$)

  - The limit charge $Q_B(t_{on})$ *to saturate the transistor is given by* :

$$Q_S = \frac{I_{C_{sat}} d_{pB}^2}{2D_{nB}}$$

  - The on state time is given by:

$$t_{ON} = \tau_n \ln\left[\frac{1}{1-(Q_S/I_B\tau_n)}\right] = \tau_n \ln\left[\frac{1}{1-(I_c/I_B\delta)}\right]$$

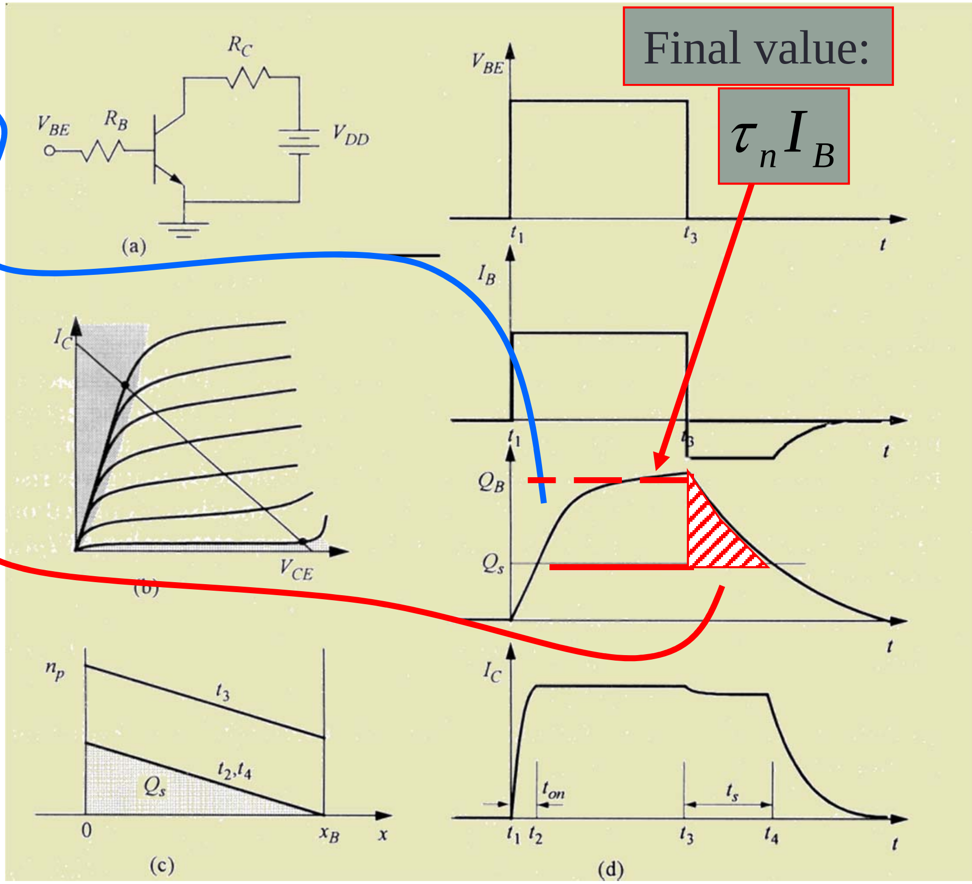


# Bipolar Transistor: a switch ?

- *Remark: the charge can increases over QB(ON) to over saturate the transistor*

- Turn off time : input with a « 0 »:
  - **Evacuation of the stored charge**
    - **This is the storage time $t_S$**

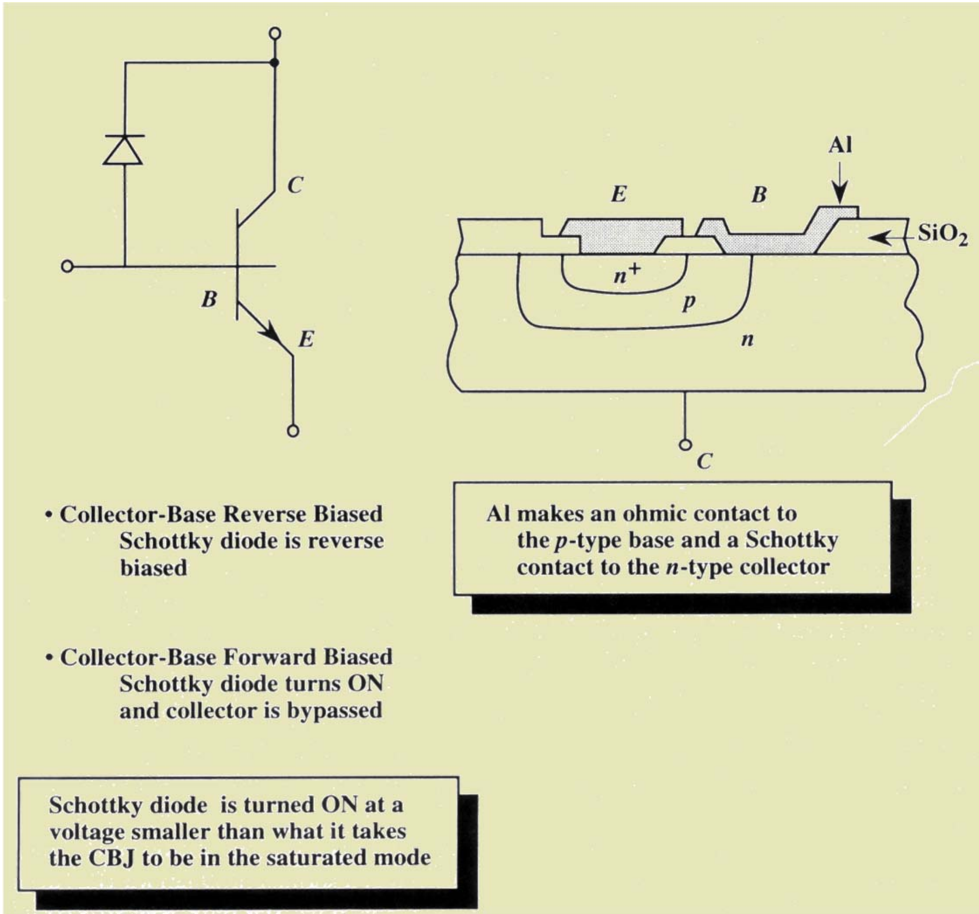
$$t_S = \tau_n \ln\left(\frac{I_B \tau_n}{Q_S}\right)$$



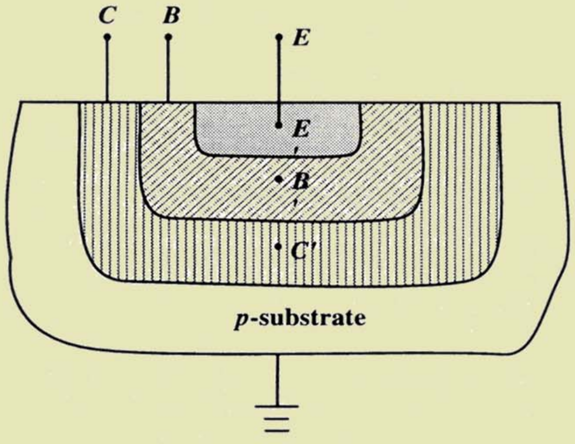

- **after, this is the same mechanism than for PN Junction**

# Bipolar Transistor: a switch ?

- Storage time (desaturation) limits the switching time
- 2 ways to reduce it:
  - Add impurities which decrease strongly the lifetime into the base
  - Schottky Diode in *//* with CB junction: avoid saturation of the transistor



# AC signal : equivalent circuit




(a)

### Equivalent Circuit Parameters

**Base-Emitter Junction (forward biased)**

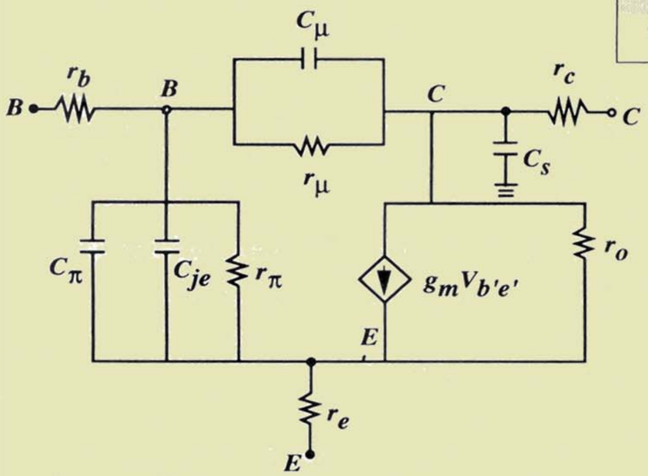
| | |
|---|---|
| $r_e$ | = resistance between $E$ and $E'$ |
| $C_\pi$ | = diffusion capacitance |
| $r_\pi$ | = junction resistance |
| $C_{je}$ | = junction capacitance |
| $r_b$ | = resistance between $B$ and $B'$ |

**Collector Emitter**

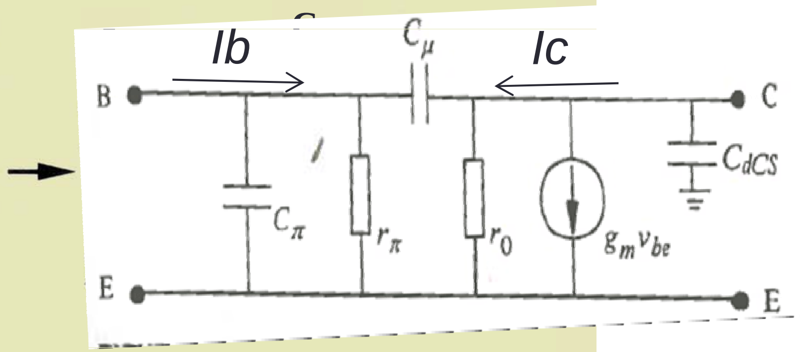
| | |
|---|---|
| $g_m V_{b'e'}$ | = current source |
| $r_o$ | = output resistance |
| $C_s$ | = collector-substrate capacitance |

**Base-Collector Junction (reverse biased)**

| | |
|---|---|
| $r_\mu$ | = junction resistance |
| $C_\mu$ | = junction capacitance |




(b)




(c)

# Transistor and *ac signal*: equivalent circuit

- ***Transconductance*** :links the variation of the collector current to the base – emiter voltage:

$$\boxed{g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{eI_C}{kT}}$$

- ***Input resistance*** : links the variation of Base current to the base – emiter voltage:

$$\boxed{r_\pi = \left(\frac{\partial I_B}{\partial V_{BE}}\right)^{-1} = \frac{kT}{eI_B} = \frac{\beta}{g_m} = h_{11}}$$

- ***Output resistance:***

$$\boxed{r_o = \left(\frac{\partial I_C}{\partial V_{CE}}\right)^{-1} \approx \frac{V_A}{I_C} = \frac{1}{h_{22}}}$$

# Transistor and *ac signal*: equivalent circuit

- ***Capacitance*** $C_{\pi}$ :

$$\boxed{C_{\pi} = C_{SE} + C_{T_{EB}}}$$

  - Storage capacitance $\boxed{C_{SE} = \tau_F g_m}$
  - transit time $\boxed{\tau_F = t_E + t_{t_B} + t_{t_{BE}} + t_{t_{BC}}}$

- ***Capacitance*** $C_{\mu}$ : CB junction capacitance reverse biased

$$\boxed{C_{\mu} = C_{T_{CB}}}$$

- ***Collector –substrate (depletion layer) capacitance:***

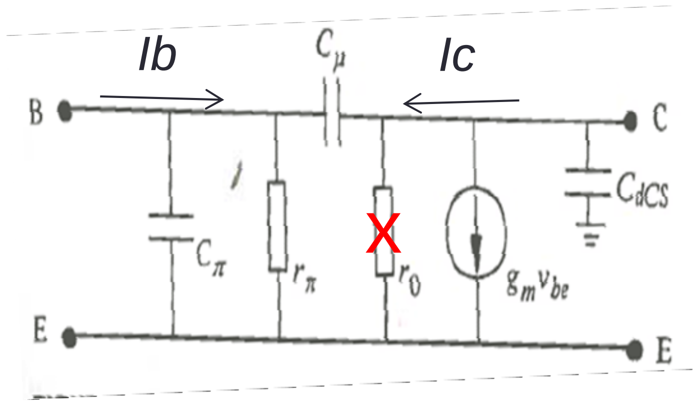
$$\boxed{C_{dCS}}$$

# Transistor and *ac signal*: equivalent circuit

- Cut off frequency (current gain =1)
  - We neglect r0

$$i_c = g_m v_{be} - j\omega C_\mu v_{be}$$

$$i_b = \left( \frac{1}{r_\pi} + j\omega C_\pi + j\omega C_\mu \right) v_{be}$$




- Current gain is given by:

$$\boxed{\beta(\omega) = \frac{i_c}{i_b} = \frac{g_m - j\omega C_\mu}{(1/r_\pi) + j\omega(C_\pi + C_\mu)} = h_{21}}$$

# Transistor and *ac signal*: equivalent circuit

- At low frequency:
  - In modern devices , in general,

$$\omega C_\mu << g_m \quad \Rightarrow \quad \boxed{\beta(\omega) \approx \frac{i_c}{i_b} = \frac{g_m r_\pi}{1 + j\omega r_\pi (C_\pi + C_\mu)}}$$

- At high frequecy, the imaginary term dominates and :

$$\boxed{\beta(\omega) \approx \frac{g_m}{j\omega (C_\pi + C_\mu)}}$$

# Transistor en *ac*: schéma équivalent

- On obtient alors la fréquence de coupure (« cutoff frequency ») en faisant $i_C/i_B=1$

- Soit encore

$$\boxed{2\pi f_T = \frac{g_m}{C_\pi + C_\mu}}$$

$$\boxed{\frac{1}{2\pi f_T} = \tau_F + \frac{kT}{eI_C}(C_{SE} + C_{T_{BC}}) + \cancel{C_{T_{BC}}(r_e + r_c)}}$$

*Temps de transit en direct*

# Transistor en *ac*: schéma équivalent

- Maximun oscillation frequency ⇔Power gain=1
  - Laborious and tedious calculation/ we have to take into account the base resistance

$$\boxed{f_{\max} = \sqrt{\frac{f_T}{8\pi r_b C_{dBC}}}}$$

# Heterojunction Bipolar Transistor

- Current gain:

$$\alpha = \frac{\gamma_E}{1-\gamma_E}\frac{\delta-1}{\delta} = \left[1-\frac{n_{i_E}^2}{N_{D_E}}\frac{D_{p_E}}{D_{n_B}}\frac{N_{A_B}}{n_{i_B}^2}\frac{W_{Beff}}{L_{p_E}}\right]\left[1-\frac{W_{Beff}^2}{2L_{n_B}^2}\right]$$

- In the case of narrow base:

$$\alpha = \frac{\gamma_E}{1-\gamma_E}\frac{\delta-1}{\delta} = \left[1-\frac{n_{i_E}^2}{N_{D_E}}\frac{D_{p_E}}{D_{n_B}}\frac{N_{A_B}}{n_{i_B}^2}\frac{W_{Beff}}{L_{p_E}}\right]$$

# Heterojunction Bipolar Transistor

$$\alpha = \frac{\gamma_E}{1-\gamma_E}\frac{\delta-1}{\delta} = \left[1 - \frac{n_{i_E}^2}{N_{D_E}}\frac{D_{p_E}}{D_{n_B}}\frac{N_{A_B}}{n_{i_B}^2}\frac{W_{Beff}}{L_{p_E}}\right]$$

- If we want a gain $\beta$ with a high value, we need $\alpha$ close to 1. It means:
  - Lowering base doping
  - Lowering base width (careful with punchthrough!)

Increase of the base resistance ⇔ $f_{max}$ *decreases*

# Heterojunction Bipolar Transistor

$$\alpha = \frac{\gamma_E}{1-\gamma_E}\frac{\delta-1}{\delta} = \left[1 - \frac{n_{i_E}^2}{N_{D_E}}\frac{D_{p_E}}{D_{n_B}}\frac{N_{A_B}}{n_{i_B}^2}\frac{W_{Beff}}{L_{p_E}}\right]$$

- Other solution:
  - Increase emitter doping
    - Improve emitter efficiency
  - Problem: « gap shrinking » ⇔ $\Delta E_g = E_{g(base)} - E_{g(émetteur)} > 0.$

$$n_i^2(émetteur) = n_i^2(Base)\exp(\frac{\Delta E_g}{kT})$$

  - This « problem » can be transform in opportunity !! (next two slides)

# Heterojunction Bipolar Transistor

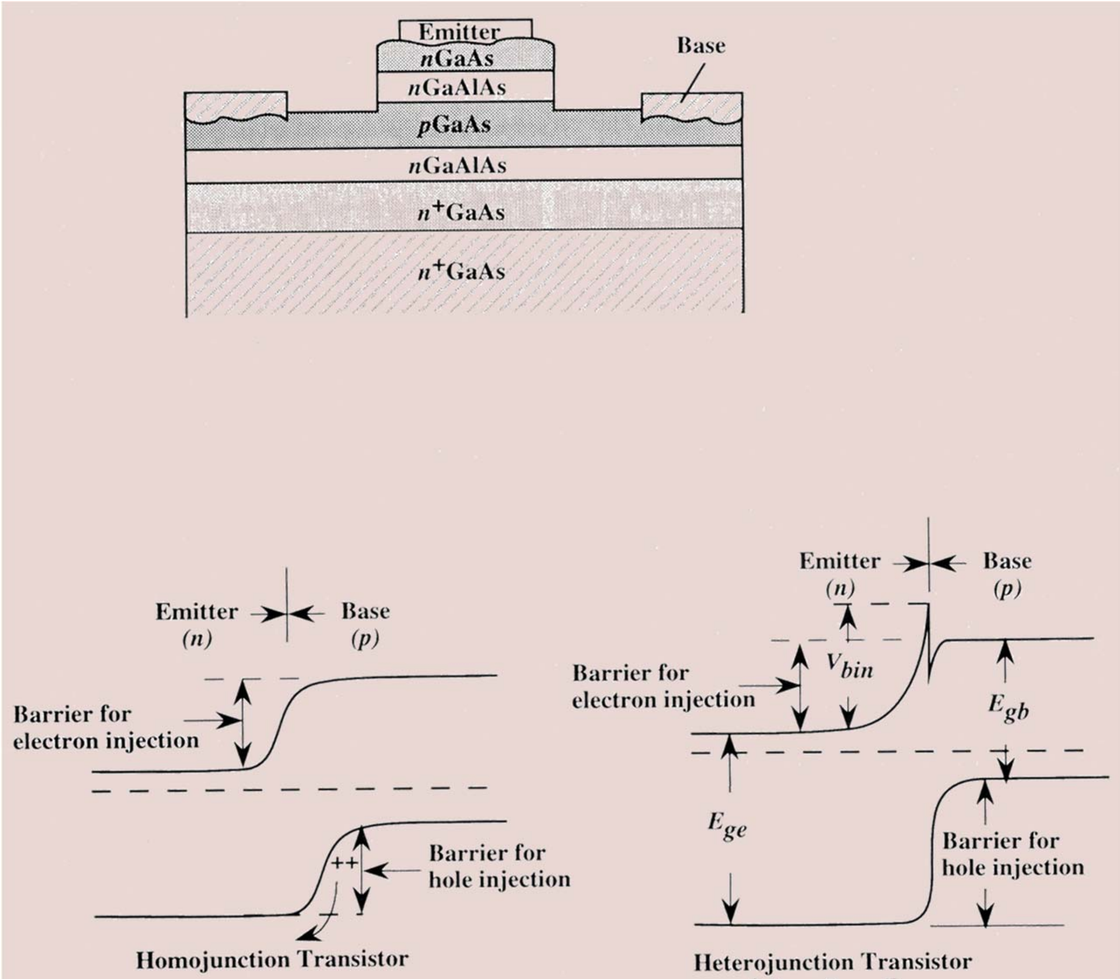
$$\alpha = \left[ 1 - \frac{\cancel{n_{i_e}^2}}{N_{D_E}} \frac{D_{p_E}}{D_{n_B}} \frac{N_{A_B}}{\cancel{n_{i_B}^2}} \frac{W_{Beff}}{L_{p_E}} \exp \frac{\Delta E_g}{kT} \right]$$

$$\beta = \frac{\alpha}{1-\alpha} = \left[ \frac{N_{D_E}}{N_{A_B}} \frac{D_{n_B}}{D_{p_E}} \frac{L_{p_E}}{W_{Beff}} \exp(-\frac{\Delta E_g}{kT}) - 1 \right]$$

We see that it is difficult to have at the same time a large emitter doping, a lightly doped and thin base and a large gain

# Heterojunction Bipolar Transistor

- We design a structure with a negative energy gap difference: this is an HBT




$$\Delta Eg = Eg_b - Eg_e$$

**Requirements for a bipolar device**

- High gain
- High emitter efficiency
- High speed

(From Singh)

**Demands and Problems for a BJT**

Demands

Problems

Heavy emitter doping

Bandgap shrinkage causing base injection

Low base doping
Narrow base width

High base resistance

Solution: Heterojunction Bipolar Transistors

- Emitter can be heavely doped using a SC with Eg larger than the base semiconductor
- Base can be heavely doped and beheavely doped  and be made narrow without increasing base resistance
- Collector can be chosen from a material to increase breakdown voltage

LINEAR SYSTEMS

*Linear Integrated Systems*

# LS301 LS302 LS303

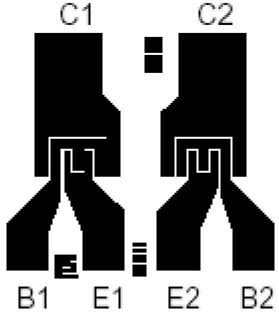
## HIGH VOLTAGE SUPER-BETA MONOLITHIC DUAL NPN TRANSISTORS

| FEATURES | |
|---|---|
| VERY HIGH GAIN | $h_{FE} \geq 2000$ @ 1.0μA TYP. |
| LOW OUTPUT CAPACITANCE | $C_{OBO} \leq 2.0pF$ |
| TIGHT $V_{BE}$ MATCHING | $\lvert V_{BE1}-V_{BE2}\rvert$ = 0.2mV TYP. |
| HIGH $f_T$ | 100MHz |

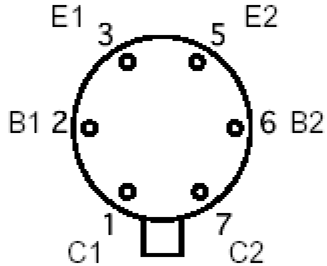
| ABSOLUTE MAXIMUM RATINGS NOTE 1 @ 25°C (unless otherwise noted) | | |
|---|---|---|
| $I_C$ | Collector Current | 5mA |

| Maximum Temperatures | |
|---|---|
| Storage Temperature | -65° to +200°C |
| Operating Junction Temperature | +150°C |

| Maximum Power Dissipation | ONE SIDE | BOTH SIDES |
|---|---|---|
| Device Dissipation @ Free Air | 250mW | 500mW |
| Linear Derating Factor | 2.3mW/°C | 4.3mW/°C |




26 X 29 MILS

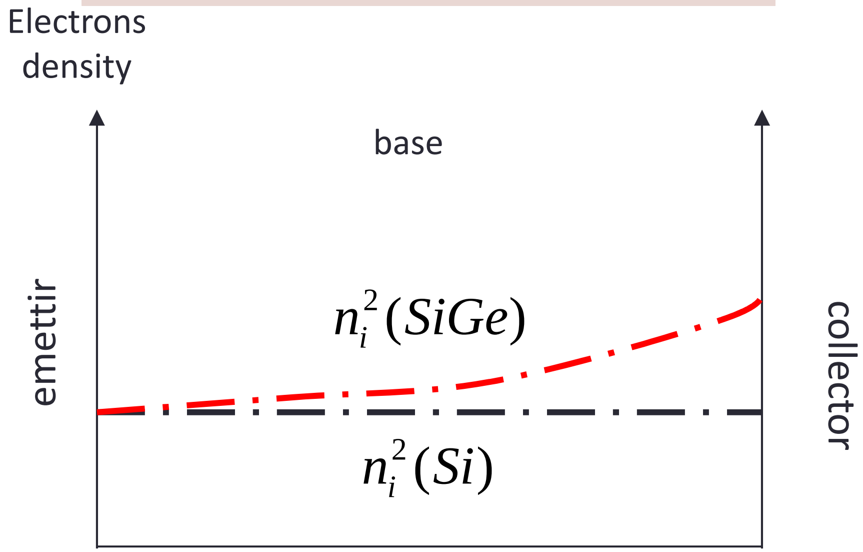


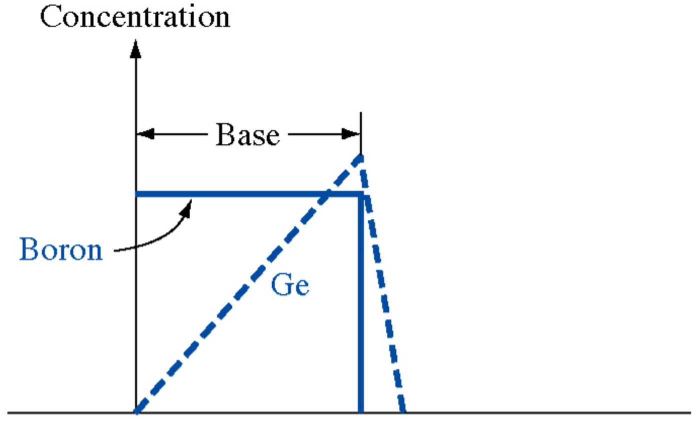

BOTTOM VIEW

# Transistor with a Silicon – Germanium base

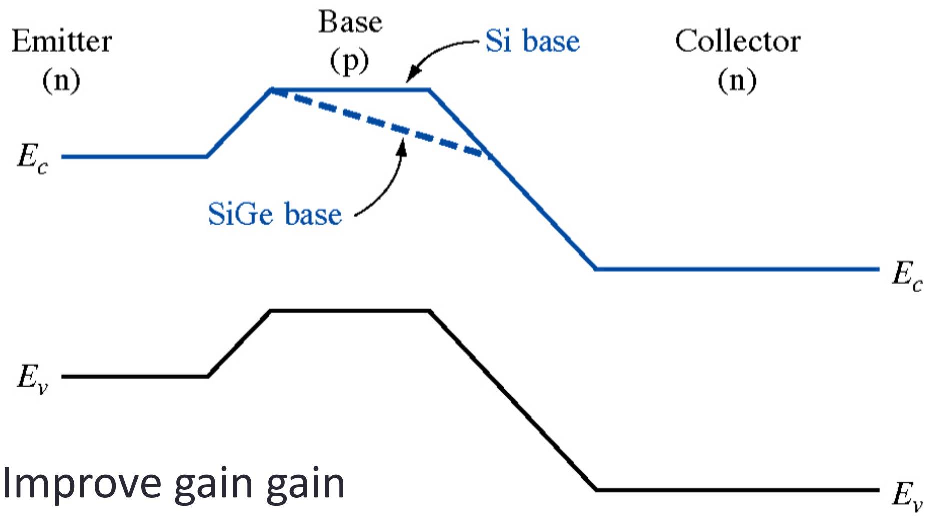
$$I_E = -\left(\frac{Ae^2 n_i^2 D_{nB}}{Q_B + Q_S} + I_{SpE}\right)\exp\frac{eV_{BE}}{kT}$$

$$I_C = +\left(\frac{Ae^2 n_i^2 D_{nB}}{Q_B + Q_S}\right)\exp\frac{eV_{BE}}{kT}$$




(a)




(b)

Improve gain gain

Improve transist time

Increase Early voltage