

MOS CAPACITOR – MOSFET TRANSISTOR – MOS INVERTERS

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Outline

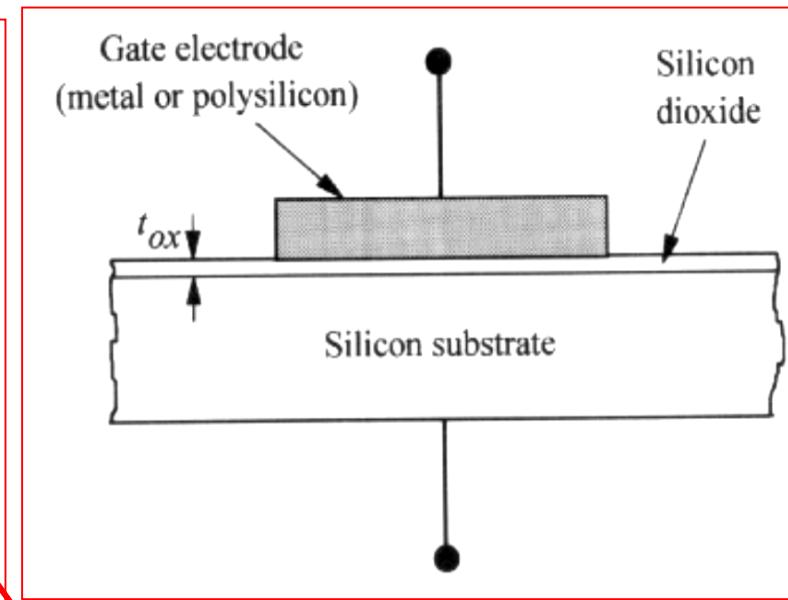
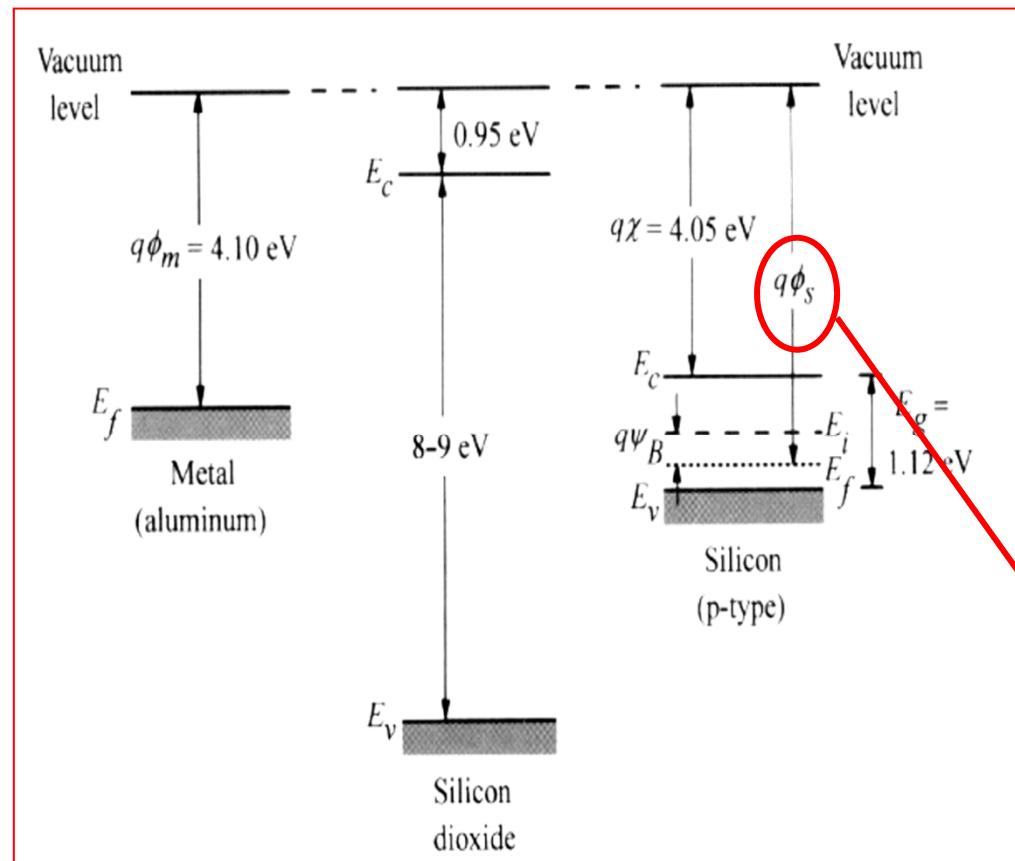
- Metal Oxyde Semiconductor Structure
- MOS Transistor
- MOS Inverters
 - NMOS
 - CMOS

- Two definitions (only 2!)

- Work Function (Travail de sortie) $e\phi_M$: this is the energy we have to give to an electron to extract it of metal without kinetic energy. It reaches the "vacuum level". Work function is the energy difference between the vacuum level and the highest occupied energy level, *i.e* the Fermi level.
- Electron Affinity (Affinité électronique) $e\chi_{SC}$: it's the difference between the vacuum level and the bottom of the conduction band. It's only defined for SC and not for Metal.
- Unity for both of them: eV (electron volt)

Metal Oxyde Semiconductor Structure

Energy band diagram of the three components of a MOS system



MOS capacitor

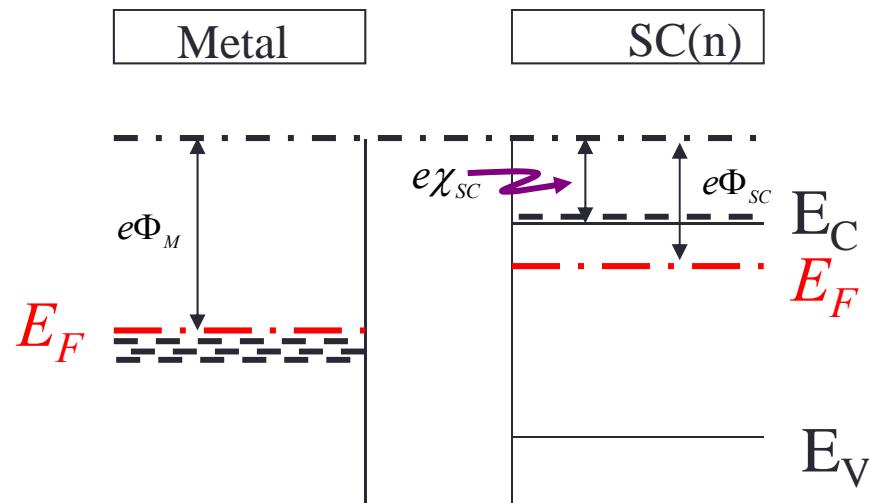
$$\phi_{SC} = \chi_{SC} + \frac{E_g}{2e} + \phi_{fi}$$

Field Effect Transistor

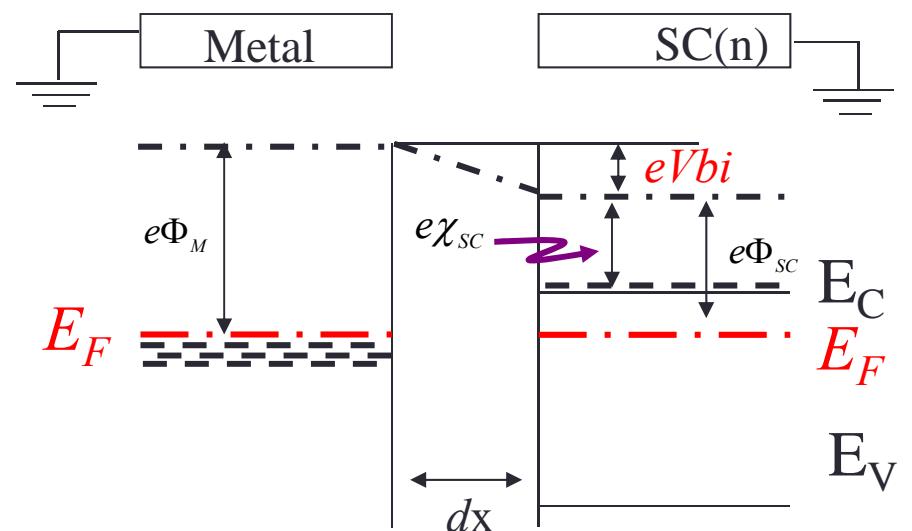
- The field effect is the variation of the conductance of a channel in a semiconductor by the application of an electric field

Equilibrium of MOS structure

$$V_{bi} = \phi_M - \phi_{SC} \quad , \quad E = -\frac{dV}{dx} \quad , \quad \frac{d^2V}{dx^2} = -\frac{\rho(x)}{\epsilon_{SC}}$$



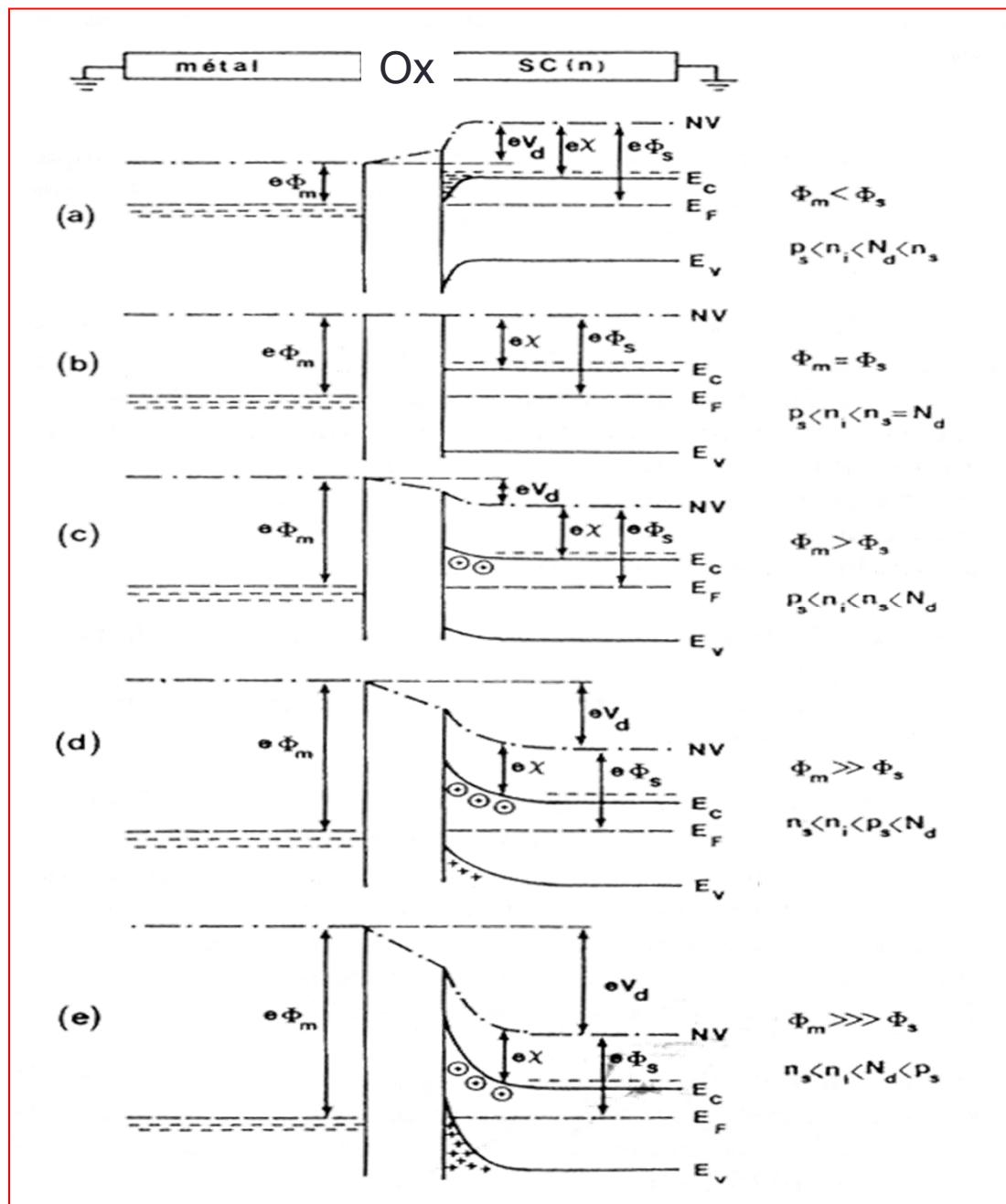
Independant system



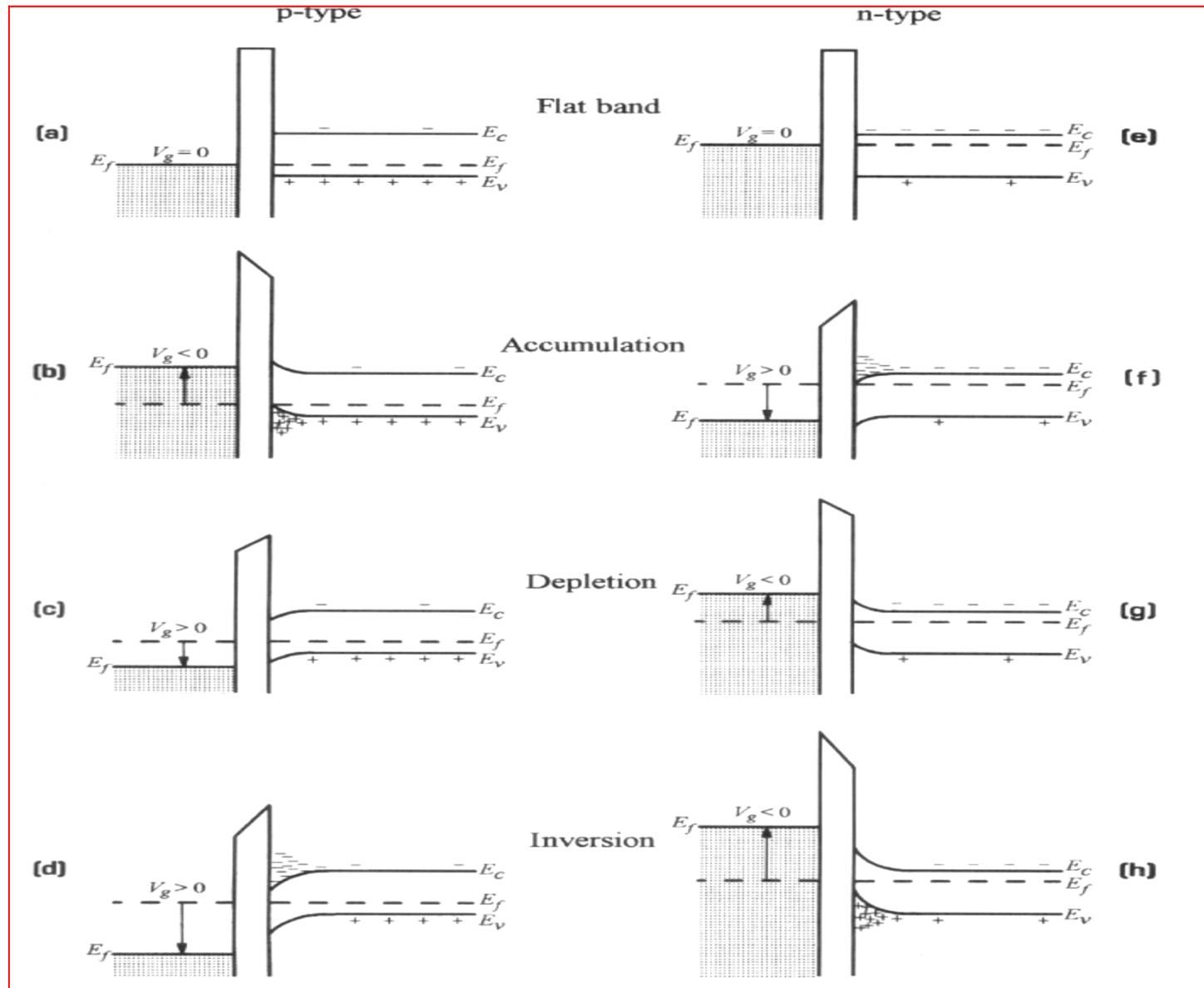
Equilibrium state

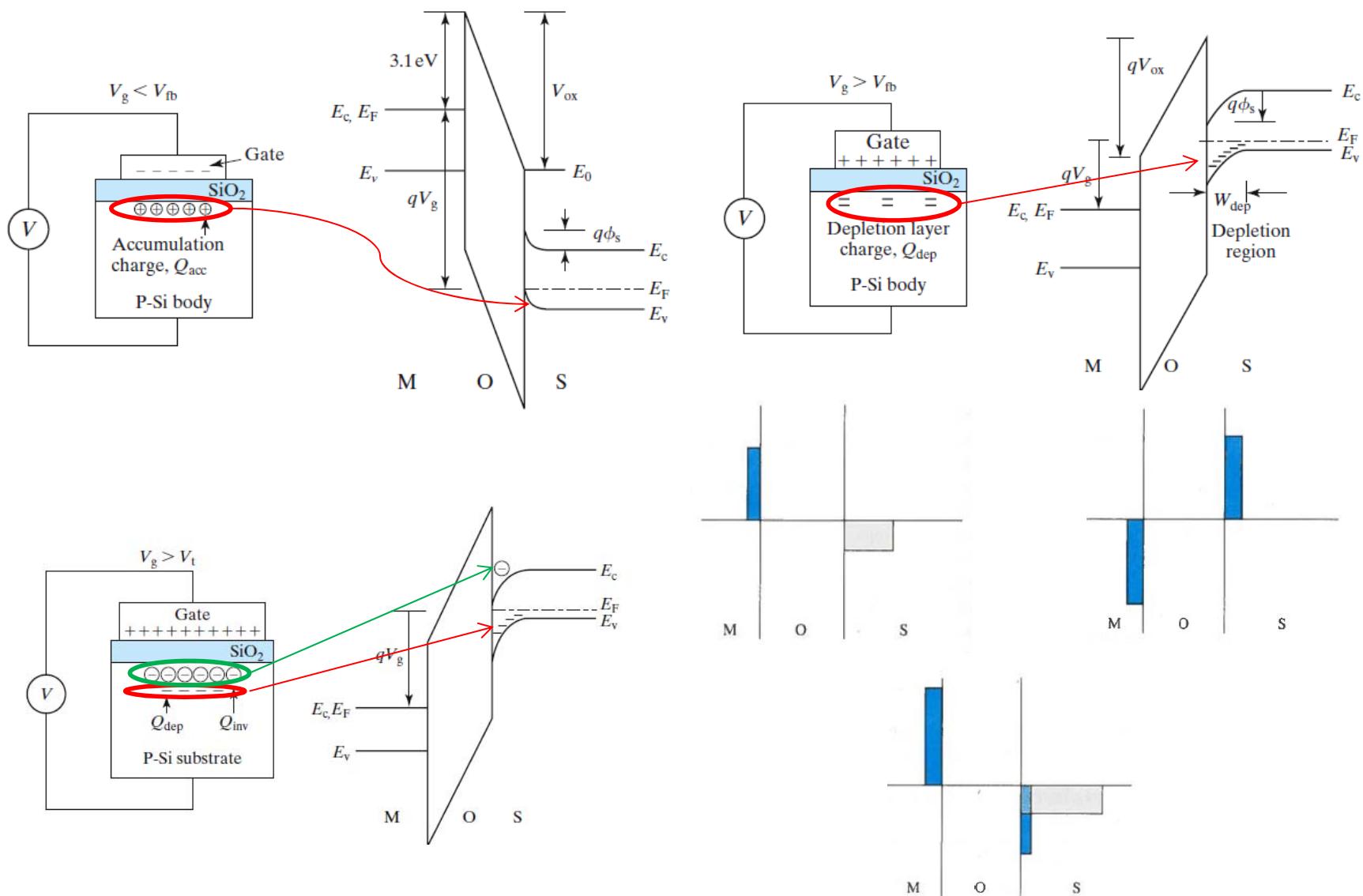
The five regimes : a function of work function

- (a) Accumulation
- (b) Flat band
- (c) Desorption / depletion
- (d) Weak inversion
- (e) Strong inversion



Energy band diagram for ideal n and p type MOS capacitors under different bias conditions





Field, potential and charges in Silicon

We suppose we deal with a **p type** semiconductor:

$$e\phi_{Fi} = |E_F - E_{Fi}| > 0$$

warning: in few books,
absolute value is not
present!!!!

$$V(x = \infty) = 0, \quad V(x = 0) = V_s, \quad V_g$$

Field, potential and charges in Silicon

- Poisson's Equation:

$$\frac{d^2V}{dx^2} = -\frac{\rho(x)}{\epsilon_{SC}}$$

$$\rho(x) = e[p(x) - n(x) + N_D^+(x) - N_A^-(x)] \text{ Charge density}$$

$$p_0 - n_0 = N_A^- - N_D^+$$

$$n_0 = n_i \exp(-\frac{e\phi_{Fi}}{kT})$$

$$p_0 = n_i \exp(\frac{e\phi_{Fi}}{kT})$$

$$n(x) = n_0 \exp(\frac{eV(x)}{kT}) = n_i \exp(\frac{e(V(x) - \phi_{Fi})}{kT})$$

$$p(x) = n_i \exp(-\frac{e(V(x) - \phi_{Fi})}{kT}) = p_0 \exp\left(-\frac{eV(x)}{kT}\right)$$

Field, potential and charges in Silicon

$$\rho(x) = e \left[n_0 - p_0 + p_0 e^{-\frac{eV(x)}{kT}} - n_0 e^{\frac{eV(x)}{kT}} \right]$$

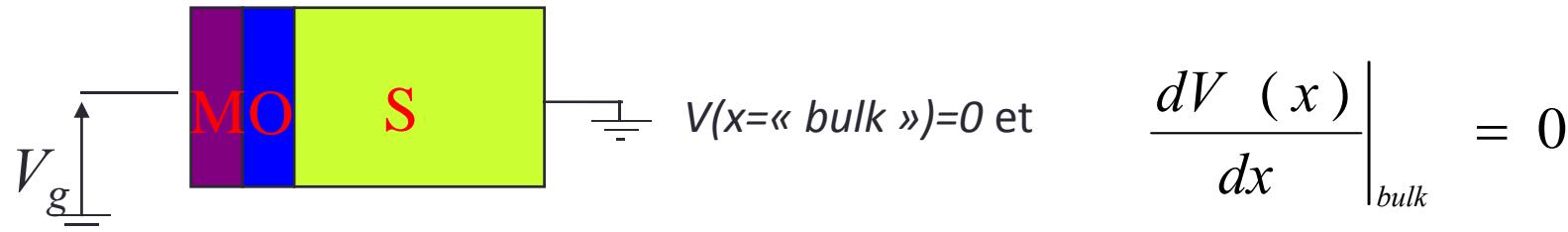
$$\frac{d^2V(x)}{dx^2} = -\frac{e}{\epsilon_{SC}} \left[p_0 (e^{-\frac{eV(x)}{kT}} - 1) - n_0 (e^{\frac{eV(x)}{kT}} - 1) \right]$$

$$\frac{d^2V(x)}{dx^2} = \frac{d}{dx} \left(\frac{dV(x)}{dx} \right) = \frac{d}{dV} \left(\frac{dV(x)}{dx} \right) \frac{dV(x)}{dx}$$

$$\frac{dV(x)}{dx} d \left(\frac{dV(x)}{dx} \right) = -\frac{e}{\epsilon_{SC}} \left[p_0 (e^{-\frac{eV(x)}{kT}} - 1) - n_0 (e^{\frac{eV(x)}{kT}} - 1) \right] dV(x)$$

Field, Potential and Charges in Silicon

- We compute the integral from bulk to a point x in SC



$$\int_0^{dV(x)/dx} \frac{dV(x)}{dx} d\left(\frac{dV(x)}{dx}\right) = -\frac{e}{\epsilon_{SC}} \int_0^{V(x)} \left[p_0 \left(e^{-\frac{eV(x)}{kT}} - 1 \right) - n_0 \left(e^{\frac{eV(x)}{kT}} - 1 \right) \right] dV(x)$$

And the Electric Field is given by: $E(x) = -\frac{dV(x)}{dx}$

$$E^2(x) = \left(\frac{dV(x)}{dx} \right)^2 = \frac{2kTp_0}{\epsilon_{SC}} \left[\left(e^{-\frac{eV(x)}{kT}} + \frac{eV(x)}{kT} - 1 \right) + \frac{n_0}{p_0} \left(e^{\frac{eV(x)}{kT}} - \frac{eV(x)}{kT} - 1 \right) \right]$$

Field, potential and charges in Silicon

$$E^2(x) = \left(\frac{dV(x)}{dx} \right)^2 = \left(\frac{kT}{e} \right)^2 \frac{2}{L_D^2} \left[\left(e^{-eV(x)/kT} + \frac{eV(x)}{kT} - 1 \right) + \frac{n_0}{p_0} \left(e^{eV(x)/kT} - \frac{eV(x)}{kT} - 1 \right) \right]$$

With the Debye length:

$$L_D = \sqrt{\frac{\epsilon_{SC} kT}{2e^2 p_o}} = \sqrt{\frac{\epsilon_{SC} kT}{2e^2 N_a}}$$

If we use the Gauss's theorem:

$$E(x=0) = E_S = -\frac{Q_{SC}}{\epsilon_{SC}}$$

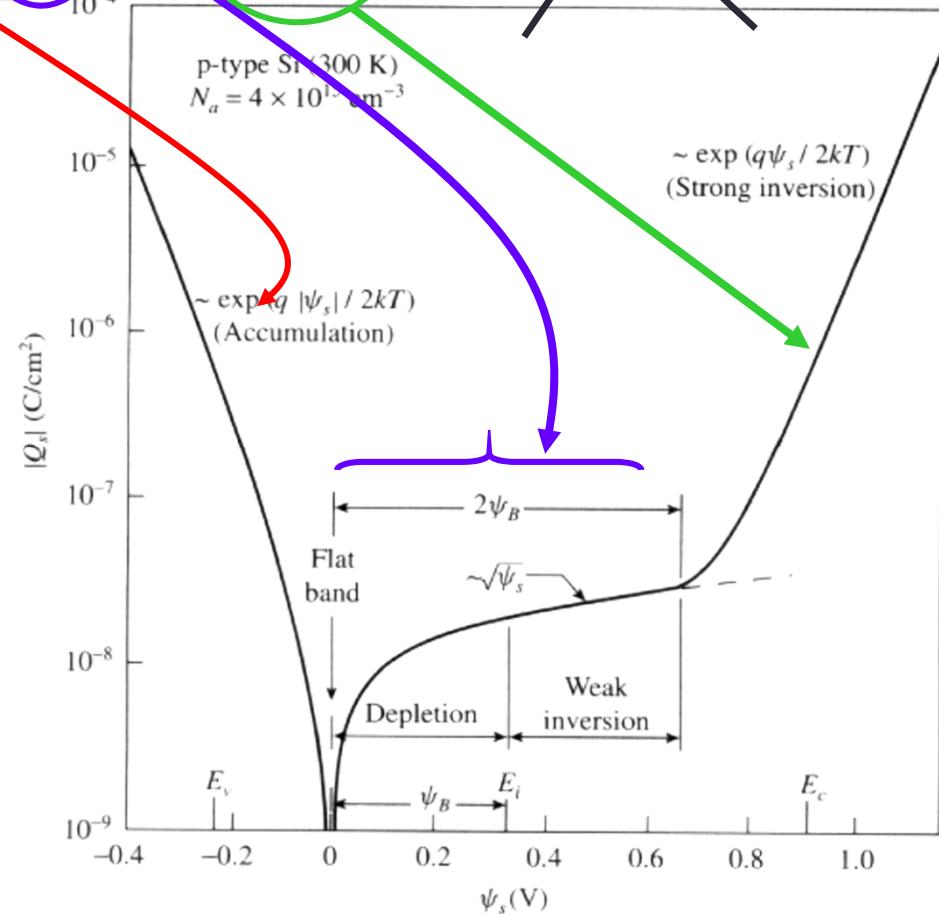
$$Q_{SC} = \pm \left(\frac{kT}{e} \right) \frac{\epsilon_{SC} \sqrt{2}}{L_D} \left[e^{-eV_S/kT} + \frac{eV_S}{kT} - 1 + e^{e(V_S - 2\phi_{FI})/kT} - \frac{n_0}{p_0} \left(\frac{eV_S}{kT} + 1 \right) \right]^{1/2} = -Q_{metal}$$

Field, potential and charges in Silicon

Allways negligible
(p type)

$$Q_{SC} = \pm \left(\frac{kT}{e} \right) \frac{\epsilon_{SC} \sqrt{2}}{L_D} \left[e^{-eV_S/kT} + \frac{eV_S}{kT} - 1 + e^{e(V_S - 2\phi_{FI})/kT} - \frac{n_0}{p_0} \left(\frac{eV_S}{kT} + 1 \right) \right]^{1/2} = -Q_{metal}$$

- For V_s (and so V_g) negative (accumulation)
- For V_s (and V_g) positive but less than $2\Phi_{fi}$ (depletion – weak inversion)
- For V_s (and Vg) $> 2\Phi_{fi}$ (strong inversion)



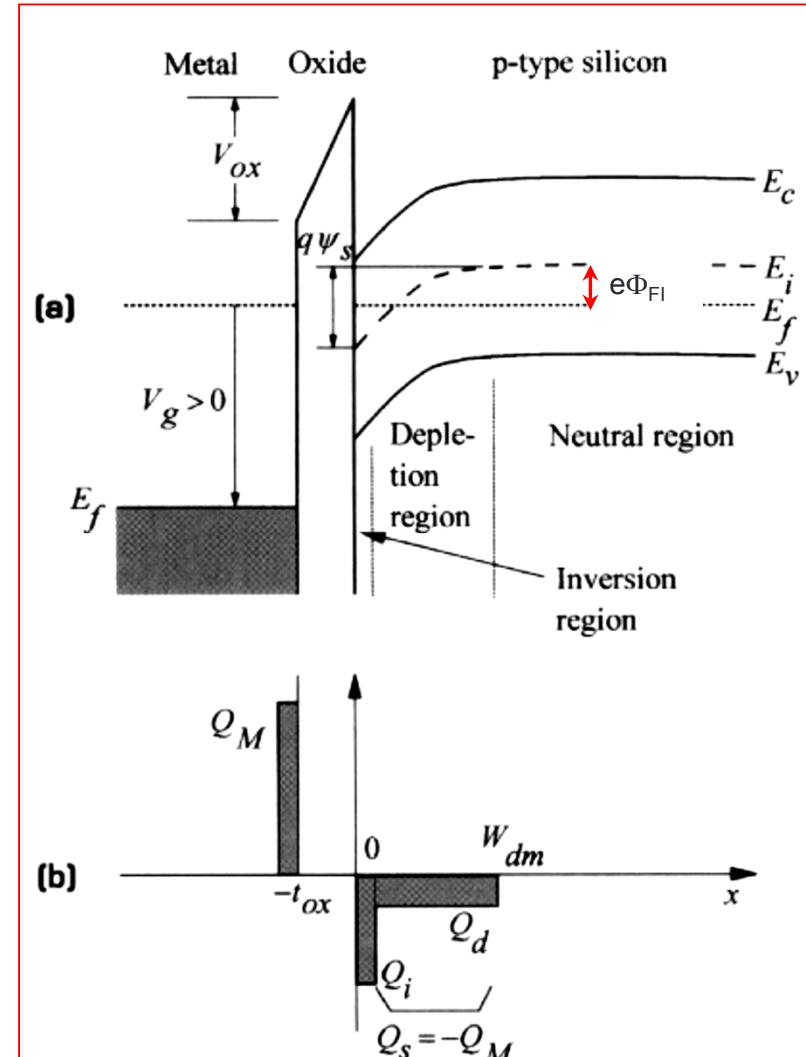
Weak / Strong Inversion

$$V_S = 2\phi_{Fi} = \frac{2kT}{e} \ln\left(\frac{N_A}{n_i}\right)$$

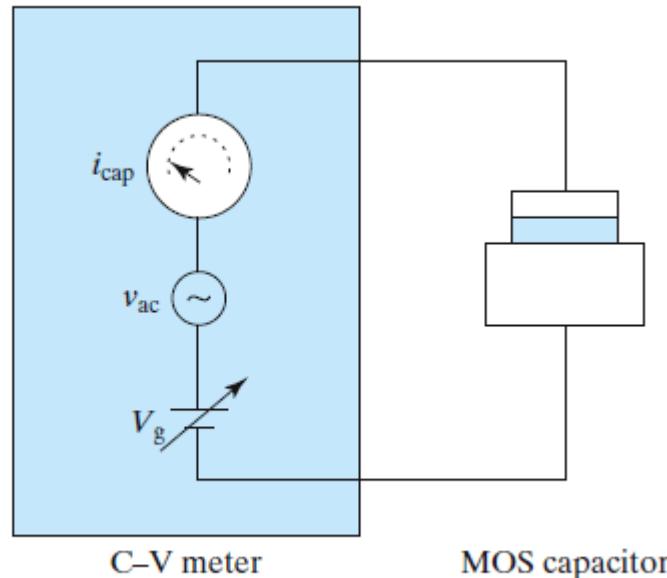


$$n_s = p_0 = N_A$$

This condition will define a very important parameter of the structure: the **threshold voltage** or the required gate voltage to put the transistor in strong inversion regime



Measurement of capacitance in Ideal MOS Structure



Setup for the C-V measurement.

The C-V curve is usually measured with a CV meter:

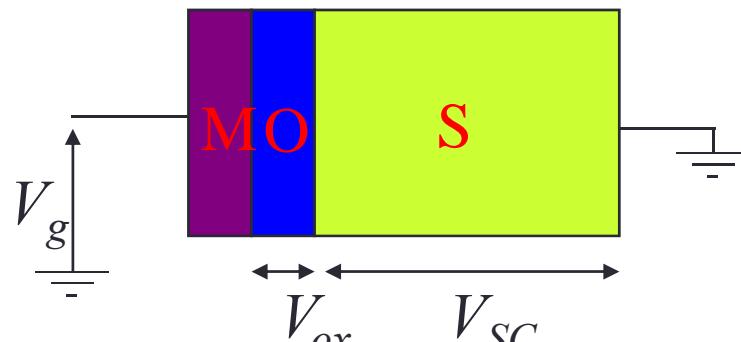
- We apply a DC bias voltage V_g + small sinusoidal signal (100 Hz to 10 MHz)
- We measure the capacitive current with an AC meter (90 degree phase shift)
=> $i_{cap}/v_{ac} = \omega C$

Measurement of capacitance in Ideal MOS Structure

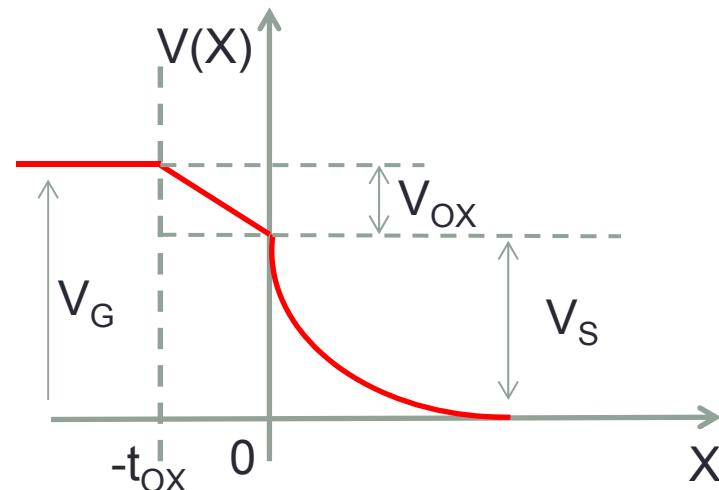
When a voltage V_g is applied on the MOS Gate, part of it appears as a potential drop across oxide and the rest of it appears as a band bending V_s in silicon:

$$V_g = V_{ox} + V_{SC} = \frac{-Q_{SC}}{C_{ox}} + V_s$$

SC is grounded,
so $V_{SC}=V_s$



Oxide and Silicon have capacitor behavior



Measurement of capacitance in Ideal MOS Structure

- Oxide capacitance: as a parallel-plate capacitor

$$C_{ox} = \frac{\epsilon_{ox}}{d_{ox}} \text{ F/cm}^2$$

- We can also write :

$$C_{ox} = \frac{Q_M}{V_{ox}} = \frac{Q_M}{(V_G - V_S)} = \frac{dQ_M}{d(V_G - V_S)}$$

$$\frac{1}{C_{ox}} = \frac{dV_G}{dQ_M} - \frac{dV_S}{dQ_M}$$

Measurement of capacitance in Ideal MOS Structure

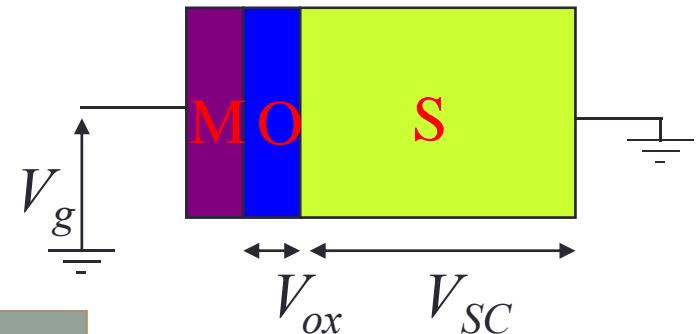
- *Semiconductor (silicon) capacitance*

$$C_{SC} = \frac{\delta(\text{charge in SC})}{\delta(\text{voltage across SC})} = \frac{d(-Q_{SC})}{dV_S} = \frac{d(Q_M)}{dV_S}$$

$$\frac{1}{C_{SC}} = \frac{dV_S}{dQ_M}$$

Measurement of capacitance in Ideal MOS Structure

- Global capacitance of the structure:



$$C_{MOS} = \frac{dQ_M}{dV_G} = -\frac{dQ_{SC}}{dV_G}$$

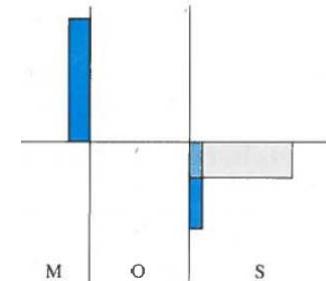
- If we combine the 3 relations above :

$$\frac{1}{C_{ox}} = \frac{dV_G}{dQ_M} - \frac{dV_S}{dQ_M} = \frac{1}{C_{MOS}} - \frac{1}{C_{SC}}$$

$$\frac{1}{C_{MOS}} = \frac{1}{C_{ox}} + \frac{1}{C_{SC}} \Leftrightarrow 2 \text{ capacitances connected in serie}$$

Measurement of capacitance in Ideal MOS Structure

- Total charge Q_{SC} depends on different regimes
↔ 2 types of charges, fixed and mobile/free:



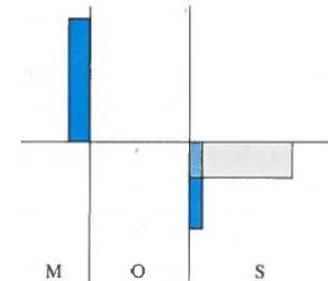
$$Q_{SC} = \text{free carriers charges} + \text{fixed charges} = Q_s + Q_{dep}$$

→ Semiconductor capacitance can be written as:

$$C_{SC} = \frac{-dQ_{sc}}{dV_s} = \frac{-(dQ_s + dQ_{dep})}{dV_s} = -\frac{dQ_s}{dV_s} - \frac{dQ_{dep}}{dV_s}$$

Measurement of capacitance in Ideal MOS Structure

- Total charge in SC depends on different regimes
↔ 2 types of charges, fixed and mobile/free:



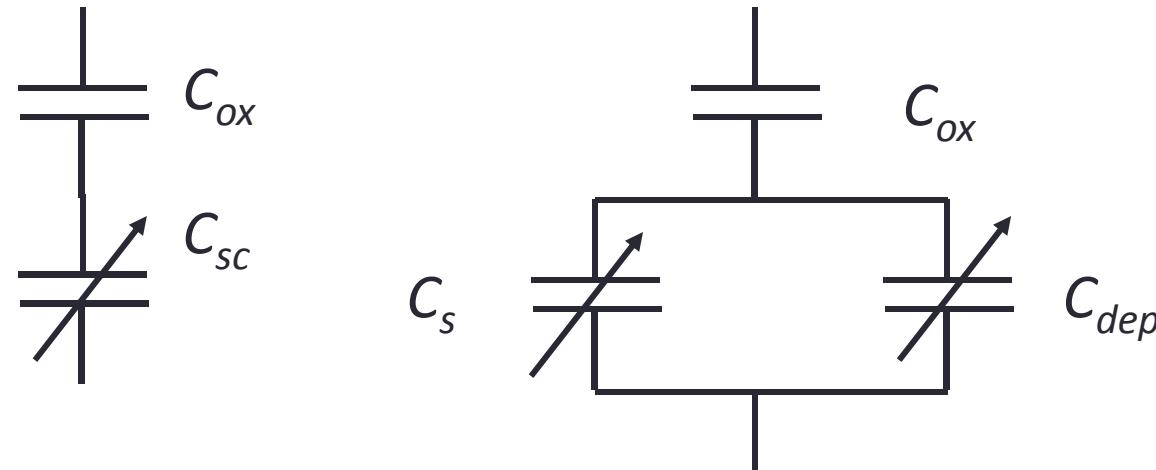
$$Q_{sc} = \text{free carriers charges} + \text{fixed charges} = Q_s + Q_{dep}$$

→ Semiconductor capacitance can be written as:

$$C_{sc} = \frac{-dQ_{sc}}{dV_s} = C_s + C_{dep}$$

Measurement of capacitance in Ideal MOS Structure

- Summary: MOS capacitor is equivalent :
 - of 2 capacitors connected in serie, C_{ox} and C_{sc}
 - C_{sc} is equivalent of two capacitors
 - the two are variable and be view as 2 capacitors in //



Conclusion: the total capacitance of MOS structure is function of bias conditions or operating regime through C_{sc}

Capacitance of MOS structure

- Accumulation Regime: $V_S < 0$ ie $V_G < 0$

$$Q_{SC} = \pm \left(\frac{kT}{e} \right) \frac{\varepsilon_{SC} \sqrt{2}}{L_D} \left[e^{-eV_S/kT} + \frac{eV_S}{kT} - 1 + e^{e(V_S - 2\phi_{FI})/kT} - \frac{n_0}{p_0} \left(\frac{eV_S}{kT} + 1 \right) \right]^{1/2} = -Q_{metal}$$

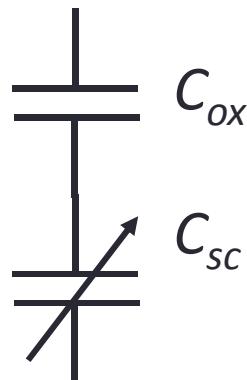
$$Q_{SC} \approx \frac{\varepsilon_{SC} \sqrt{2} kT}{e L_D} e^{-\frac{eV_S}{2kT}} > 0$$

$$C_{SC} = \frac{-dQ_{SC}}{dV_s} = \frac{e}{2kT} Q_{SC} = \frac{e}{2kT} C_{ox} |V_g - V_S|$$

Capacitance of MOS structure

- Accumulation Regime: $V_S < 0$ ie $V_G < 0$

$$Q_{SC} = \pm \left(\frac{kT}{e} \right) \frac{\varepsilon_{SC} \sqrt{2}}{L_D} \left[e^{-eV_S/kT} - \frac{eV_S}{kT} - 1 + \frac{n_0}{p_0} \left(e^{eV_S/kT} - \frac{eV_S}{kT} - 1 \right) \right]^{1/2} = -Q_{metal}$$



$$\frac{1}{C_{MOS}} = \frac{1}{C_{ox}} + \frac{1}{C_{SC}} = \frac{1}{C_{ox}} + \frac{2kT/e}{|V_g - V_S|}$$

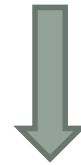
$$\frac{1}{C_{MOS}} = \frac{1}{C_{ox}} \left(1 + \frac{2kT/e}{|V_g - V_S|} \right)$$

Capacitance of MOS structure

- Accumulation Regime: $V_S < 0$ ie $V_G < 0$

$$Q_{SC} = \pm \left(\frac{kT}{e} \right) \frac{\varepsilon_{SC} \sqrt{2}}{L_D} \left[e^{-eV_S/kT} - \frac{eV_S}{kT} - 1 + \frac{n_0}{p_0} \left(e^{eV_S/kT} - \frac{eV_S}{kT} - 1 \right) \right]^{1/2} = -Q_{metal}$$

- $kT=26$ meV, in accumulation regime V_S is around -0,3 V to -0,4 V, \Leftrightarrow as soon as $V_G < -1$ to -2 V, so we can simplify to:



$$\frac{1}{C_{MOS}} = \frac{1}{C_{ox}} \left(1 + \frac{2kT}{|V_g - V_S|} \right) \underset{\cancel{2kT/e}}{\approx} \frac{1}{C_{ox}}$$

Capacitance of MOS structure

- Flat Band: $V_S = 0 \text{ V}$ ie $V_G = 0 \text{ V}$
(warning : ideal structure!!!!)

Analytical computing: ||| 

$$C_{SC}(fb) = \frac{\epsilon_{SC}}{L_D}$$

$$C_{MOS}(fb) = \frac{\epsilon_{ox}}{d_{ox} + \frac{\epsilon_{ox}}{\epsilon_{SC}} L_D} = \frac{\epsilon_{ox}}{d_{ox} + \frac{\epsilon_{ox}}{\epsilon_{SC}} \sqrt{\frac{kT}{2e^2} \frac{\epsilon_{SC}}{N_A}}} \approx C_{ox}$$

$\ll d_{ox}$

Capacitance of MOS structure

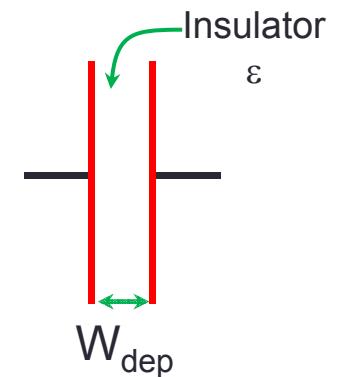
- Depletion regime and weak inversion



$$0 < V_S < 2\phi_{Fi}$$

$$Q_{SC} = -\frac{\sqrt{2}\epsilon_{SC}kT}{eL_D} \left(\frac{eV_S}{kT} \right)^{\frac{1}{2}} = -[2eN_A\epsilon_{SC}V_S]^{\frac{1}{2}} = Q_{dep} < 0$$

$$C_{SC} = -\frac{dQ_{SC}}{dV_S} = \left(\frac{eN_A\epsilon_{SC}}{2V_S} \right)^{\frac{1}{2}} = \frac{\epsilon_{SC}}{W_{dep}}$$



Capacitance of MOS structure

- Depletion regime and weak inversion



$$0 < V_S < 2\phi_{Fi}$$

$$C_{SC} = -\frac{dQ_{SC}}{dV_S} = \left(\frac{eN_A \epsilon_{SC}}{2V_S} \right)^{1/2} = \frac{\epsilon_{SC}}{W_{dep}}$$

$$C_{MOS}(\text{depletion}) = \frac{\epsilon_{ox}}{d_{ox} + \frac{\epsilon_{ox}}{\epsilon_{SC}} W_{dep}} = \frac{C_{ox}}{\sqrt{1 + (2C_{ox}^2 V_g / \epsilon_{SC} e N_A)}}$$

Capacitance of MOS structure

- Strong inversion

$$V_S > 2\phi_{FI}$$

$$Q_{SC} = \pm \left(\frac{kT}{e} \right) \frac{\varepsilon_{SC} \sqrt{2}}{L_D} \left[e^{-eV_S/kT} + \frac{eV_S}{kT} - 1 + e^{e(V_S - 2\phi_{FI})/kT} - \frac{n_0}{p_0} \left(\frac{eV_S}{kT} + 1 \right) \right]^{1/2} = -Q_{metal}$$

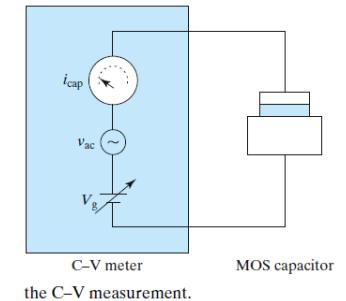
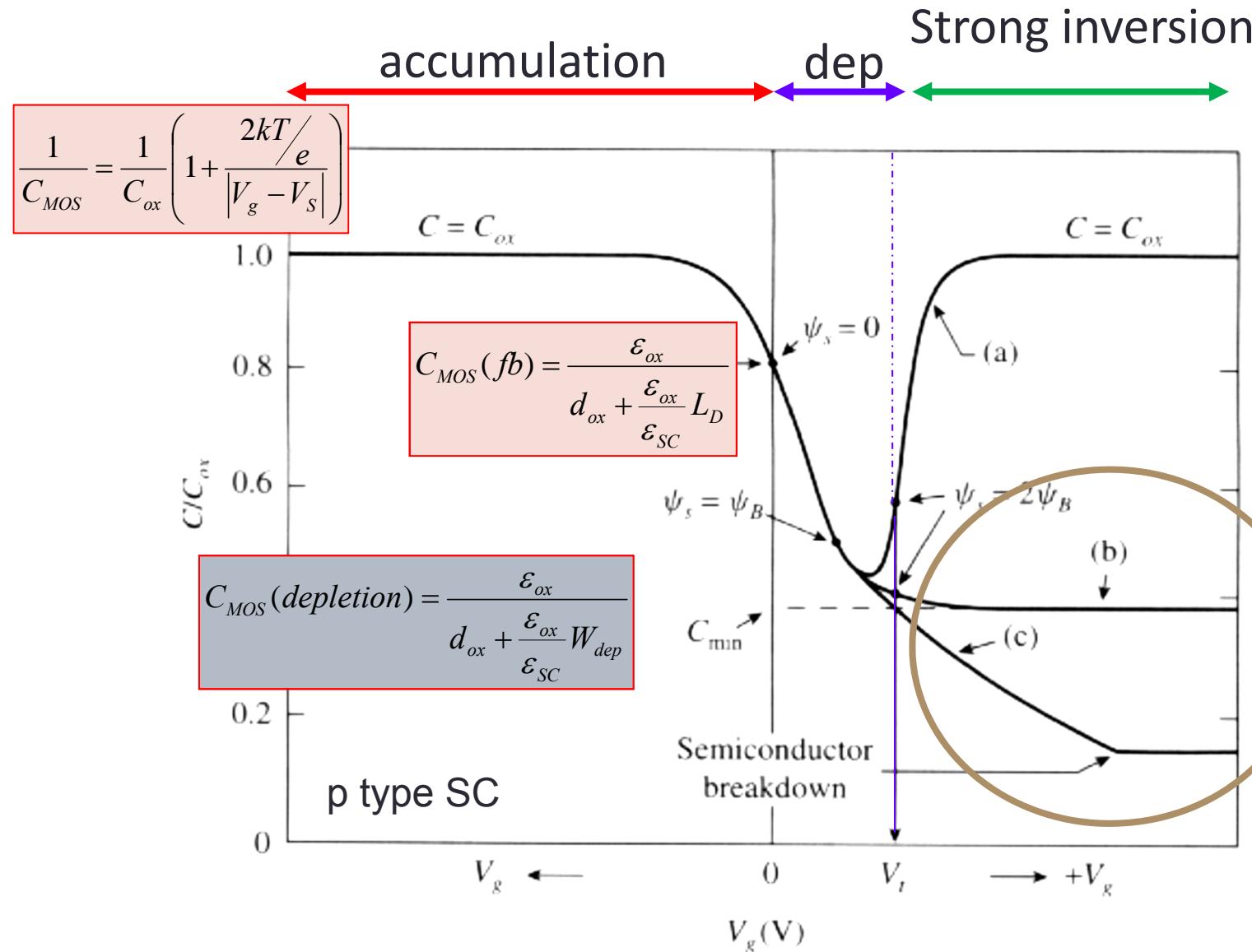
$$Q_{SC} \approx - \frac{\varepsilon_{SC} \sqrt{2} kT}{e L_D} e^{\frac{e(V_S - 2\phi_{FI})}{2kT}} < 0$$

$$C_{SC} = \frac{-dQ_{SC}}{dV_s} = \frac{\varepsilon}{\sqrt{2} L_D} e^{\frac{e(V_s - 2\phi_{FI})}{2kT}}$$

⇒

$$\frac{1}{C_{MOS}} = \frac{1}{C_{ox}} + \frac{1}{C_{SC}} \approx \frac{1}{C_{ox}}$$

Capacitance of MOS structure



???

Capacitance of MOS structure

- Strong inversion:



Which mechanism governs the onset of strong inversion layer?

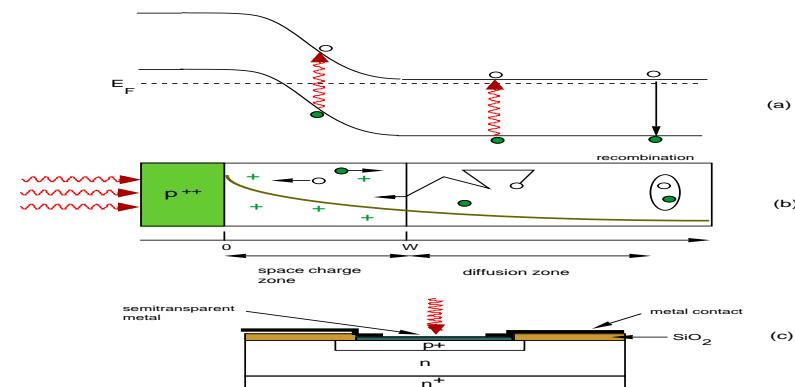
- P type SC : we must create electrons at oxide/SC interface. Where they come from?
 - From Metal : **NO** because oxide barrier
 - From SC (neutral region) : **NO** minority carriers (e-)



Only one solution: thermal (or optical) generation

Capacitance of MOS structure

- Strong inversion:
 - Thermal generation?
 - #1 :In the space charge + dissipation of charge by electric field
 - #2 : In the neutral region



First mechanism dominates but it's a slow one.



Capacitance of MOS structure

- Strong inversion
 - Which Delay time to create strong inversion layer ?

Shockley-Read equation

$$g_{th} = \frac{n_i}{2\tau_m}$$

Strong inversion limit: $n_s = N_A$

$$g_{th}\tau_s = N_A$$

\Rightarrow

$$\tau_s = 2 \frac{N_A}{n_i} \tau_m$$

More realistic

$$\tau_s = 1 - 10 \frac{N_A}{n_i} \tau_m$$

Si:

$$n_i = 10^{10} \text{ cm}^{-3}$$

$$N_A = 10^{15} \text{ cm}^{-3}$$

$$\tau_m = 10^{-5} \text{ s}$$

$$\tau_s = 1 \text{ s} !!$$

Capacitance of MOS structure

- When we measure $C(V)$, results depend on YES or NO, we give enough time to create this layer
 - YES: we measure capacitance due to inversion layer
 - NO : Depletion layer preserves the neutrality of the system with an increase of its width . The limit is the breakdown of the semiconductor



Results are frequency dependant

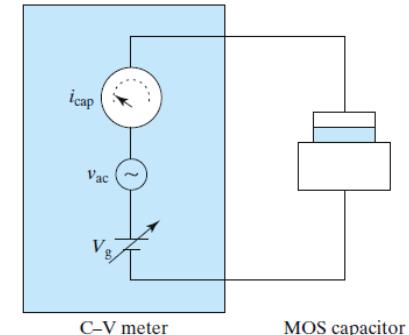
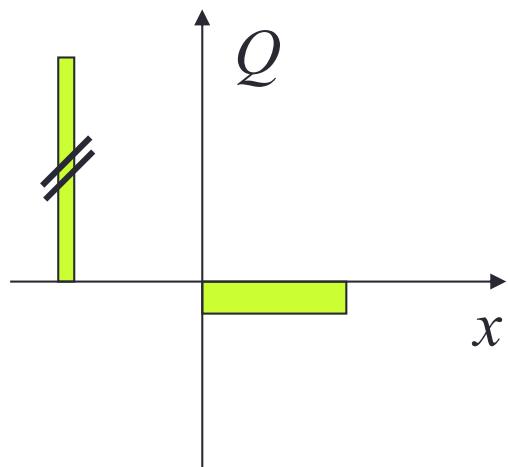
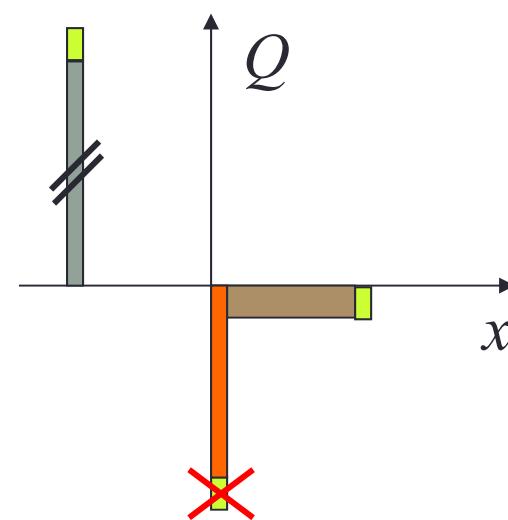
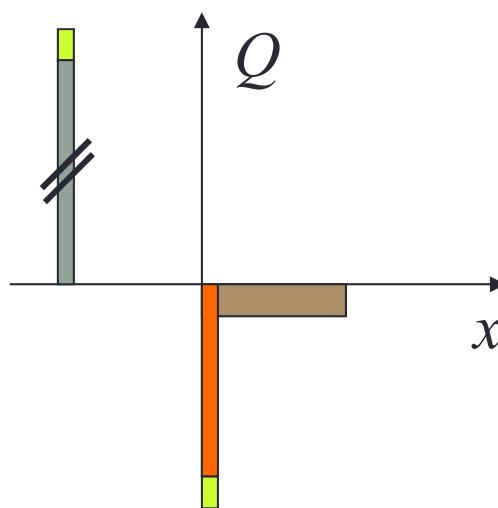
Capacitance of MOS structure: strong inversion

3 cases :

Low frequency
+
Slow ramp V_g

High frequency
+
Slow ramp V_g

High frequency
+
High ramp V_g



Setup for the C-V measurement.

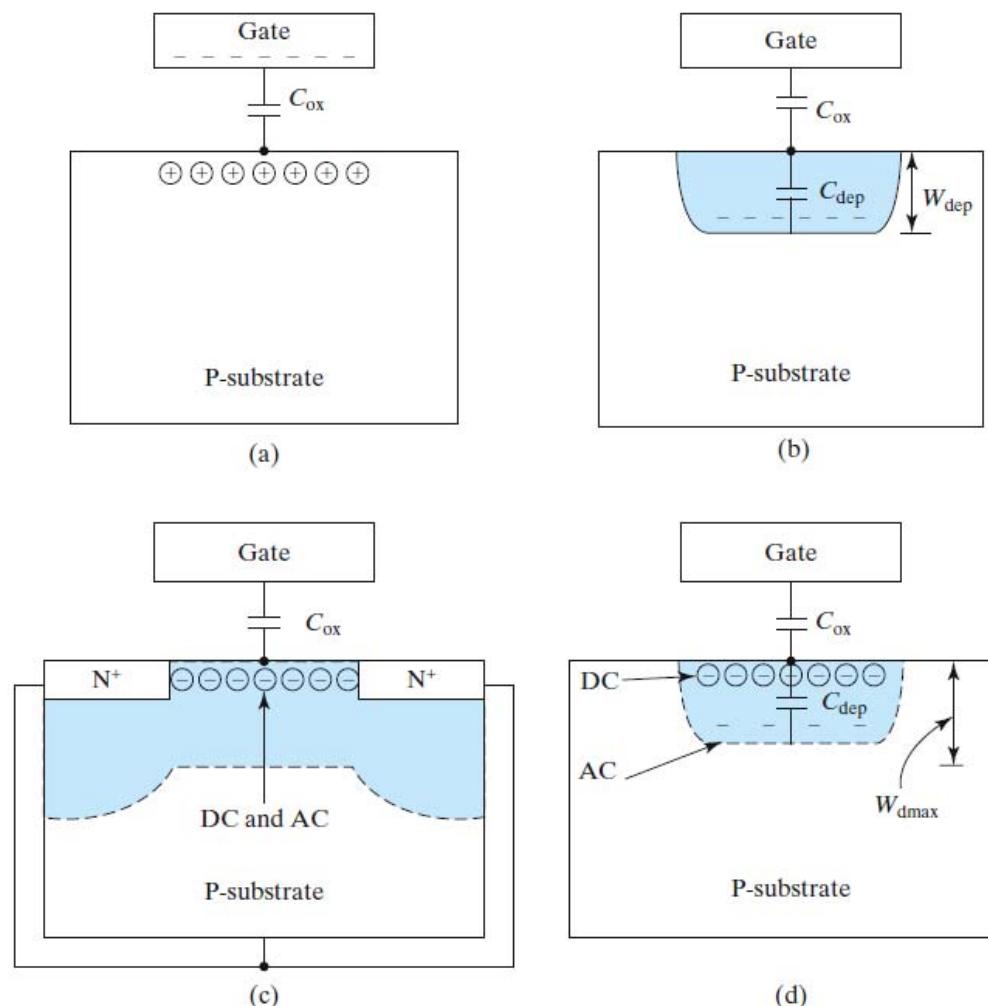


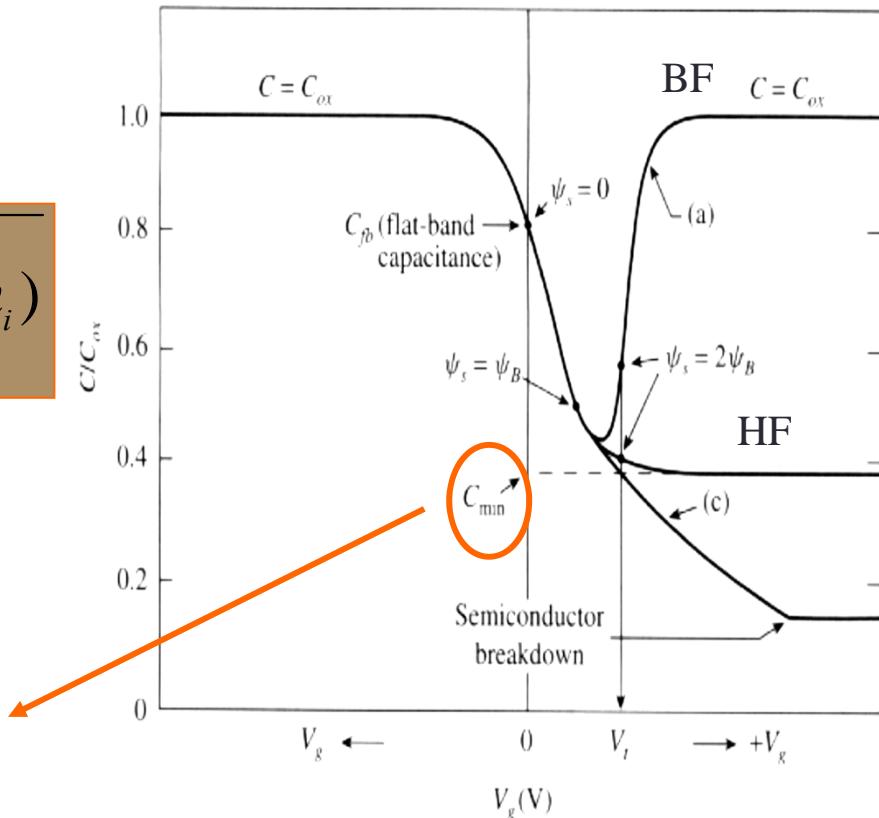
FIGURE 5-17 Illustration of the MOS capacitor in all bias regions with the depletion-layers shaded. (a) Accumulation region; (b) depletion region; (c) inversion region with efficient supply of inversion electrons from the N region corresponding to the transistor $C-V$ or the quasi-static $C-V$; and (d) inversion region with no supply of inversion electrons (or weak supply by thermal generation) corresponding to the high-frequency capacitor $C-V$ case.

Capacitance of MOS structure: strong inversion

- minimum capacitance (HF):

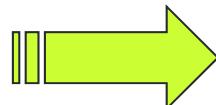
$$W_{\max} = \sqrt{\frac{2\varepsilon_{sc}}{eN_A} 2\phi_{Fi}} = \sqrt{\frac{4\varepsilon_{sc} kT}{e^2 N_A} \ln(N_A / n_i)}$$

$$\frac{1}{C_{\min}} = \frac{1}{C_{ox}} + \sqrt{\frac{4kT \ln(N_A / n_i)}{\varepsilon_{sc} e^2 N_A}}$$



MOS capacitor : parasitic effects

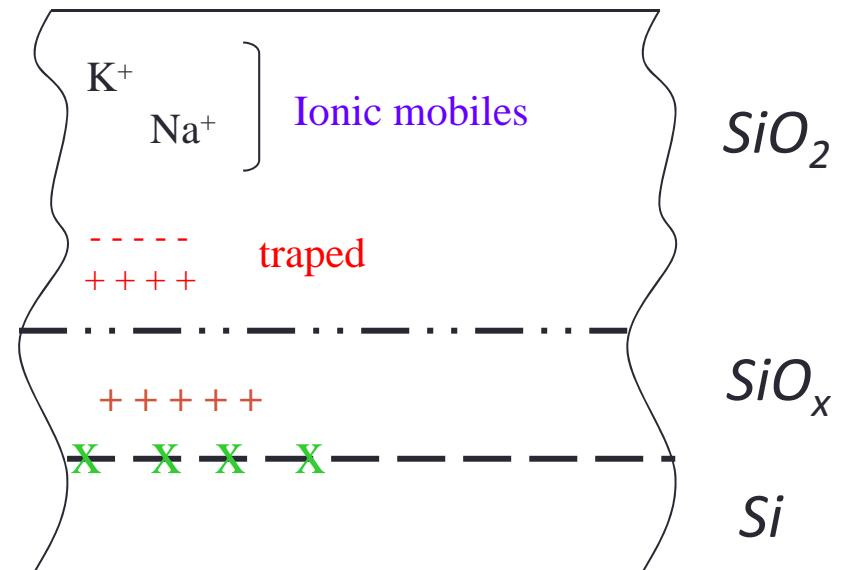
- 2 factors modify « ideal » structure of MOS capacitor.
 - The charges in oxide and/or charges at interface Oxide – SC.
 - The difference between the work function of the Metal and the SC



Influence on the threshold voltage V_T of the structure.

MOS capacitor :oxide charge

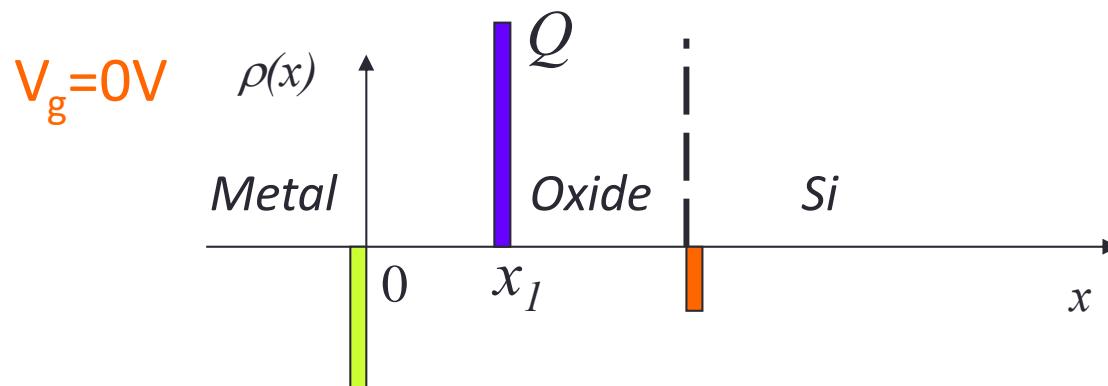
- Distribution of charges in the oxide :
 - Mobile ionic charges
 - Oxide traped charges
 - Fixed oxide charges
 - Traped charges at Si-SiO₂ interface



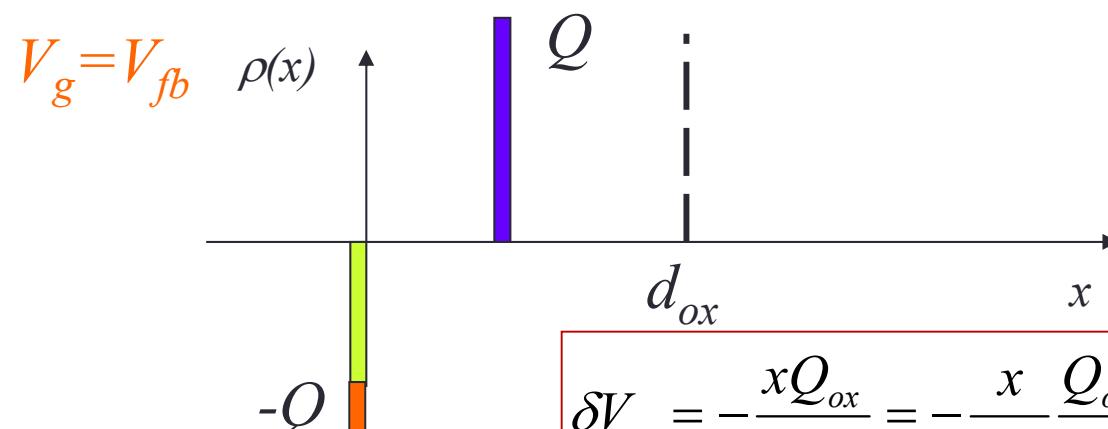
Depending on their position in the oxide, the charges will influence more or less on the electron population below the gate.

MOS capacitor :oxide charge

- Effect of a sheet charge of a real density Q within the oxide layer of an MOS capacitor:*



Oxide charges are compensated with charges in Metal AND SC.



If $V_g = V_{fb}$, charges in SC must be zero. Only Metal « DO the job »

$$\delta V_g = -\frac{x Q_{ox}}{\epsilon_{ox}} = -\frac{x}{d_{ox}} \frac{Q_{ox}}{C_{ox}}$$

MOS capacitor :oxide charge

- The effect is maximum when the charges are located at the interface oxide - SC, ie $Q_{ox} = Q_{SS}$ (*and no effect if Q_{ox} close to Metal*)

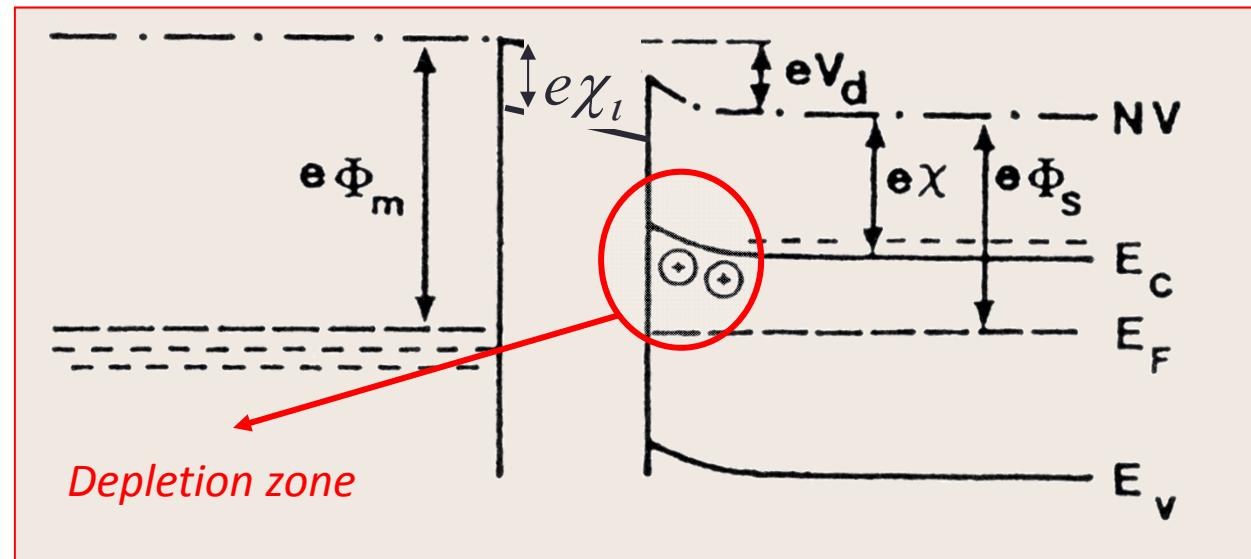
$$x = d_{ox} \implies \delta V_g = -\frac{Q_{ss}}{C_{ox}}$$

It is a common practice to define an equivalent oxide charge per unit area Q_{ox} located at the oxide – silicon interface (named Q_{ss}):

$$\Delta V_g(V_s) = -\frac{Q_{ox}(V_s)}{C_{ox}} = -\frac{Q_{ss}(V_s)}{C_{ox}} = V_{FB}$$

Work function difference

- Work function difference \Leftrightarrow non zero oxide field.
 - Even when $V_g = 0$ V, structure show a band bending



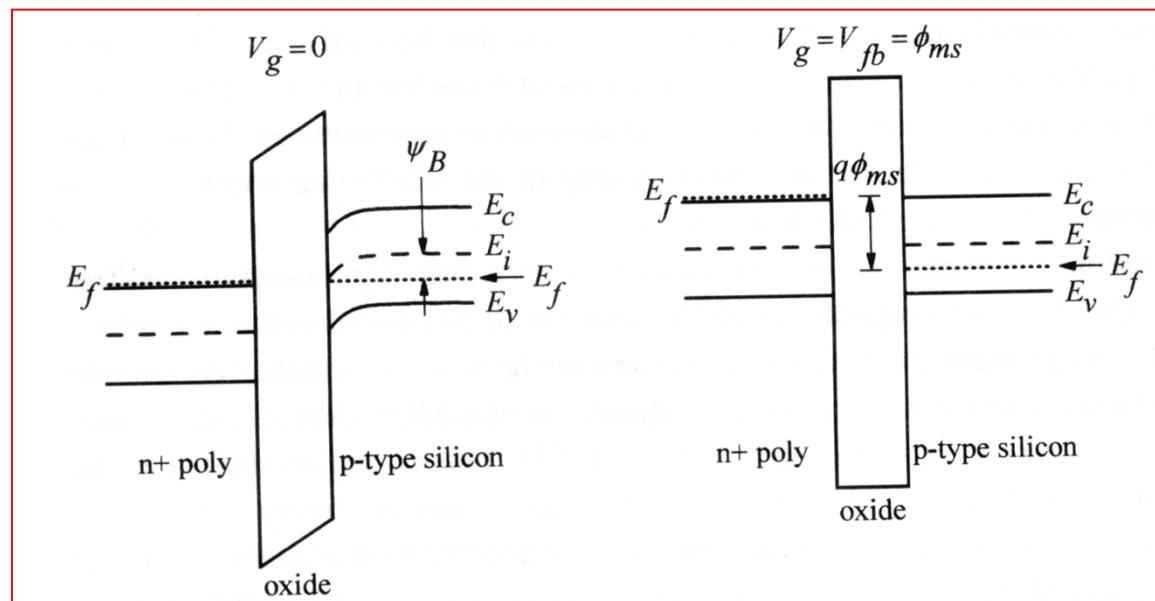
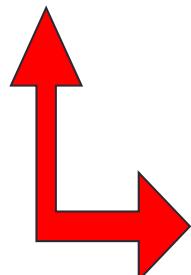
A gate voltage must be applied to restore the flat band condition $\Leftrightarrow V_{FB} = \phi_M - \phi_S = \phi_{MS}$: this voltage is called Flat Band voltage V_{FB}

Work function difference

- Work function difference.
 - Example: polysilicon n⁺ gate on p-MOS

$$\phi_{poly_{n^+}} = e\chi_{silicium}$$

$$\phi_{SC} = \chi_{Silicium} + \frac{E_g}{2e} + \phi_{fi}$$



$$V_{FB} = \varphi_{MS}^{poly} = -\frac{E_g}{2e} - \varphi_{fi} = -0.56 - \frac{kT}{e} \ln\left(\frac{N_a}{n_i}\right) < 0$$

Non ideal MOS capacitor

- Taking into account both Oxide charges and work-function difference, the global flat band voltage can be written as:

$$V_{FB} = \phi_{MS} - \frac{Q_{ox}}{C_{ox}}$$

Warning: this is the **voltage** we have to **apply** on the gate to **restore** de flat band condition.

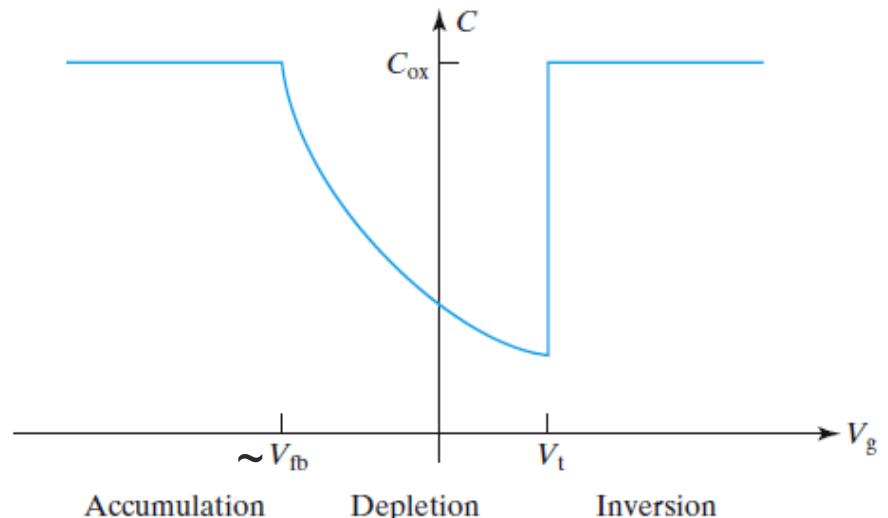
Capacitance of Non ideal MOS structure:

- Imagine the depletion regime of the MOS capacitor ($Q_{ss}=0$)
- We know that :

$$V_{ox} = -\frac{Q_{dep}}{C_{ox}} = \frac{eN_a W_{dep}}{C_{ox}} = \frac{\sqrt{eN_a 2\varepsilon_{sc} V_s}}{C_{ox}}$$

$$V_s = \frac{eN_a W_{dep}^2}{2\varepsilon_{sc}}$$

$$V_g = V_{ox} + V_s + V_{fb} = \frac{eN_a W_{dep}}{C_{ox}} + \frac{eN_a W_{dep}^2}{2\varepsilon_{sc}} + V_{fb}$$



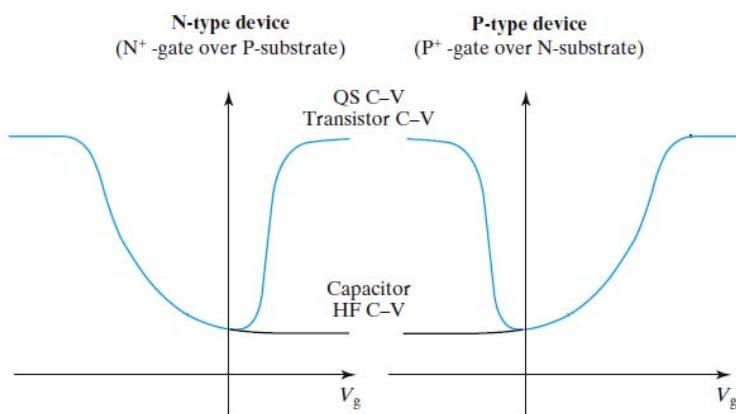
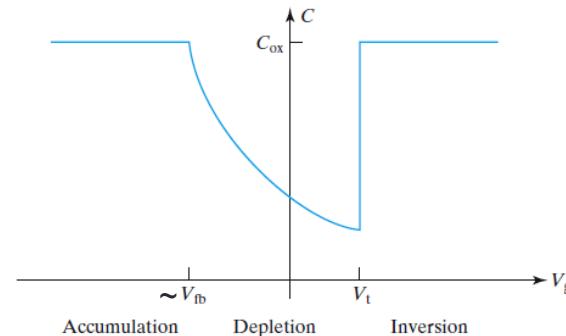
Capacitance of Non ideal MOS structure:

- Imagine the depletion regime of the MOS capacitor ($Q_{ss}=0$)
- We know that :

$$C_{sc} = C_{dep} = \frac{\epsilon_{sc}}{W_{dep}}$$

$$\frac{1}{C_{MOS}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

$$\frac{1}{C_{MOS}} = \sqrt{\frac{1}{C_{ox}^2} + \frac{2(V_g - V_{fb})}{eN_a\epsilon_{sc}}}$$



Threshold voltage

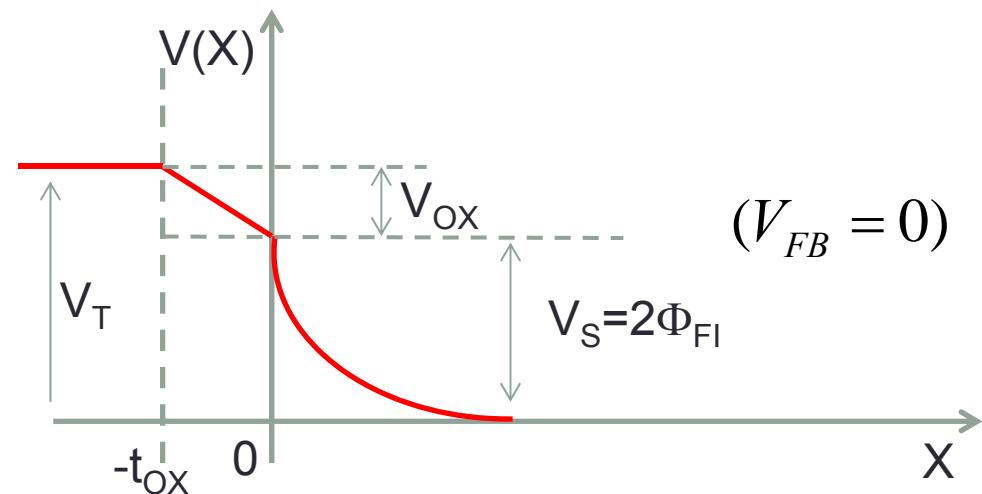
- Key parameter for behavior understanding of transistor
- Many definitions (*same results!*):
 - $n_s = N_A$
 - $V_s = 2 \phi_{fi}$
 - ...

Threshold voltage

V_T is simply the applied gate voltage when the surface potential or band bending reaches $2\Phi_{Fi}$ and the silicon charge is equal to the bulk depletion charge for that potential

$$V_T = V_g(V_S = 2\Phi_{Fi}) = \frac{\sqrt{4\epsilon_{SC}eN_A\Phi_{Fi}}}{C_{OX}} + 2\Phi_{Fi} + V_{FB} \quad (\text{from slide 16})$$

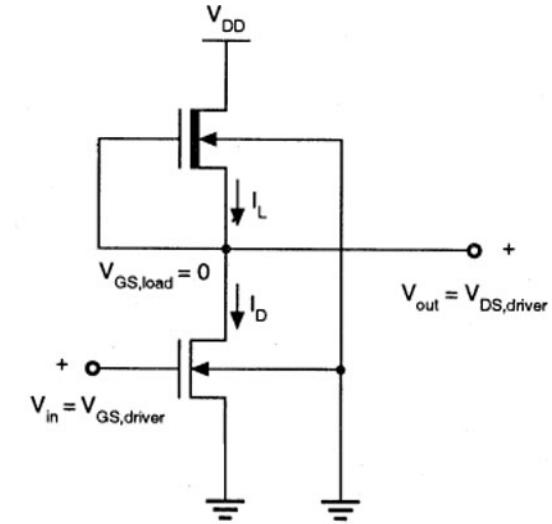
(we suppose here that no bias on the bulk is present
 \Leftrightarrow no body effect)



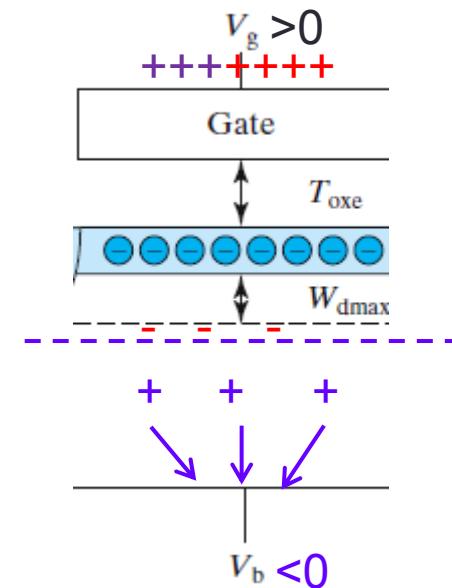
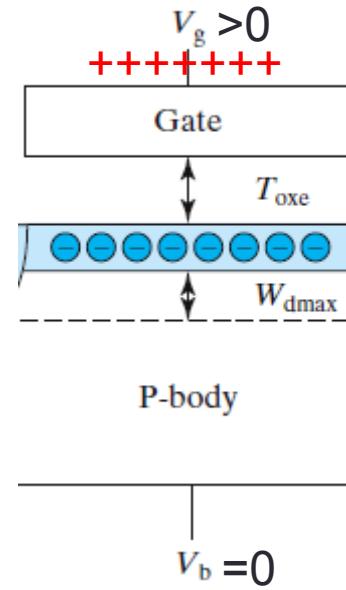
Threshold voltage

- Substrate sensitivity - Body Effect

- In general the MOS devices have a common silicon substrate
 \Leftrightarrow substrate voltage is equal for all transistor.
- **BUT** when multiple NFETs (or PFETs) are connected in series in a circuit, they share a common body (the silicon substrate) but their sources do not have the same voltage. We must introduce a coefficient that accounts for this effect : γ



Threshold voltage



One part of Gate voltage is no more used to create inversion layer but just to compensate the extra depletion width $\Leftrightarrow V_T$ will increase

Threshold voltage

- The new threshold voltage taking account the body effect can be written as:

$$V_T = V_{T0} + \gamma \left(\sqrt{|2\Phi_{Fi} + V_{SB}|} - \sqrt{|2\Phi_{Fi}|} \right)$$

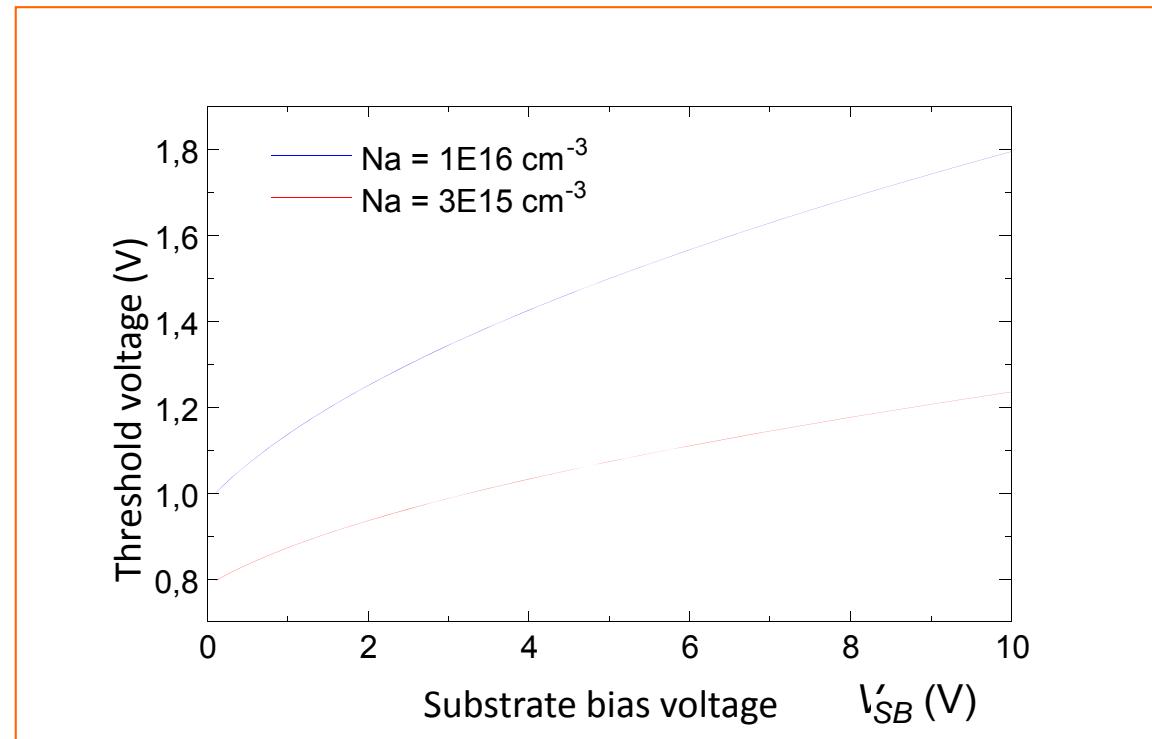
$$\gamma = \frac{\sqrt{2eN_A\epsilon_{sc}}}{C_{ox}}$$

- The substrate sensitivity as:

$$\frac{dV_T}{dV_{SB}} = -\frac{1}{C_{ox}} \frac{dQ}{dV_{SB}} = \frac{\sqrt{\epsilon_{sc} e N_a / 2(2\Phi_{Fi} + V_{SB})}}{C_{ox}} \quad \text{et} \quad \Delta V_T = -\frac{\Delta Q}{C_{ox}}$$

- Of course substrate bias have to be reverse to prevent current flow

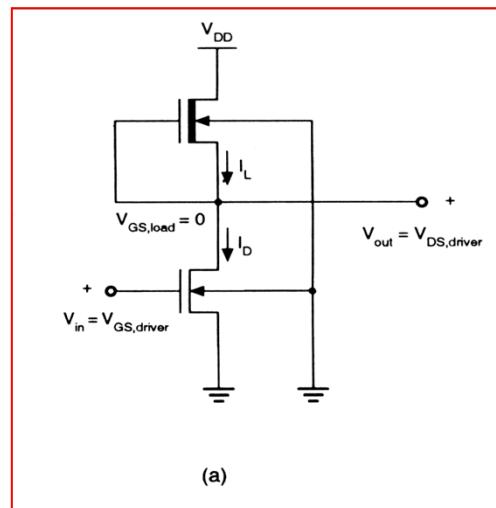
Threshold voltage



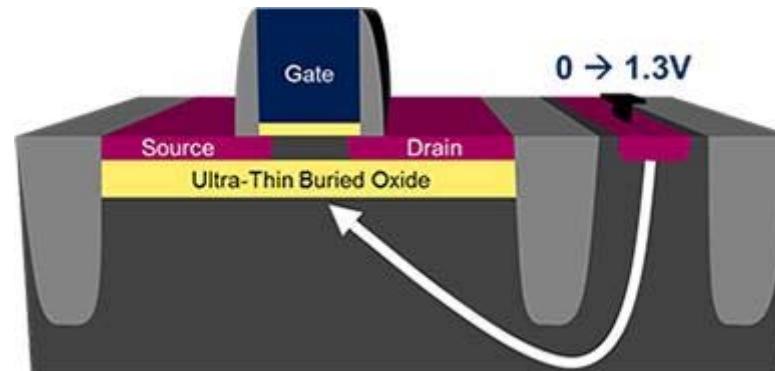
The effect of (reverse) substrate bias is to widen the bulk depletion region and raise the threshold voltage:

- The back contact acts as a back Gate
- We can tune V_T !

Threshold voltage : body effect

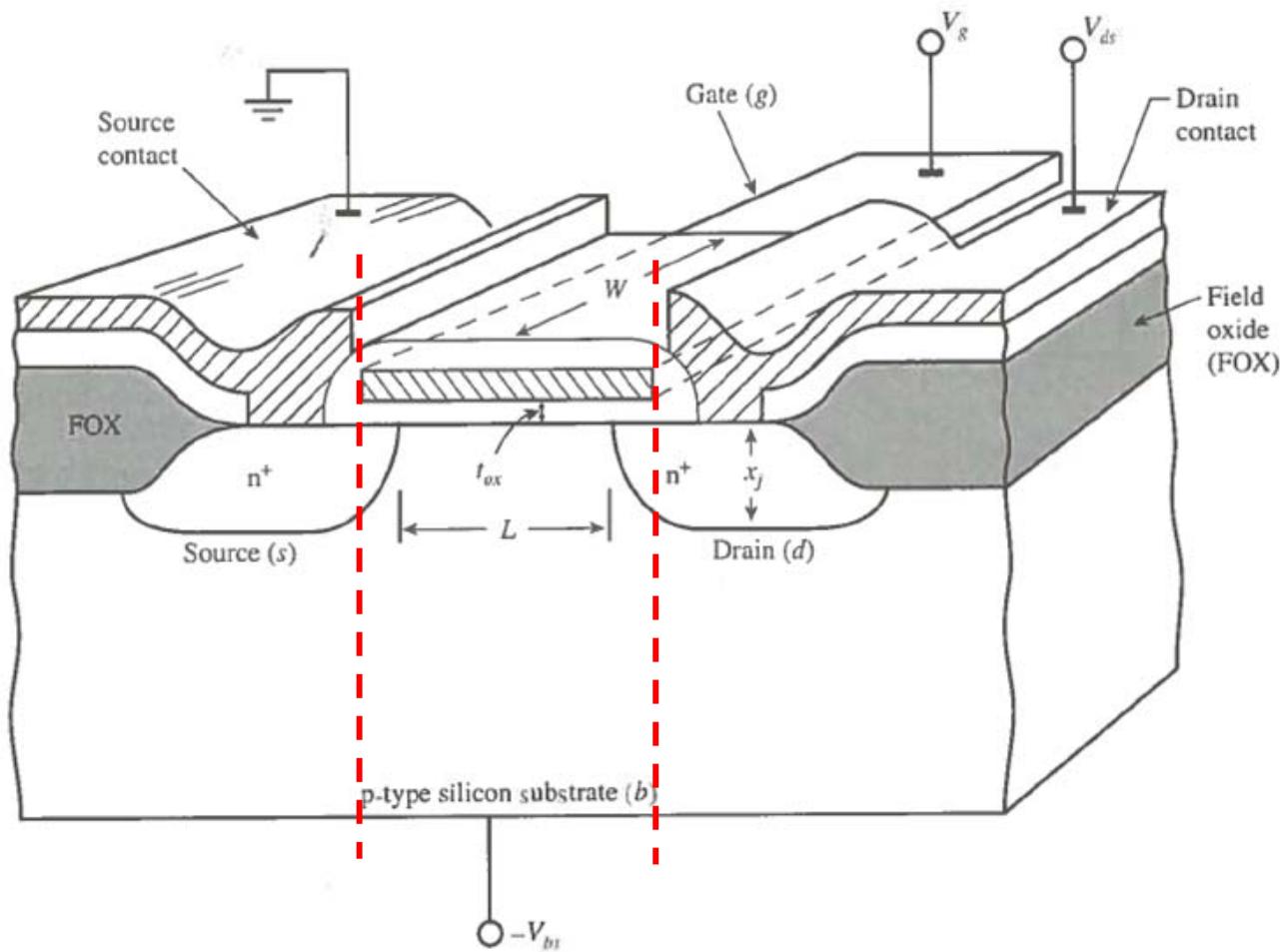


(a)

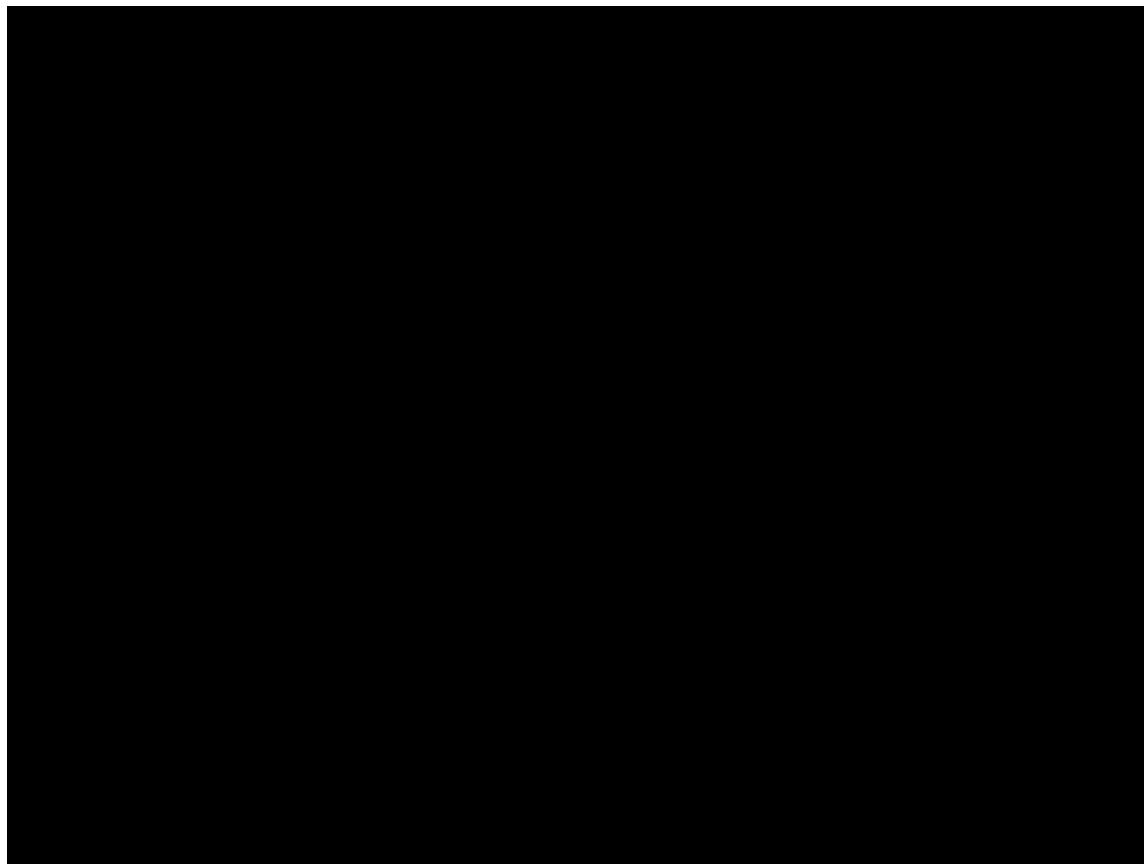


MOS-FET TRANSISTOR

MOS-FET transistor

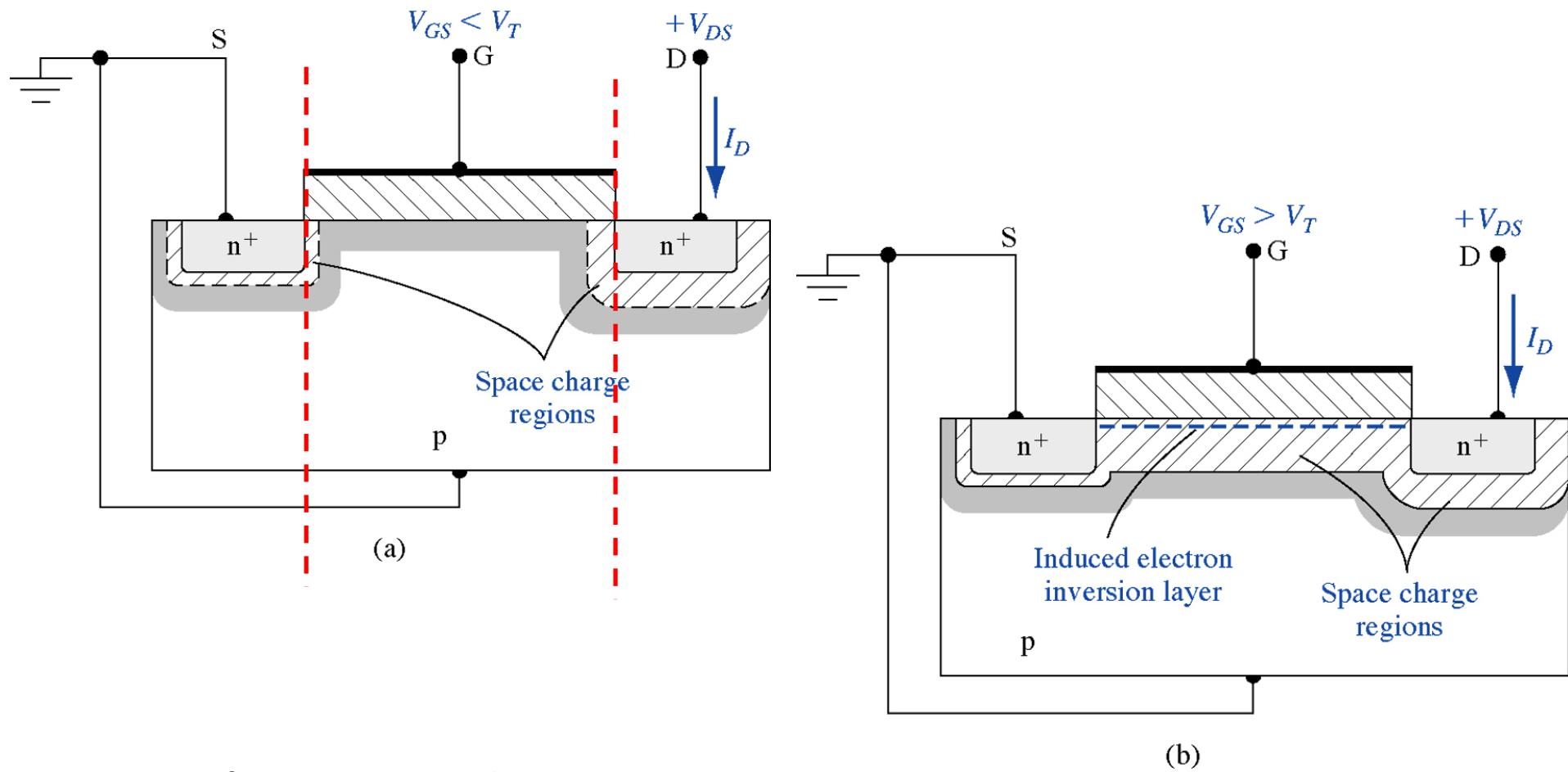


Graphical summary of the major processing steps in the formation of a MOSFET Transistor



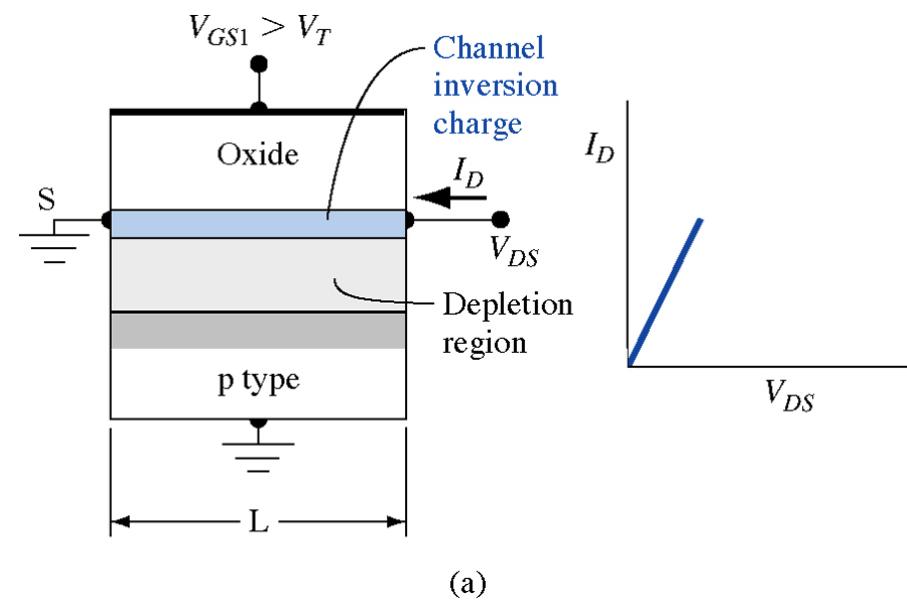
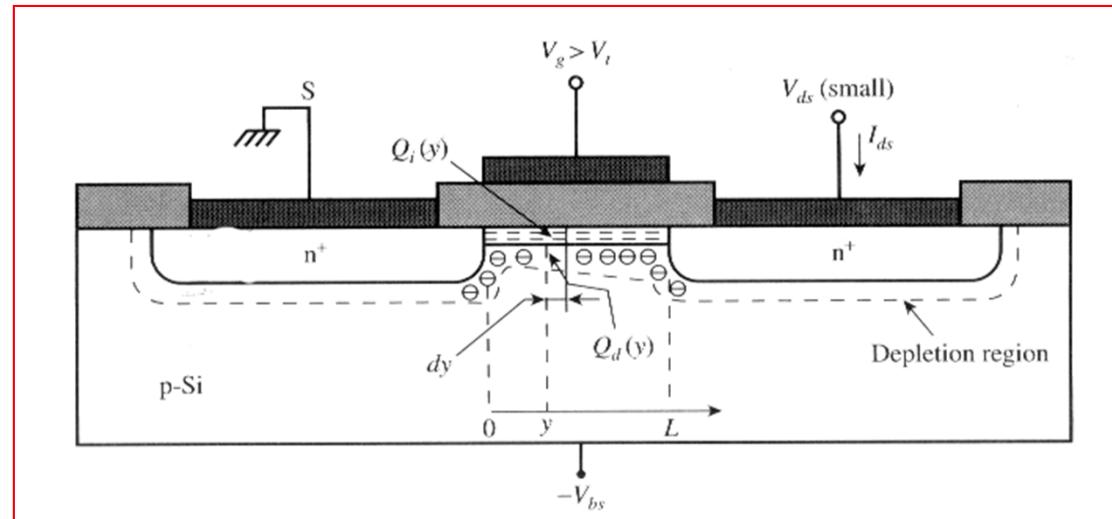
<http://www.youtube.com/watch?v=dR-Qtv-7uWI>

MOS-FET transistor

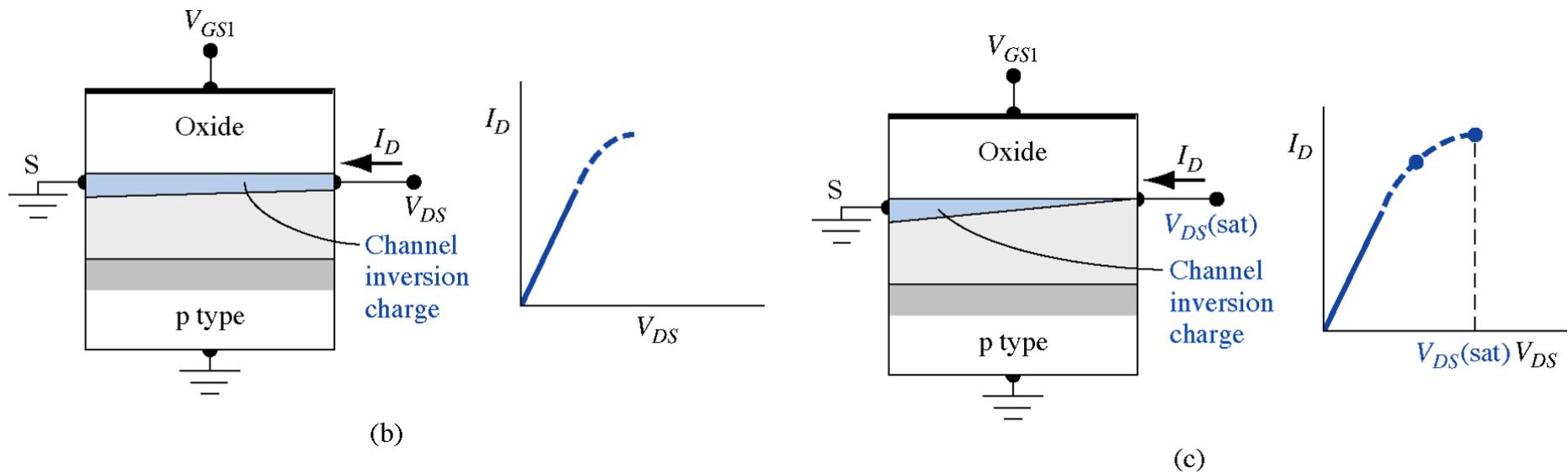
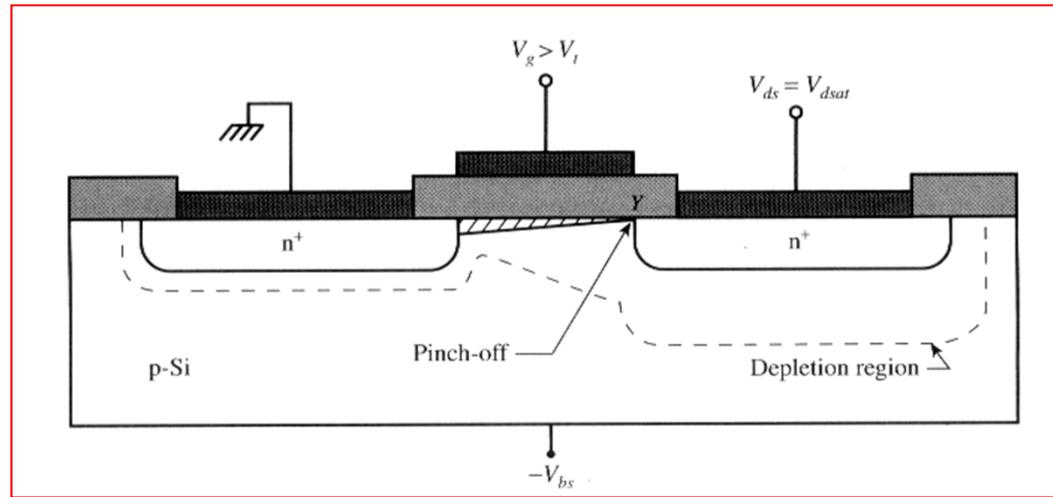


Stockage time ?

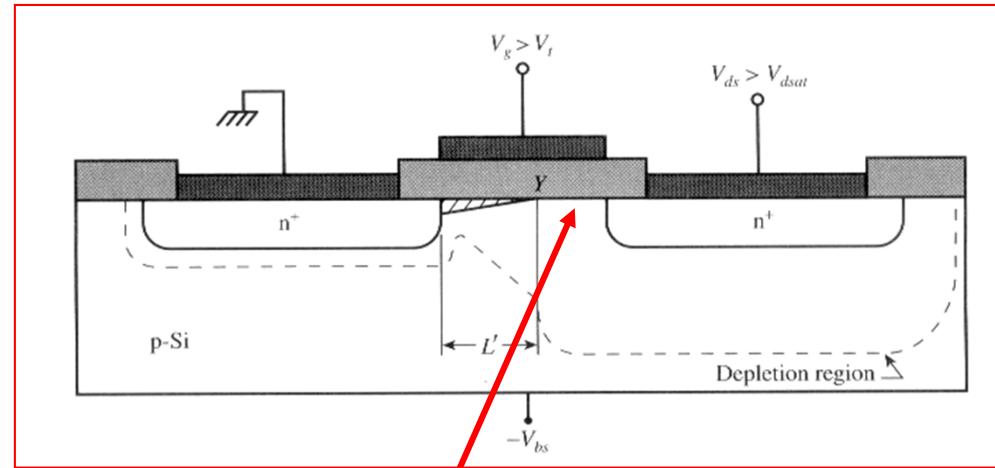
Linear regime



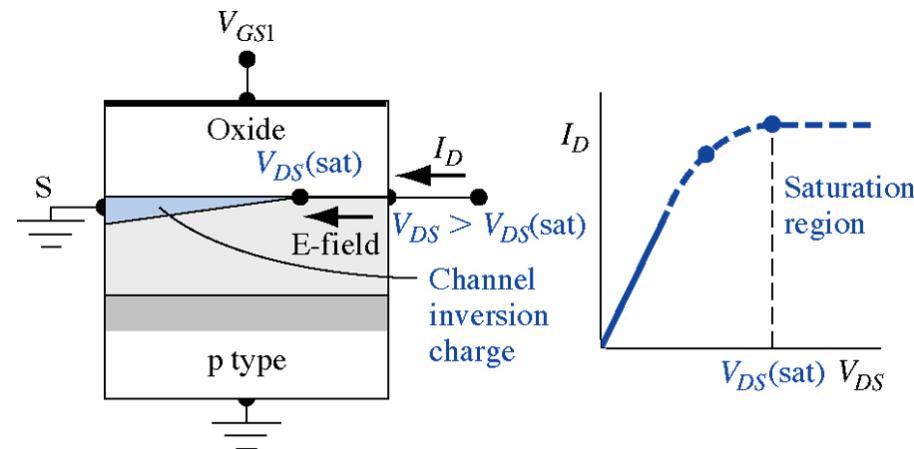
Saturation / linear limit



Saturation regime



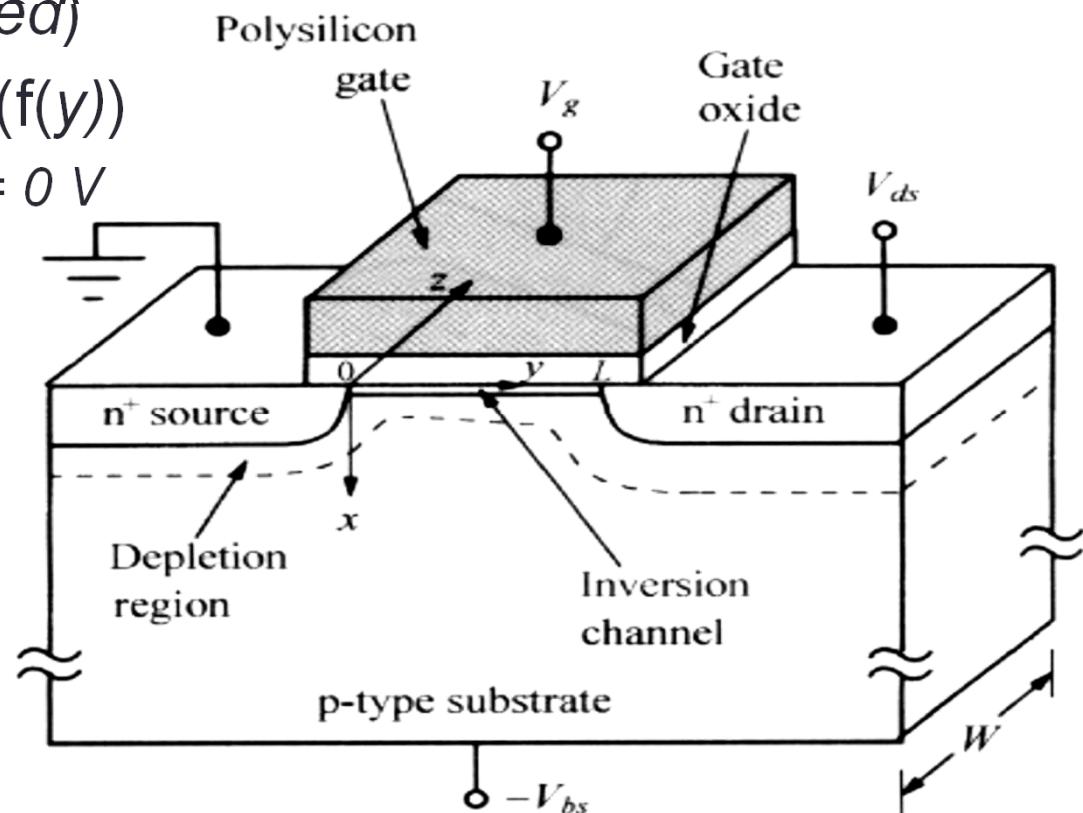
Effective length of canal decreases from L to L'



(d)

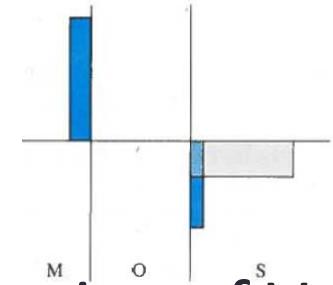
Basic MOSFET IV Model

- L , canal length(y oriented)
- W , canal width(z oriented)
- V , voltage in the canal ($f(y)$)
 - $V(y=0) = V(\text{source}) = V_s = 0 \text{ V}$
 - $V(y=L) = V(\text{drain}) = V_{ds}$
- V_g , gate voltage
- $-V_{BS}$, body voltage



Charge sheet approximation

- Analytical solution \Leftrightarrow we simplify the model:
 - Charge sheet approximation ($x_i=0$):
 - We assume all the inversion charges are located at the silicon interface without any thickness
 - No potential drop across this layer
 - No band bending across this layer



Charge sheet approximation

First step: calculation of inversion layer charge function of V_g

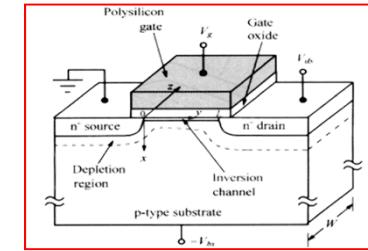
$$Q_{dep} = -eN_A W_M = -\sqrt{2eN_A \epsilon_{SC} V_S(y)} = -\sqrt{2eN_A \epsilon_{SC} (2\Phi_{Fi} + V(y))}$$

$$Q_{sc}(y) = -Q_{métal}(y) = -C_{ox} (V_g - V_{FB} - V_S(y)) = -C_{ox} (V_g - V_{FB} - 2\Phi_{Fi} - V(y))$$

$$Q_{inv} = Q_{sc} - Q_{dep} = -C_{ox} (V_g - V_{FB} - 2\Phi_{Fi} - V(y)) + \sqrt{2eN_A \epsilon_{SC} (2\Phi_{Fi} + V(y))}$$

$$n_s(y) = \frac{|Q_{inv}|}{e} = \frac{|Q_{sc}|}{e} - \frac{|Q_{dep}|}{e} = \frac{C_{ox} (V_g - V_{FB} - 2\Phi_{Fi} - V(y))}{e} - \left[\frac{2N_A \epsilon_{SC} (2\Phi_{Fi} + V(y))}{e} \right]^{\frac{1}{2}}$$

Charge sheet approximation



- Current density in the channel can be caused by diffusion and drift components

$$J_n = -qn\mu_0 \frac{dV(y)}{dy} + q\mu_0 \frac{kT}{q} \frac{dn}{dy}$$

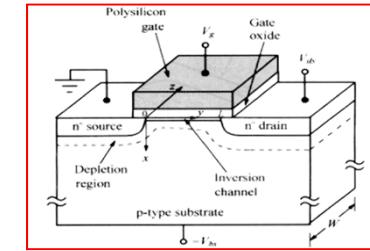
- Current is simply given (integration over channel section)

$$I_{DS} = \int_0^W dz \int_0^{x_i} qn\mu_0 \frac{dV}{dy} dx - \int_0^W dz \int_0^{x_i} q\mu_0 \frac{kT}{q} \frac{dn}{dy} dx$$

$$I_{DS} = W \int_0^{x_i} qn\mu_0 \frac{dV}{dy} dx - W \int_0^{x_i} q\mu_0 \frac{kT}{q} \frac{dn}{dy} dx$$

There is a sign change because we want $I_{DS}>0$ in $-y$ direction

Charge sheet approximation



- The previous relation can be rewritten

$$I_{DS} = W\mu_0 \frac{dV}{dy} \int_0^{x_i} qndx - W\mu_0 \frac{kT}{q} \frac{d}{dy} \left[\int_0^{x_i} qndx \right]$$

- If we remember that: $Q_{inv} = -q \int_0^{x_i} n(x, y)dx$
- Current expression can be found $I_{DS} = -W\mu_0 Q_{inv}(V) \frac{dV}{dy} + W\mu_0 \frac{kT}{q} \frac{dQ_{inv}(V)}{dy}$
- And so, by integrationg from $y=0$ to $y=L$ and as current is independant of y :

$$\int_0^L I_{DS} dy = W\mu_0 \left[- \int_{V(0)}^{V(L)} Q_{inv} dV + \frac{kT}{q} \int_{Q_{inv}(0)}^{Q_{inv}(L)} dQ_{inv} \right]$$

conduction diffusion

Charge sheet approximation

- If we want to derive basic expressions for long channel current in *linear and saturation* regions, we can neglect drift component

$$\int_0^L I_{DS} dy = -W\mu_0 \int_{V(0)}^{V(L)} Q_{inv}(V) dV = -W\mu_0 \int_0^{V_{DS}} Q_{inv}(V) dV$$

with $Q_{inv} = -C_{ox}(V_g - V_{FB} - 2\Phi_{Fi} - V(y)) + \sqrt{2eN_A\epsilon_{sc}(2\Phi_{Fi} + V(y))}$

After few simple steps:

$$I_{DS} = \mu_n \frac{W}{L} C_{ox} \left[\left(V_g - V_{FB} - 2\Phi_{Fi} - \frac{V_{DS}}{2} \right) V_{DS} - \frac{2}{3} \frac{\sqrt{2\epsilon_{sc} e N_A}}{C_{ox}} \left[(2\Phi_{Fi} + V_{DS})^{\frac{3}{2}} - (2\Phi_{Fi})^{\frac{3}{2}} \right] \right]$$

!! C_{ox} is the oxide capacitance per surface unit (Fm^{-2} ou Fcm^{-2})!!

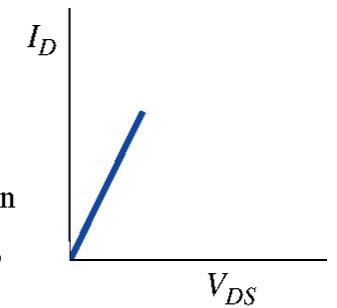
Characteristics in the linear (triode) region

When V_{DS} is small ($V_{DS} \ll 2\Phi_{Fi}$) , one can expand the previous equation into power series in V_{DS} and keep only first order term:

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{fb} - 2\Phi_{Fi} - \frac{\sqrt{4\varepsilon_{sc} e N_A \Phi_{Fi}}}{C_{ox}}) V_{DS} \right]$$

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

We recognize threshold voltage V_T^{on}



In the linear region, the MOSFET simply acts like a resistor modulated by the gate voltage

Characteristics in the linear (triode) region

- For larger values of V_{DS} we have to keep second order term (quadratic term) and a good approximation of current is:

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{gs} - V_T) V_{DS} - \frac{m}{2} V_{DS}^2 \right]$$

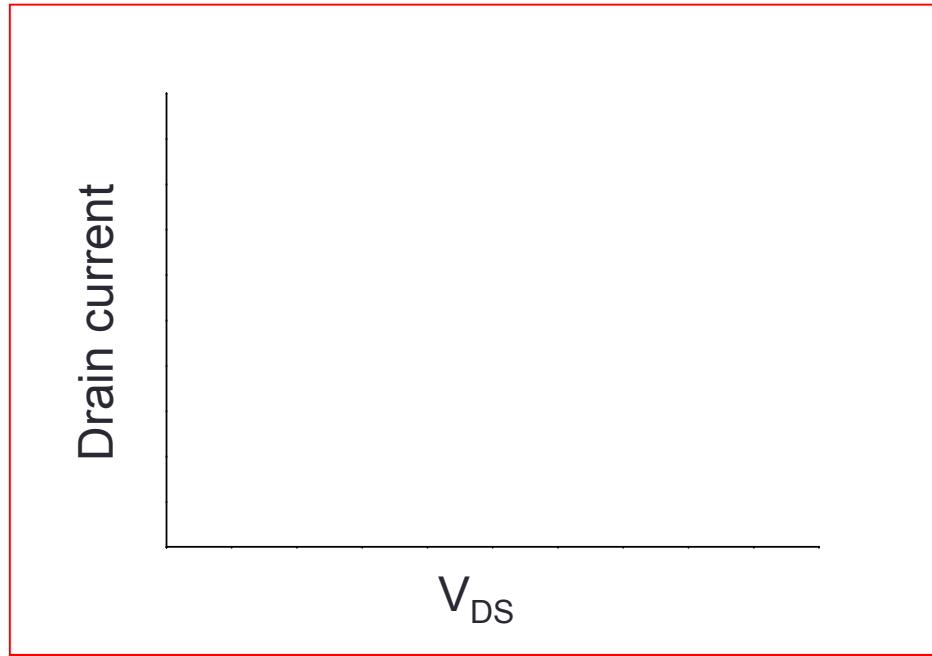
with

$$m = 1 + \frac{\sqrt{\varepsilon_{sc} e N_A / 4 \Phi_{Fi}}}{C_{ox}} = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{3d_{ox}}{W_m} \approx 1$$

C_{dm} is the bulk depletion capacitance in limit of strong inversion

Characteristics in the saturation region

- Previous equation is a parbole. I_{ds} follows a parabolic curve with V_{DS} until a maximun (or saturation) value is reached when $V_{DS} = V_{dsat}$.



$$V_D = V_{Dsat} = \frac{(V_{gs} - V_T)}{m}$$

$$I_{DS} = I_{Dsat} = \mu_n C_{ox} \frac{W}{L} \frac{(V_{gs} - V_T)^2}{2m}$$

In the case of thin oxide and low doping m can be reduced to 1 and yield the well known expression:

$$I_{DS} = I_{Dsat} = \mu_n C_{ox} \frac{W}{2L} (V_{gs} - V_T)^2$$

Characteristics in the saturation region

- Without any approximation (series expand,...), complete expressions for I_{DSAT} can be expressed as:

$$I_{dsat} = \mu_n \frac{W}{6L} C_{ox} \left[(V_{Dsat} + 2\Phi_{Fi})(V_{Dsat} + 2\Phi_{Fi} + 2V_{gs} + 2V_{FB}) - 12\Phi_{Fi}(V_{gs} + V_{FB} - \Phi_{Fi} - \frac{4(eN_A \varepsilon_{sc} \Phi_{Fi})^{\frac{1}{2}}}{3C_{ox}}) \right]$$

$$V_{Dsat} = V_{gs} - V_{FB} - 2\Phi_{Fi} + \frac{\varepsilon_{sc} e N_A}{C_{ox}^2} - \sqrt{\frac{2\varepsilon_{sc} e N_A}{C_{ox}^2} (V_{gs} - V_{FB} + \frac{\varepsilon_{sc} e N_A}{2C_{ox}^2})}$$

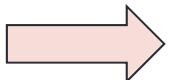
If we suppose high value for C_{ox} (thin oxyde) and low doping level, threshold voltage can be simplified as $V_T \approx 2\phi_{Fi} + V_{FB}$ and at the same time we can rewrite $V_{dsat} = V_{gs} - V_T \approx V_{gs} - 2\phi_{Fi} - V_{FB}$

$$V_{Dsat} = V_{gs} - V_T$$

$$I_{Dsat} \approx \mu_n \frac{W}{2L} C_{ox} (V_{gs} - V_T)^2 = \mu_n \frac{W}{2L} C_{ox} V_{Dsat}^2$$

Subthreshold characteristics

– weak inversion region

- Three regimes:
 - Triode (Linear)
 - Saturation
 - OFF state (if $V_g < V_T$ for nMOS)
 - Transition ON /OFF is not so sharp
 - Weak inversion for $\Phi_{fi} < V_s < 2\Phi_{Fi}$
 - Subthreshold behavior is of importance:
 - Low power
 - Low voltage
- 
- digital logic and memory circuits

MOSFET basics

- Subthreshold current: « OFF » is not totally « OFF »
 - Previous analysis $\Leftrightarrow V_{GS} < V_T$, NMOS (NFET) turns OFF
 - In reality, for $V_{GS} \sim V_T$, a « weak » inversion layer still exists and some current (**drift component**) can flow between S and D.
 - This is the so called “subthreshold conduction”

$$I_{DS} = I_{ON} \exp \frac{e(V_{GS} - V_T)}{\eta kT} \propto B \times \exp \frac{eV_{GS}}{\eta kT}$$

$$I_{OFF}(V_{GS} = 0) = I_{ON} \exp \frac{-eV_T}{\eta kT}$$

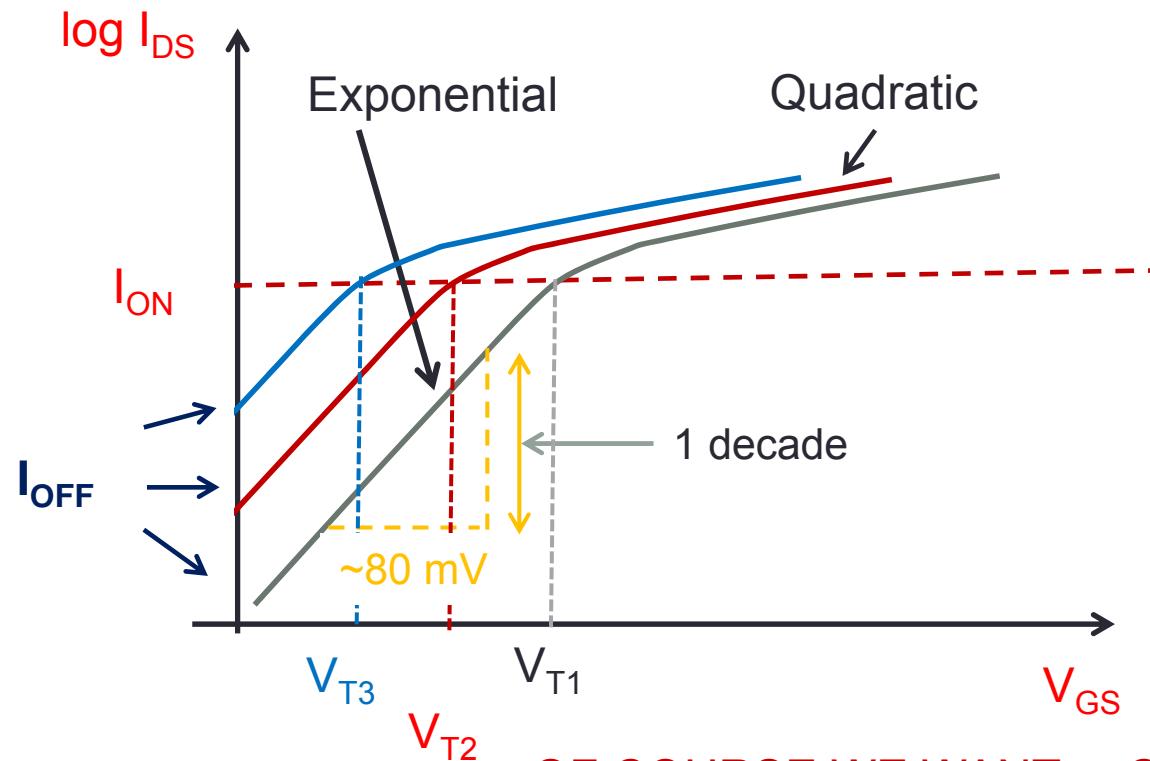
with η , a ideality (or nonideality) factor (≥ 1)

- Remember that $\exp \frac{V_{GS}}{\eta kT}$ changes by 10 for every $\eta \times 60 \text{ mV}$ change in V_{GS} .
- Typically, if I_{DS} decreases for one decade , then V_{GS} must decrease by at least $\eta \times 60 \text{ mV}$ (in fact around 80 mV, $\eta > 1$) (at 300K!).

MOSFET basics

- Subthreshold current :

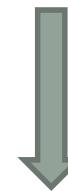
$$I_{DS} = I_{ON} \exp \frac{e(V_{GS} - V_T)}{\eta kT} \quad (\text{for } V_{GS} < V_T)$$



For example:

$$I_{OFF}(V_{GS} = 0) = I_{ON} \exp \frac{-eV_T}{\eta kT}$$

- If we suppose $V_T = 0,3V$



- $0,3V/80 \text{ mV} = 3,75$



- $I_{ON}/I_{OFF} = 10^{3,75} \sim 5600$

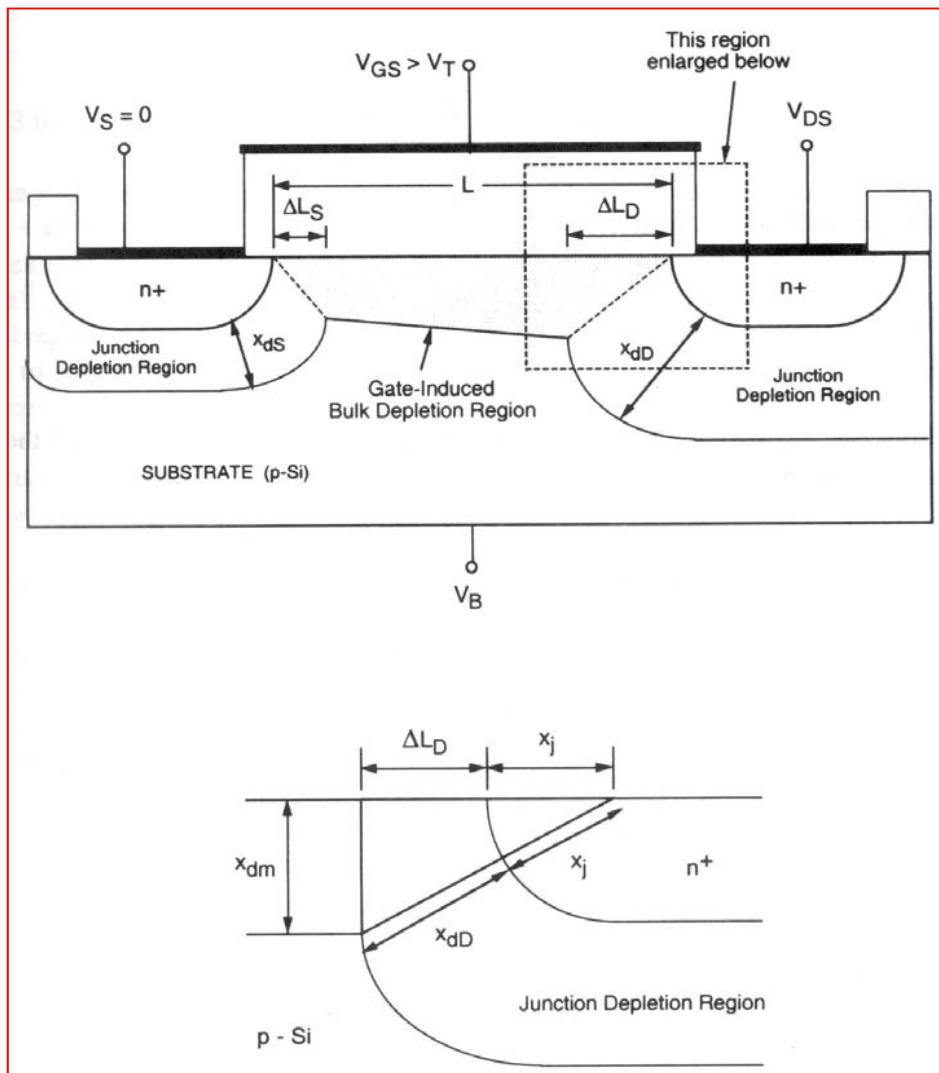
- If $V_T = 0,6V$, $I_{ON}/I_{OFF} > 10^7 !!$

OF COURSE WE WANT η CLOSE TO UNITY

Short channel MOSFETs

- Threshold voltage reduction
- Drain Induced Barrier Lowering (DIBL)
- Channel length modulation
- MOSFETs breakdown
- ...

Threshold voltage reduction: short channel effect (Kang et al)



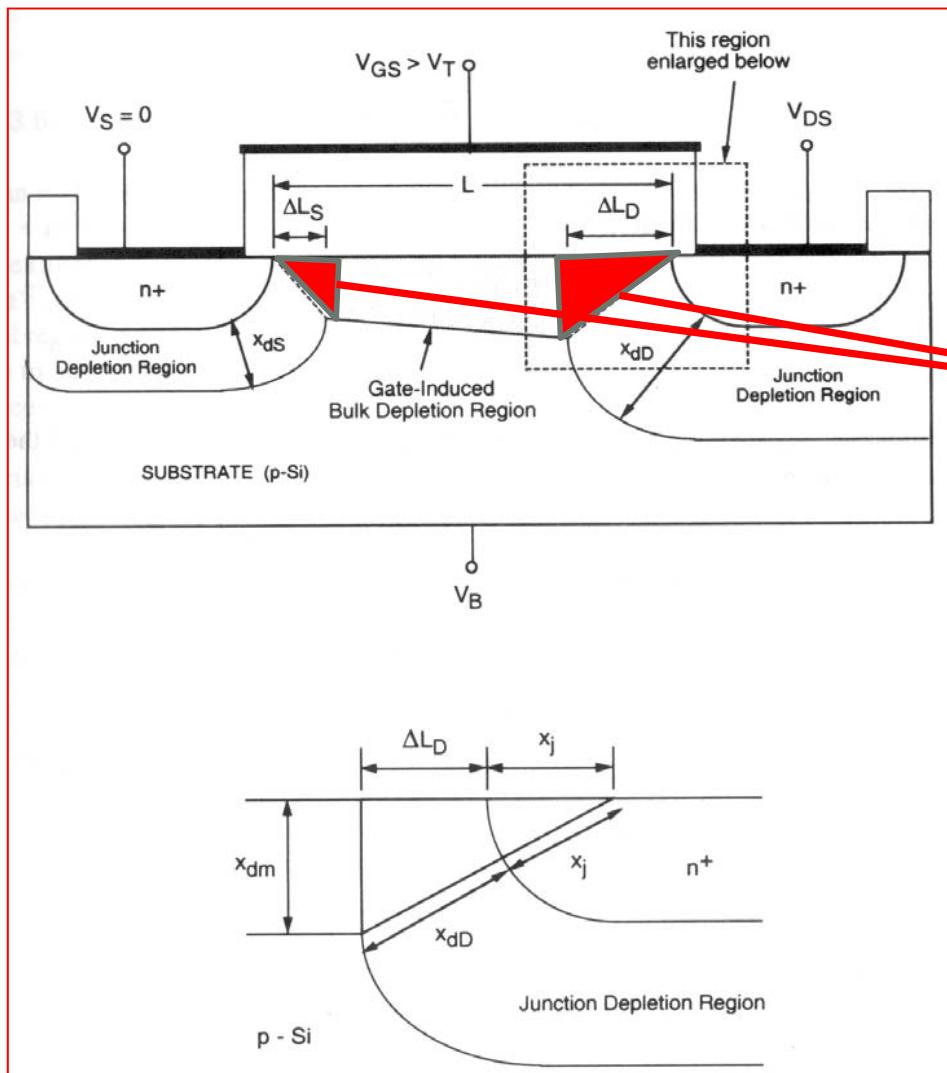
- **Origin:**

- Previous V_T expression supposes channel depletion region comes only from gate
- In fact one part is created by depletion region associated by source/channel and drain/channel pn junctions
- Overestimation of charge induced by gate \Leftrightarrow overestimation of V_T
- This reduction more prominent for MOSFET with shorter channel length



$$V_T(\text{shortchannel}) = V_{T0}(\text{longchannel}) - \Delta V_{T0}$$

Threshold voltage reduction: short channel effect (Kang et al)



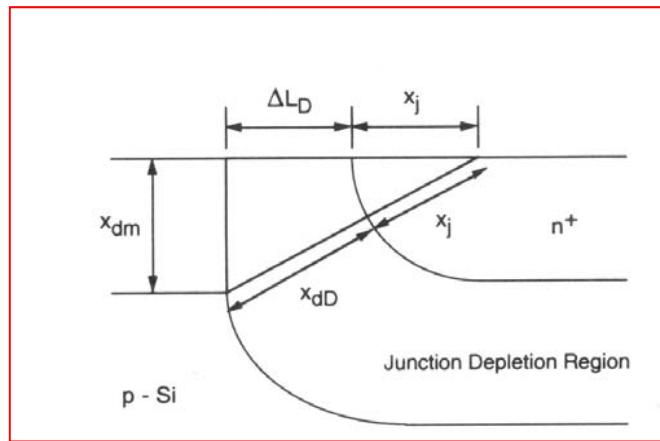
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$$V_T(\text{shortchannel}) = V_{T0}(\text{longchannel}) - \Delta V_{T0}$$

Threshold voltage reduction: short channel effect (Kang et al)



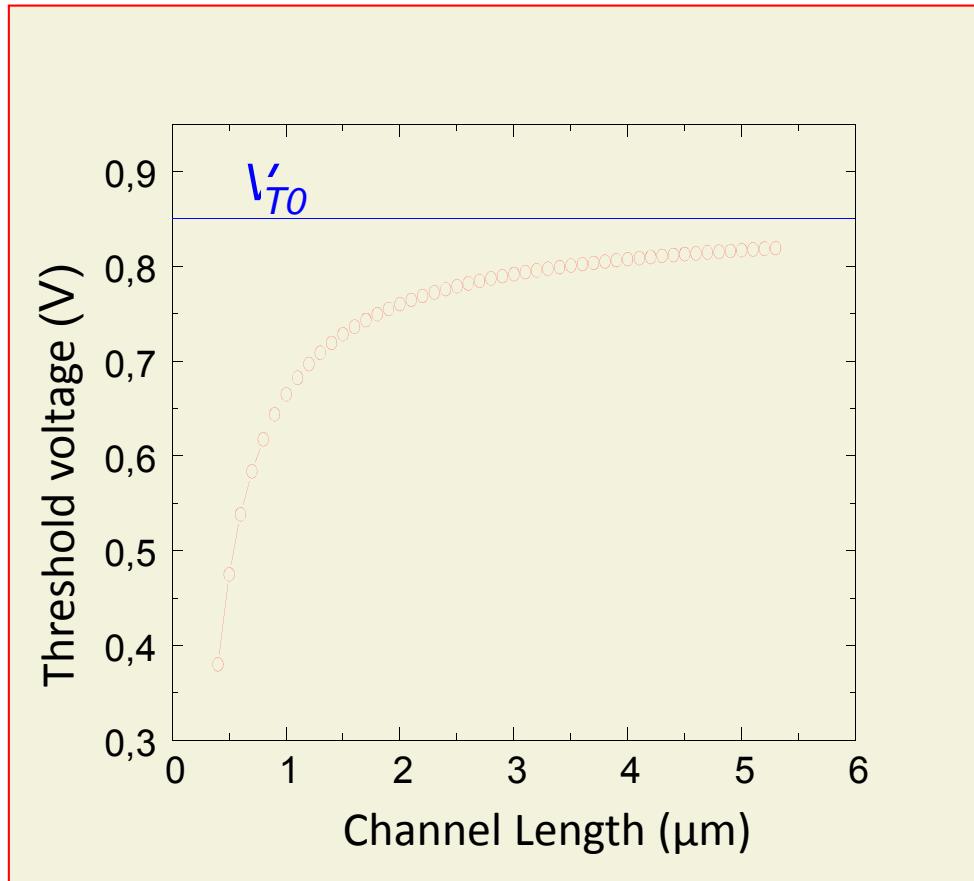
$$x_{dS} = \sqrt{\frac{2\epsilon_{Si}}{eN_A} V_{bi}}$$

$$x_{dD} = \sqrt{\frac{2\epsilon_{Si}}{eN_A} (V_{bi} + V_{DS})}$$

$$\Delta L_{S,D} \cong x_j \cdot \left(\sqrt{1 + \frac{2x_{dS,D}}{x_j}} - 1 \right)$$

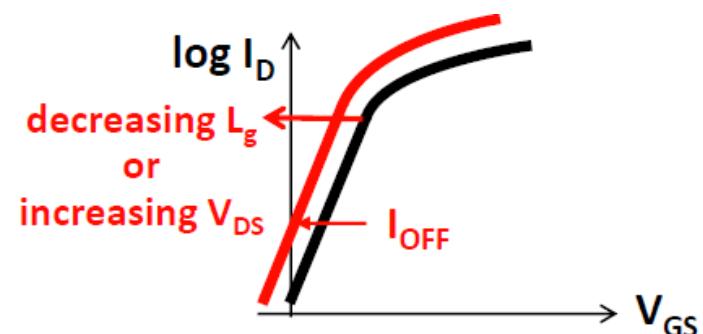
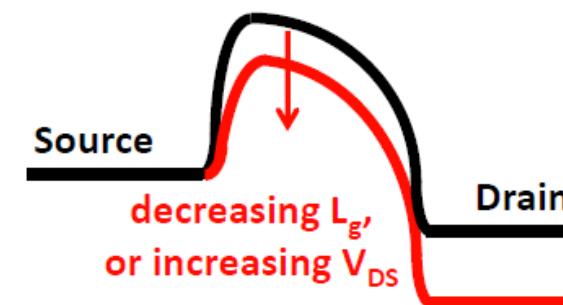
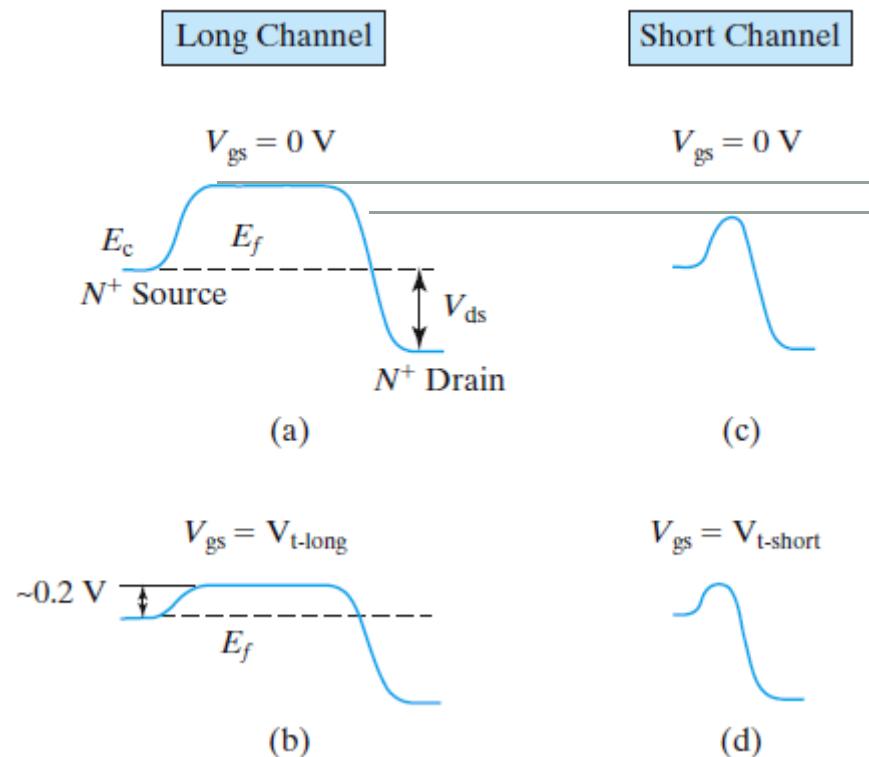
$$\Delta V_{T0} = \frac{1}{C_{ox}} \sqrt{4e\epsilon_{Si} N_A \phi_{Fi}} \frac{x_j}{2L} \left[\left(\sqrt{1 + \frac{2x_{dS}}{x_j}} - 1 \right) + \left(\sqrt{1 + \frac{2x_{dD}}{x_j}} - 1 \right) \right]$$

Threshold voltage reduction: short channel effect (Kang et al)

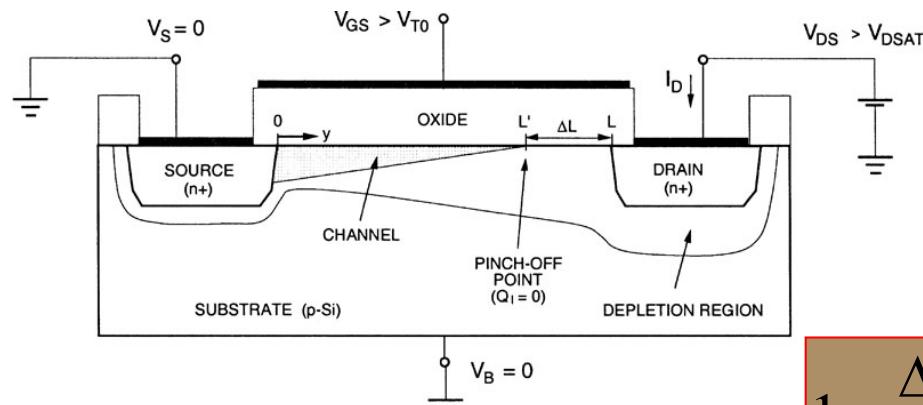


- Threshold voltage is function of:
 - Channel length
 - Drain –Source voltage V_{ds} through x_{dD}

Drain Induced Barrier Lowering (DIBL)



Channel length modulation (saturation operation)



- At the onset of pinch-off ($V_{DS} > V_{Dsat}$), the effective channel length (the length of inversion layer) is reduced.

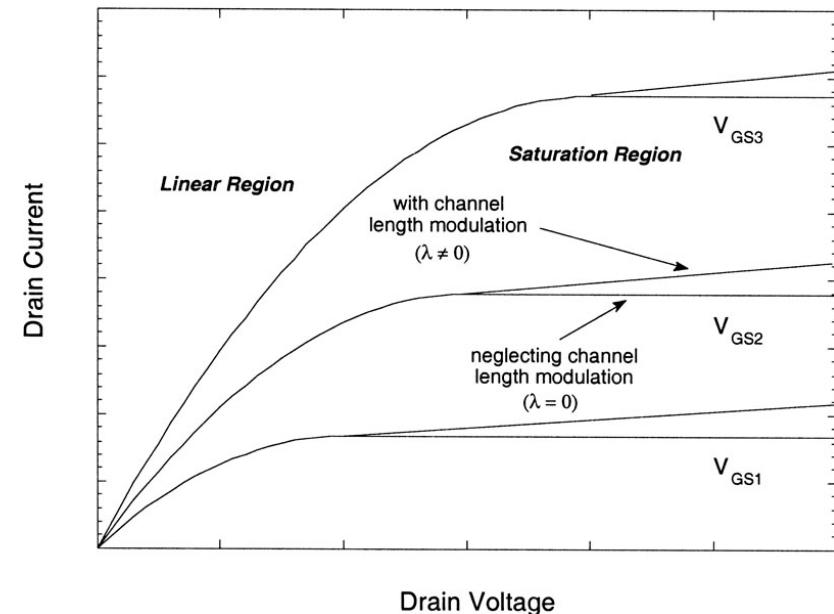
$$1 - \frac{\Delta L}{L} \approx 1 - \lambda V_{DS}$$

$$I_D = \frac{L}{L - \Delta L(V_{DS})} I_{Dsat}$$

$$\text{If } \lambda V_{DS} \ll 1$$



$$I_D(sat) = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$



MOSFET Breakdown

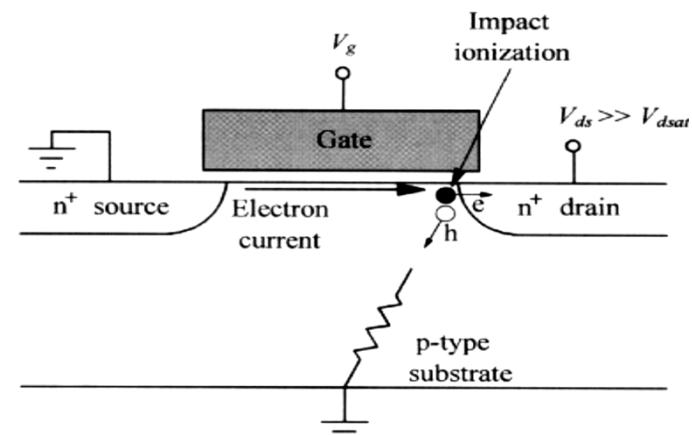
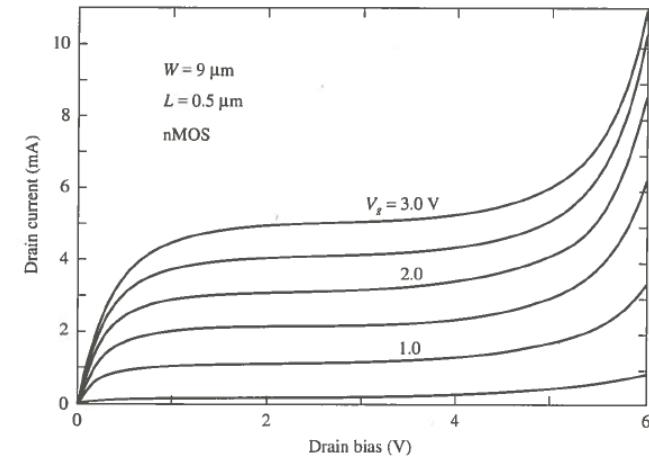
- 2 main effects:

- punchthrough breakdown

- Punch through in a MOSFET is an extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region.
- Punch through causes a rapidly increasing current with increasing drain-source voltage
- No current saturation

- Impact ionisation at the drain:

- Electron acceleration in the channel
- Impact ionisation \Leftrightarrow holes electrons pairs generated
- Holes collected by substrate \Leftrightarrow substrate current \Leftrightarrow voltage drop in the channel
- Reduction of VT (body effect)
- Increase of current and so on !
- Permanent damage



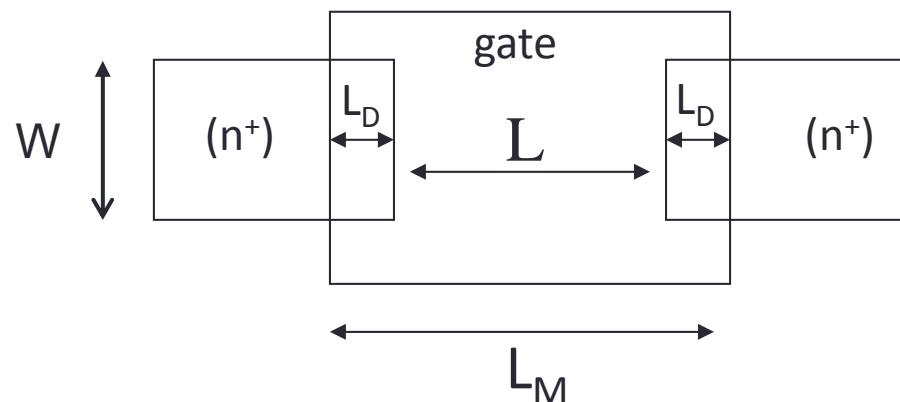
MOSFET capacitances

- Difficulties:
 - In general, capacitances associated with MOS circuits are a complicated function of geometries and process
 - Not lumped capacitances but distributed capacitances
- In the following, first approximation model
 - Sufficiently accurate to represent main characteristics of MOSFET charge voltage behavior
 - All the capacitances are lumped
- Three differents physical origins
 - Overlay capacitance
 - Oxyde capacitance
 - Junction capacitance

Important point : capacitances are dependent of bias voltage / working point.

MOSFET capacitances

- Overlay capacitances:
 - L_D , gate – drain and gate – source overlay
 - L_M , mask length



$$L = L_M - 2 \cdot L_D$$

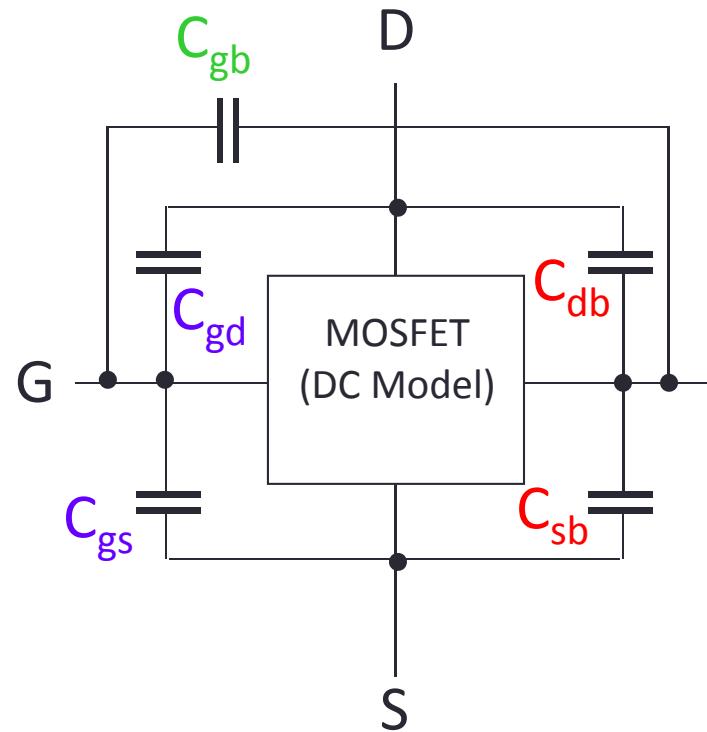
$$C_{GS}(\text{overlap}) = C_{ox} \cdot W \cdot L_D$$

$$C_{GD}(\text{overlap}) = C_{ox} \cdot W \cdot L_D$$

$$C_{ox} = \frac{\epsilon_{ox}}{d_{ox}}$$

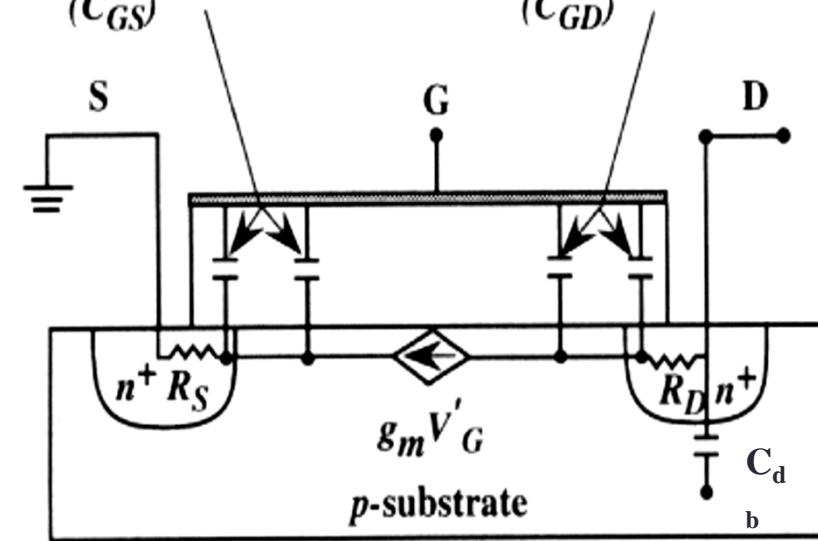
MOSFET capacitances

Lumped representation of parasitics capacitances



Equivalent model (with overlap capacitances)

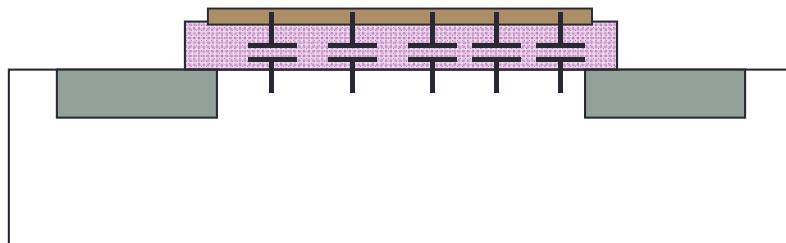
Total gate capacitance includes overlay effects (C_{GS})



Gate-Drain capacitance includes parasitic effect (C_{GD})

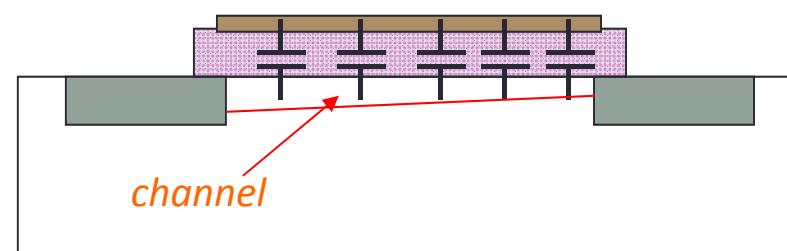
Gate – Channel capacitances

- Cut off mode:



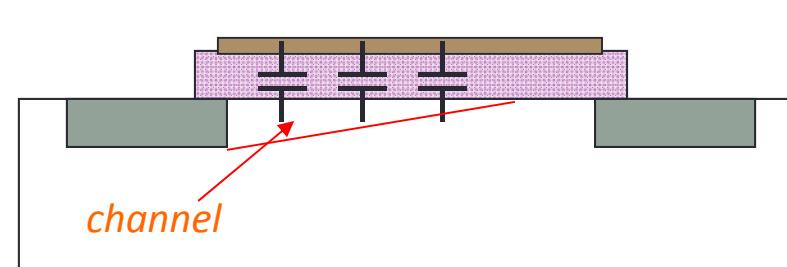
$$\begin{aligned}C_{gs} &= C_{gd} = 0 \\C_{gb} &= C_{ox} WL\end{aligned}$$

- Linear mode



$$\begin{aligned}C_{gs} &= C_{gd} = \frac{1}{2} C_{ox} WL \\C_{gb} &= 0 \text{ (channel shields substrate)}\end{aligned}$$

- Saturation mode



$$\begin{aligned}C_{gs} &= \frac{2}{3} C_{ox} WL, C_{gd} = 0 \\C_{gb} &= 0 \text{ (channel shields substrate)}\end{aligned}$$

Oxyde capacitance

Capacitance	Cut off	Linear	saturation
$C_{gb}(\text{total})$	$C_{ox}WL$	0	0
$C_{gd}(\text{total})$	$C_{ox}WL_D$	$\frac{1}{2}C_{ox}WL + C_{ox}WL_D$	$C_{ox}WL_D$
$C_{gs}(\text{total})$	$C_{ox}WL_D$	$\frac{1}{2}C_{ox}WL + C_{ox}WL_D$	$\frac{2}{3}C_{ox}WL + C_{ox}WL_D$

Dynamic characteristics (1)

- Conductance:

$$g_D = \frac{\partial I_D}{\partial V_D} \Big|_{V_g=cte} = \mu_n \frac{W}{L} C_{ox} \left[V_{gs} - V_{FB} - 2\Phi_{Fi} - V_{DS} - \frac{\sqrt{2\varepsilon_{sc} N_a}}{C_{ox}} \sqrt{V_{DS} - 2\Phi_{Fi}} \right]$$

- Linear mode

$$g_{D_{lin}} = \frac{\mu_n W}{L} C_{ox} (V_{gs} - V_T)$$

- Saturation mode

$$g_{D_{sat}} \approx 0 \quad \text{ou} \quad g_{D_{sat}} = \frac{\mu_n C_{ox} W}{2L} (V_{gs} - V_T)^2 \lambda \approx \lambda I_D$$

Dynamic characteristics (2)

- transconductance: device speed
 - linear

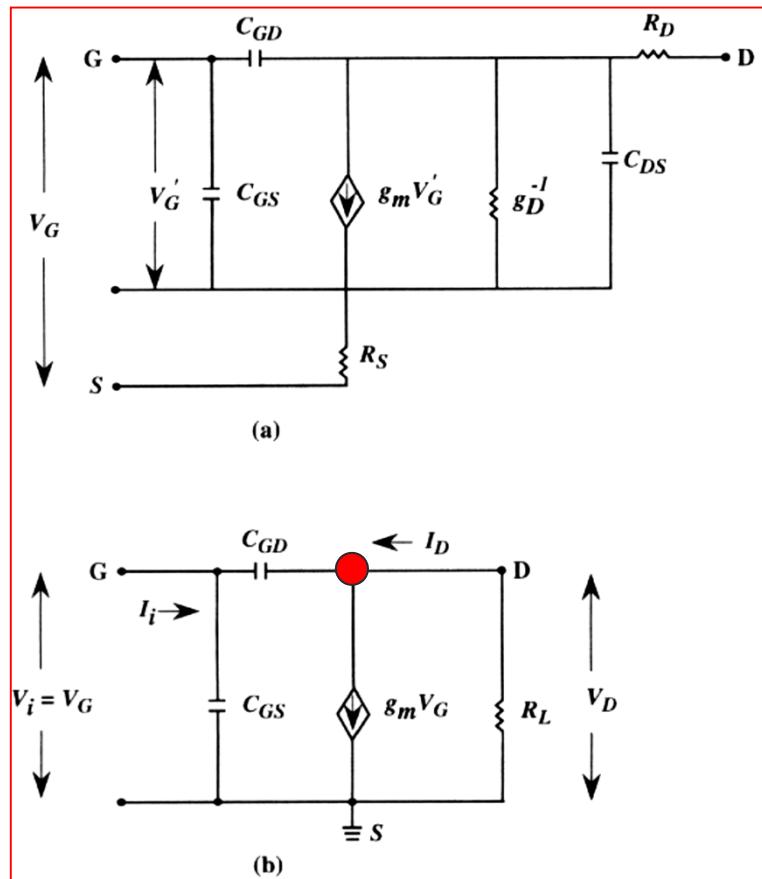
$$g_{m_{lin}} = \mu_n C_{ox} \frac{W}{L} V_{DS}$$

- « *active region* »

$$g_{msat} = \frac{\mu_n W}{L} C_{ox} (V_{gs} - V_T) = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{Dsat}} = \frac{2I_{Dsat}}{(V_{gs} - V_T)}$$

HF Characteristics

- Cut off frequency \Leftrightarrow current gain = 1



$$I_{in} = j\omega C_{GS} V_g + j\omega C_{GD} (V_g - V_D)$$

$$\frac{V_D}{R_L} + g_m V_g + j\omega C_{GD} (V_D - V_g) = 0$$

$$I_{in} = j\omega \left[C_{GS} + C_{GD} \left(\frac{1 + g_m R_L}{1 + j\omega R_L C_{GD}} \right) \right] V_g$$

If we neglect $j\omega R_L C_{gd}$ (small)

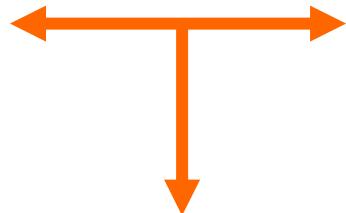
$$I_{in} = j\omega (C_{GS} + C_{GD} (1 + g_m R_L)) V_g$$

$$I_{in} = j\omega (C_{GS} + C_M) V_g$$

C_M : Miller capacitance

HF Characteristics

$$I_{out} = I_D = g_m V_{gs}$$



$$I_{in} = I_{out}$$

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_M)}$$

If $C_M = 0$ (or minimum) \Leftrightarrow cut off frequency is maximum (saturation mode):

$$f_{T\max} = \frac{\mu_n(V_G - V_T)}{2\pi L^2}$$

or (if short channel and/or v_{sat})

$$f_{T\max} = \frac{v_s}{2\pi L}$$

HF Characteristics

- An other figure of merit : power gain =1 \Leftrightarrow *oscillation frequency*

$$f_{\max} \approx \frac{f_T}{\sqrt{4R_g(g_d + \omega_T C_{gd})}}$$

R_g : gate resistance

R_s : negligable

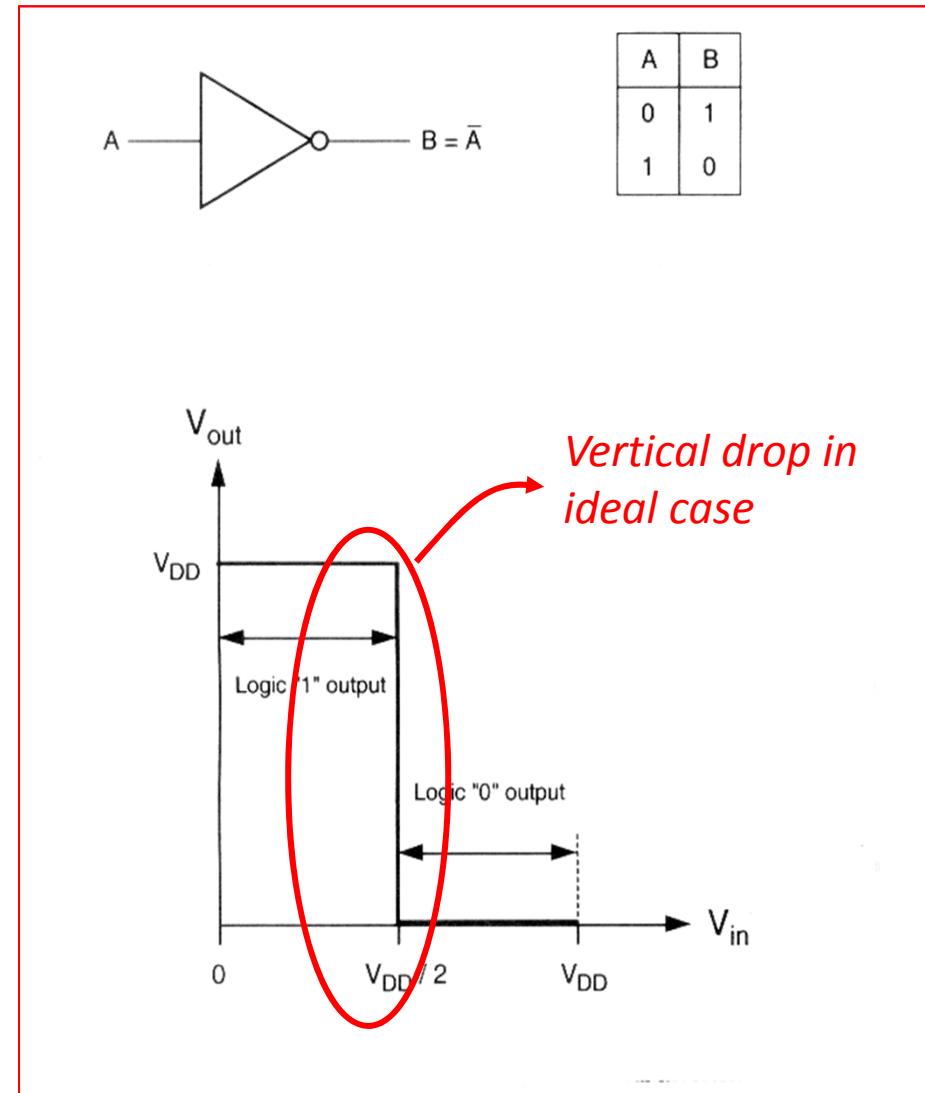
Ref: (Tsividis)

MOS TRANSISTORS INVERTERS

Statics characteristics

ideal Inverter : definition

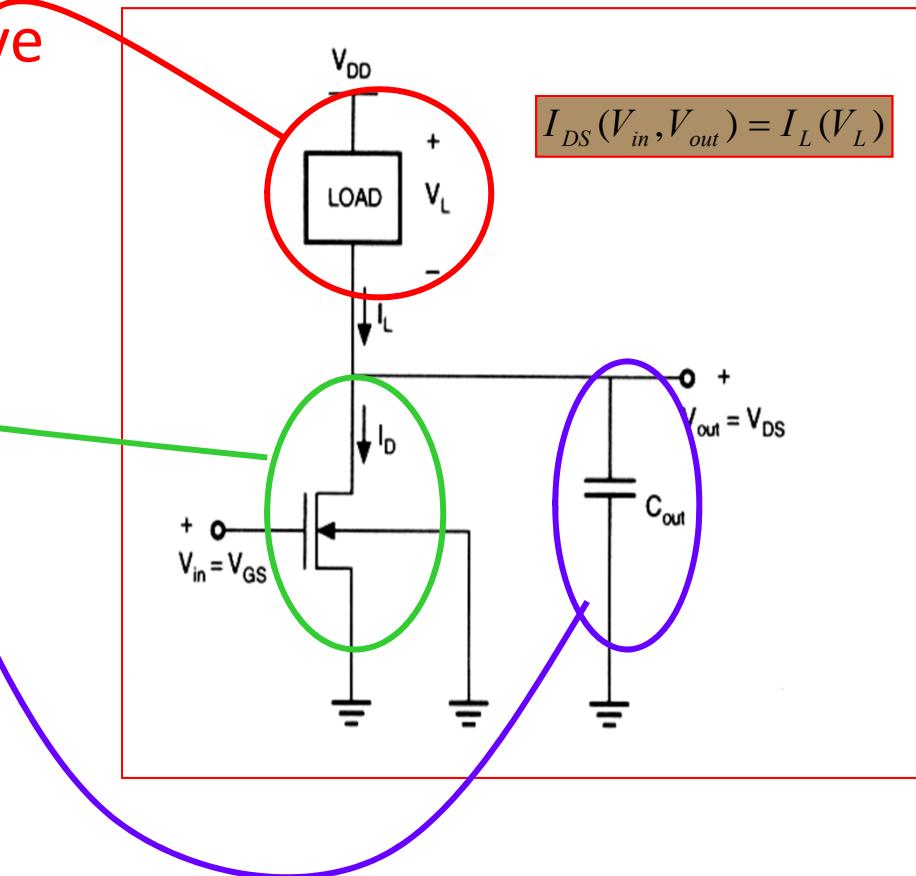
- Input voltage: V_{in}
- Output voltage: V_{out}
- Inverter threshold voltage: $V_{th} = V_{DD}/2$
- Logic « 1 » output :
 - $0 < V_{in} < V_{th}$
- Logic « 0 » output:
 - $V_{th} < V_{in} < V_{DD}$



NMOS Inverter: general circuit structure

- Load: active (MOS) or passive (resistor)
- « driver »

- C_{load} : lumped capacitance
- Input Voltage: $V_{in} = V_{gs}$
- Output Voltage: $V_{out} = V_{ds}$



- DC domain: no input current neither output current
- Kirchoff's current law: $I_{LOAD}(V_L) = I_{DS}(V_{in}, V_{out})$

Inverter: voltage transfer characteristics

With analytical solving

$I_{DS}(V_{in}, V_{out}) = I_L(V_L)$ we found the VTC characteristics:

$$V_{out} = f(V_{in})$$

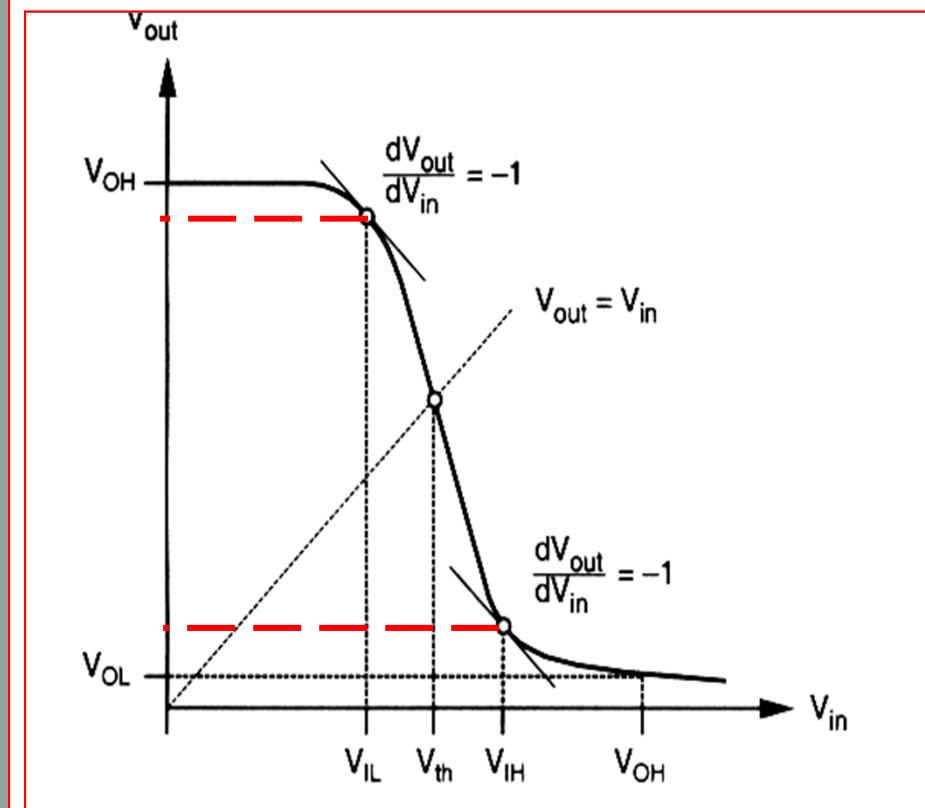
Key voltages:

V_{IL} : maximum input voltage which can be interpreted as a « 0 » logic input

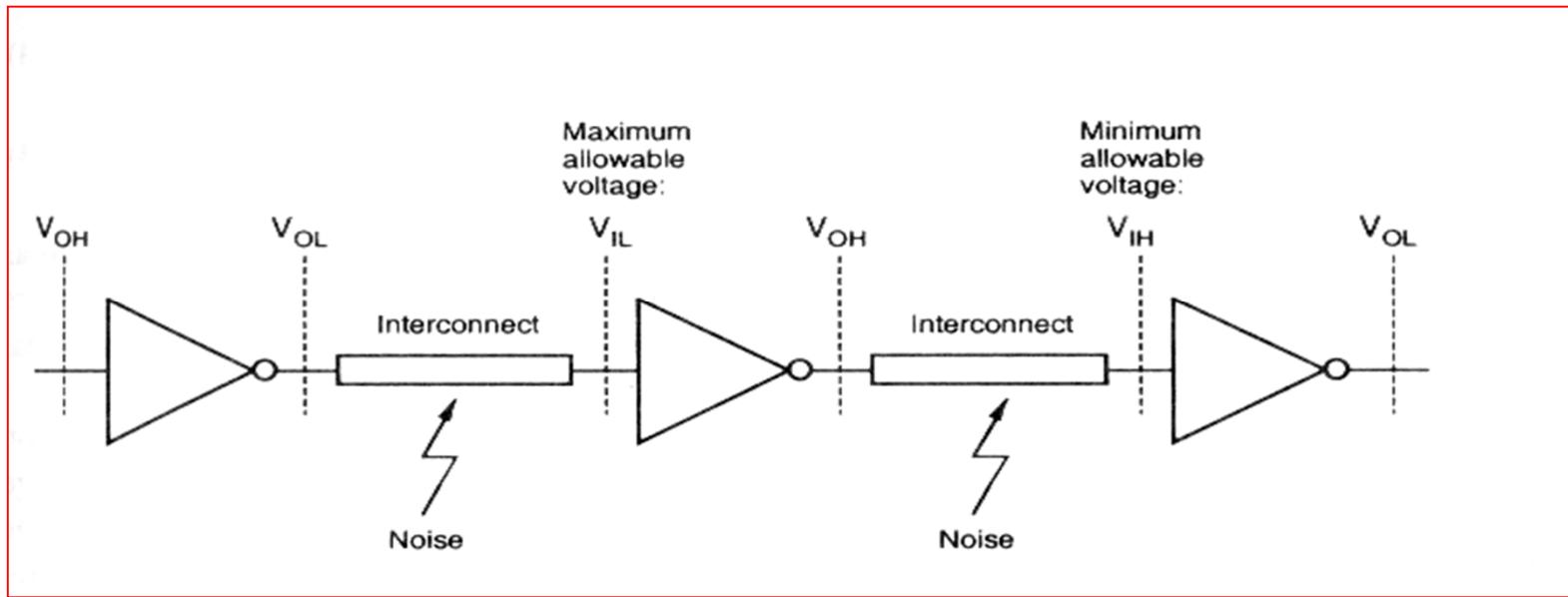
V_{IH} : minimum input voltage which can be interpreted as a « 1 » logic input

V_{OL} : minimum output voltage when the output level is logic « 0 »

V_{OH} : maximum output voltage when the output level is logic « 1 »



Inverters: noise margins



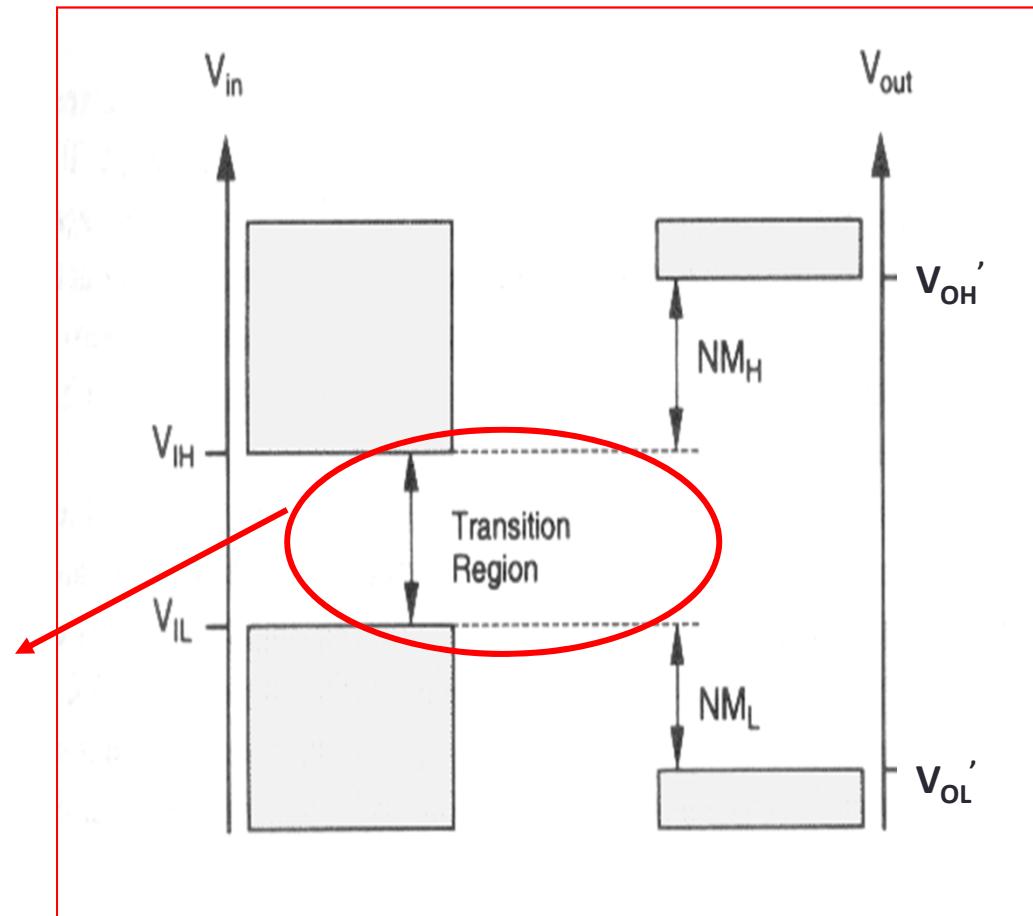
- Interconnexions and gate noise can add parasitics voltage \Leftrightarrow logic faults . We introduce for quantify the noise immunity of the circuit the «noise margins ».
- The noise immunity increases with the noise margins

Inverters: noise margins

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

Uncertainty region \Leftrightarrow must be reduce \Leftrightarrow we must have $V_{IL} \sim V_{IH}$ \Leftrightarrow VTC close to ideal inverter



Inverters: brief summary

- Preceding discussions of inverter static (DC) characteristics show that shape of the VTC in general and noise immunity in particular are very important criteria for design priorities.

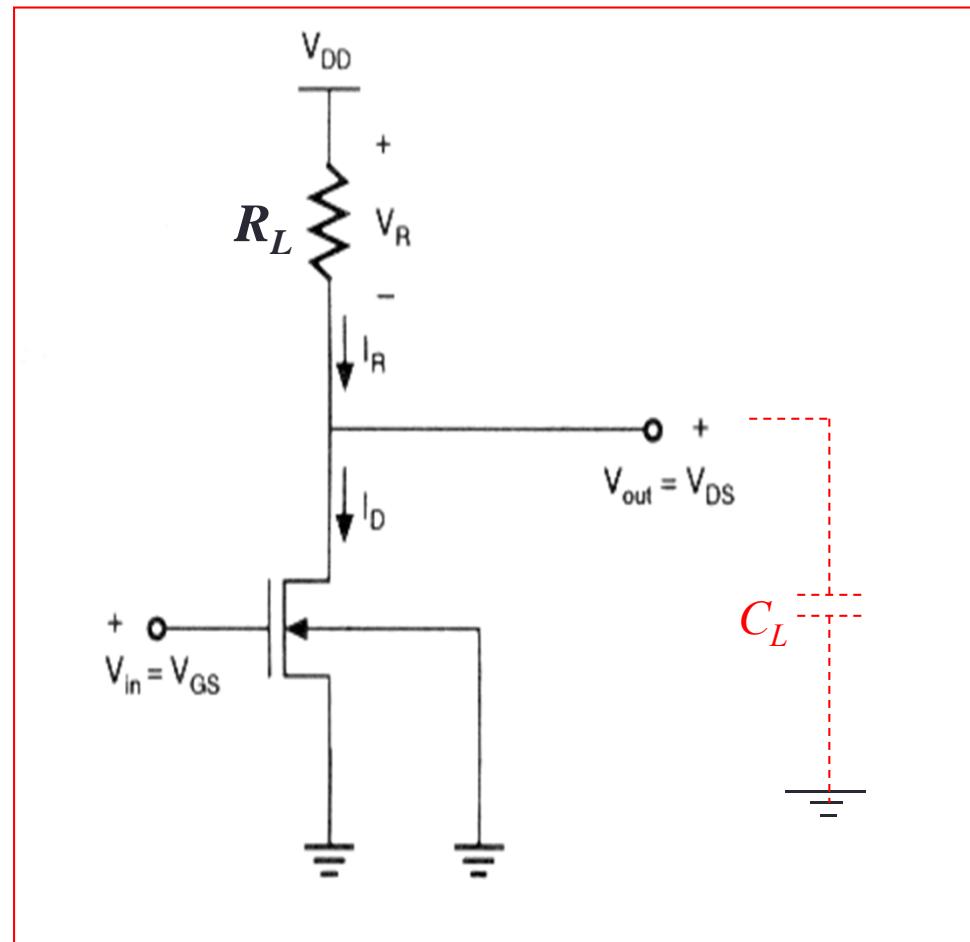
For any inverter circuit five critical points (V_{IL} , V_{IH} , ...) fully determine the properties.

Accurate estimation of these voltage points have to be determined.

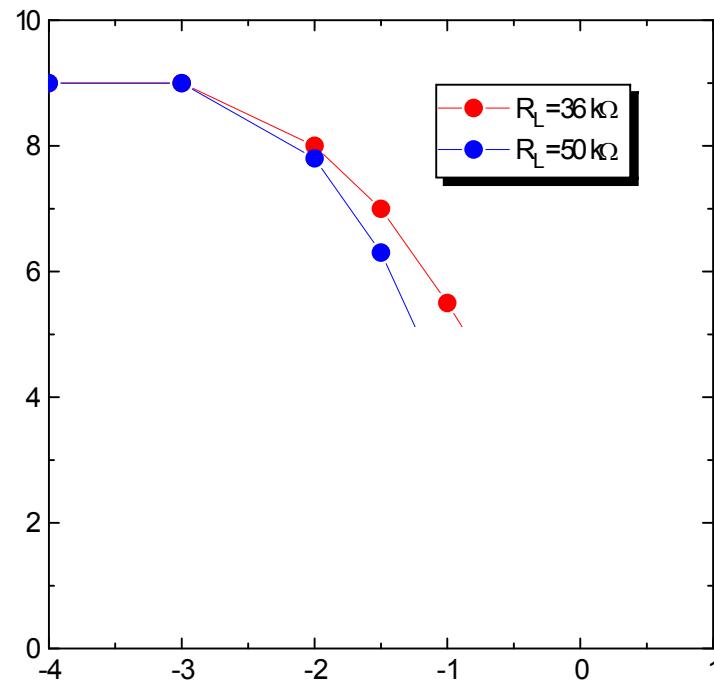
Resistive-load Inverter

- $V_{in} = V_{GS}$
 - $V_{in} = \ll 1 \gg$: n-MOS is ON \Leftrightarrow at first order, Drain grounded $\Leftrightarrow V_{out} = \ll 0 \gg$
 - $V_{in} = \ll 0 \gg$: n-MOS is OFF \Leftrightarrow open circuit $\Leftrightarrow I_L = I_{DS} = 0 \Leftrightarrow V_{out} = V_{DD} = \ll 1 \gg$

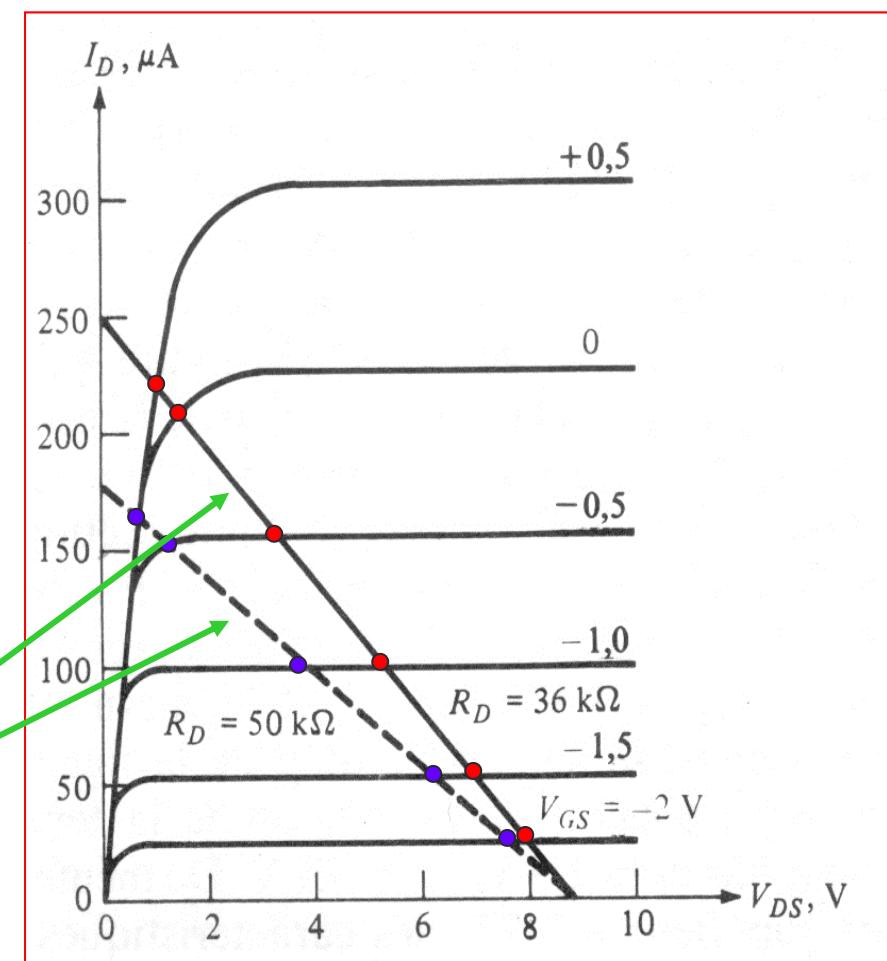
Input Voltage Range	Operating Mode
$V_{in} < V_{T0}$	Cut off
$V_{T0} < V_{in} < V_{out} + V_{T0}$	Saturation
$V_{in} > V_{out} + V_{T0}$	Linear



Resistive-load Inverter : VTC



$$I_L = \frac{V_{DD} - V_{out}}{R_L} = I_{DS}$$



Resistive-load Inverter : VTC

$$V_{OH} = V_{DD}$$

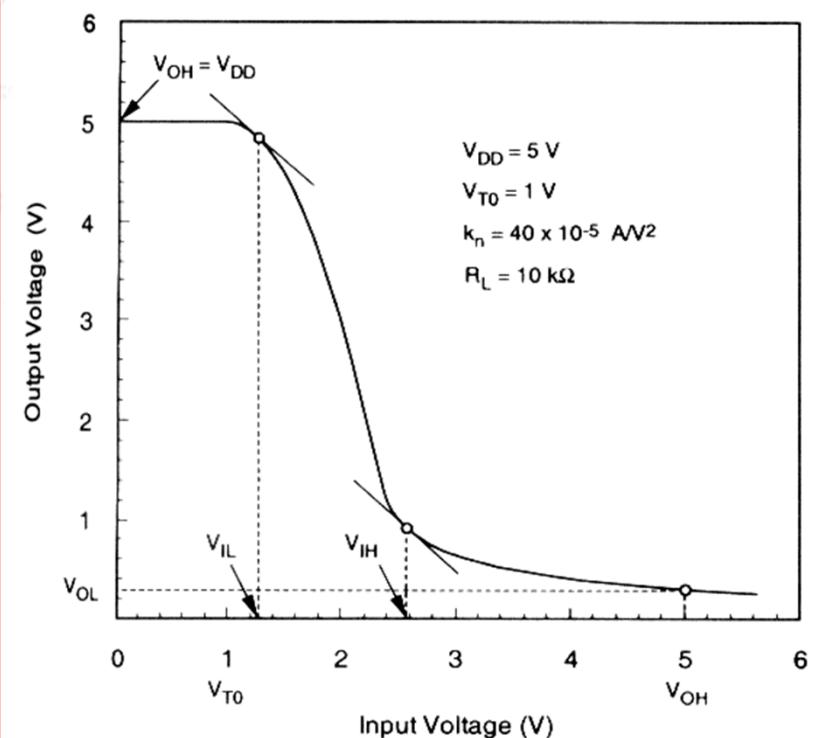
$$V_{OL} = V_{DD} - V_{Tn} + \frac{1}{k_n R_L} - \sqrt{(V_{DD} - V_{Tn} + \frac{1}{k_n R_L})^2 - \frac{2V_{DD}}{k_n R_L}}$$

$$V_{IL} = V_{Tn} + \frac{1}{k_n R_L}$$

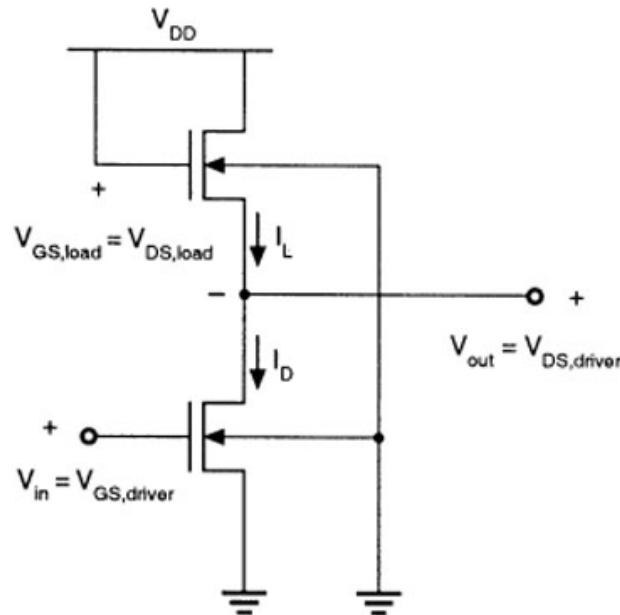
$$V_{IH} = V_{Tn} + \sqrt{\frac{8}{3} \frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L}$$



(good exercise !)



Saturated enhancement-type nMOS Inverters :



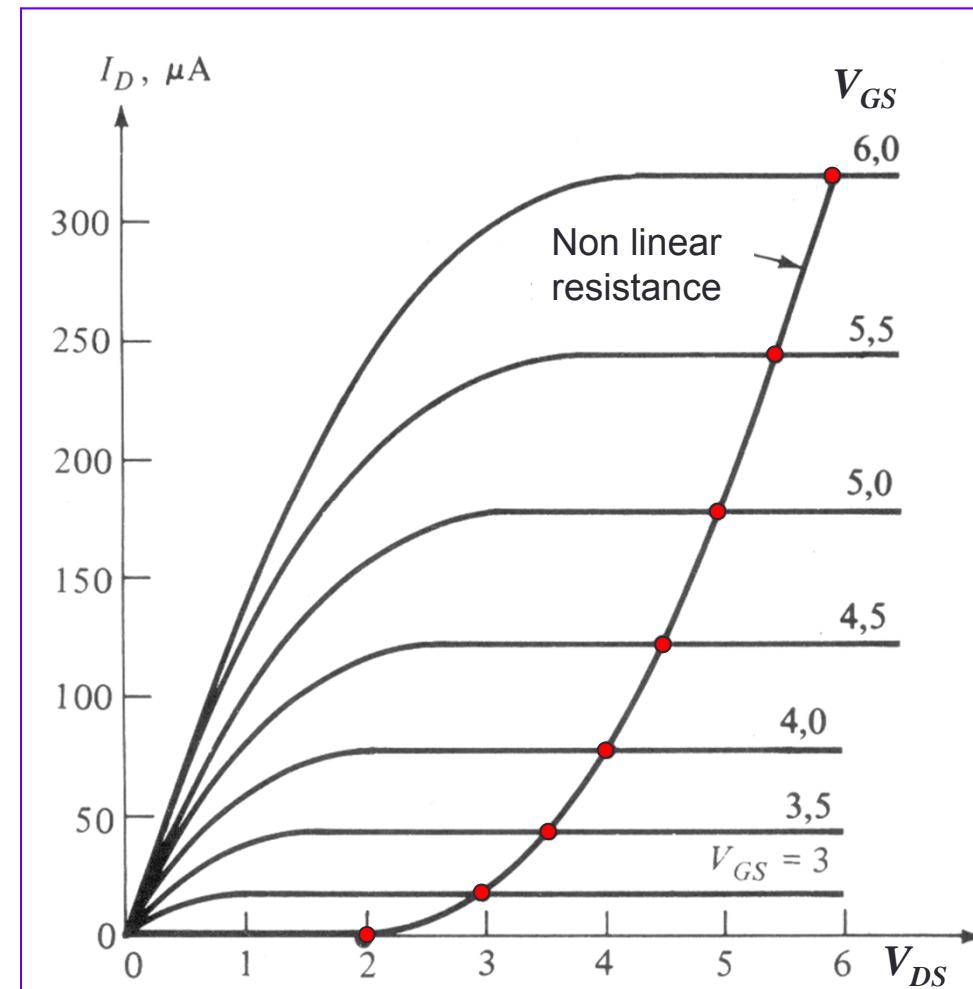
- $V_{GS} = V_{DS} \Leftrightarrow V_{GS} - V_T < V_{DS}$
 \Leftrightarrow saturation mode
- **Warning :** if $V_{out} > V_{DD} - V_T \Leftrightarrow$
cut-off $\Leftrightarrow V_{OH} = V_{DD} - V_T$

Saturated enhancement-type nMOS Inverters : graphic analysis

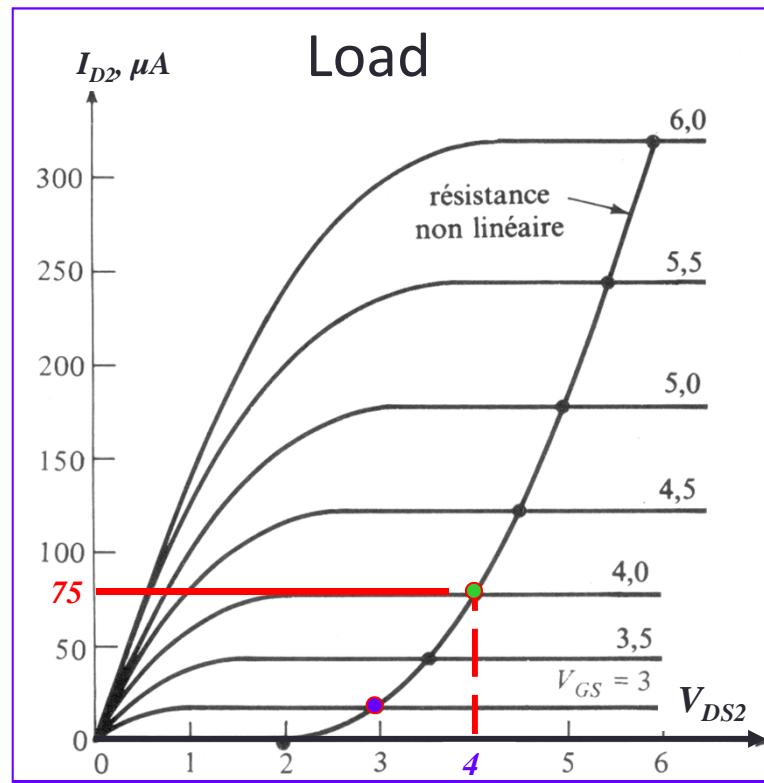
The representative points of the load line are given by :

$$V_{GS} = V_{DS}$$

The load NMOS is equivalent to a non linear resistance



Saturated enhancement-type nMOS Inverters : graphic analysis

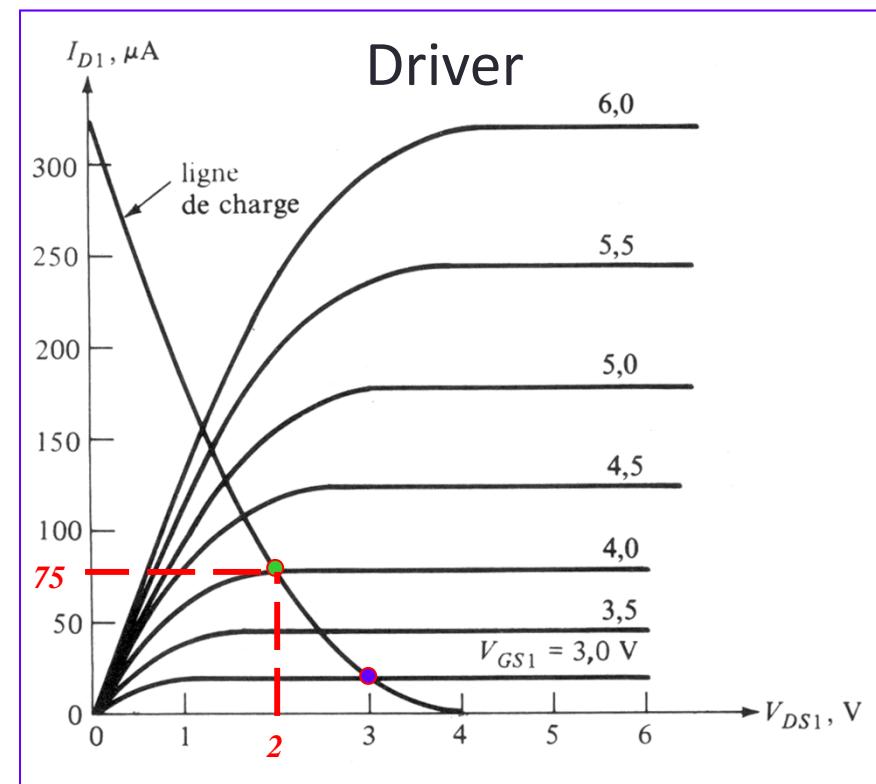


$$V_{DS1} = 6 - 4 = 2 \text{ V}$$

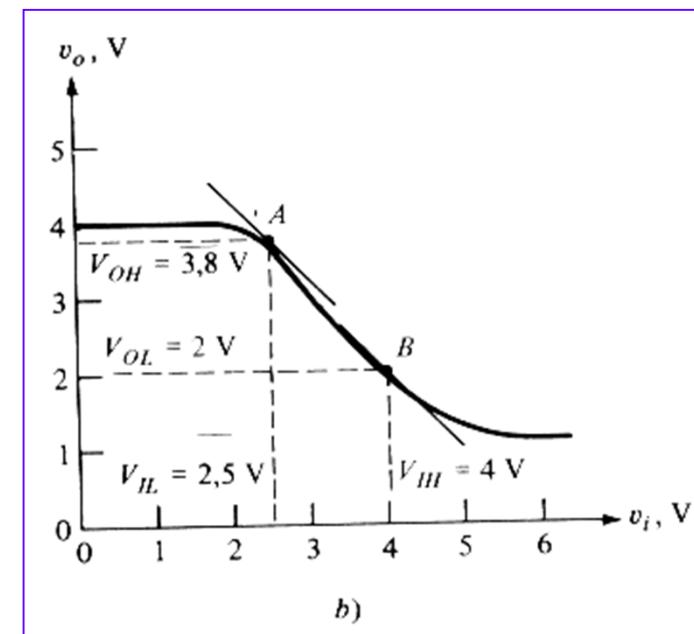
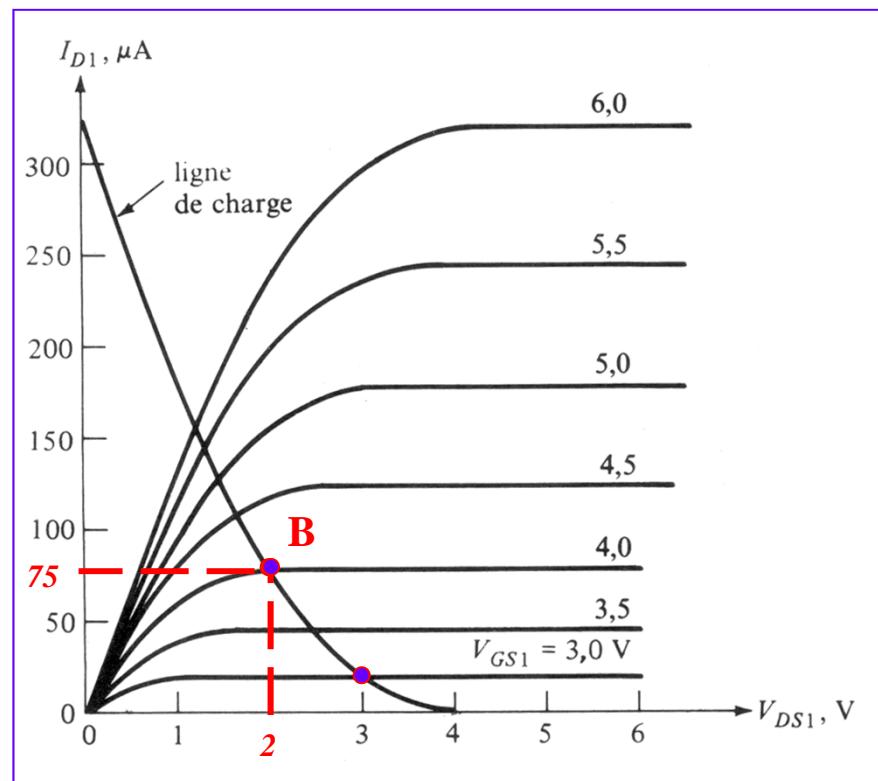
$$I_{D2} = 75 \mu\text{A} = I_{D1}$$

⇒

$$V_{DS1} = V_{DD} - V_{DS2} = 6 - V_{DS2}$$



Saturated enhancement-type nMOS Inverters : graphic analysis



$$NM_H = V_{OH} - V_{IH} = -0.2 \text{ V} < 0$$

By changing the ratio W/L , we can improve NM.

Inverter with linear enhancement type load

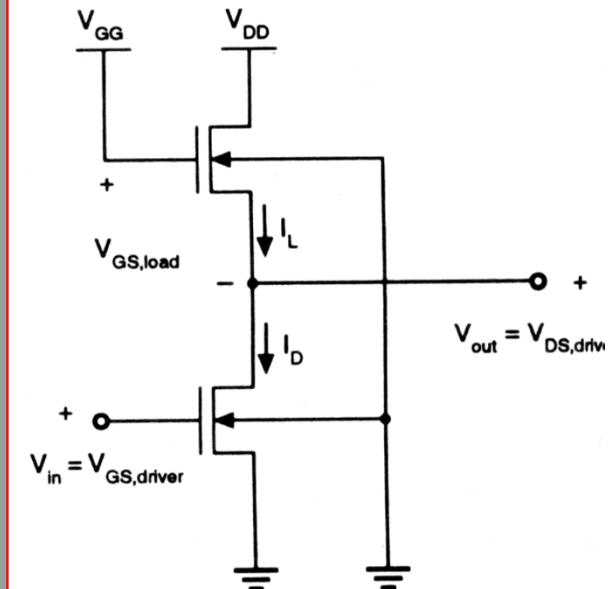
Load transistor never in saturation mode:

$$\square V_{GS,load} - V_{T,load} > V_{DS,load} \quad (1)$$

$$\square V_{GS,load} - V_{DS,load} = V_{GG} - V_{DD}$$

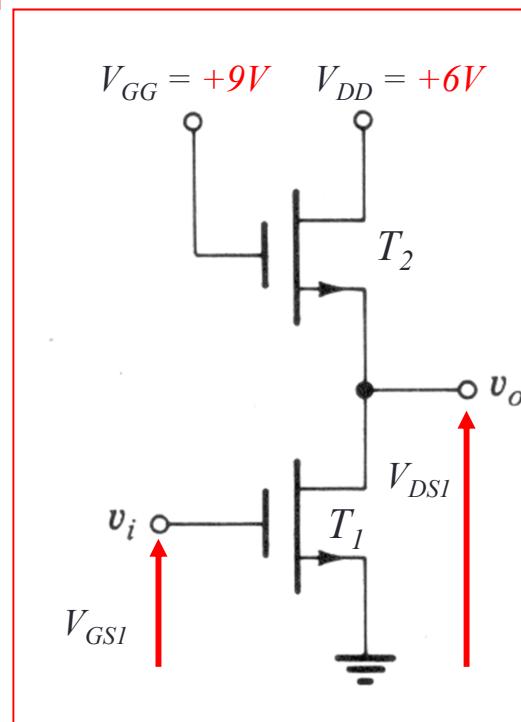
$$\square (1) \text{ OK } \Leftrightarrow V_{GG} - V_{DD} > V_{T,load}$$

→ *non saturated load*



drawback : 2 separated power supply voltage !!

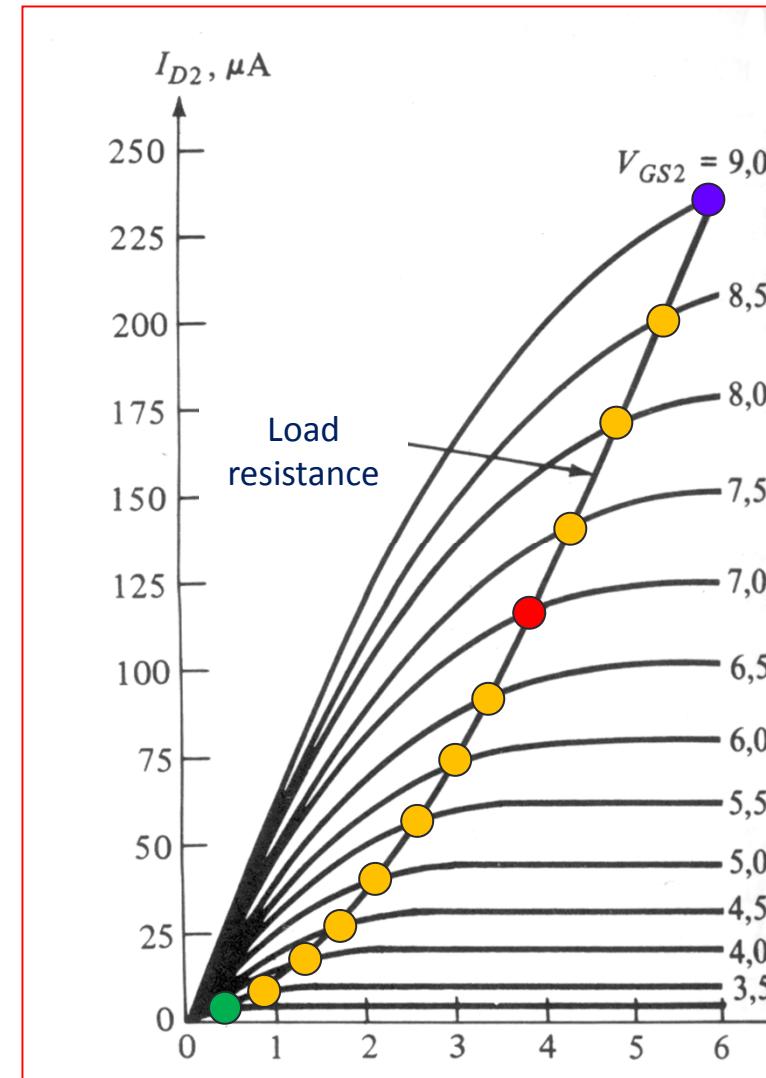
Inverter with linear enhancement type load



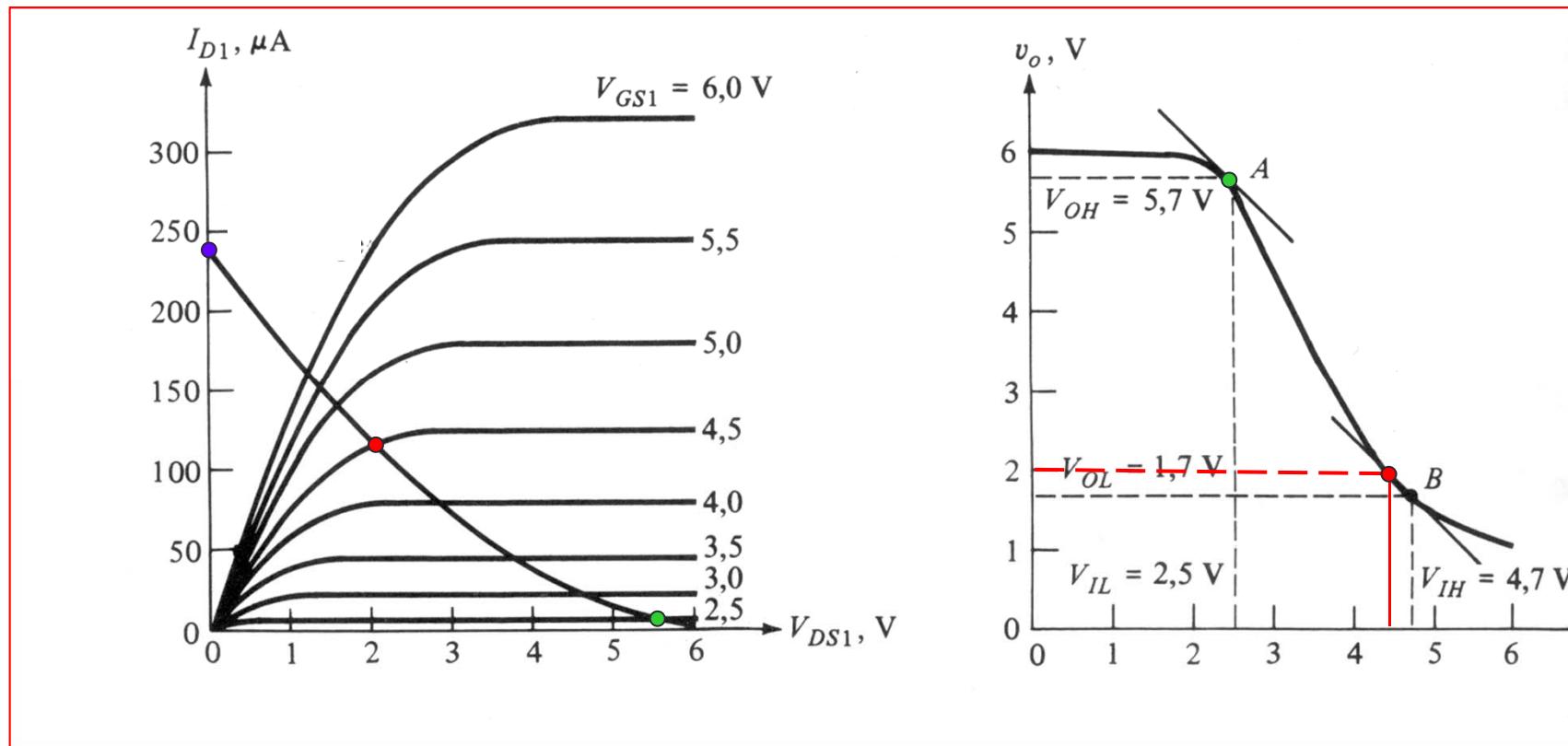
$$V_{GS2} - V_{DS2} = V_{GG} - V_{DD} = 3V$$

$$V_{DS2} = V_{GS2} - 3V$$

Load
resistance

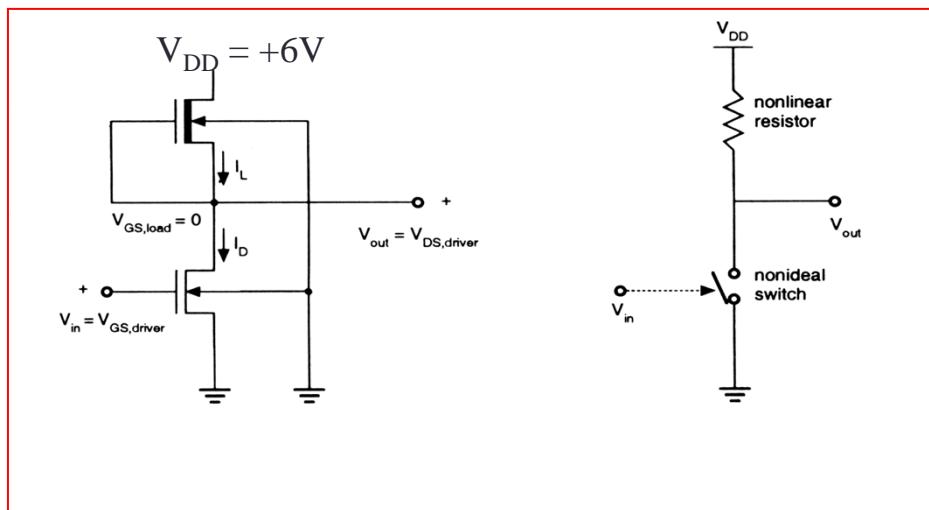


Inverter with linear enhancement type load



$$V_{DS1} = 6 - V_{DS2}$$

Depletion Load NMOS inverter



Vin	Vout	Driver	load
V_{OL}	V_{OH}	Cut off	Linear
V_{IL}	$\sim V_{OH}$	Saturation	Linear
V_{IH}	small	Linear	Saturation
V_{OH}	V_{OL}	linear	saturation

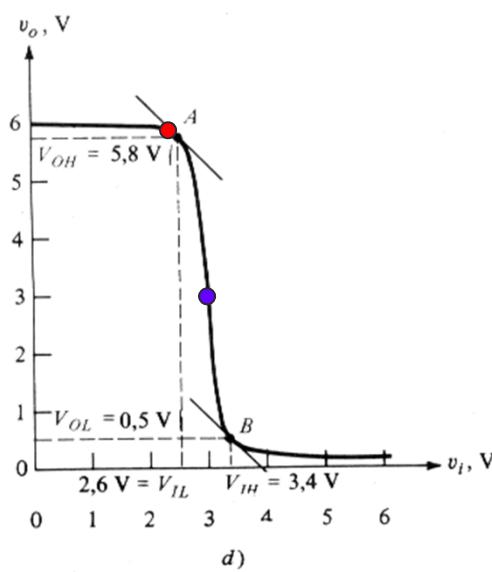
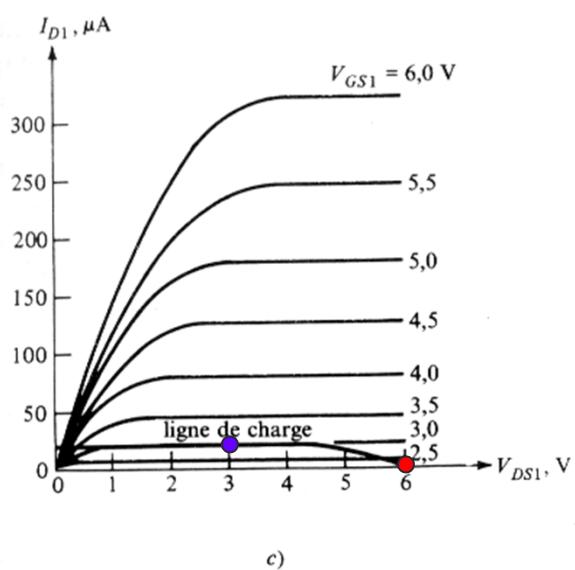
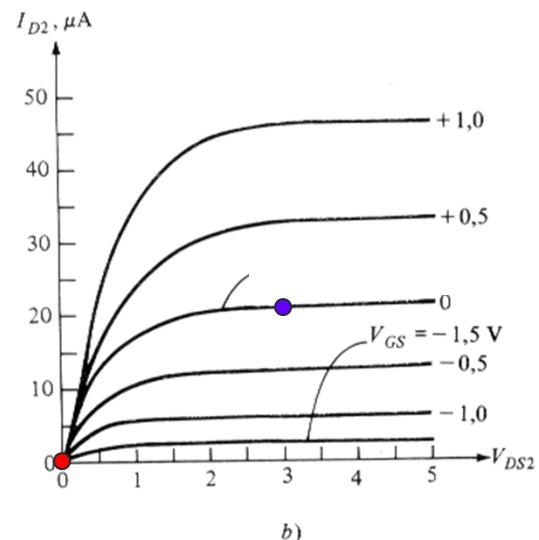
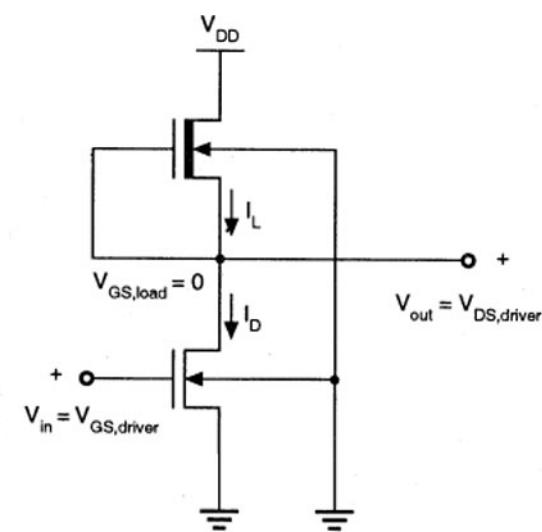
Driver : enhancement $\Leftrightarrow V_{T,Driver} > 0$

Load : depletion $\Leftrightarrow V_{T,load} < 0 \Leftrightarrow V_{GS,load} = 0 > V_{T,load}$

$$V_{SB,load} = V_{DS,pilote} = V_{out} \Leftrightarrow V_{T,load} \text{ sensitive to body effect}$$

$$V_{T,load}(V_{out}) = V_{T0} + \gamma \left(\sqrt{|2\Phi_{Fi}| + V_{out}} - \sqrt{|2\Phi_{Fi}|} \right)$$

Depletion Load NMOS inverter



- $V_{DS2} = 0 \text{ V}, I_{DS2} = 0 \mu\text{A}$

$V_{DS1} = 6 - 0 = 6 \text{ V}$

- $V_{DS2} = 3 \text{ V}, I_{DS2} = 22 \mu\text{A}$

$V_{DS1} = 6 - 3 = 3 \text{ V}$

Depletion Load NMOS inverter

(good exercise!)

$$V_{OH} = V_{DD}$$

$$V_{OL} = V_{OH} - V_{TO,driver} - \sqrt{(V_{OH} - V_{TO,driver})^2 - \frac{k_{load}}{k_{driver}} |V_{T,load}(V_{OL})|^2}$$

$$V_{IL} = V_{T,driver} + \frac{k_{load}}{k_{driver}} [V_{out} - V_{DD} + |V_{T,load}(V_{out})|]$$

$$V_{IH} = V_{T,driver} + 2V_{out} + \frac{k_{load}}{k_{driver}} [-|V_{T,load}(V_{out})|] \frac{dV_{T,load}}{dV_{out}}$$

Drawback (compare to enhancement load Inverter):

- Additional processing step (V_T adjust for load)

Advantages (compare to enhancement load Inverter):

- Sharp VTC transition
- Better noise margins
- Single power supply
- Smaller layout area

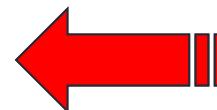
Depletion Load NMOS inverter: power considerations

- $V_{in} = 0$ et $V_{out} = V_{OH}$ \Leftrightarrow driver is cut off $\Leftrightarrow I_{DS}=0$.
No power
- $V_{in}=V_{DD}$ et $V_{out}=V_{OL}$ \Leftrightarrow both transistors ON \Leftrightarrow large current

$$I_{DC}(V_{in} = V_{DD}) = I_{load}(\text{sat}) = I_{driver}(\text{lin})$$

50% of time logic « 1 »

$$P_{DC} = \frac{V_{DD}}{2} \frac{k_{load}}{2} \left[-V_{T,load}(V_{OL}) \right]^2$$

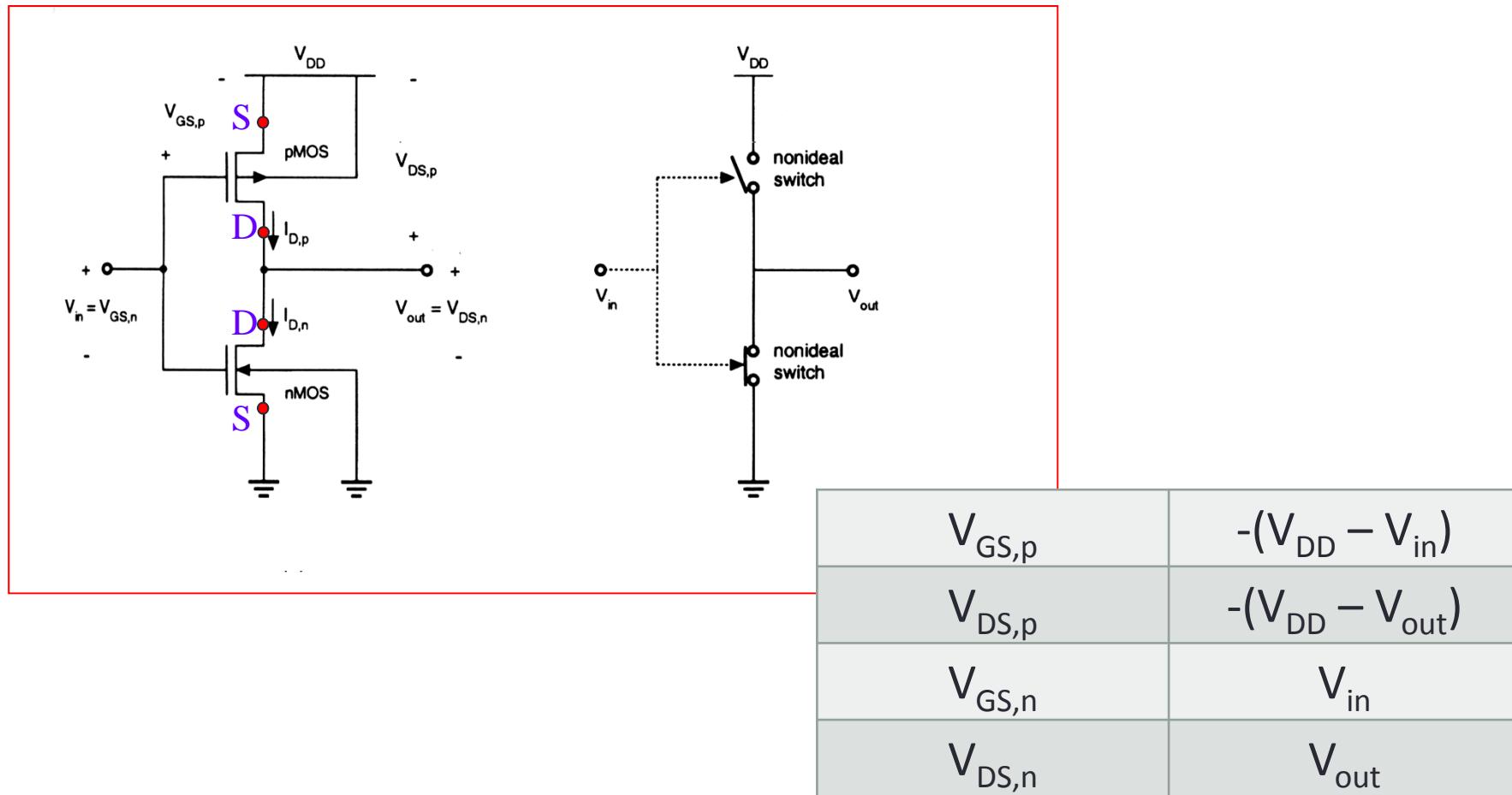


unacceptable

C-MOS inverter

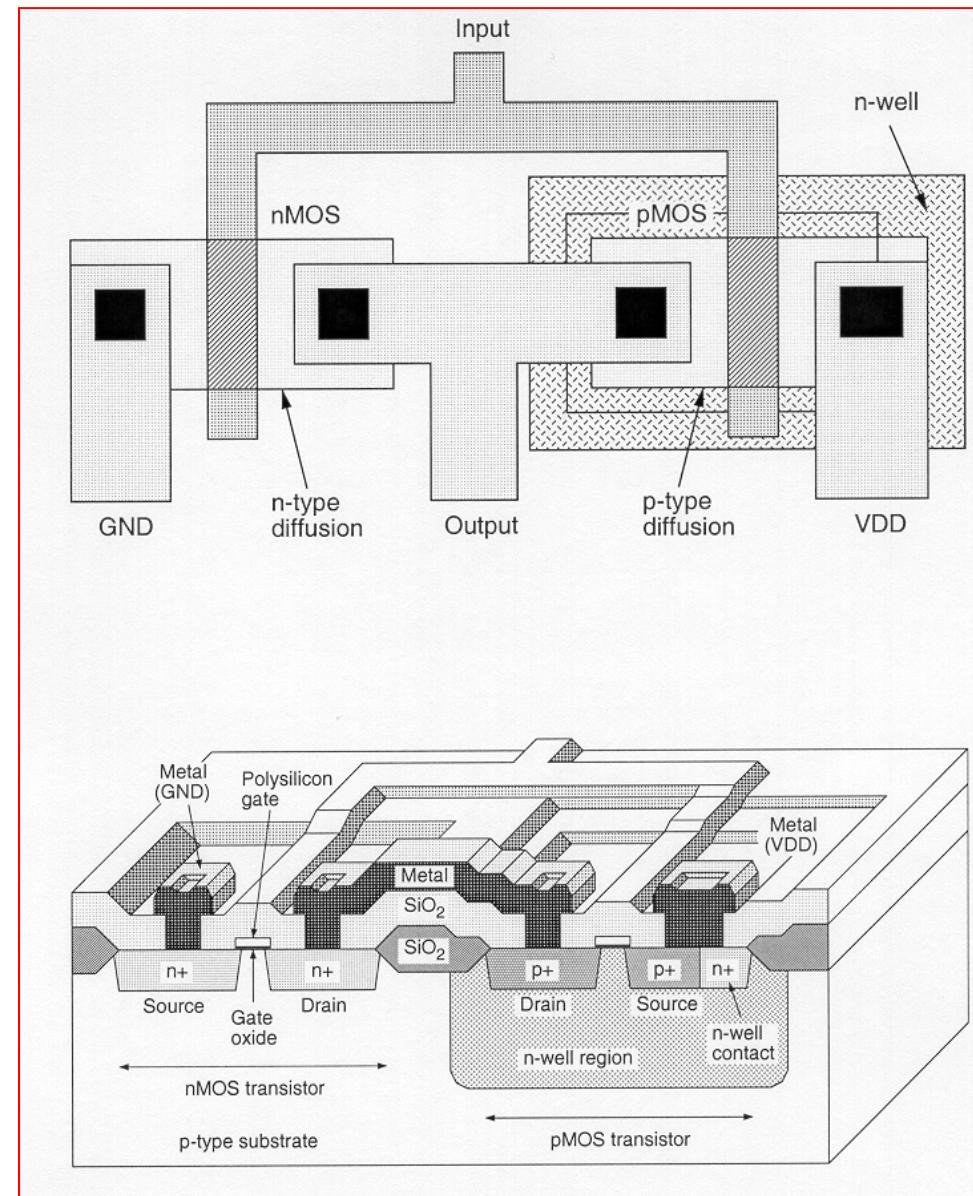
- All previous Inverters are based on :
 - enhancement driver NMOS
 - a load which can be a resistor, an enhancement or depletion NMOS.
- Major drawback: in one state (output level « 0 ») DC consumption or power dissipation nonzero
- New concept /design :
 - One enhancement NMOS and one enhancement PMOS (Complementary MOS or CMOS).
 - Depending on input Voltage, NMOS is the load and PMOS the driver and *vice versa*.
 - Advantages:
 - No DC (steady state) power dissipation (except leakage current)
 - Full output voltage swing between V_{DD} and 0
 - Very sharp VTC transition : very similar to ideal inverter

C-MOS inverter



C-MOS inverter

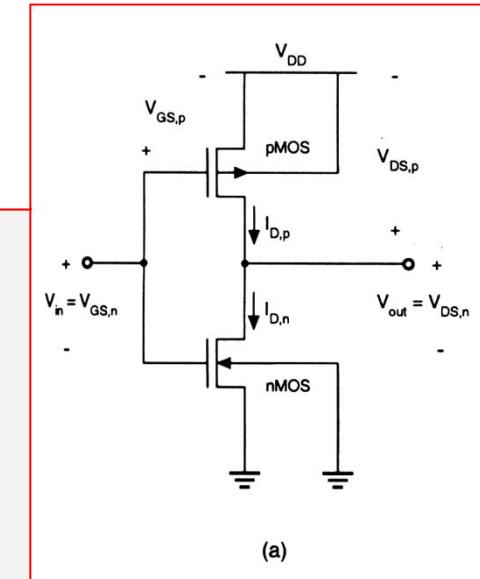
The structure complexity of CMOS is the price to be paid for the improvements achieved in power consumption and the noise margins



C-MOS inverter

- careful! $V_{Tn} > 0$ et $V_{Tp} < 0$
- 1st case: $V_{in} < V_{Tn}$
 - $V_{GS,n} < V_{Tn} \Leftrightarrow n\text{MOS cut off}$
 - $V_{GS,p} < V_{Tp} \Leftrightarrow p\text{MOS 'ON'}$

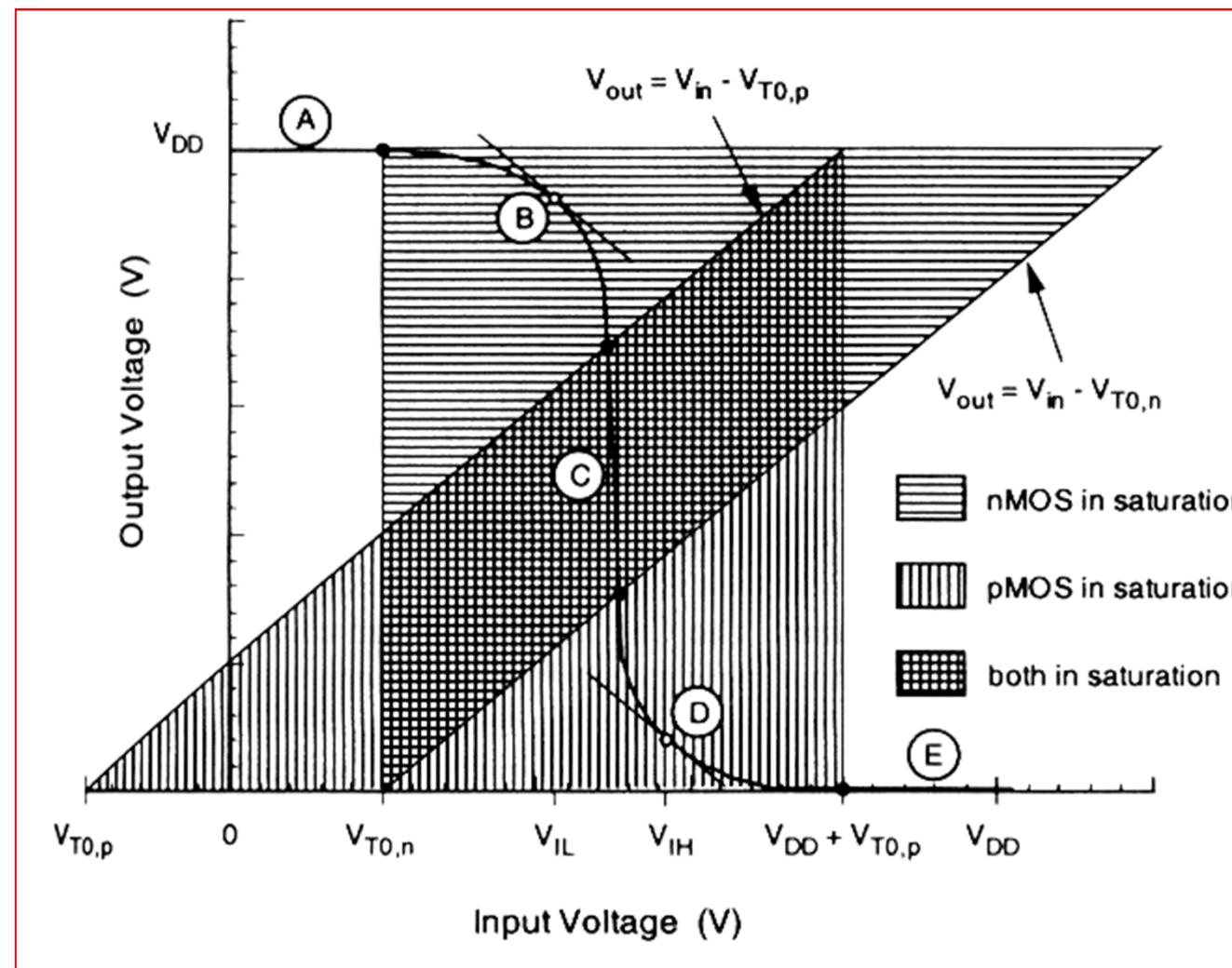
} zero current
 $V_{out} = V_{DD} = V_{OH}$



- 2nd case: $V_{in} > V_{DD} + V_{Tp}$
 - $V_{GS,n} > V_{Tn} \Leftrightarrow n\text{MOS 'ON'}$
 - $V_{GS,p} > V_{Tp} \Leftrightarrow p\text{MOS cutoff}$

} zero current
 $V_{out} = V_{OL} = 0$

C-MOS inverter



C-MOS inverter

Region	V_{in}	V_{out}	nMOS	pMOS
A	$< V_{Tn}$	V_{OH}	Cut off	linear
B	V_{IL}	« 1 » $\approx V_{OH}$	Saturation	linear
C	V_{th}	V_{th}	Saturation	Saturation
D	V_{IH}	« 0 » $\approx V_{OL}$	linear	Saturation
E	$> (V_{DD} + V_{T,p})$	V_{OL}	linear	Cut off



Consumption zone when switching

C-MOS inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = 0$$

$$V_{IL} = \frac{2V_{out} + V_{T,p} - V_{DD} + k_R V_{T,n}}{1 + k_R}$$

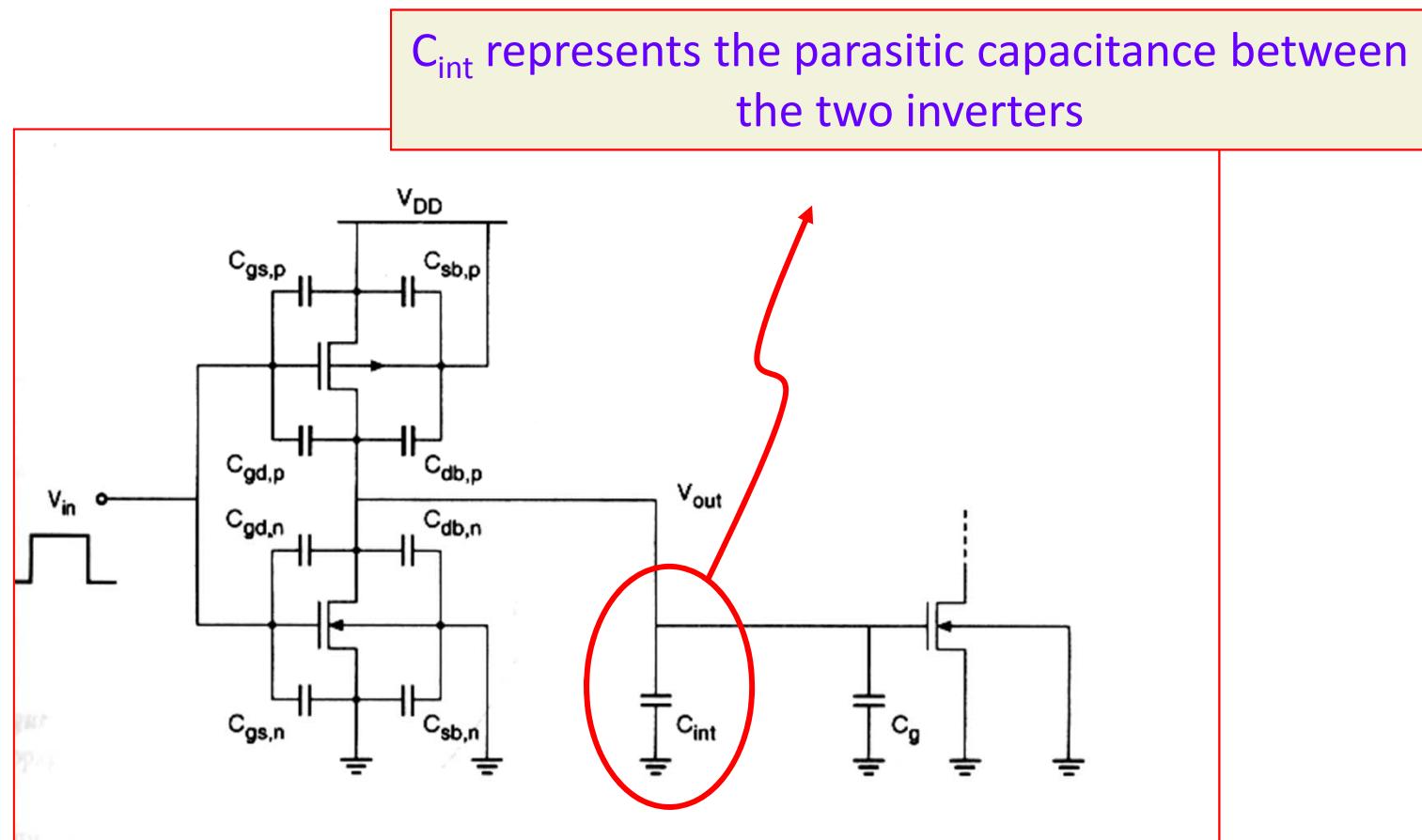
$$V_{IH} = \frac{V_{DD} + V_{T,p} + k_R \cdot (2V_{out} + V_{T,n})}{1 + k_R}$$

$$V_{th} = \frac{V_{T,n} + \sqrt{\frac{1}{k_r} (V_{DD} + V_{T,p})}}{(1 + \sqrt{\frac{1}{k_r}})}$$

$$k_R = \frac{k_{p_n}}{k_{p_p}} \quad k_p = \mu C_{ox} \frac{W}{L}$$

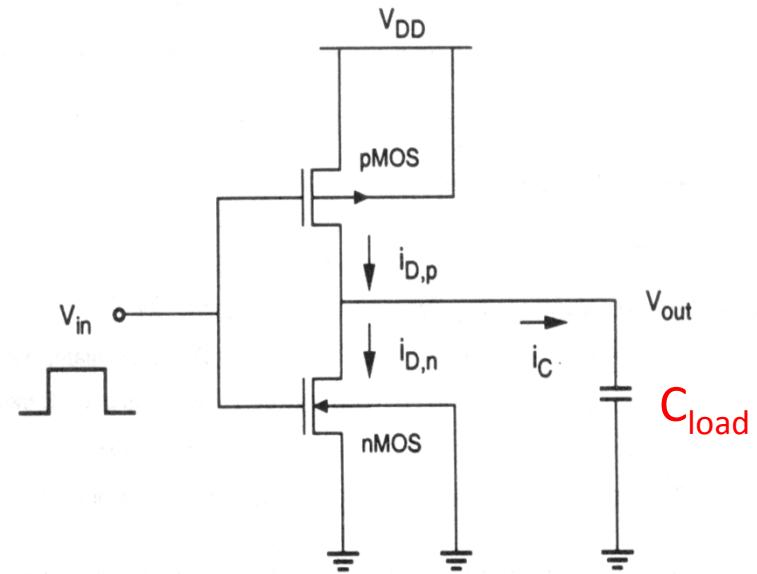
C-MOS inverter: switching characteristics

Interconnect effects



C-MOS inverter: switching characteristics

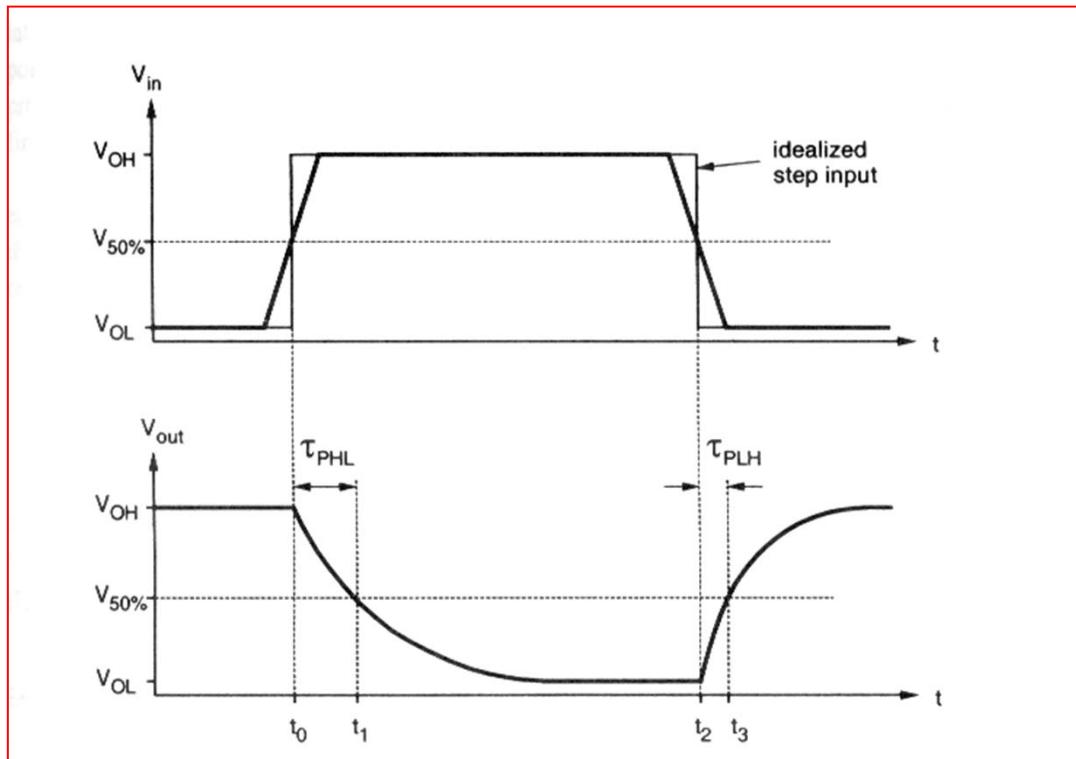
- To simplify the problem, all the capacitances are combined into a unique lumped linear capacitance C_{load}
- The question of inverter transient response is reduced to finding the charge-up and charge-down time of a single capacitance which is charged and discharged through a transistor (NMOS or PMOS).



$$C_{load} = C_{gd,n} + C_{gd,p} + C_{db,n} + C_{db,p} + C_{int} + C_g$$

C-MOS inverter: switching characteristics

- Delay-time or Propagation-time:



τ_{PLH} : delay time from « 0 » to « 1 ».

τ_{PHL} : delay time from « 1 » to « 0 ».

The average propagation delay time :

$$\tau_p = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

C-MOS inverter: switching characteristics

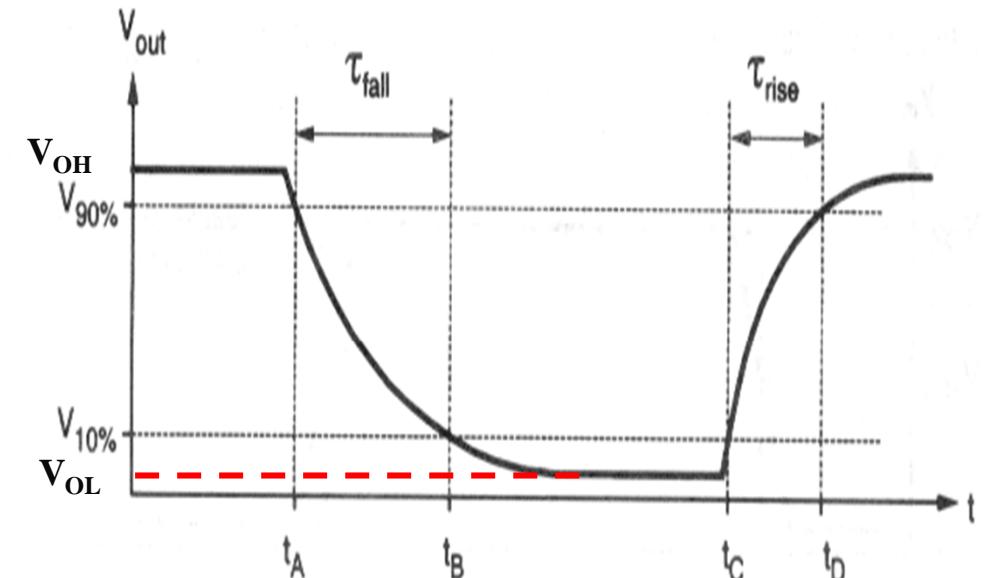
- Output voltage Rise and Fall time:

$$V_{10\%} = V_{OL} + 0.1(V_{OH} - V_{OL})$$

$$V_{90\%} = V_{OL} + 0.9(V_{OH} - V_{OL})$$

$$\tau_{fall} = t_B - t_A$$

$$\tau_{rise} = t_D - t_C$$



C-MOS inverter: switching characteristics

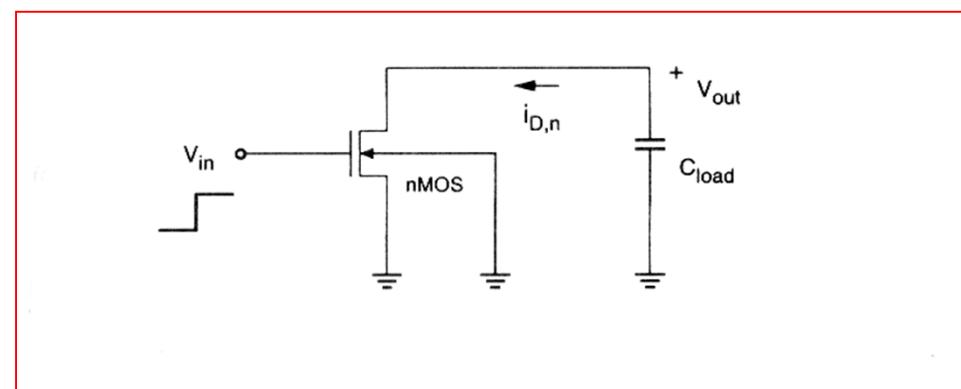
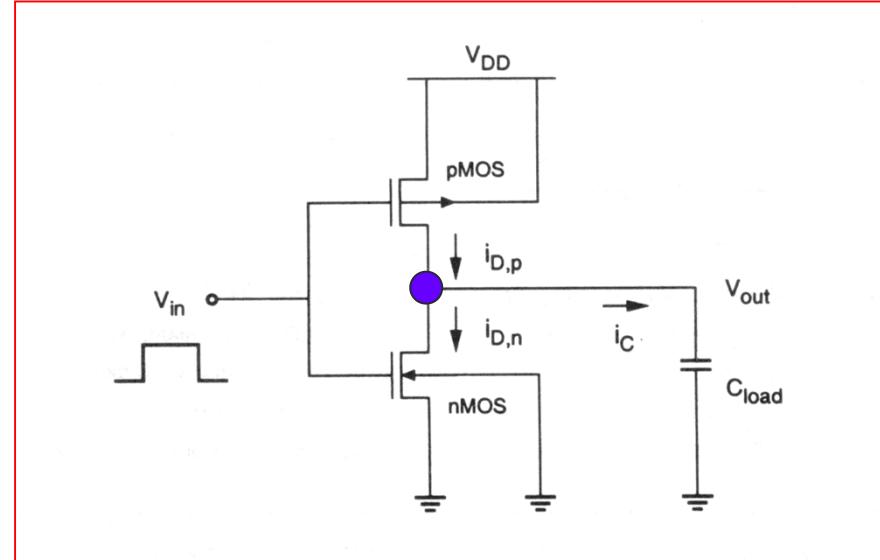
Calculation of delay times:

$$C_{load} \frac{dV_{out}}{dt} = i_C = i_{D,p} - i_{D,n}$$

Fall time calculation:

- V_{in} switches from V_{OL} to V_{OH}
- nMOS is turned 'ON' and it starts to discharge C_{load}
- pMOS is switched off $\Leftrightarrow i_{D,p} \approx 0$

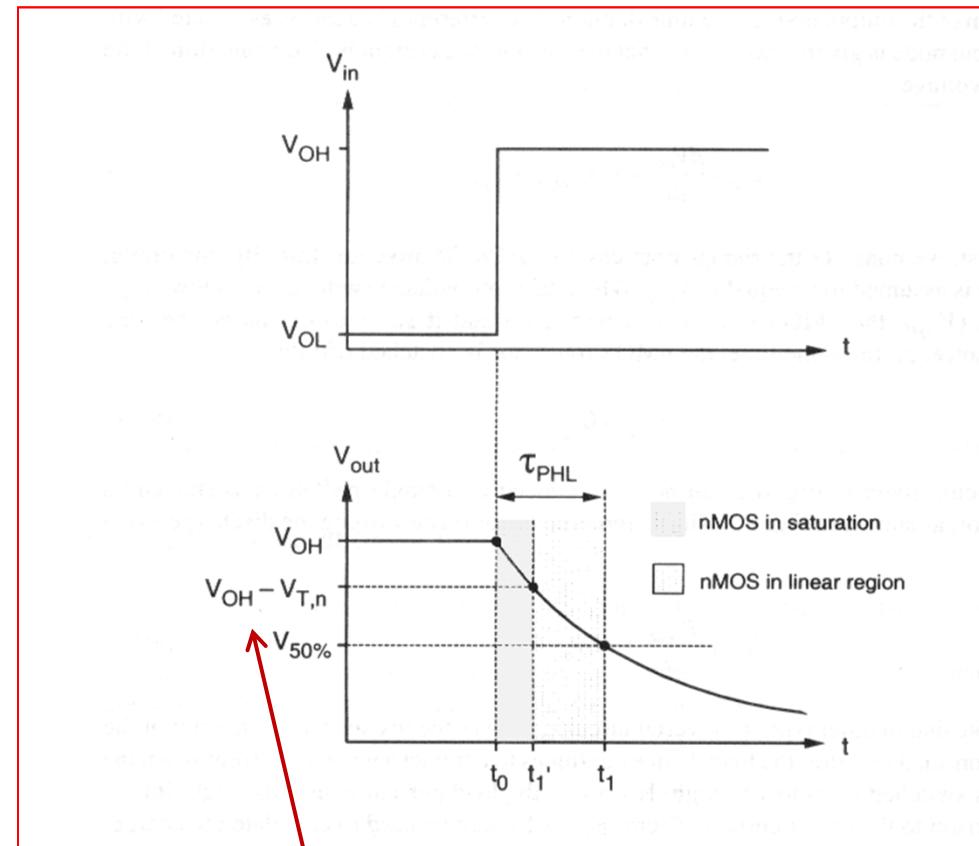
$$C_{load} \frac{dV_{out}}{dt} = -i_{D,n}$$



C-MOS inverter: switching characteristics

Be carefull : during the switching, operating mode of MOS changes !!

In our case , we have to decompose the calcul in two delay-times



NMOS in saturation ?

$$V_{GSn} - V_{TN} < V_{DS} \Leftrightarrow V_{in} - V_{TN} < V_{out} \Leftrightarrow V_{OH} - V_{Tn} < V_{out}$$

C-MOS inverter: switching characteristics

- After few steps

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{OH} - V_{T,n})} \left[\frac{2V_{T,n}}{V_{OH} - V_{T,n}} + \ln \left(\frac{4(V_{OH} - V_{T,n})}{V_{OH} + V_{OL}} - 1 \right) \right]$$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{OH} - V_{OL} - |V_{T,p}|)} \left[\frac{2|V_{T,p}|}{V_{OH} - V_{OL} - |V_{T,p}|} + \ln \left(\frac{2(V_{OH} - V_{OL} - |V_{T,p}|)}{V_{OH} - V_{50\%}} - 1 \right) \right]$$

C-MOS inverter: switching characteristics

- Other method (more simple, less accurate): average current method

$$\tau_{PHL} = \frac{C_{load} \times \Delta V_{HL}}{I_{avg\,HL}} = \frac{C_{load} \times (V_{OH} - V_{50\%})}{I_{avg\,HL}}$$

$$I_{avg\,HL} = \frac{1}{2} [i_c(V_{in} = V_{OH}, V_{out} = V_{OH}) + i_c(V_{in} = V_{OH}, V_{out} = V_{50\%})]$$

C-MOS inverter: switching characteristics

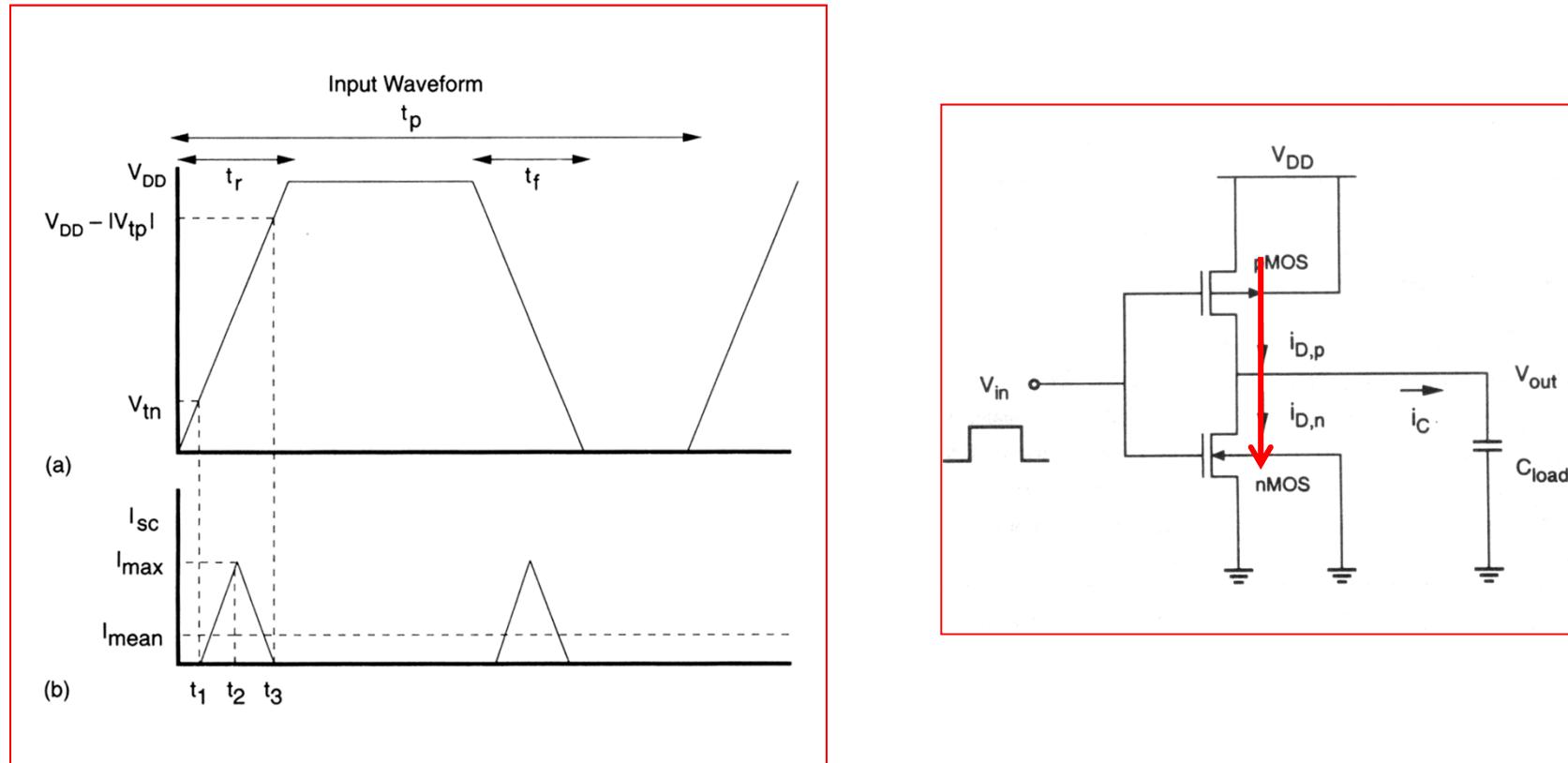
Power dissipation for a gate CMOS during switching : this is the power used to charge and discharge the capacitance C_{load} .

$$P_{avg} = \frac{1}{T} \int_0^T v(t) \times i(t) \times dt$$

$$P_{avg} = C_{load} V_{DD}^2 f$$

C-MOS inverter: switching characteristics

Another source of power consumption: the short-circuit current, *i.e.* a direct pathway from power supply to ground through PMOS and NMOS, both of them being in “ON” state.



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Figures and tables mainly from these references

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THANK YOU FOR YOUR
ATTENTION!

感谢您的关注

