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Training on
Verification Methodologies for IP and SoC Designs

LAB
Assertions

Objectives

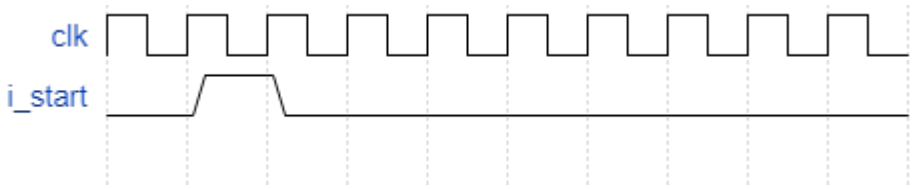
This lab proposes to implement assertions within an SystemVerilog interface.

The goal is to become familiar with the main assertion constructs in the context of protocol checking.

Instructions

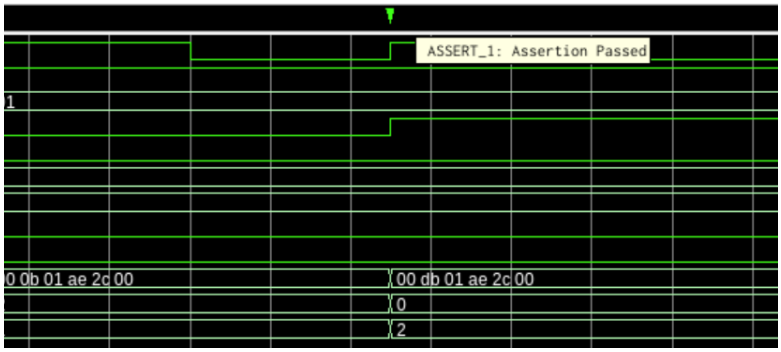
Follow instructions given in “aedv_training_labs_intructions_for_questa.pdf”.
Open the file <SANDBOX>/labs-Xdays/labNN-systemverilog_assertions/lab_v2.sv”
Select

Step 1: First Assertion



- The *i_start* signal must only be active for one clock cycle

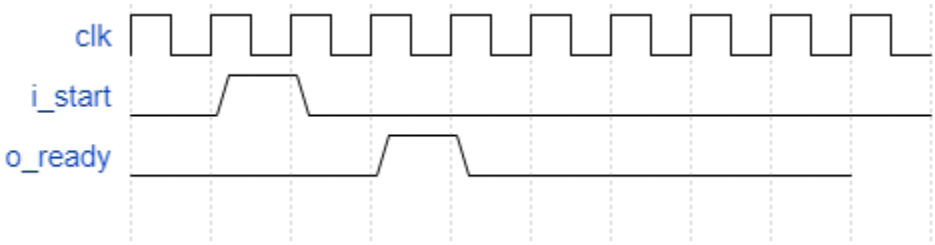
- Open the file: <SANDBOX>/labs-Xdays/labNN-systemverilog_assertions /adder_if.sv
- Search for ***LAB-TODO-STEP1-a***
- Uncomment the block to create the assertion to deal this feature
- Re-run
- Open the waveform window:



- You can see your assertion on the waveform window like this image above.

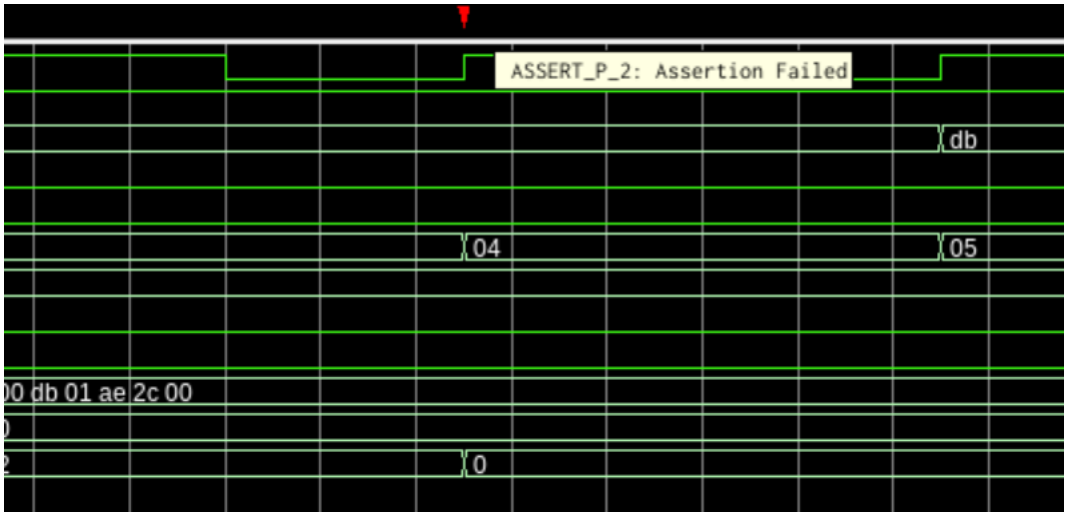
- Questions:
  - What do the |-> operator mean?
  - What do the ##1 operator mean?
- Search for ***LAB-TODO-STEP1-b***
- Replace the -> #1 with =>
- Re-run
- Question:
  - Why do not we need ##1 anymore?

Step 2: Second Assertion



- The *o_ready* signal must be active 2 clock cycles after the *i_start* one.

- Search for ***LAB-TODO-STEP2-a***
- Uncomment the block to create the assertion to deal this feature
- Re-run
- Question:
  - Did you get an assertion fail?
  - What do you think that is the problem?



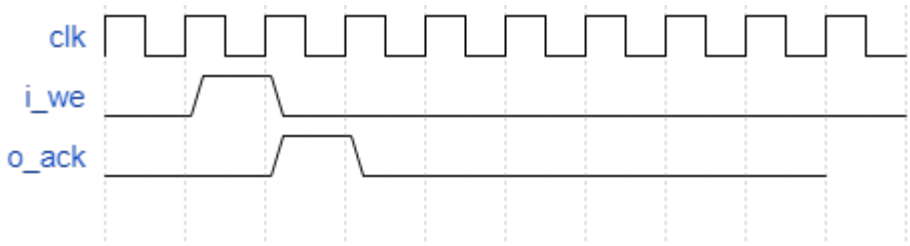
- You can see the assertion fail on the waveform window like this image above.

- Open the file: <SANDBOX>/labs-Xdays/labNN-systemverilog_assertions /dut/full_adder_if.sv
- Search for ***LAB-TODO-STEP2-b***
- Uncomment the following line to fix the design
- Open the file: <SANDBOX>/labs-Xdays/labNN-systemverilog_assertions /adder_if.sv
- Search for the first ***LAB-TODO-STEP2-c***
- Uncomment the block to create a sequence to replace the *##2 o_ready* statement
- Search for the second ***LAB-TODO-STEP2-c***

- Replace the previous statement with the sequence

- Search for the first ***LAB-TODO-STEP2-d***
- Create a property inside the clocking block *cb* to perform the same property from the ASSERTION_2.
- Search for the second ***LAB-TODO-STEP2-d***
- Delete the ASSERTION_2 above and create the assertion that uses the property declared inside the *cb*
- Question:
    - Why is it interesting create a property inside the *cb* block?

Step 3: Third Assertion



- The *o_ack* signal must be active one clock cycle after the *i_we* one is set and must following active until the following clock edge where the *i_we* is inactive indicating that the writing was performed.
- Search for the first ***LAB-TODO-STEP3-a***
- Create the assertion by yourself.