AEDVICES Consulting
166B Rue du Rocher de Lorzier
38430 Moirans– France
trainings@aedvices.com
http://www.aedvices.com

Training on
Verification Methodologies for IP and SoC Designs

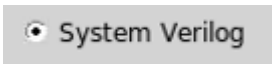
LAB
Threads and Clocking Blocks

Objectives

This lab goes through the main programming concepts of SystemVerilog clocking blocks and thread controls. It shows how to use SystemVerilog language to create clocking schemes to sample or drive signals and how threads can be used to control different parts of the testbenches.

Instructions

Follow instructions given in "aedv_training_labs_intructions_for_questa.pdf".
Open the file <SANDBOX>/labs-Xdays/labNN-systemverilog_programs/lab.sv"
Select



LAB Instruction:

- Open the file "trainings/verification_methodology/5-day-labs/lab03/lab.sv" in your favourite editor.
- Search for "LAB-TODO"
- Follow the instructions presents in this file.

Run the code and analyse the waveforms.

Question:

- What ##10 means ?
- What happens if you replace **input #1step** with **input negedge** ? with **input 100ps** ?
- What happens if you replace output negedge with **output 100ns** ? with 100ps ?
- What is the potential issue in case we use both input negedge and output negedge ?