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Training on
Verification Methodologies for IP and SoC Designs

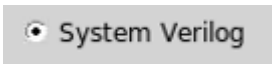
LAB
Checkers

Objectives

This labs proposes to implement assertions within a SystemVerilog checker and instantiate it in an interface..

Instructions

Follow instructions given in “aedv_training_labs_intructions_for_questa.pdf”.
Open the file <SANDBOX>/labs-Xdays/labNN-systemverilog_programs/lab_v2.sv”
Select



Step 1: Create the Checker

- Search for ***LAB-TODO-STEP1-a***
- Declare the checker ports
- Search for ***LAB-TODO-STEP1-b***
- Crete the checker assertions (you can copy the previous assertions created in the previous lab)

Step 2: Instantiate the Checker

- Search for ***LAB-TODO-STEP2-a***
- Declare the checker ports.