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Training on
Verification Methodologies for IP and SoC Designs

LAB
Threads and Clocking Blocks

Commenté [AM1]: I accept suggestions about this lab. I would like to improve it, but I would like some tips before. What do you think about to use the block to the driver and monitor?

Objectives

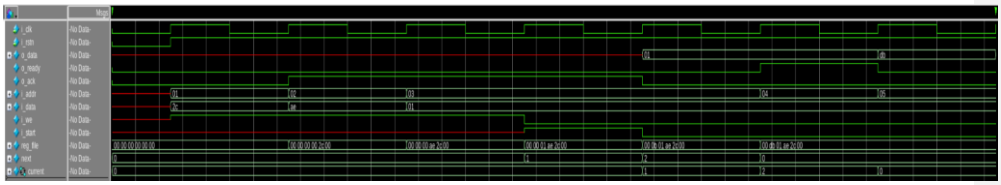
This lab goes through the main programming concepts of SystemVerilog clocking blocks. It shows how to use SystemVerilog language to create clocking schemes to sample or drive signals.

Instructions

Follow instructions given in "aedv_training_labs_intructions_for_questa.pdf".
Open the file <SANDBOX>/labs-Xdays/labNN-systemverilog_programs/lab.sv"
Select

Step 0: Run Simulation

- Run the simulation and look to the waveform.
- It should be something like this:



Step 1: Declare the Clocking Block.

- Open the file: <SANDBOX>/labs-Xdays/labNN-systemverilog_threads /adder_if.sv
- Search for ***LAB-TODO-STEP1-a***
- Declare the clocking block
- Search for ***LAB-TODO-STEP1-b***
- Use the *cb* ports as driver ports

```
    modport driver  (clocking cb, input i_clk, input i_rstn);
```

Step 1: Adapting the Driver.

- Open the file: <SANDBOX>/labs-Xdays/labNN-systemverilog_threads /project_utils_pkg.sv

- Search for ***LAB-TODO-STEP2-a***
- Replace the current assignments with assignments like that:

```
this.vif.cb.i_addr    <= tr.addr;
```

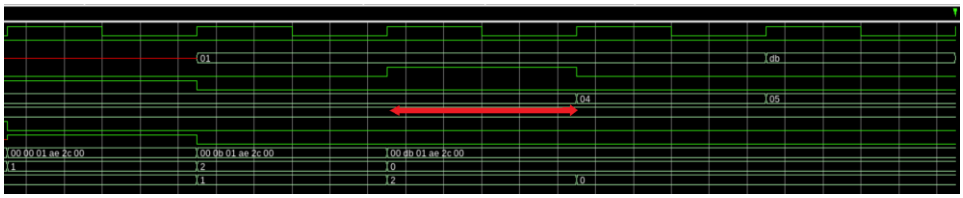
- Do not forget the *while* statement:

```
while(vif.cb.o_ready !== 'h1)
```

- Search for ***LAB-TODO-STEP2-b***
- Replace the delays with:

```
    @(this.vif.cb);
```

- Re-run
- Questions:
  - Why is there a read transaction after compute of the address *0x03*?
  - Look to the waveform. Does it show something like this:



  - Why does this delay exist? (Tip: Skew and "Waiting by o_ready")

Step 3: Default Skews

- Search for ***LAB-TODO-STEP3-a***
- Declare the default output skew equal to #0 (This is not advisable, but we will jut take a look)
- Re-run
- Questions:
  - The delay disappeared now? Why?
- Search for ***LAB-TODO-STEP3-b***
- Replace the default input skew with another value
- Search for ***LAB-TODO-STEP3-***
- Replace the default output skew with #2
- Questions:
  - What happened? And if you replace it with *negedge*?