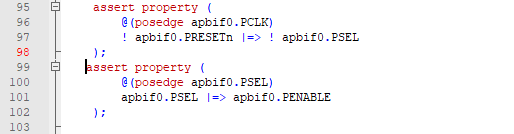
Verification de circuits – systèm verilog – TP3

# introduction

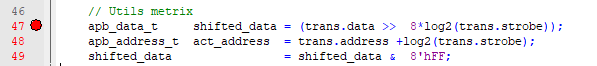
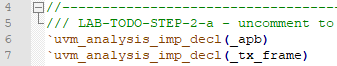
The goal of this lab is to implement a scoreboard checking mechanism between the register interface of the UART and the external serial interface of the UART on the TX line. It focuses on understanding how the scoreboard is connected to multiple monitors and understanding data checking mechanisms.

The DUT here is a UART 16550 from *opencores.org*. The goal of this design is to perform serial transfers on the Tx line and receive Rx transfers from the Rx line, given registers programmable via a APB interface. In this lab we will implement a scoreboard between the APB Register programming interface of the UART and the Tx data that are actually sent by the DUT.

# simple assertion



# connect the scoreboard



# TX scoreboard

# conclusion