STM32F7 SOM (System-On-Module)

Hardware Architecture

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1. Introduction

This document describes the hardware architecture of the Emcraft Systems STM32F7 SOM (System-On-Module).

The STM32F7 SOM is intended to provide a flexible platform for embedded applications that require rich connectivity, low power and flexibility of the STM32F746 coupled with a full-fledged uClinux software execution environment running on the ARM Cortex-M7 processor core.

The STM32F7 SOM is based on the ST Microelectronics STM32F746 versatile, low-power, high-integration microcontroller.

Using a miniature mezzanine form factor, the STM32F7 SOM is specifically designed to provide the primary STM32F7-based intelligence on various boards targeting industrial automation, system and power management, wireless networking / sensors and other embedded applications. STM32F7 SOM hardware and software are architected to ensure flexibility in customizing its functionality for the needs of particular products and/or customers.

2. Hardware Platform

This section defines the hardware platform of the STM32F7 SOM.

2.1. Hardware Platform Overview

The following are the key hardware features of the STM32F7 SOM:

- Compact (30 mm x 46 mm) mezzanine module;
- External interface using two 80-pin 0.4 mm-pitch connectors;
- Mounting hole reducing the risk of connector-to-PCB intermittence;
- Compliant with the Restriction of Hazardous Substances (RoHS) directive;
- STM32F746 MCU in TFBGA-216 package capable of running the system clock at up to 216 MHz;
- ARM SWJ-DP: a combined JTAG and serial wire debug port;
- Powered from single +3.3 V power supply;
- Low-power mode with short startup times;
- Deep-sleep power mode with ultra-low power consumption profiles;
- On-module clocks;
- 32/64 MBytes SDRAM;
- 16 MBytes NOR Flash;
- Serial console interface at UART CMOS levels;
- 802.3 Ethernet interface;
- USB 2.0 full-speed device/host/OTG controller with on-chip PHY;
- Watchdog Timer (WDT);
- Real-Time Clock (RTC);
- All otherwise uncommitted interfaces of the STM32F7 MCU available on the interface connectors.

2.2. Functional Block Diagram

The following figure is a functional block diagram of the STM32F7 SOM:

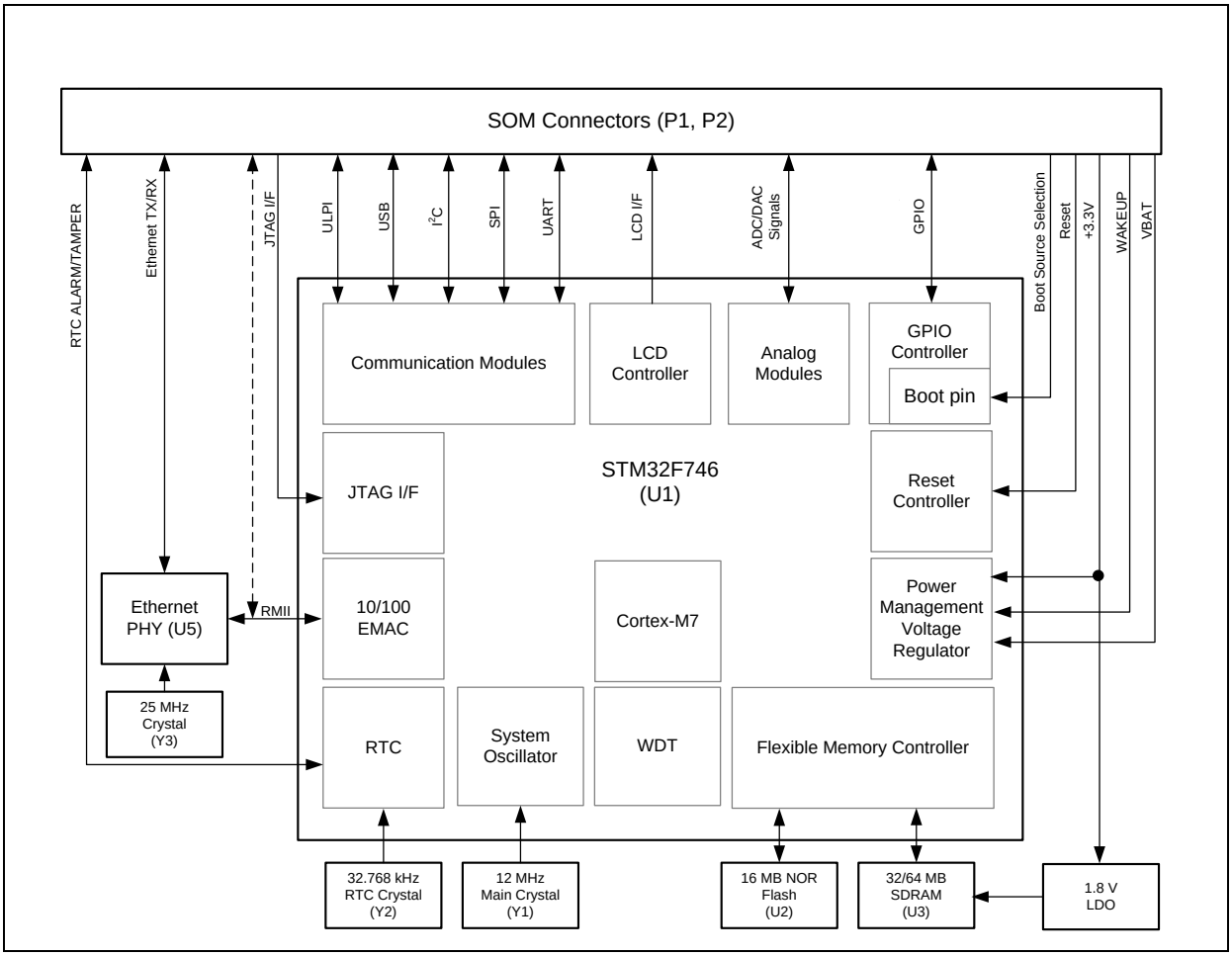

Figure 1: STM32F7 SOM Functional Block Diagram

2.3. Microcontroller

2.3.1. STM32F7 MCU

The architecture of the STM32F7 SOM is built around the STMicro STM32F746 MCU that combines a 32-bit ARM Cortex-M7 processor core with a wide range of the integrated peripheral controllers.

2.4. JTAG Interface

The STM32F7 SOM provides the ARM combined JTAG and serial wire debug interface (SWJ-DP) on the interface connectors. The SWJ-DP interface is routed to the corresponding signals of the STM32F7 device.

2.5. Power

2.5.1. Power Source

The STM32F7 SOM is powered from a single +3.3 V power source provided through multiple pins of the interface connectors. The SOM converts the +3.3V input power into other power sources required by the STM32F7 SOM design using an appropriate on-module circuitry.

2.5.2. Power Modes

The STM32F7 SOM supports the following power modes:

- Full-power mode. This is the normal mode of operation. The main clock is running and the Cortex-M7 is active running RTOS and/or application code. All memory controllers are enabled.

  The software is configured to enable only those STM32F7 sub-systems that are used by the installed device drivers; all other sub-systems are in reset and do not consume power. If the Ethernet interface is not enabled by a corresponding device driver, the Ethernet PHY is in a low power mode (refer to section 2.12.5). When the software doesn't use the external NOR Flash the NOR Flash device is automatically switched to a low power mode (refer to section 2.9.2).

- Low-power mode. The software may be configured to enter this mode of operation when the STM32F7 SOM is idle from the software perspective. The STM32F7 MCU supports three low-power modes: Sleep mode, Stop mode, and Standby mode. Standby mode is used to achieve the lowest power consumption, but all embedded SRAM data and value of all internal registers (except backup domain registers) are lost in this mode. Stop mode achieves the lowest power consumption while retaining the contents of the embedded SRAM and internal registers.

  For switching external off-module devices in a low-power mode, the STM32F7 SOM provides a dedicated output which is available on pin 16 of the P1 interface connectors.

  When the STM32F7 SOM is switched to the low-power mode, it activates the low-power mode signal. Off-module devices are expected to react on activation of this signal by switching themselves to low-power modes. Conversely, when the STM32F7 SOM is switched back to the full-power mode, it de-asserts the low-power mode signal, indicating to off-board devices that they are expected to return to the full-power mode.

2.6. System Reset

2.6.1. Reset Architecture Overview

The STM32F7 SOM implements a reset architecture that ensures that the STM32F7 MCU is reset as appropriate on various hardware and software events.

The STM32F7 SOM ensures that the on-module PHY and Flash devices are reset as soon as the STM32F7 SOM is reset, by connecting the MCU reset signal to reset inputs of these on-module devices.

Those off-module devices that require synchronization of their resets with the reset of the STM32F7 SOM should have their reset inputs connected to the active-low nRESET_OUT signal of the STM32F7 SOM, which is available on pin 15 of the P1 interface connector.

2.6.2. Types of System Resets

The following types of reset are implemented in the STM32F7 SOM:

- Power-on reset (POR). This type of reset occurs when the STM32F7 SOM is being powered-up. The POR threshold is in a range of 1.64V to 1.8.

- Power down reset (PDR). This type of reset occurs when the +3.3V power supply of the STM32F7 SOM falls below the PDR threshold which value is in the range of 1.6V to 1.76V. The hysteresis between the POR and PDR threshold values of a specific STM32F7 chip is 40mV.

- Brown-out reset (BOR). In case when the +3.3 V power supply falls below a user-selectable threshold value (3 regions in the range from 2.13V to 2.97V are available) the BOR system generates a reset of the STM32F7 MCU. After the brown-out reset has occurred, the BOR system holds the STM32F7 MCU in reset until the supply voltage will rise 100mV above the current brownout threshold value.

- Software reset. This type of reset is activated by the software running on the STM32F4 SOM using the STM32F7 software reset sequence.

- WDT reset. This type of reset is activated when the integrated WDT of the STM32F7 MCU expires.
- Manual reset. To activate this type of reset, a baseboard drives low the nRESET signal of the STM32F7 SOM which is available on pin 13 of the P1 interface connector.

2.7. System Clocks

The STM32F7 SOM provides a 12 MHz crystal resonator as a reference to the internal HSE oscillator of the STM32F7 MCU.

After the power-on reset the 16MHz internal HSI RC oscillator is selected as a default CPU clock. After that, the software reconfigures internal clocks of the STM32F7 MCU.

The STM32F7 MCU contains integrated PLLs driven by the internal HSE oscillator, from which various clocks required by subsystems of the STM32F7 MCU are derived.

In addition to the 12 MHz crystal resonator, the STM32F7 SOM provides a dedicated clock reference for the Ethernet sub-section (refer to section 2.12.3).

2.8. SDRAM

2.8.1. SDRAM Architecture

The STM32F7 SOM provides 32/64 MBytes of 216 MHz 32-bit SDRAM memory using the ESMT M12L2561616A-6BIG2K device or the ISSI Mobile SDRAM IS42SM16160K-6BLIxxx device for 32 Mbytes SDRAM and the ISSI IS42S16320F-7BLI device for 64 MBytes SDRAM. The SDRAM memory resides at chip select FMC_SDNE0 of the integrated Flexible Memory Controller (FMC) of the STM32F7 MCU.

2.8.2. SDRAM Operational Mode

The STM32F7 Flexible Memory controller operates the SDRAM with the SDRAM clock of 100 MHz (HCLK/2) and Burst length = 8.

2.8.3. SDRAM Self Refresh Mode

When in a Self Refresh Mode, the SDRAM current consumption is of the ESMT device is 3 mA, of the ISSI device is 0.7 mA.

2.9. NOR Flash

2.9.1. NOR Flash Architecture

The STM32F7 SOM provides 16 MBytes of the NOR Flash memory, using the Spansion S29GL128S10DHI010 device. The NOR Flash memory resides at chip select FMC_NE1 of FMC of the STM32F7 MCU.

2.9.2. NOR Flash Low-Power Mode

When not accessed, the NOR Flash current consumption is only 100 uA.

2.10. Boot Configuration

An STM32F7 boot configuration is set by a state of pins BOOT1 and BOOT0 after the STM32F7 MCU reset. The levels on the BOOT pins are latched on the 4th rising edge of SYSCLK after the reset. In the STM32F7 SOM the BOOT0 pin is connected to the ground, so the CPU boots from the integrated Flash memory regardless of the state of the BOOT1 pin.

2.11. Serial

2.11.1. UART Controller

The STM32F7 SOM provides an UART serial interface at CMOS levels (no RS-232 buffer) on the interface connectors using the integrated USART1 controller of the STM32F7 MCU.

This interface is intended as a serial console for the U-Boot and uLinux software.

2.11.2. Serial Baud Rate

The UART controller features an internal divider that allows this serial interface to operate at standard baud rates up to 5.25 Mbps.

2.12. Ethernet

2.12.1. Ethernet Controller

The STM32F7 SOM provides a full-featured, configurable Ethernet interface capable of 10/100 Mbps data rates using the integrated MAC 802.3 of the STM32F7 MCU.

2.12.2. Ethernet Physical Layer

The physical layer of the Ethernet port is implemented using the Micrel KSZ8081RNL PHY device to provide a full-featured 802.3-compliant 10/100 Mbps interface.

2.12.3. Ethernet Clock

The STM32F7 SOM provides a 25 MHz quartz crystal as a clock reference to the Ethernet PHY device.

The KSZ8081RNL PHY device drives the 50 MHz RMII reference clock input of the integrated Ethernet controller of the STM32F7 MCU.

2.12.4. Ethernet Status LEDs

The STM32F7 SOM provides two status signals for the Ethernet channel on the interface connectors for controlling off-module Ethernet LEDs. The functionality of these signals is as follows:

- LED_ACT: used to indicate the link availability status (Link when low, No Link when high) and the RX activity when toggling;
- LED_SPD: used to indicate the 10/100 Mbps link status (100 Mbps when low, 10 Mbps when high).

On a baseboard, the status LEDs should be connected between the STM32F7 SOM status signals and the +3.3V power supply.

2.12.5. Ethernet Low Power Mode

When not accessed, the PHY can be switched to the Power-Down mode under the software control. When in the Power-Down mode, the PHY current consumption is only 2 mA.

2.12.6. Ethernet Configuration

The STM32F7 SOM can be build-time configured to use the on-module Ethernet PHY or an external off-module RMII Ethernet PHY. By default, the on-module PHY is used. When using an external PHY resistors, the SOM is assembled as follows:

- R7-R12, R18, and R34 (33 Ohm, package 1005) not installed;
- R26-R31 (0 Ohm, package 1005), R33, R35, R32 (33 Ohm, package 1005) installed.

When configured for using an external RMII PHY, the MDIO/MDC signals are available on the P1 interface connector pins 22 and 36 and the RMII signals are available on the P2 interface

connector pins 2, 4, 8, 10, 14, 18, and 22 as shown in Table 1 and Table 2. The JTAG_nTRST signal is available on the P1 interface connector pin 50, when the STM32F7 SOM is configured for using an external RMII PHY.

2.13. WDT

The STM32F7 SOM provides a hardware watchdog function using two embedded WDT peripherals: Independent and Window. The independent watchdog (IWDG) is clocked by its own dedicated low-speed clock (LSI) and therefore stays active even if the main clock fails. The window watchdog (WWDG) clock is prescaled from the APB1 clock and has a configurable time-window that can be programmed to detect abnormally late or early application behavior.

If the WDT is enabled and the software fails to strobe the WDT within the predefined period of time, the watchdog triggers reset.

The WDT timeout period is defined by the software.

2.14. RTC

The STM32F7 SOM supports a Real-Time Clock (RTC) functionality using the Real-Time Counter System of the STM32F7 MCU.

The RTC clock source is the low-power 32.768 KHz oscillator of the STM32F7 MCU.

The battery switching circuitry continuously compares the battery voltage (the VBATT signal on the interface connector) with the voltage of the main digital power supply (the VDD pin of the STM32F7 MCU) and automatically powers the RTC and the 32.768 KHz oscillator from the battery whenever the battery voltage is approximately 0.6 V or more, above the voltage on the VDD pin. This allows both the RTC and the 32.768 KHz oscillator to function when the +3.3V power supply is removed.

2.15. External Interface

2.15.1. Interface Connectors

The external interfaces of the STM32F7 SOM are routed through two 80-pin Hirose DF40 series 0.4 mm-pitch board-to-board connectors.

2.15.2. Connectors Pin-Out

The following table details the allocation of the external interface connectors pins on the P1 connector:

Pin	Name	Type	Description	STM32F7 pins	Notes
Power (15 pins)					
2, 3, 5, 8, 9, 11, 14, 57, 75, 76	GND	Power	STM32F7 SOM ground	VSS pins: F2, H6, K7, K8, K10, G10, F6-F10, G6, J6, K6, L6, K9, J10, H10; BYPASS_REG pin: L5; VSSA pin: M1; VREF- pin: N1	Must be connected to GND on a baseboard.

Pin	Name	Type	Description	STM32F7 pins	Notes
77, 79	VCC3	Power	STM32F7 SOM +3.3V power supply	VDD pins: E7-10; F4, F5, F11, G5, H5, H11, J5, J11, K5, L7-L10, K11; VDDUSB pin: G11	An external +3.3 V+/- 5% power supply must be applied to these pins.
74	VBAT	Power	STM32F7 VBAT	C1	An external backup power supply of +1.65 V to +3.6 V can be applied to this pin.
13	nRESET_IN	Input	STM32F7 SOM reset input (NRST)	J1	Active-low hardware reset to the SOM. Connected to P1 pin 15 (nRESET_OUT) on the STM32F7 SOM. Driven low during internal STM resets.
15	nRESET_OUT	Output	STM32F7 SOM reset output (NRST)	J1	Active-low reset from the SOM to external devices. Connected to P1 pin 13 (nRESET_IN) on the STM32F7 SOM.
JTAG (6 pins)					
20	JTAG_TCK	Input	STM32F7 JTCK-SWCLK	A14	
24	JTAG_TMS	Input	STM32F7 JTMS-SWDIO	A15	
36	JTAG_nTRST/ MDIO	Input/Output	STM32F7 NJTRST	A9 (through resistor R34)	Default option (R34 installed, R33 not installed).
			STM32F7 PA2/USART2_TX/ TIM5_CH3/ TIM9_CH1/ TIM2_CH3/ ETH_MDIO	P2 (through resistor R33)	Build-time option used for the Ethernet PHY Management Interface (R33 installed, R34 not installed)
38	JTAG_TDO	Output	STM32F7 JTDO/TRACESWO	A10 (through resistor R13)	
47	JTAG_TDI	Input	STM32F7 JTDI	A13	

Pin	Name	Type	Description	STM32F7 pins	Notes
50	E_JTAG_nTRST	Not connected	Not connected on STM32F7 SOM	Not connected to STM32F7 (resistor R35 is not installed)	Default option
		Input	STM32F7 NJTRST	A9 (through resistor R35)	Build-time option
Ethernet (6 pins)					
1	LED_ACT	Output	SOM Ethernet PHY Link/Activity status	Not connected to STM32F7	Low – Link, High – No Link, Toggling – RX activity.
4	TD_P	Output	SOM Ethernet PHY differential positive transmit signal	Not connected to STM32F7	TD_P and TD_N signals should be routed on a baseboard with a 100 Ohm differential impedance.
6	TD_N	Output	SOM Ethernet PHY differential negative transmit signal	Not connected to STM32F7	
7	LED_SPD	Output	SOM Ethernet PHY 10/100Mbps link status	Not connected to STM32F7	Low – 100 Mbps, High – 10 Mbps.
10	RD_P	Input	SOM Ethernet PHY differential positive receive signal	Not connected to STM32F7	RD_P and RD_N signals should be routed on a baseboard with a 100 Ohm differential impedance.
12	RD_N	Input	SOM Ethernet PHY differential negative receive signal	Not connected to STM32F7	
Ethernet PHY Management Interface (2 pins)					
22	RMII_MDC	Input/Output	STM32F7 PC1/**ETH_MDC**	M3	
36	JTAG_nTRST/ MDIO	Input/Output	STM32F7 NJTRST	A9 (through resistor R34)	Default option used for the JTAG interface (R34 installed, R33 not installed)
			STM32F7 PA2/USART2_TX/ TIM5_CH3/ TIM9_CH1/ TIM2_CH3/ **ETH_MDIO**	P2 (through resistor R33)	Build-time option (R33 installed, R34 not installed)
Multifunction pins (40 pins)					
16	PF10	Input/Output	STM32F7 PF10/FMC_INTR/ DCMI_D11/ LCD_DE/ ADC3_IN8	L1	

Pin	Name	Type	Description	STM32F7 pins	Notes
17	BOOT0	Input/Output	STM32F7 BOOT0/VPP	E6	
19	PH13	Input/Output	STM32F7 PH13/TIM8_CH1N/ CAN1_TX/FMC_D21/ LCD_G2	E12	
21	PI9	Input/Output	STM32F7 PI9/CAN1_RX/ FMC_D30/ LCD_VSYNC	E4	
23	PB2	Input/Output	STM32F7 PB2/SAI1_SD_A/ SPI3_MOSI/ I2S3_SD/ UQADSPI_CLK/ EVENTOUT	M5	
25	PH11/ I2C4_SCL	Input/Output	STM32F7 PH11/TIM5_CH2/ I2C4_SCL/ DCMI_D2/FMC_D19/ LCD_R5	N15	
26	PH12/ I2C4_SDA	Input/Output	STM32F7 PH12/TIM5_CH3/ I2C4_SDA/ DCMI_D3/FMC_D20/ LCD_R6	M15	
27	I2C_0_SDA	Input/Output	STM32F7 PB7/TIM4_CH2/ I2C1_SDA/ USART1_RX/ FMC_NL	B5	
28	UART_1_TXD	Input/Output	STM32F7 PC6/I2S2_MCK/ TIM8_CH1/ SDIO_D6/ USART6_TX/ DCMI_D0/ TIM3_CH1/ LCD_HSYNC	H15	
29	UART_0_TXD	Input/Output	STM32F7 PB6/I2C1_SCL/ TIM4_CH1/ CAN2_TX/ DCMI_D5/ USART1_TX/ FMC_SDNE1	B6	Used for the software console interface.
30	UART_0_RXD	Input/Output	STM32F7 PA10/USART1_RX/ TIM1_CH3/ OTG_FS_ID/ DCMI_D1	D15	Used for the software console interface.
31	UART_1_RXD	Input/Output	STM32F7 PC7/I2S3_MCK/ TIM8_CH2/ SDIO_D7/ USART6_RX/ DCMI_D1/ TIM3_CH2/LCD_G6	G15	

Pin	Name	Type	Description	STM32F7 pins	Notes
33	I2C_0_SCL	Input/Output	STM32F7 PB8/TIM4_CH3/ SDIO_D4/ TIM10_CH1/ DCMI_D6/ ETH_MII_TXD3/ I2C1_SCL/ CAN1_RX/LCD_B6	A7	
37	PG12	Input/Output	STM32F7 PG12/FMC_NE4/ USART6_RTS/ SPI6_MISO/ LCD_B1/LCD_B4	C7	
40	PA4/ ADC12_IN4/ DAC1_OUT	Input/Output	STM32F7 PA4/SPI1_NSS/ SPI3_NSS/ USART2_CK/ DCMI_HSYNC/ OTG_HS_SOF/ I2S3_WS/ LCD_VSYNC/ ADC12_IN4/ DAC1_OUT	N4	
41	PI6/ SAI2_SD_A	Input/Output	STM32F7 PI6/TIM8_CH2/ SAI2_SD_A/ DCMI_D6/FMC_D28/ LCD_B6	D6	
42	PA8/MCO1	Input/Output	STM32F7 PA8/MCO1/ USART1_CK/ TIM1_CH1/ I2C3_SCL/ OTG_FS_SOF/ LCD_R6	F15	
44	PD3	Input/Output	STM32F7 PD3/SPI2_SCK/ I2S2_CK/ USART2_CTS/ FMC_CLK/LCD_G7	C11	
46	PH8	Input/Output	STM32F7 PH8/I2C3_SDA/ DCMI_HSYNC/ FMC_D16/LCD_R2	P14	
48	PH9	Input/Output	STM32F7 PH9/I2C3_SMBA/ TIM12_CH2/ DCMI_D0/ FMC_D17/LCD_R3	N14	
49	PD6	Input/Output	STM32F7 PD6/SPI3_MOSI/ I2S3_SD/ SAI1_SD_A/ USART2_RX/ FMC_NWAIT/ LCD_B2	B11	

Pin	Name	Type	Description	STM32F7 pins	Notes
51	PF8/ADC3_IN6	Input/Output	STM32F7 PF8/TIM13_CH1/ FMC_NIOWR/ SPI5_MISO/ SAI1_SCK_B/ ADC3_IN6	L3	
52	PH14	Input/Output	STM32F7 PH14/TIM8_CH2N/ DCMI_D4/FMC_D22/ LCD_G3	E13	
53	PI2	Input/Output	STM32F7 PI2/TIM8_CH4/ SPI2_MISO/ DCMI_D9/ I2S2ext_SD/ FMC_D26/LCD_G7	C14	
54	PH6	Input/Output	STM32F7 PH6/I2C2_SMBA/ TIM12_CH1/ ETH_MII_RXD2/ SPI5_SCK/ DCMI_D8/ FMC_SDNE1	P13	
56	RTC_AF2	Input/Output	STM32F7 EVENTOUT/ RTC_TAMP2/ RTS_TS/WKUP3	C2	
58	PH15	Input/Output	STM32F7 PH15/TIM8_CH3N/ DCMI_D11/ FMC_D23/LCD_G4	D13	
59	PF9/ SPI5_MOSI	Input/Output	STM32F7 PF9/TIM14_CH1/ FMC_CD/ SPI5_MOSI/ SAI1_FS_B/ QUADSPI_BK1_IO1/ ADC3_IN7	L2 (through resistor R38)	
60	PA0-WKUP	Input/Output	STM32F7 PA0-WKUP/ TIM2_CH1/ TIM2_ETR/ TIM5_CH1/ TIM8_ETR/ USART2_CTS/ UART4_TX/ SAI2_SD_B/ ADC123_IN0/WKUP	N3	WKUP function is used to wake up the STM32F7 MCU from the Standby, Stop and Sleep modes
61	PH7/ SPI5_MISO	Input/Output	STM32F7 PH7/I2C3_SCL/ ETH_MII_RXD3/ SPI5_MISO/ DCMI_D9/ FMC_SDCKE1	N13	

Pin	Name	Type	Description	STM32F7 pins	Notes
63	SPI0_DO	Output	STM32F7 PB15/SPI2_MOSI/ I2S2_SD/ TIM1_CH3N/ TIM8_CH3N/ TIM12_CH2/ RTC_50HZ/ OTG_HS_DP	R15 (through resistor R19)	
64	RTC_AF1	Input/Output	STM32F7 EVENTOUT/ RTC_TAMP1/ RTS_TS/RTS_OUT/ WKUP2	D1	
65	SPI0_DI	Input/Output	STM32F7 PB14/SPI2_MISO/ TIM1_CH2N/ TIM12_CH1/ USART3_RTS/ TIM8_CH2N/ I2S2ext_SD/ OTG_HS_DM	R14	
66	PI0	Input/Output	STM32F7 PI0/TIM5_CH4/ SPI2_NSS/ I2S2_WS/ DCMI_D13/ FMC_D24/LCD_G5	E14	
67	PF7/SPI5_MCK	Input/Output	STM32F7 PF7/TIM11_CH1/ FMC_NREG/ SPI5_SCK/ UART7_Tx/ SAI1_MCLK_B/ ADC3_IN5	K1 (through resistor R39)	
68	PI3	Input/Output	STM32F7 PI3/TIM8_ETR/ SPI2_MOSI/ I2S2_SD/ DCMI_D10/ FMC_D27	C13	
69	PF6/SPI5_NSS	Input/Output	STM32F7 PF6/TIM10_CH1/ FMC_NIORD/ SPI5_NSS/ UART7_Rx/ SAI1_SD_B/ ADC3_IN4	K2 (through resistor R40)	
70	PA6/ ADC12_IN6	Input/Output	STM32F7 PA6/SPI1_MISO/ TIM8_BKIN/ TIM13_CH1/ DCMI_PIXCLK/ TIM3_CH1/ TIM1_BKIN/ LCD_G2/ ADC12_IN6	P3	

Pin	Name	Type	Description	STM32F7 pins	Notes
71	SPI0_CLK	Input/Output	STM32F7 PI1/SPI2_SCK/ I2S2_CK/ DCMI_D8/ FMC_D25/LCD_G6	D14 (through resistor R20)	
73	SPI0_nSS	Input/Output	STM32F7 PB9/SPI2_NSS/ I2S2_WS/ TIM4_CH4/ TIM11_CH1/ SDIO_D5/ DCMI_D7/ I2C1_SDA/ CAN1_TX/LCD_B7	B4 (through resistor R21)	
Unconnected pins of STM32F7 SOM (13 pins)					
18, 32, 34, 35, 39, 43, 45, 55, 62, 72, 78, 80	-	Not connected	Not connected on STM32F7 SOM	Not connected to STM32F7	-
50	E_JTAG_nTRST	Not connected	Not connected on STM32F7 SOM	Not connected to STM32F7 (resistor R35 is not installed)	Default option
		Input	STM32F7 JTAG controller reset (NJTRST)	A9 (through resistor R35)	Build-time option

Table 1: STM32F7 SOM P1 Connector

The following table details the allocation of the external interface connectors pins on the P2 connector:

Pin	Name	Type	Description	STM32F7 pins	Notes
Power (8 pins)					
1, 6, 7, 12, 20, 24, 28, 52	GND	Power	STM32F7 SOM ground	VSS pins: F2, H6, K7, K8, K10, G10, F6-F10, G6, J6, K6, L6, K9, J10, H10; BYPASS_REG pin: L5; VSSA pin: M1; VREF- pin: N1	Must be connected to GND on a baseboard.
RMII pins/Multifunction pins (7 pins)					
2	E_RMII_TXD1	Not connected	Not connected on STM32F7 SOM	Not connected to STM32F7 (resistor R26 is not installed)	Default option

Pin	Name	Type	Description	STM32F7 pins	Notes
		Input/Output	STM32F7 PG14/FMC_A25/ USART6_TX/ ETH_MII_TXD1/ ETH_RMII_TXD1/ SPI6_MOSI	A4 (through resistors R26 and R8)	Build-time option
4	E_RMII_TXD0	Not connected	Not connected on STM32F7 SOM	Not connected to STM32F7 (resistor R27 is not installed)	Default option
		Input/Output	STM32F7 PG13/FMC_A24/ USART6_CTS/ ETH_MII_TXD0/ ETH_RMII_TXD0/ SPI6_SCK	B3 (through resistors R27 and R9)	Build-time option
8	E_RMII_RXD1	Not connected	Not connected on STM32F7 SOM	Not connected to STM32F7 (resistor R29 is not installed)	Default option
		Input/Output	STM32F7 PC5/ ETH_RMII_RX_D1/ ETH_MII_RX_D1/ ADC12_IN15	P5 (through resistors R29 and R10)	Build-time option
10	E_RMII_RXD0	Not connected	Not connected on STM32F7 SOM	Not connected to STM32F7 (resistor R30 is not installed)	Default option
		Input/Output	STM32F7 PC4/ ETH_RMII_RX_D0/ ETH_MII_RX_D0/ ADC12_IN14	N5 (through resistors R30 and R11)	Build-time option
14	E_RMII_TXEN	Not connected	Not connected on STM32F7 SOM	Not connected to STM32F7 (resistor R28 is not installed)	Default option
		Input/Output	STM32F7 PG11/ FMC_NCE4_2/ ETH_MII_TX_EN/ ETH_RMII_TX_EN/ DCMI_D3/LCD_B3	B8 (through resistors R28 and R7)	Build-time option
18	E_RMII_CRSDV	Not connected	Not connected on STM32F7 SOM	Not connected to STM32F7 (resistor R31 is not installed)	Default option
		Input/Output	STM32F7 PA7/SPI1_MOSI/ TIM8_CH1N/ TIM14_CH1/ TIM3_CH2/ ETH_MII_RX_DV/ TIM1_CH1N/ ETH_RMII_CRS_DV/ ADC12_IN7	R3 (through resistors R31 and R12)	Build-time option

Pin	Name	Type	Description	STM32F7 pins	Notes
22	E_RMII_CLK	Not connected	Not connected on STM32F7 SOM	Not connected to STM32F7 (resistor R32 is not installed)	Default option
		Input/Output	STM32F7 PA1/USART2_RTS/ UART4_RX/ ETH_RMII_REF_CLK/ ETH_MII_RX_CLK/ TIM5_CH2/ TIM2_CH2/ ADC123_IN1	N2 (through resistor R32)	Build-time option
ULPI USB pins/Multifunction pins (12 pins)					
26	ULPI_CLK/PA5	Input/Output	STM32F7 PA5/SPI1_SCK/ **OTG_HS_ULPI_CK/** TIM2_CH1_ETR/ TIM8_CH1N	P4	
30	ULPI_DATA7/PB5	Input/Output	STM32F7 PB5/I2C1_SMBA/ CAN2_RX/ OTG_HS_ULPI_D7/ ETH_PPS_OUT/ TIM3_CH2/ SPI1_MOSI/ SPI3_MOSI/ DCMI_D10/ I2S3_SD/ FMC_SDCKE1	A8	
32	ULPI_DATA6/PB13	Input/Output	STM32F7 PB13/SPI2_SCK/ I2S2_CK/ USART3_CTS/ TIM1_CH1N/ CAN2_TX/ OTG_HS_ULPI_D6/ ETH_RMII_TXD1/ ETH_MII_TXD1/ OTG_HS_VBUS	K14	
34	ULPI_DATA5/PB12	Input/Output	STM32F7 PB12/SPI2_NSS/ I2S2_WS/ I2C2_SMBA/ USART3_CK/ TIM1_BKIN/ CAN2_RX/ OTG_HS_ULPI_D5/ ETH_RMII_TXD0/ ETH_MII_TXD0/ OTG_HS_ID	L13	
36	ULPI_DATA4/PB11	Input/Output	STM32F7 PB11/I2C2_SDA/ USART3_RX/ OTG_HS_ULPI_D4/ ETH_RMII_TX_EN/ ETH_MII_TX_EN/ TIM2_CH4/LCD_G5	R13	

Pin	Name	Type	Description	STM32F7 pins	Notes
38	ULPI_DATA3/PB10	Input/Output	STM32F7 PB10/SPI2_SCK/ I2S2_CK/ I2C2_SCL/ USART3_TX/ OTG_HS_ULPI_D3/ ETH_MII_RX_ER/ TIM2_CH3/LCD_G4	P12	
40	ULPI_DATA2/PB1	Input/Output	STM32F7 PB1/TIM3_CH4/ TIM8_CH3N/ OTG_HS_ULPI_D2/ ETH_MII_RXD3/ TIM1_CH3N/ LCD_R6/ADC12_IN9	R4	
42	ULPI_DATA1/PB0	Input/Output	STM32F7 PB0/TIM3_CH3/ TIM8_CH2N/ OTG_HS_ULPI_D1/ ETH_MII_RXD2/ TIM1_CH2N/ LCD_R3/ADC12_IN8	R5	
44	ULPI_DATA0/PA3	Input/Output	STM32F7 PA3/USART2_RX/ TIM5_CH4/ TIM9_CH2/ TIM2_CH4/ OTG_HS_ULPI_D0/ ETH_MII_COL/ LCD_B5	R2	
46	ULPI_DIR/PI11	Input/Output	STM32F7 PI11/ OTG_HS_ULPI_DIR	F3	
48	ULPI_NXT/PH4	Input/Output	STM32F7 PH4/I2C2_SCL/ OTG_HS_ULPI_NXT	H4	
50	ULPI_STP/PC0	Input/Output	STM32F7 PC0/ OTG_HS_ULPI_STP/ FMC_SDNWE/ ADC123_IN10	M2	
USB FS pins / Multifunction pins (3 pins)					
3	USB0D_P	Input/Output	STM32F7 PA12/USART1_RTS/ CAN1_TX/ TIM1_ETR/LCD_R5/ OTG_FS_DP	B15	
5	USB0D_N	Input/Output	STM32F7 PA11/USART1_CTS/ CAN1_RX/ TIM1_CH4/LCD_R4/ OTG_FS_DM	C15	
9	USB_PWR	Input/Output	STM32F7 PA9/USART1_TX/ TIM1_CH2/ I2C3_SMBA/ DCMI_D0/ OTG_FS_VBUS	E15	

Pin	Name	Type	Description	STM32F7 pins	Notes
LCD-TFT RGB Interface pins (STM32F746NGH6 only) / Multifunction pins (28 pins)					
15	LCD_CLK/PI14	Input/Output	STM32F7 PI14/LCD_CLK/ EVENTOUT	H3 (through resistor R25)	
17	LCD_DE/PK7	Input/Output	STM32F7 PK7/LCD_DE/ EVENTOUT	C4	
19	LCD_HSYNC/PI12	Input/Output	STM32F7 PI12/ LCD_HSYNC/ EVENTOUT	E3	
21	LCD_VSYNC/PI13	Input/Output	STM32F7 PI13/LCD_VSYNC/ EVENTOUT	G3	
23	LCD_B0/PJ12	Input/Output	STM32F7 PJ12/LCD_B0/ EVENTOUT	B10	
25	LCD_B1/PJ13	Input/Output	STM32F7 PJ13/LCD_B1/ EVENTOUT	B9	
27	LCD_B2/PJ14	Input/Output	STM32F7 PJ14/LCD_B2/ EVENTOUT	C9	
29	LCD_B3/PJ15	Input/Output	STM32F7 PJ15/LCD_B3/ EVENTOUT	D10	
31	LCD_B4/PK3	Input/Output	STM32F7 PK3/LCD_B4/ EVENTOUT	D8	
33	LCD_B5/PK4	Input/Output	STM32F7 PK4/LCD_B5/ EVENTOUT	D7	
35	LCD_B6/PK5	Input/Output	STM32F7 PK5/LCD_B6/ EVENTOUT	C6	
37	LCD_B7/PK6	Input/Output	STM32F7 PK6/LCD_B7/ EVENTOUT	C5	
39	LCD_G0/PJ7	Input/Output	STM32F7 PJ7/LCD_G0/ EVENTOUT	J12	
41	LCD_R1/PJ0	Input/Output	STM32F7 PJ0/LCD_R1/ EVENTOUT	R6	
43	LCD_R2/PJ1	Input/Output	STM32F7 PJ1/LCD_R2/ EVENTOUT	R7	
45	LCD_R3/PJ2	Input/Output	STM32F7 PJ2/LCD_R3/ EVENTOUT	P7	
47	LCD_R4/PJ3	Input/Output	STM32F7 PJ3/LCD_R4/ EVENTOUT	N8	

Pin	Name	Type	Description	STM32F7 pins	Notes
49	LCD_R5/PJ4	Input/Output	STM32F7 PJ4/LCD_R5/ EVENTOUT	M9	
51	LCD_R6/PJ5	Input/Output	STM32F7 PJ5/LCD_R6/ EVENTOUT	M14	
53	LCD_R7/PJ6	Input/Output	STM32F7 PJ6/LCD_R7/ EVENTOUT	K12	
55	LCD_G1/PJ8	Input/Output	STM32F7 PJ8/LCD_G1/ EVENTOUT	H12	
57	LCD_G2/PJ9	Input/Output	STM32F7 PJ9/LCD_G2/ EVENTOUT	J13	
59	LCD_G3/PJ10	Input/Output	STM32F7 PJ10/LCD_G3/ EVENTOUT	H13	
61	LCD_G4/PJ11	Input/Output	STM32F7 PJ11/LCD_G4/ EVENTOUT	G12	
63	LCD_G5/PK0	Input/Output	STM32F7 PK0/LCD_G5/ EVENTOUT	G13	
65	LCD_G6/PK1	Input/Output	STM32F7 PK1/LCD_G6/ EVENTOUT	F12	
67	LCD_G7/PK2	Input/Output	STM32F7 PK2/LCD_G7/ EVENTOUT	F13	
69	LCD_R0/PI15	Input/Output	STM32F7 PI15/LCD_R0/EVEN TOUT	G4	
SD Card Interface/Multifunction pins (6 pins)					
62	PC11/SDIO_D3	Input/Output	STM32F7 PC11/I2S3ext_SD/ SPI3_MISO/ UART4_RX/ USART3_RX/ SDIO_D3	B13	
64	PC10/SDIO_D2	Input/Output	STM32F7 PC10/SPI3_SCK/ I2S3_CK/ UART4_TX/ USART3_TX/ SDIO_D2/LCD_R2	B14	
66	PC9/SDIO_D1	Input/Output	STM32F7 PC9/I2S_CKIN/ MCO2/TIM8_CH4/ SDIO_D1/ I2C3_SDA/DCMI_D3	F14	

Pin	Name	Type	Description	STM32F7 pins	Notes
68	PC8/SDIO_D0	Input/Output	STM32F7 PC8/TIM8_CH3/ SDIO_D0/ TIM3_CH3/ USART6_CK/ DCMI_D2	G14	
72	PC12/SDIO_CK	Input/Output	STM32F7 PC12/UART5_TX/ SDIO_CK/ DCMI_D9/ SPI3_MOSI/ I2S3_SD/ USART3_CK	A12 (through resistor R22)	
74	PD2/SDIO_CMD	Input/Output	STM32F7 PD2/TIM3_ETR/ UART5_RX/ SDIO_CMD/ DCMI_D11	D12	
GPIOs/Multifunction pins (11 pins)					
11	PH10/TIM5_CH1	Input/Output	STM32F7 PH10/TIM5_CH1/ DCMI_D1/FMC_D18/ LCD_R4	P15	
13	PG7	Input/Output	STM32F7 PG7/FMC_INT3/ USART6_CK/ DCMI_D13/LCD_CLK	J14	
54	PI10	Input/Output	STM32F7 PI10/ ETH_MII_RX_ER/ FMC_D31/ LCD_HSYNC	D5	
70	PE2	Input/Output	STM32F7 PE2/SPI4_SCK/ SAI1_MCLK_A/ QUADSPI_BK1_IO2/ ETH_MII_TXD3/ FMC_A23	A3	
71	PH3/SAI2_MCK_B	Input/Output	STM32F7 PH3/ QUADSPI_BK2_IO1/ SAI2_MCK_B/ ETH_MII_COL/ FMC_SDNE0/ LCD_R1	J4	
75	PI7/SAI2_FS_A	Input/Output	STM32F7 PI7/TIM8_CH3/ SAI2_FS_A/ DCMI_D7/ FMC_D29/LCD_B7	D4	
76	PI4/SAI2_MCK_A	Input/Output	STM32F7 PI4/TIM8_BKIN/ SAI2_MCK_A/ DCMI_D5/ FMC_NBL2/LCD_B4	C3	

Pin	Name	Type	Description	STM32F7 pins	Notes
77	PI5/SAI2_SCK_A	Input/Output	STM32F7 PI5/TIM8_CH1/ SAI2_SCK_A/ DCMI_VSYNC/ FMC_NBL3/LCD_B5	D3	
78	PG10/SAI2_SD_B	Input/Output	STM32F7 PG10/FMC_NCE4_1/ FMC_NE3/ SAI2_SD_B/ DCMI_D2/LCD_B2/ LCD_G3	C8	
79	PH2/SAI2_SCK_B	Input/Output	STM32F7 PH2/ QUADSPI_BK2_IO0/ SAI2_SCK_B/ ETH_MII_CRS/ FMC_SDCKE0/ LCD_R0	K4	
80	PG9/SAI2_FS_B	Input/Output	STM32F7 PG9/USART6_RX/ QUADSPI_BK2_IO2/ SAI2_FS_B/ FMC_NE2/ FMC_NCE/ DCMI_VSYNC	D9	
Unconnected pins STM32F7 SOM (5 pins)					
16, 56, 58, 60, 73	-	Not connected on STM32F7 SOM	Not connected on STM32F7 SOM	Not connected to STM32F7	-

Table 2: STM32F7 SOM P2 Connector

2.15.3. Unavailable Signals of STM32F7

In the STM32F7 SOM all signals of the STM32F7 MCU are either used in the memory interfaces or connected to the interface connectors. The memory interface signals are not available on the interface connectors.

3. Mechanical Specifications

3.1. STM32F7 SOM Mechanicals

The STM32F7 SOM is implemented as a miniature 30 mm x 46 mm x 4.8 mm module.

The STM32F7 SOM PCB thickness is 1.6 mm +/- 0.16 mm. The maximum height of the SOM components is 1.8 mm.

The STM32F7 SOM includes a mounting hole so that the module can be mechanically secured to a baseboard, reducing the risk of connector-to-PCB intermittence that might occur during NEBS vibration and earthquake testing (or during the real events those tests simulate).

The following figure shows locations of the mounting hole and the SOM connectors on the module:

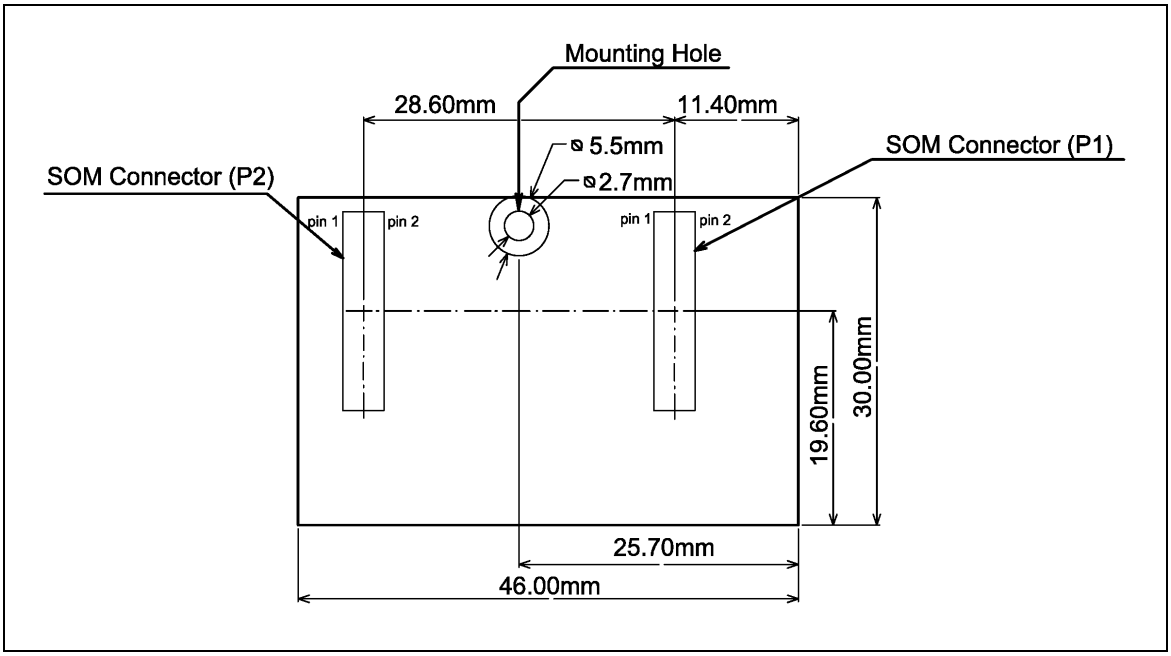

Figure 2: STM32F7 SOM Bottom View

3.2. STM32F7 SOM Connector Mechanicals

On a baseboard, the STM32F7 SOM is installed into two 80-pin Hirose DF40 series 0.4 mm-pitch board-to-board connectors. The exact part number of the connectors is Hirose DF40C-80DP-0.4V(51).

The recommended part number of mating connectors for a baseboard is Hirose DF40HC(4.0)-80DS-0.4V, which provides 4 mm stacking height for the STM32F7 SOM. The maximum height of the SOM above a baseboard for 4 mm stacking height is 7.6 mm.

Other possible options of mating connectors for the baseboard are:

- DF0C(2.0)-80DS-0.4V provides 5.7 mm of a maximum height of the SOM above the baseboard. This option does not allow placing components and conductive traces on the baseboard under the SOM.
- DF0HC(3.0)-80DS-0.4V provides 6.6 mm of a maximum height of the SOM above the baseboard. This option does not allow placing components on the baseboard under the SOM.
- DF40HC(3.5)-80DS-0.4V provides 7.1 mm of a maximum height of the SOM above the baseboard.

4. Environment Specifications

4.1. Recommended Operating Conditions

The following table lists the recommended operating conditions of the STM32F7 SOM:

Symbol	Parameter	Range
Ta	Ambient temperature	-40 to +85 ºC (Industrial)
VCC3	+3.3 V power supply	+3.3 V +/-5%

Table 5: Recommended Operating Conditions

5. Ordering Specifications

The following table provides the ordering information for the STM32F7 SOM:

Ordering Part Number	Specification
SOM-STM32F7	STmicro STM32F746, 216MHz, Industrial (-40 to +85C), 32MB SDRAM, 16MB NOR Flash, ETH PHY
SOM-STM32F7-R64	STmicro STM32F746, 216MHz, Industrial (-40 to +85C), 64MB SDRAM, 16MB NOR Flash, ETH PHY
SOM-STM32F7-xETH	STmicro STM32F746, 216MHz, Industrial (-40 to +85ºC), 32MB SDRAM
SOM-STM32F7-R64-xETH	STmicro STM32F746, 216MHz, Industrial (-40 to +85ºC), 64MB SDRAM

Table 3: Ordering Specifications

6. Document Revision History

Revision	Date	Changes Summary
1.7	December 6, 2017	Corrected mistakes in Table 2 "STM32F7 SOM P2 Connector" for pin 15 and pin 25.
1.6	July 6, 2017	Added information on the 64 MB SDRAM variant.
1.5	August 26, 2016	Added references to the ISSI Mobile SDRAM IS42SM16160K-6BLIxxx device.
1.4	June 3, 2016	The MCU frequency is changed to "216 MHz" in Section 2.1 "Hardware Platform Overview".
1.3	April 6, 2016	Replaced Micrel KSZ8051 with Micrel KSZ8081.
1.2	January 28, 2016	Corrected a typo in Section 2.9.1 "NOR Flash Architecture".
1.1	July 13, 2015	Corrected a mistake in Table 2 "STM32F7 SOM P2 Connector" for pin 13 (PG7).
1.0	February 20, 2015	Initial revision.