E4 - HPC

2) • SIMD lanes

cache line  512bit (64 byte)

registes  depending on extension (128 bit, 256 bit)

SIMD depending on data type

SIMD is a concept of data parallelism
the processor can operate on the registes
depending on the register size and the
data type (float, double) this corresponds to
operations on multiple data !

1) Amdahls law

f_1: seial fraction

f_p: improvable fraction

improved system: $t_p = f_1 \cdot t_1 + \frac{f_p \cdot t_1}{p} - \left(f_1 + \frac{f_p}{p}\right) t_1$

speed-up $S_p = \frac{1}{f_1 + f_p/p}$

a) bus: 55 km → 90 min

(i) train: 36 km → $36/70 \approx 0.5\,h = 30\,min$

55 km → $55/70 \approx 42.86\,min$

$p = \frac{90\,min}{42.86\,min} = 2.099$

$\underline{\underline{S_p = \frac{1}{\frac{19}{55} + \frac{36}{55}/2.099}}} = \underline{\underline{1.52}}$

(ii) train: dist → ~0s

$p \to \infty$