

## E4 - HPC

### 2) SIMD lanes

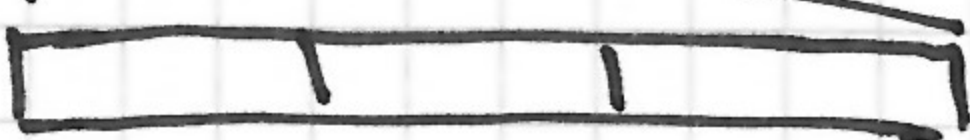
cache line



registers



SIMD



512 bit (64 byte)

depending on extension  
(128 bit, 256 bit)

depending on data type

SIMD is a concept of data parallelism  
the processor can operate on the register  
depending on the register size and the  
data type (float, double) this corresponds to  
operations on multiple data!

### 1) Amdahl's law

$f_s$ : serial fraction

$f_p$ : improvable fraction

improved system:  $t_p = f_s \cdot t_s + \frac{f_p \cdot t_s}{p} = (f_s + \frac{f_p}{p}) \cdot t_s$

speed-up  $S_p = \frac{1}{f_s + f_p/p}$

a) bus: 55 km  $\rightarrow$  90 min

(i) train: 36 km  $\rightarrow$   $36/70 \approx 0.514 \text{ h} = 30.8 \text{ min}$   
55 km  $\rightarrow$   $55/70 \approx 0.786 \text{ h} = 47.1 \text{ min}$

$$p = \frac{90 \text{ min}}{47.1 \text{ min}} = 1.91$$

$$\underline{S_p} = \frac{1}{\frac{19}{55} + \frac{36}{55/1.91}} = \underline{\underline{1.52}}$$

(ii) train: dist  $\rightarrow$   $\sim 0.5$

$p \rightarrow \infty$