

## Main Block:

3 BCDs with tick rate equals to 1 millisecond. The top one is timer; mid one is stopper and the bot one is watch.

Each BCD (except stopper) has load option, which being performed via button2(right) and has several conditions that are has to be met. Verification of the conditions performed via AND3 gate with input:

- XOR with **timer\_load** and **watch\_load** inputs.
- **timer\_load/watch\_load** is '1', respectively.
- **Step** is pressed.

Each BCD has an output of 32-bit, which is the current result of every counter in BCD. Then there is a block called **time\_selector**, which controls the current display group of numbers. There are 2 options controlled with switch **t\_sel**:

- milliseconds and seconds
- minutes and hours.

**Flicker** is Verilog-written block, which makes current load segments to flick: once every half a second.

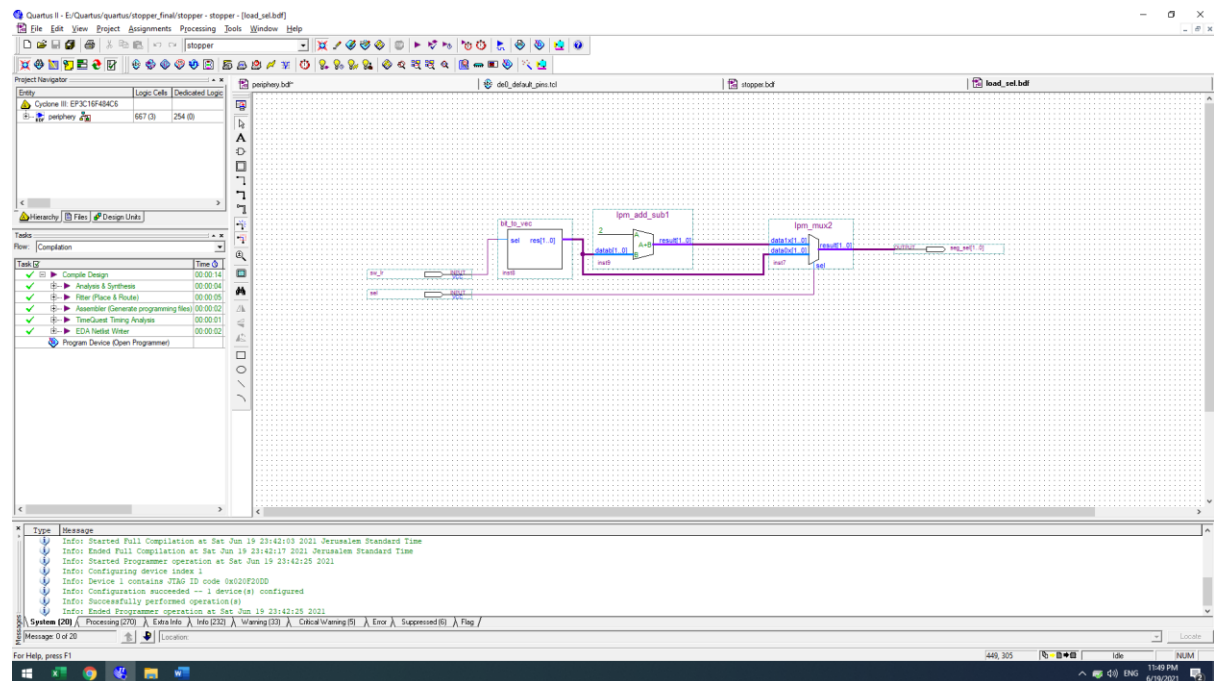
**PWMgen** is Verilog-written block, which is responsible for brightness control with **button0**(left) to decrease and **button1**(middle) to increase.

**3-to-1 VecMux** to choose the display block: timer, stopper, watch.

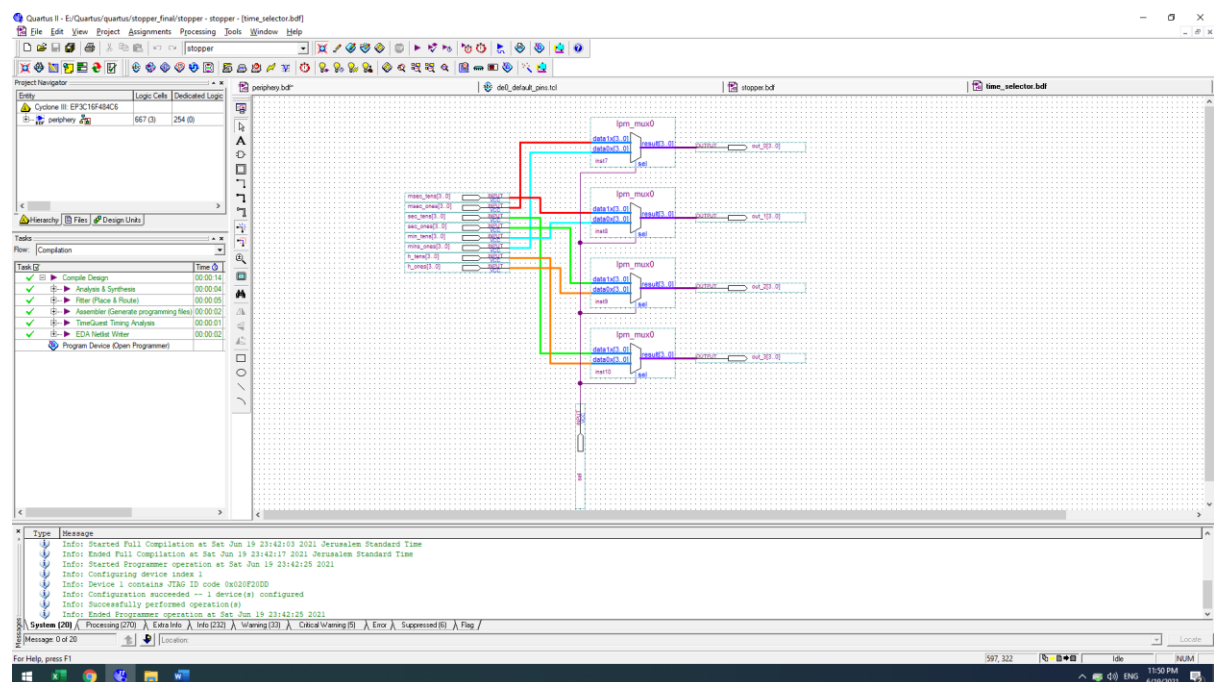
**4 hexsse** to convert binary to hex.

**load\_sel** block to choose which counter in BCD is being loaded. Not used in watch, but could be.

## load\_sel



## time\_selector



## flicker\_sel

Quartus II - E:\Quartus\quartus\_final\stopper - stopper - [flicker\_sel.bdf]

File Edit View Project Assignments Processing Tools Window Help

Project Navigator: Entity: Cyclone III EP3K10K10AC6, periphery: 687 (G) 254 (D)

Task List: Compile Design (00:00:14), Analyze & Synthesize (00:00:04), Filter (Place & Route) (00:00:05), Assemble (Generate programming files) (00:00:02), TimeQuest Timing Analysis (00:00:01), EDA Netlist Writer (00:00:02), Program Device (Open Programmer)

Messages: Info: Started Full Compilation at Sat Jun 19 23:42:03 2021 Jerusalem Standard Time, Info: Ended Full Compilation at Sat Jun 19 23:42:17 2021 Jerusalem Standard Time, Info: Started Programmer operation at Sat Jun 19 23:42:25 2021, Info: Configuring device index 1, Info: Device 1 contains JTAG ID code 0x020F2000, Info: Configuration succeeded -- 1 device(s) configured, Info: Successfully performed operation(s), Info: Ended Programmer operation at Sat Jun 19 23:42:25 2021

## flicker

Quartus II - E:\Quartus\quartus\_final\stopper - stopper - [flicker.v]

File Edit View Project Assignments Processing Tools Window Help

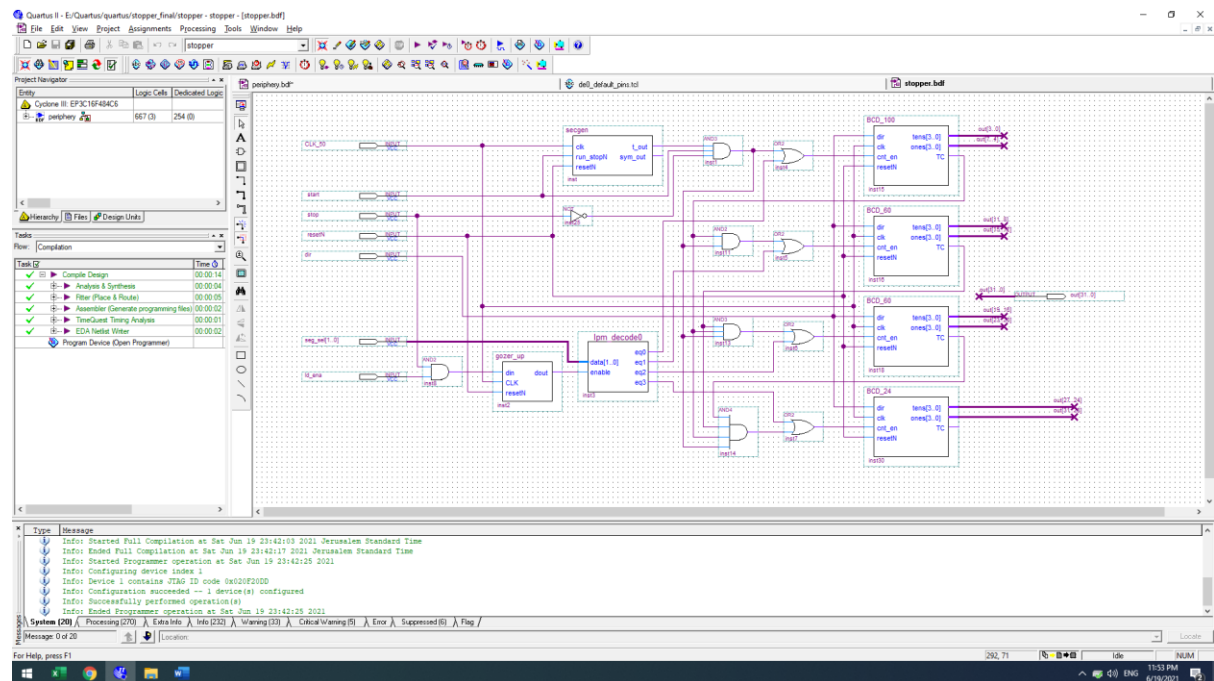
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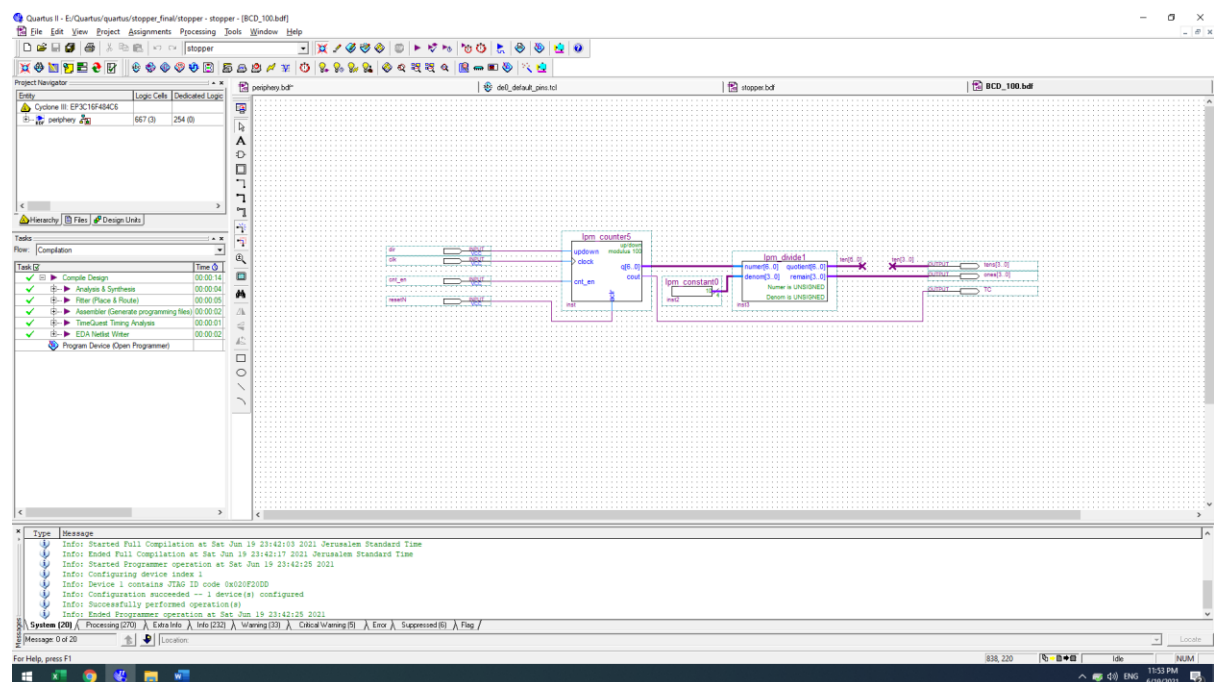
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```
1 module flicker
2   (
3     ena,
4     clk,
5     out
6   );
7   input ena;
8   input clk;
9   output out;
10  wire tap_out;
11  reg[7:0] tap;
12
13  always @(posedge clk)
14  begin
15    if(ena == 1)
16    begin
17      if(tap == 25000000)
18      begin
19        tap_out <= ~tap_out;
20        tap <= 0;
21      end
22    else
23      tap <= tap + 1;
24    end
25  end
26  begin
27    tap <= 0;
28    tap_out <= 0;
29  end
30
31  assign out = tap_out;
32 endmodule
```

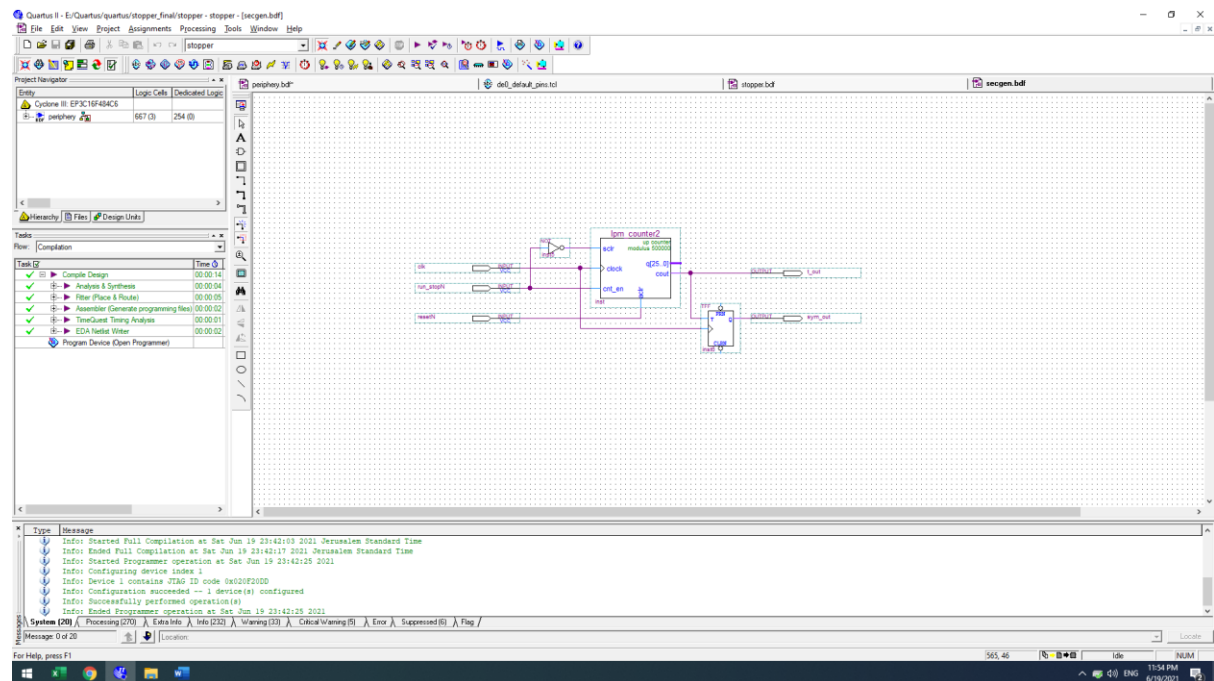
## stopper



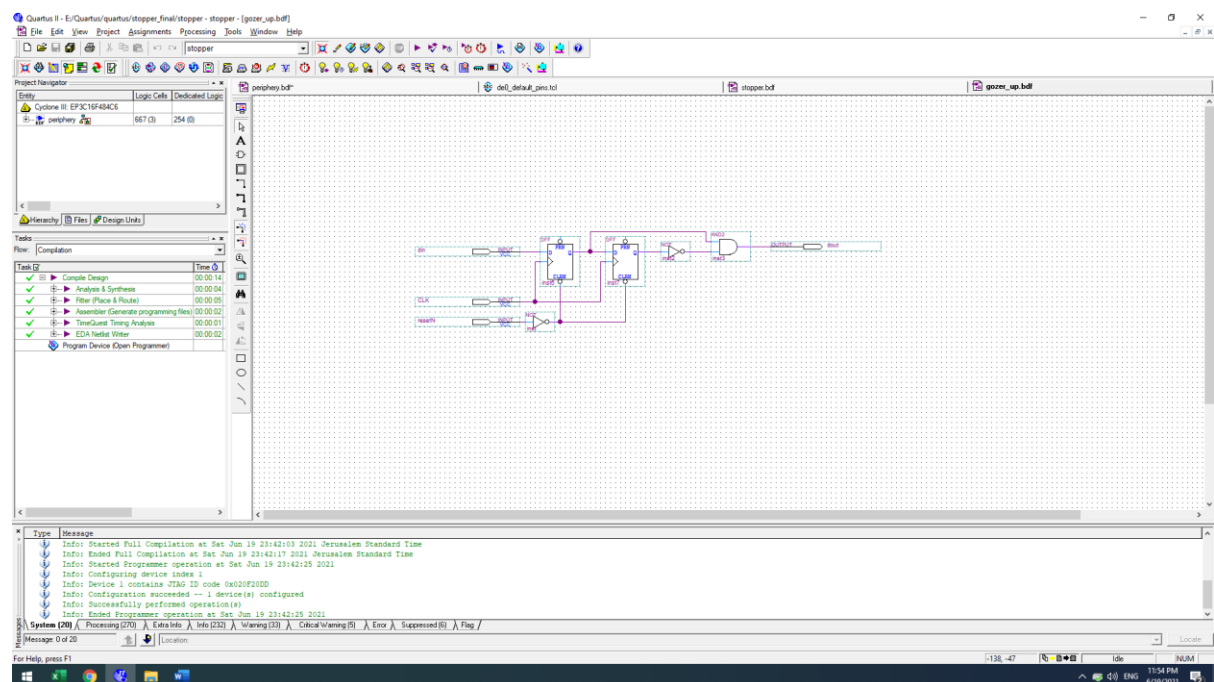
## BCD 24/60/100



secgen (centgen actually)

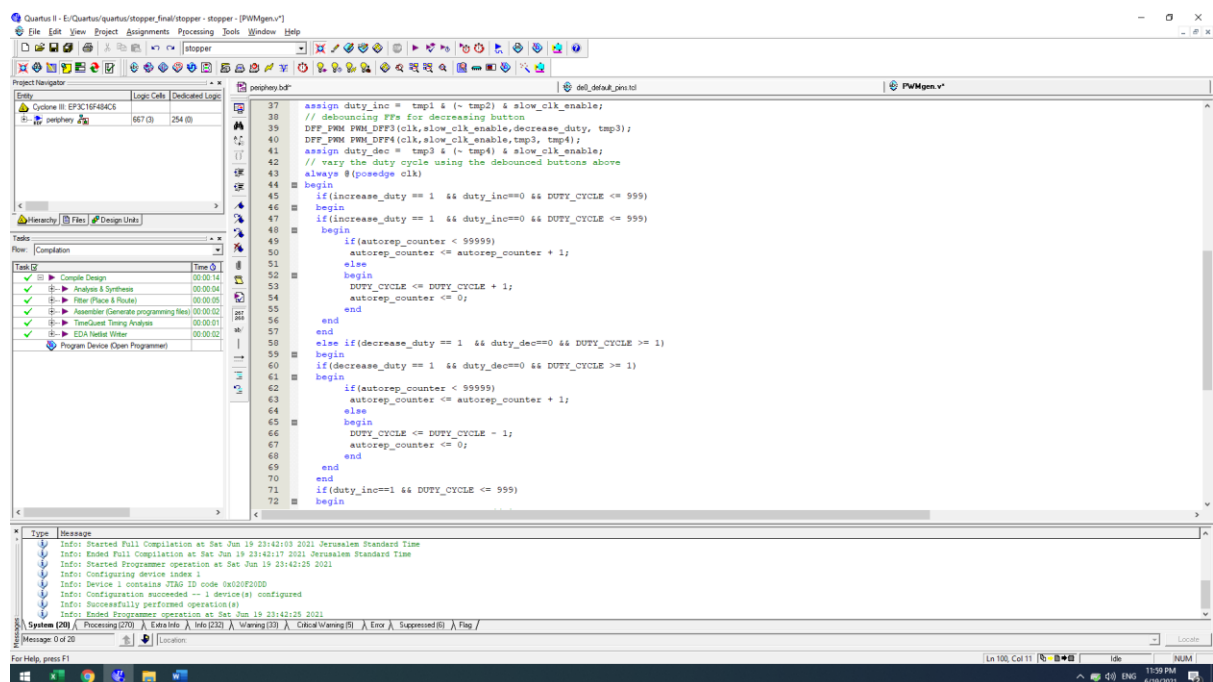
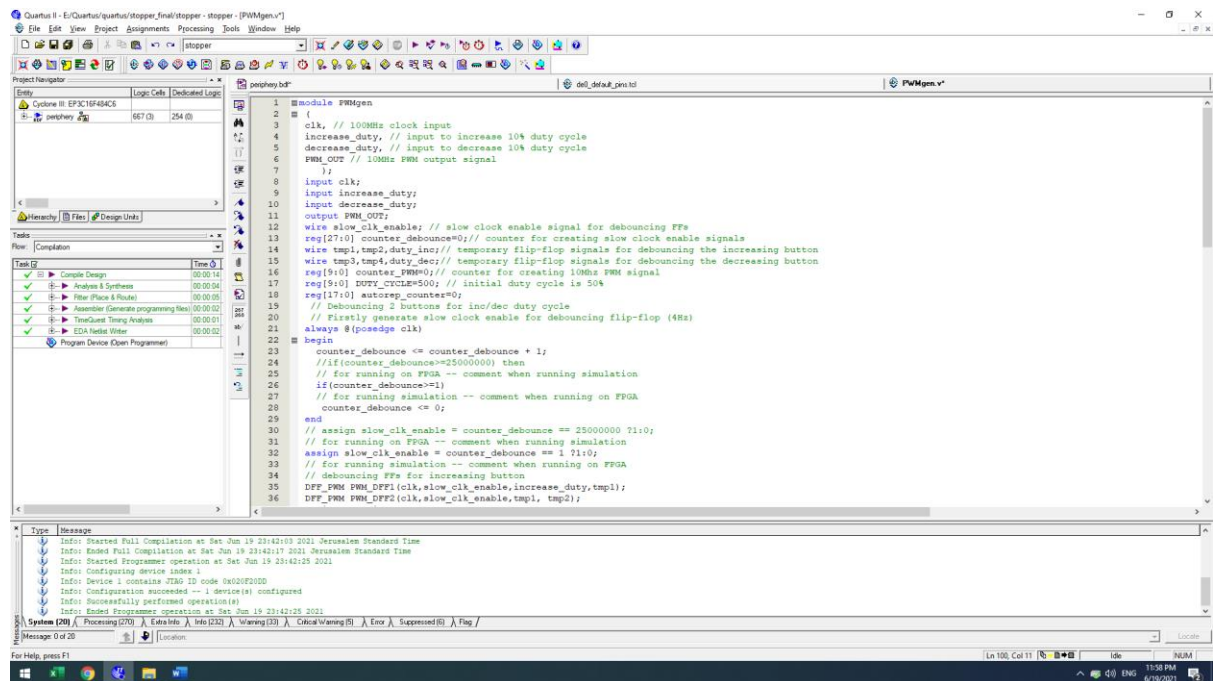


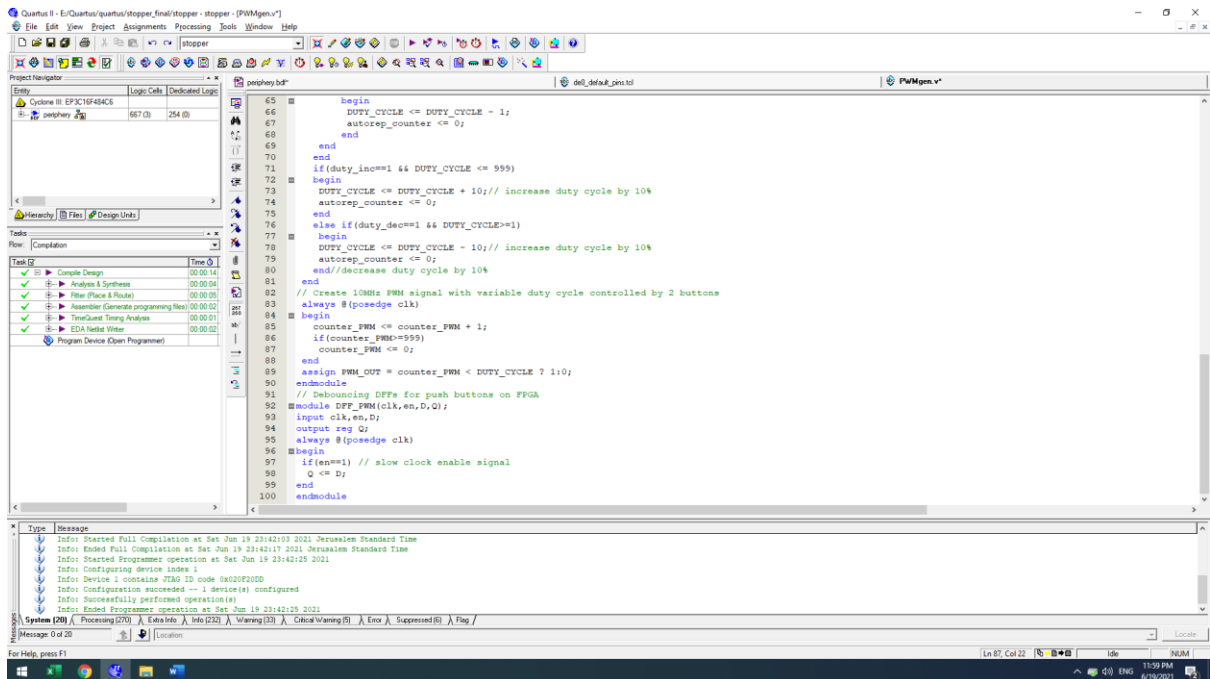
gozer\_up (sync rise detector)



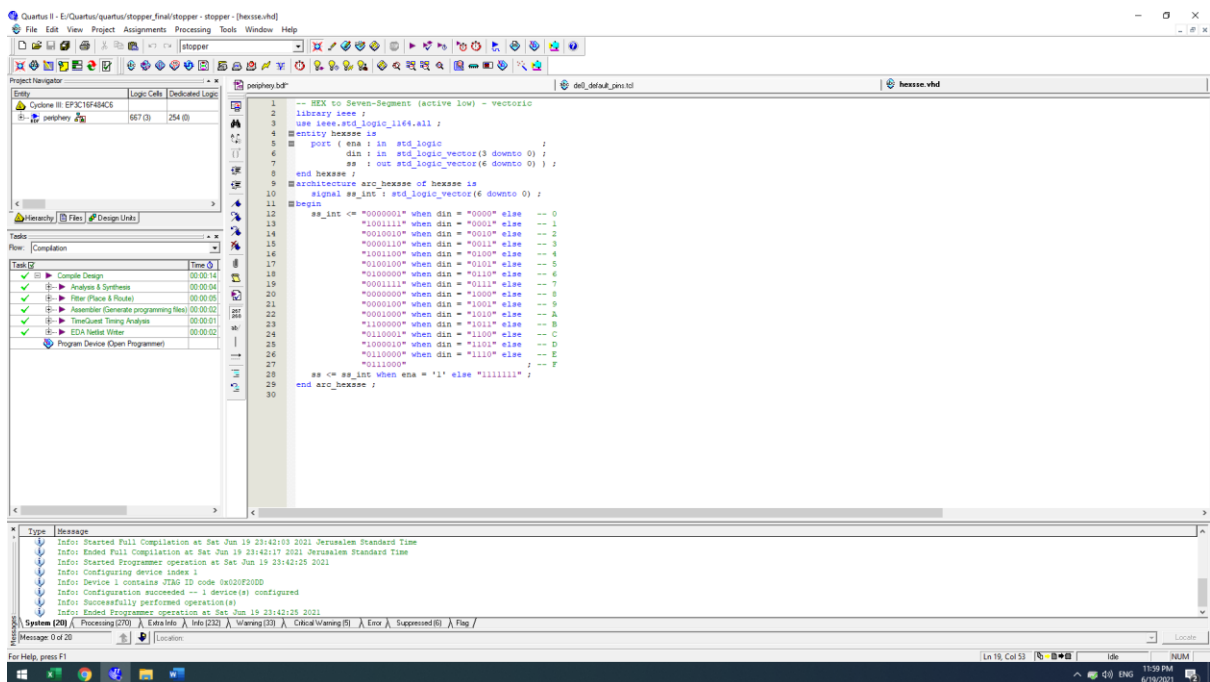


# PWMgen

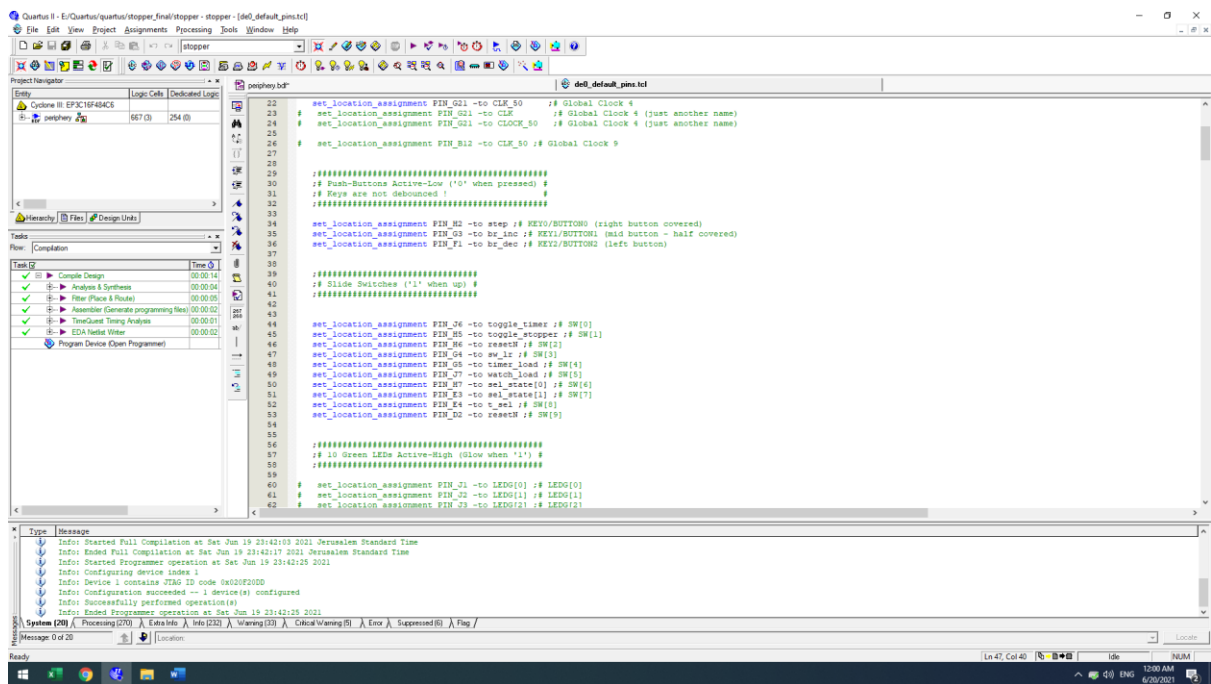
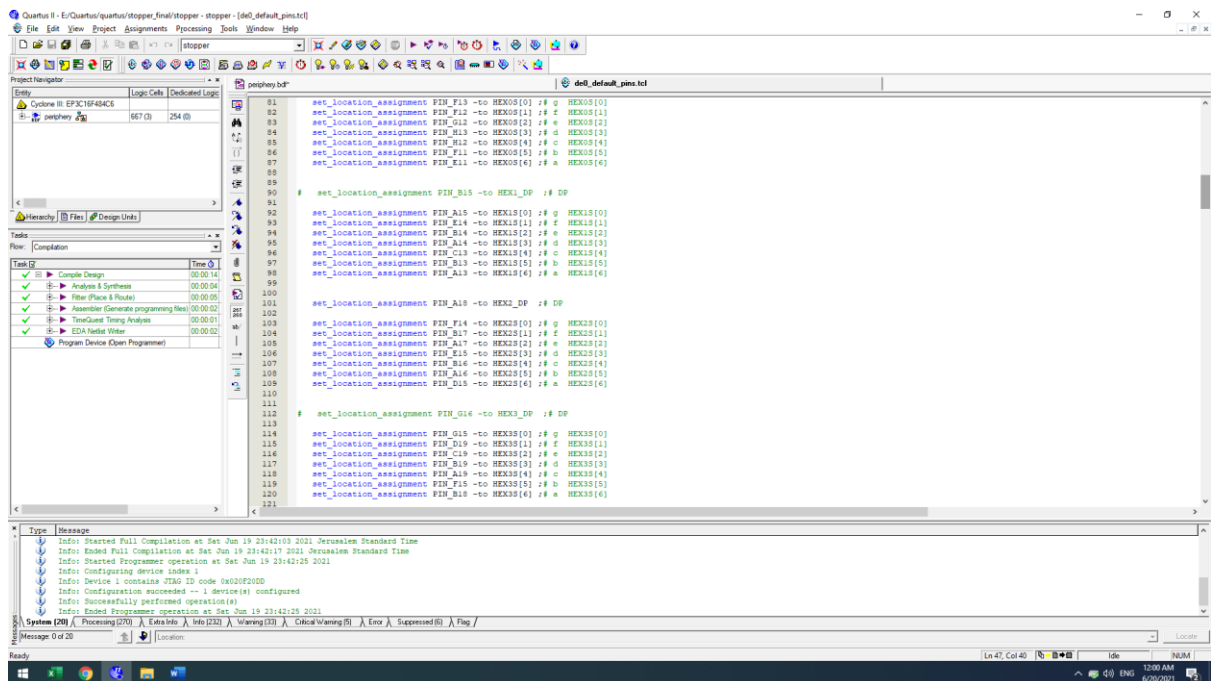




## hexsse

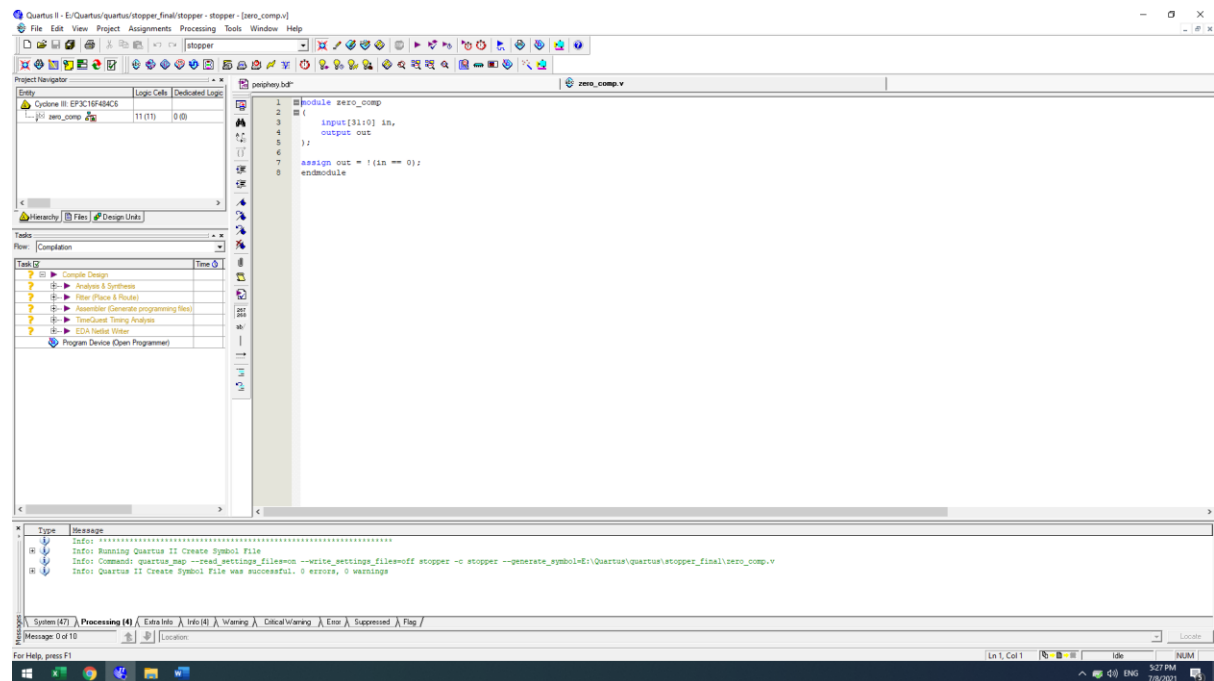


pins





## zero\_comp



Output is inverted to stop timer count on 00:00:00:000.