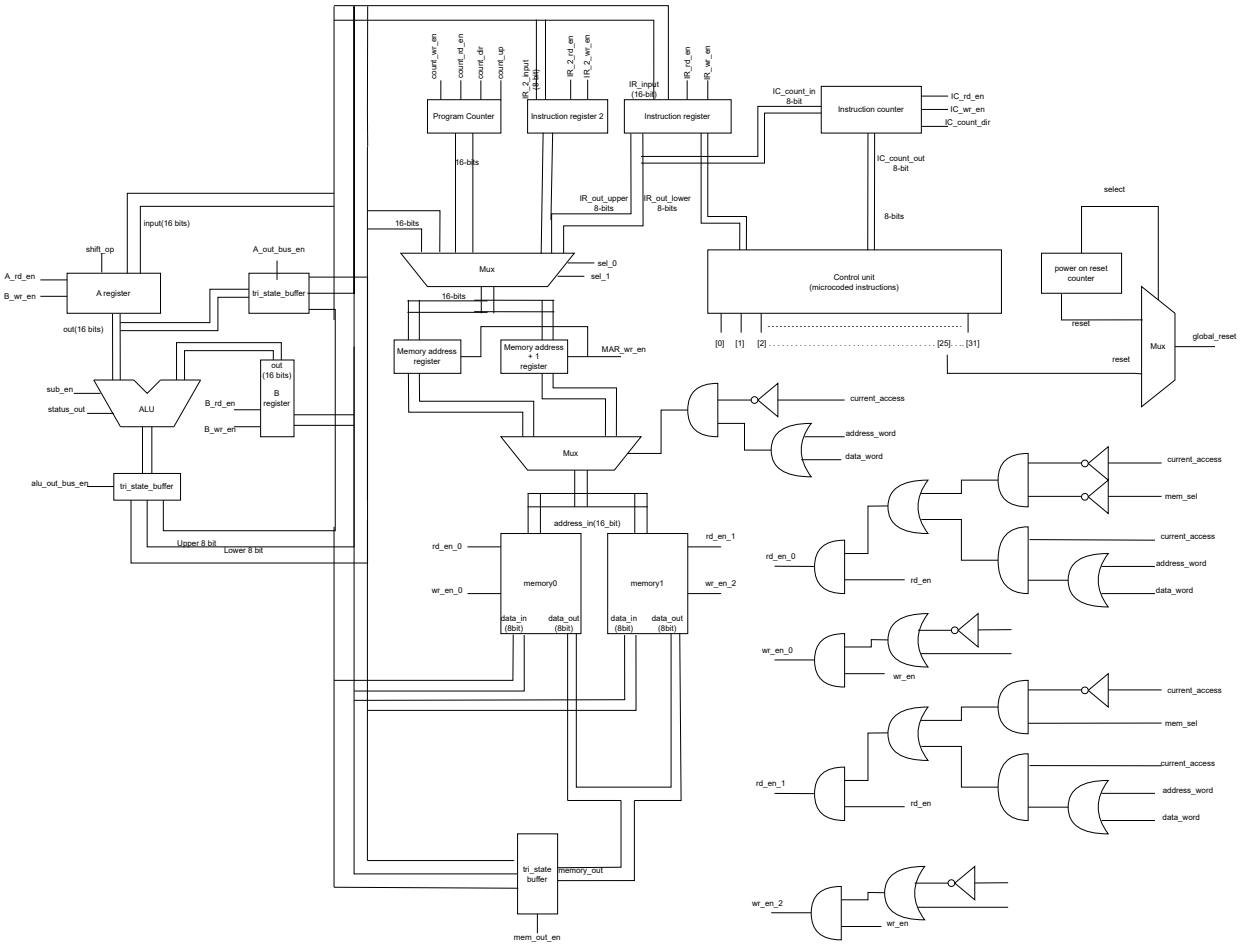


```
a_rd_en = control_signals[0];
a_wr_en = control_signals[1];
a_shift = control_signals[2];
a_bus_out_en = control_signals[3];

b_rd_en = control_signals[4];
b_wr_en = control_signals[5];

alu_sub_en = control_signals[6];
alu_status_out_en = control_signals[7];
alu_bus_out_en = control_signals[8];

ic_rd_en = control_signals[9];
ic_wr_en = control_signals[10];
ic_count_dir = control_signals[11];

ir_rd_en = control_signals[12];
ir_wr_en = control_signals[13];

mar_mux_sel = control_signals[14:15];
mar_wr_en = control_signals[16];

mem_rd_en = control_signals[17];
mem_wr_en = control_signals[18];
mem_addr_valid = 1;

count_wr_en = control_signals[19];
count_rd_en = control_signals[20];
count_dir = control_signals[21];
count = control_signals[22];

mem_bus_out_en = control_signals[23];

main_reset = control_signals[24];
ic_rst = control_signals[25];
ir_2_rd_en = control_signals[26]
ir_2_wr_en = control_signals[27]
current_access = control_signals[28]
address_word = control_signals[29]
data_word = control_signals[30]
mem_sel = control_signals[31]
```