Bit order: MSB --> LSB. last five bits are empty

	A_register			A_reg_tristate	B_register		ALU			ALU_tristate	Instr_cnt			Instr_reg		MAR_mux		MAR	memory		prog_cnt				memory tristate				
Control pins-->	rd_en	wr_en	shift	tristate_en	rd_en	wr_en	sub_en	status_out_en	tristate_en	rd_en	wr_en	cnt_dir	rd_en	wr_en	mux_sel[1]	mux_sel[0]	wr_en	rd_en	wr_en	wr_en	rd_en	cnt_dir	count_up	tristate_en	main_rst	word_op	ins_ctr_rst	remaining 5 bits
fetch	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0
decode	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	1	1	0	1	0
execute	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	0	0	1	0	0	1	0
word operations																												
LDA -->	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0
LDB -->	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0
byte operations	the byte operations has program counter incremented by only one instead of two times during first three stages - fetch, decode and execute																											
fetch	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0
decode	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	1	0
execute	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	0	0	1	0	0	1	0
ADD -->	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0