Computer Architecture and Programming Languages
Jacobs University Bremen
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Course: CO20-320241
October 7th, 2019

Homework 5 - Addition, Subtraction and MIPS Instruction Set Architecture

- Template file for submitting the solutions:
  https://grader.eecs.jacobs-university.de/courses/320241/2019_2/lectures/template_hw.tex
- The TAs are grading solutions to the problems according to the following criteria:
  https://grader.eecs.jacobs-university.de/courses/320241/2019_2/Grading_Criteria_CAPL.pdf

Problem 5.1 *Addition and subtraction* (2 points)

Perform the following addition/subtraction operations by showing and writing down intermediate steps:

(a) $14 + 37$ using binary representation

(b) $12 - 27$ using binary and 2's complement representation

(c) $69 + 58$ using BCD representation

(d) $275 + 642$ using BCD representation

(e) $6AF + 23C$ using hexadecimal representation

(f) $594 - 3A8$ using hexadecimal representation

Problem 5.2 *MIPS arithmetics* (2 points)

Perform the following arithmetic operations by writing down the corresponding MIPS code:

(a) `a = b + c`

(b) `a = b - d + c`

(c) `a = 3 *b`

(d) `a = (1 + b) *2`

Assume that the variable `a` is stored in register `$t0`, `b` is in register `$s0`, `c` is in register `$s1`, and `d` is in `$s2`. You are not allowed to use the `mul` operation. Comment each relevant code block.

Problem 5.3 *Binary codes for instructions* (2 points)

Write down the corresponding binary codes of the MIPS instructions for the operations (a) and (b) from **Problem 5.2**.

Problem 5.4 *Memory access in MIPS* (1 point)

Assume that you have the following C code:

```
B[5] = A[4] + A[2];
```

Write down the MIPS code corresponding to this code. Assume that the base address of `A` is stored in `$s0`, and the base address of `B` is stored in `$s1`. Comment the relevant code blocks.

Problem 5.5 *Memory access using an index variable* (2 points)

Assume that you have the following C code:

```
B[x] = A[x+7] + A[x+2];
```

Write down the MIPS code corresponding to this code. Assume that the base address of `A` is stored in `$s0`, the base address of `B` is stored in `$s1`, and the value of `x` is in `$t0`. Comment the relevant code blocks.

Problem 5.6 *MIPS instruction format* (1 point)

The register instruction format for the instruction `addi` uses 6 bits for the opcode, 5 bits for the first register, 5 bits for the second register, and 16 bits for the constant value that is to be added. Assume that a detailed analysis of machine code has revealed that not more than 12 registers are needed for the processor and therefore it has been decided to reduce the number of general purpose registers to 16. How and why could the instruction format for the `addi` instruction be changed?

How to submit your solutions

You can submit your solutions via *Grader* at **`https://grader.eecs.jacobs-university.de`** as a generated PDF file from the given template TEX file.
If there are problems with *Grader* (but only then), you can submit the file by sending mail to `k.lipskoch@jacobs-university.de` **with a subject line that starts with CO20-320241**.

Please note, that after the deadline it will not be possible to submit solutions. It is useless to send solutions by mail, because they will not be graded.

This homework is due by Monday, October 14th, 23:00.