Computer Architecture and Programming Languages
Jacobs University Bremen
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Course: CO20-320241
November 4th, 2019

Homework 8 - MIPS Instruction Set Architecture/Performance

- Template file for submitting the solutions:
  https://grader.eecs.jacobs-university.de/courses/320241/2019_2/lectures/template_hw.tex
- The TAs are grading solutions to the problems according to the following criteria:
  https://grader.eecs.jacobs-university.de/courses/320241/2019_2/Grading_Criteria_CAPL.pdf

Problem 8.1 *Floating point binary representation* (2 points)

Compute the IEEE 754 single precision binary representation of the following numbers:

(i)	$\frac{25}{32}$
(ii)	27.3515625

Write down your complete calculations, not just the final results.

Problem 8.2 *MIPS properties* (1 point)

true	false	
☐	☐	MIPS has an alignment restriction, that means words must start at addresses that are multiples of 4.
☐	☐	All MIPS instructions are 30 bits long.
☐	☐	MIPS can perform arithmetic operations on memory locations.
☐	☐	Parameters to functions are always passed via the stack.
☐	☐	A procedure jumps to the address stored in the stack pointer register after it finishes execution.

Problem 8.3 *Machine code to MIPS* (1 point)

In MIPS assembly language, registers `$s0` to `$s7` map onto register 16 to 23, and registers `$t0` to `$t7` map onto register 8 to 15. The opcode for addition and subtraction is 0. The function code is 32 for addition and 34 for subtraction. Given all this, translate the following binary word into a MIPS instruction:

```
000000 10000 10101 01011 00000 100000
```

Problem 8.4 *MIPS questions* (1 point)

(a) How many bits can be used for the destination address in the `j` (jump) instruction?

(b) If the address representation within the instruction does not cover the full 32-bit range (as in the previous question), what can be done to still be able to jump "anywhere" (assuming 32-bit addresses)?

Problem 8.5 *Performance I* (3 points)

Two different implementations that render an image are run on computers P1 and P2. Both computers use the same instruction set architecture. There are five classes of instructions (A - E) in the instruction set.

Class	CPI on P1	CPI on P2	Frequency
A	1	2	60%
B	2	2	10%
C	3	2	10%
D	4	4	10%
E	3	4	10%

P1 has a clock rate of 4 GHz, P2 has a clock rate of 6 GHz. The average number of cycles for each instruction class for P1 and P2 is given in the table above. Which computer will finish rendering the image first? How much faster is the computer that finishes first (a fraction is sufficient)?
Write down your complete calculations.

Problem 8.6 *Performance II* (3 points)

Consider two different implementations P1 and P2 of the same instruction set. There are five classes of instructions (A - E) in the instruction set.

Class	CPI on P1	CPI on P2
A	1	2
B	3	3
C	3	2
D	4	3
E	2	3

P1 has a clock rate of 2 GHz, P2 has a clock rate of 4 GHz. The average number of cycles for each instruction class for P1 and P2 is as in the table above. If the number of instructions executed in a certain program is divided equally among the classes of instructions as above except for class A, which occurs twice as often as each of the others, how much faster is P2 than P1?
Write down your complete calculations.

How to submit your solutions

You can submit your solutions via *Grader* at **`https://grader.eecs.jacobs-university.de`** as a generated PDF file from the given template TEX file.
If there are problems with *Grader* (but only then), you can submit the file by sending mail to `k.lipskoch@jacobs-university.de` **with a subject line that starts with CO20-320241**.

Please note, that after the deadline it will not be possible to submit solutions. It is useless to send solutions by mail, because they will not be graded.

This homework is due by Monday, November 11th, 23:00.