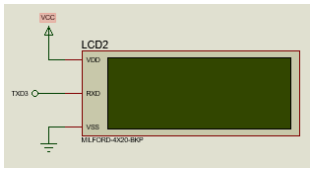
PI práctica 4

jueves, 8 de diciembre de 2022 11:03

Pantalla Milford 4x20 BKP



• **Cómo escribimos en ella:**
1) Serial3.write(0xFE)
2) Serial3.write(comando)

Tabla de comandos			
Prefix	**Command**	**Description**	**Execution time**
-	-	Display Character Write (0x00 ~ 0xFF)	
0xFE	1	Clear Screen	10mS
0xFE	24	Scroll display one character left	
0xFE	28	Scroll display one character right	
0xFE	0	Home (and undo scrolling)	10mS
0xFE	16	Move cursor one character left	
0xFE	20	Move cursor one character right	
0xFE	14	Turn on underline cursor	
0xFE	13	Turn on blinking cursor	
0xFE	12	Turn off cursor	
0xFE	8	Blank the display (retaining data)	
0xFE	12	Restore the display (without cursor)	
0xFE	128 + address	Set display (DD) RAM address	
0xFE	64+address	Set character (CG) RAM address	

Tabla 4.- Tabla de comandos de la pantalla Milford 4x20 BKP

4x20 LCD

Line 1	address:	0	1	2	3	4	19
0x80	DD address:	128	129	130	131	132	147
Line 2	address:	64	65	66	67	68	83
0xC0	DD address	192	193	194	195	196.....	211
Line 3	address:	20	21	22	23	24.....	39
0x94	DD address:	148	149	150	151	152	167
Line 4	address:	84	85	86	87	88	103
0xD4	DD address	212	213	214	215	216.....	231

Posicionarse en la línea 1: Serial3.write(0xFE); Serial3.write(0x00);
Posicionarse en la línea 2: Serial3.write(0xFE); Serial3.write(0xC0);
Posicionarse en la línea 3: Serial3.write(0xFE); Serial3.write(0x94);
Posicionarse en la línea 4: Serial3.write(0xFE); Serial3.write(0xD4);

Memoria DS3232

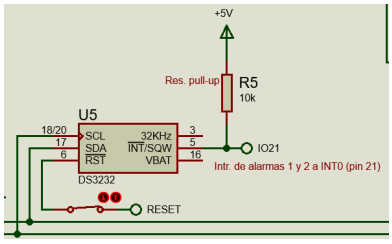


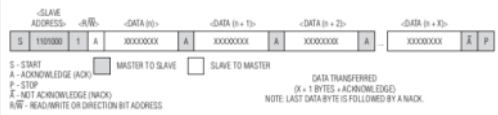
Figure 1. Address Map for DS3232 Timekeeping Registers and SRAM

ADDRESS	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB	FUNCTION	RANGE
00h	0	10 Seconds			Seconds				Seconds	00–59
01h	0	10 Minutes			Minutes				Minutes	00–59
02h	0	12/24	AM/PM	10 Hour	Hour				Hours	1–12 + AM/PM 00–23
03h	0	0	0	0	0	Day			Day	1–7
04h	0	0	10 Date		Date				Date	1–31
05h	Century	0	0	10 Month	Month				Month/ Century	01–12 + Century
06h	10 Year				Year				Year	00–99
07h	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00–59
08h	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00–59
09h	A1M3	12/24	AM/PM	10 Hour	Hour				Alarm 1 Hours	1–12 + AM/PM 00–23
0Ah	A1M4	DY/DT	10 Date		Day Date				Alarm 1 Day Alarm 1 Date	1–7 1–31
0Bh	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00–59
0Ch	A2M3	12/24	AM/PM	10 Hour	Hour				Alarm 2 Hours	1–12 + AM/PM 00–23
0Dh	A2M4	DY/DT	10 Date		Day Date				Alarm 2 Day Alarm 2 Date	1–7 1–31
0Eh	EOSC	BBSQW	CONV	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0Fh	OSF	BB32kHz	CRATE1	CRATE0	EN32kHz	BSY	A2F	A1F	Control/Status	—
10h	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	Aging Offset	—
11h	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	MSB of Temp	—
12h	DATA	DATA	0	0	0	0	0	0	LSB of Temp	—
13h	0	0	0	0	0	0	0	0	Not used	Reserved for test
14h–0FFh	x	x	x	x	x	x	x	x	SRAM	00h–0FFh

Note: Unless otherwise specified, the registers' state is not defined when power is first applied.

MODO ESCRITURA

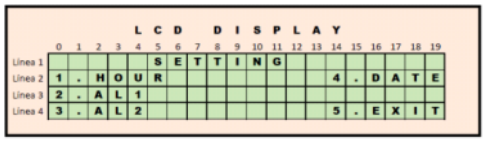
MODO LECTURA



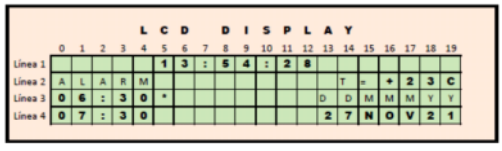
DY/DT=1 → se refiere a día de la semana
DY/DT=0 → se refiere a día del mes

Menú:

- #*: Entrada modo configuración



- *#: Salida modo configuración



- #: Tecla enter
- *: Tecla backspace

Alarmas

ALARMA 1

ADDRESS	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB	FUNCTION	RANGE
07h	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00–59
08h	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00–59
09h	A1M3	12/24	AM/PM	10 Hour	Hour				Alarm 1 Hours	1–12 + AM/PM 00–23
0Ah	A1M4	DY/DT	10 Date		Day Date				Alarm 1 Day Alarm 1 Date	1–7 1–31

DY/DT	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

ALARMA 2

ADDRESS	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB	FUNCTION	RANGE

Timers

TIMER3

Función: Actualizar información de la pantalla a partir de los datos suministrados por el RS3232
Modo: FAST PWM
TOP = OCR3A
N 1024
F = 1hz

$$f_{OC3PWM} = \frac{f_{clk}}{N \cdot (1 + TOP)} \Rightarrow TOP = \frac{f_{clk}}{f_{OC3PWM} \cdot N} - 1 = \frac{16 \cdot 10^6}{1 \cdot 1024} - 1 = 15624$$

$$\boxed{TOP = OCR3A = 15624}$$

TCCR3A = 00000011
TCCR3B = 00011101

TIMSK3 |= (1 << TOIE3);

TIMER1

Función: Explorar el display y el teclado 4x3
Modo: CTC
TOP = OCR1A
N = 64
F = 100hz

TCCR1A = 00000000
TCCR1B = 00001011

$$f_{OC1A} = \frac{f_{clk}}{2 \cdot N \cdot (1 + OCR1A)} \Rightarrow OCR1A = \frac{f_{clk}}{f_{OC1A} \cdot 2 \cdot N} - 1 = \frac{16 \cdot 10^6}{100 \cdot 2 \cdot 64} - 1$$

$$\boxed{OCR1A = 1249}$$

ISR(INT0_vect):

Interrupción externa, asociada al pin 21, que se activa cada vez que se produzca una alarma en el **Chip DS3232**

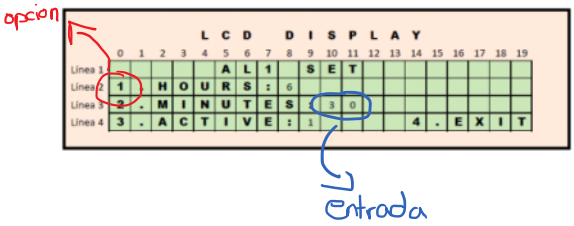
EIMSK – External Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0	
0x1D (0x3D)	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0	EIMSK

ALARMA 2

ADDRESS	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB	FUNCTION	RANGE
0Bh	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00-59
0Ch	A2M3	12/$\overline{24}$	AM/$\overline{PM}$	10 Hour	Hour				Alarm 2 Hours	1–12 + AM/$\overline{PM}$ 00-23
			20 Hour							
0Dh	A2M4	DY/$\overline{DT}$	10 Date		Day				Alarm 2 Day	1–7
					Date				Alarm 2 Date	1–31

DY/$\overline{DT}$	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match



Registro TCCR3A

17.11.2 TCCR3A – Timer/Counter 3 Control Register A

Bit	7	6	5	4	3	2	1	0	
(0x90)	COM3A1	COM3A0	COM3B1	COM3B0	COM3C1	COM3C0	WGM31	WGM30	TCCR3A
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The COMnA1:0, COMnB1:0, and COMnC1:0 control the output compare pins (OCnA, OCnB, and OCnC respectively) behavior.

- If one or both of the COMnA1:0 bits are written to one, the OCnA output overrides the normal port functionality of the I/O pin it is connected to.
- If one or both of the COMnB1:0 bits are written to one, the OCnB output overrides the normal port functionality of the I/O pin it is connected to.
- If one or both of the COMnC1:0 bits are written to one, the OCnC output overrides the normal port functionality of the I/O pin it is connected to.
- However, note that the Data Direction Register (DDR) bit corresponding to the OCnA, OCnB or OCnC pin must be set in order to enable the output driver.

Table 17-3. Compare Output Mode, non-PWM

COMnA1 COMnB1 COMnC1	COMnA0 COMnB0 COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected
0	1	Toggle OCnA/OCnB/OCnC on compare match
1	0	Clear OCnA/OCnB/OCnC on compare match (set output to low level)
1	1	Set OCnA/OCnB/OCnC on compare match (set output to high level)

Table 17-4 shows the COMnx1:0 bit functionality when the WGMn3:0 bits are set to the fast PWM mode.

Table 17-4. Compare Output Mode, Fast PWM

COMnA1 COMnB1 COMnC1	COMnA0 COMnB0 COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected
0	1	WGM13:0 = 14 or 15: Toggle OC1A on Compare Match, OC1B and OC1C disconnected (normal port operation). For all other WGM1 settings, normal port operation, OC1A/OC1B/OC1C disconnected
1	0	Clear OCnA/OCnB/OCnC on compare match, set OCnA/OCnB/OCnC at BOTTOM (non-inverting mode)
1	1	Set OCnA/OCnB/OCnC on compare match, clear OCnA/OCnB/OCnC at BOTTOM (inverting mode)

Note: A special case occurs when OCRnA/OCRnB/OCRnC equals TOP and COMnA1/COMnB1/COMnC1 is set. In this case the compare match is ignored, but the set or clear is done at BOTTOM. See "Fast PWM Mode" on page 146. for more details.

Table 17-5 shows the COMnx1:0 bit functionality when the WGMn3:0 bits are set to the phase correct and frequency correct PWM mode.

Table 17-5. Compare Output Mode, Phase Correct and Phase and Frequency Correct PWM

COMnA1 COMnB1 COMnC1	COMnA0 COMnB0 COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected
0	1	WGM13:0 =9 or 11: Toggle OC1A on Compare Match, OC1B and OC1C disconnected (normal port operation). For all other WGM1 settings, normal port operation, OC1A/OC1B/OC1C disconnected
1	0	Clear OCnA/OCnB/OCnC on compare match when up-counting Set OCnA/OCnB/OCnC on compare match when downcounting
1	1	Set OCnA/OCnB/OCnC on compare match when up-counting Clear OCnA/OCnB/OCnC on compare match when downcounting

Note: A special case occurs when OCRnA/OCRnB/OCRnC equals TOP and COMnA1/COMnB1//COMnC1 is set. See "Phase Correct PWM Mode" on page 148. for more details.

Registro TCCR3B

17.11.8 TCCR5B – Timer/Counter 5 Control Register B

Bit	7	6	5	4	3	2	1	0	
(0x121)	ICNC5	ICES5	–	WGM53	WGM52	CS52	CS51	CS50	TCCR5B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – ICNCn: Input Capture Noise Canceler**

Setting this bit (to one) activates the Input Capture Noise Canceler. When the Noise Canceler is activated, the input from the Input Capture Pin (ICPn) is filtered. The filter function requires four successive equal valued samples of the ICPn pin for changing its output. The input capture is therefore delayed by four Oscillator cycles when the noise canceler is enabled.

- **Bit 6 – ICESn: Input Capture Edge Select**

This bit selects which edge on the Input Capture Pin (ICPn) that is used to trigger a capture event. When the ICESn bit is written to zero, a falling (negative) edge is used as trigger, and when the ICESn bit is written to one, a rising (positive) edge will trigger the capture.

EIMSK – External Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0	
0x1D (0x3D)	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0	EIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Modos de funcionamiento

Mode	WGMn3	WGMn2 (CTCn)	WGMn1 (PWMn1)	WGMn0 (PWMn0)	Timer/Counter Mode of Operation	TOP	Update of OCRnx at	TOVn Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCRnA	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICRn	BOTTOM	BOTTOM
9	1	0	0	1	PWM,Phase and Frequency Correct	OCRnA	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICRn	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCRnA	TOP	BOTTOM
12	1	1	0	0	CTC	ICRn	Immediate	MAX
13	1	1	0	1	(Reserved)	–	–	–
14	1	1	1	0	Fast PWM	ICRn	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCRnA	BOTTOM	TOP

Tabla 2. Modos de funcionamiento del Timer 3

Interrupciones

Nombre	Flag de habilitación (TIMSK3)	Número de vector	Nombre del vector para ISR()
Capture	ICIE3	32	TIMER3_CAPT_vect
Compare match A	OCIE3A	33	TIMER3_COMPA_vect
Compare match B	OCIE3B	34	TIMER3_COMPB_vect
Compare match C	OCIE3C	35	TIMER3_COMPC_vect
Overflow	TOIE3	36	TIMER3_OVF_vect

Tabla 1. Interrupciones del Timer 3

Los eventos (fuentes) que pueden generar una interrupción son:

- Flaco de subida o bajada en el pin Input Capture (ICP3)
- Igualdad (o match) entre el registro OCR3A y el registro del timer TCNT3
- Igualdad (o match) entre el registro OCR3B y el registro del timer TCNT3
- Igualdad (o match) entre el registro OCR3C y el registro del timer TCNT3
- Overflow. Según el modo de funcionamiento, se produce en el: MAX, TOP o BOTTOM.

Registro TIMSK3

17.11.34 TIMSK3 – Timer/Counter 3 Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0	
(0x71)	–	–	ICIE3	–	OCIE3C	OCIE3B	OCIE3A	TOIE3	TIMSK3
Read/Write	R	R	R/W	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 5 – ICIEn: Timer/Countern, Input Capture Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Countern Input Capture interrupt is enabled. The corresponding Interrupt Vector (see "Interrupts" on page 101) is executed when the ICFn Flag, located in TIFRn, is set.

- **Bit 3 – OCIEnC: Timer/Countern, Output Compare C Match Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Countern Output Compare C Match interrupt is enabled. The corresponding Interrupt Vector (see "Interrupts" on page 101) is executed when the OCFnC Flag, located in TIFRn, is set.

- **Bit 2 – OCIEnB: Timer/Countern, Output Compare B Match Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Countern Output Compare B Match interrupt is enabled. The corresponding Interrupt Vector (see "Interrupts" on page 101) is executed when the OCFnB Flag, located in TIFRn, is set.

- **Bit 1 – OCIEnA: Timer/Countern, Output Compare A Match Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Countern Output Compare A Match interrupt is enabled. The corresponding Interrupt Vector (see "Interrupts" on page 101) is executed when the OCFnA Flag, located in TIFRn, is set.

- **Bit 0 – TOIEn: Timer/Countern, Overflow Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Countern Overflow interrupt is enabled. The corresponding Interrupt Vector (see "Interrupts" on page 101) is executed when the TOVn Flag, located in TIFRn, is set.

Modos de funcionamiento y frecuencias (timer 16 bits)

Modo	Frecuencias en salidas OC3A, OC3B y OC3C
Normal (toogle en salida)	**F = 16 MHz / (2 x N x (1+TOP))** TOP = MAX (0xFFFF)
CTC (toogle en salida)	**F = 16 MHz / (2 x N x (1+TOP))** TOP = OCR3A o ICR3 (0x0000-0xFFFF)
Fast PWM, rampa simple	**F = 16 MHz / (N x (1+TOP))** TOP= 0x00FF, 0x01FF, 0x3FF, OCR3A o ICR3
Phase correct PWM , rampa doble	**F = 16 MHz / (2 x N x TOP)** TOP= 0x00FF, 0x01FF, 0x3FF, OCR3A o ICR3
Phase and frequency correct PWM, rampa doble	**F = 16 MHz / (2 x N x TOP)** TOP= OCR3A o ICR3
N: prescaler (1,8,64,256 o 1024)	

$$f_{clk-timer} = \frac{f_{clk}}{N}$$

17.11.8 TCCR5B – Timer/Counter 5 Control Register B

Bit	7	6	5	4	3	2	1	0	
(0x121)	ICNC5	ICES5	–	WGM53	WGM52	CS52	CS51	CS50	TCCR5B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – ICNCn: Input Capture Noise Canceler**

Setting this bit (to one) activates the Input Capture Noise Canceler. When the Noise Canceler is activated, the input from the Input Capture Pin (ICPn) is filtered. The filter function requires four successive equal valued samples of the ICPn pin for changing its output. The input capture is therefore delayed by four Oscillator cycles when the noise canceler is enabled.

- **Bit 6 – ICESn: Input Capture Edge Select**

This bit selects which edge on the Input Capture Pin (ICPn) that is used to trigger a capture event. When the ICESn bit is written to zero, a falling (negative) edge is used as trigger, and when the ICESn bit is written to one, a rising (positive) edge will trigger the capture.

When a capture is triggered according to the ICESn setting, the counter value is copied into the Input Capture Register (ICRn). The event will also set the Input Capture Flag (ICFn), and this can be used to cause an Input Capture Interrupt, if this interrupt is enabled.

When the ICRn is used as TOP value (see description of the WGMn3:0 bits located in the TCCRnA and the TCCRnB Register), the ICPn is disconnected and consequently the input capture function is disabled.

- **Bit 5 – Reserved Bit**

This bit is reserved for future use. For ensuring compatibility with future devices, this bit must be written to zero when TCCRnB is written.

- **Bit 4:3 – WGMn3:2: Waveform Generation Mode**

See TCCRnA Register description.

- **Bit 2:0 – CSn2:0: Clock Select**

The three clock select bits select the clock source to be used by the Timer/Counter, see Figure 17-10 and Figure 17-11 on page 152.

Table 17-6. Clock Select Bit Description

CSn2	CSn1	CSn0	Description
0	0	0	No clock source. (Timer/Counter stopped)
0	0	1	$clk_{I/O}$/1 (No prescaling
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	$clk_{I/O}$/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on Tn pin. Clock on falling edge
1	1	1	External clock source on Tn pin. Clock on rising edge

If external pin modes are used for the Timer/Countern, transitions on the Tn pin will clock the counter even if the pin is configured as an output. This feature allows software control of the counting.

Secuencia de teclas	Descripción
*#	Entrada en modo configuración (setting)
#*	Salida del modo de configuración. Retorno a la pantalla de visualización normal
#	Salvo en las dos primeras filas, la tecla # hace de "retorno de carro"
*	Salvo en las dos primeras filas, la tecla * hace de "delete"

Menú1 (principal)	Menú2 (secundario)	Petición de datos
1.- Ajustar hora	1.- Hora: 2.- Minuto 3.- Segundo 4.- Exit	Introducir hora: 13 Introducir min: 25 Introducir seg: 54
2.- Ajustar fecha	1.- Día 2.- Mes 3.- Año 4.- Exit	Introducir día: 13 Introducir mes: 10 Introducir año: 2021
3.- Ajustar alarma 1		
4.- Ajustar alarma 2		

	TOP = OCR3A o ICR3 (0x0000-0xFFFF)
Fast PWM, rampa simple	**F = 16 MHz / (N x (1+TOP))** TOP= 0x00FF, 0x01FF, 0x3FF, OCR3A o ICR3
Phase correct PWM , rampa doble	**F = 16 MHz / (2 x N x TOP)** TOP= 0x00FF, 0x01FF, 0x3FF, OCR3A o ICR3
Phase and frequency correct PWM, rampa doble	**F = 16 MHz / (2 x N x TOP)** TOP= OCR3A o ICR3
N: prescaler (1,8,64,256 o 1024)	

$$f_{clk-timer} = \frac{f_{clk}}{N}$$

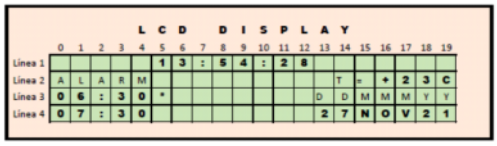


Figura 2. Información a mostrar en pantalla LCD

Por criterios de homogeneidad, en la siguiente tabla se muestran los diferentes campos a visualizar en la pantalla LCD indicándose posición y posibles valores a visualizar:

Campo	Fila	Columna	Caracteres	Descripción
Hora	1	5	8	Hora en formato → hh:mm:ss
Etiqueta (fija)	2	0	5	Etiqueta: ALARM
Etiqueta (fija)	2	14	2	Etiqueta: T=
Temperatura (T)	2	16	3	Temperatura medida por el DS3232
Etiqueta (fija)	2	19	1	Etiqueta: C
ALARMA1	3	0	5	Hora de la ALARMA 1
ACTIVE1	3	5	1	*: Activa espacio: No activa
Etiqueta	3	13	7	Etiqueta: DDMMMYY
ALARMA2	4	0	5	Hora de la ALARMA 2
ACTIVE2	4	5	1	*: Activa espacio: No activa
Fecha	4	13	7	DDMMMYY MMM → JAN-FEB-MAR-APR-MAY-JUN-JUL-AUG-SEP-OCT-NOV-DEC

Tabla 1.- Campos de información de la pantalla LCD

→ f = 200hz

$f_{CLK-TIMER} = \frac{f_{CLK}}{N} \Rightarrow N = \frac{16 \cdot 10^6}{2 \cdot 10^6} = 8$

$2 \cdot 10^6 = \frac{16 \cdot 10^6}{N}$

N=8

$f = \frac{16 \cdot 10^6}{N(1+TOP)} \rightarrow TOP = \frac{16 \cdot 10^6}{200 \cdot 8} - 1$

TOP = 9999

de 0 a 9999 niveles de potencia.

Ancho pulso	Grados
1 ms	0°
2 ms	90°
3 ms	180°

↳ 10000 niveles

TCCR3A : 00001011

TCCR3B: 00011010

100 % = 10000 = 5 ms

x % = X = 2 ms

$TOP = \frac{10000 \cdot t}{5}$