A Self-Interference Cancelling Front-End for In-Band Full-Duplex Wireless and its Phase Noise Performance

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***Abstract*— This paper describes a frequency-agile RF front-end in 65nm CMOS targeting short-range full-duplex wireless communication. Complementing previous work on a self-interference cancelling receiver, this work describes the co-integrated transmitter and reports the phase noise advantages of using correlated clock resources to clock all up- and downconverters present in the system. The hardware is capable of frequency-agile operation from 0.15 to 3.5GHz carrier frequency. Measurements at 2.5 GHz indicate that the RX noise floor is only 1 dB degraded by phase noise when operated from a commercial PLL with ~ -38 dBc phase noise.**

***Index Terms*—Full-duplex, transmitter, self-interference, phase noise, interference cancellation**

I. Introduction

Full-duplex (FD) wireless communication, i.e. *simultaneous* transmission and reception *in the same frequency channel*, is a promising way to increase spectral efficiency. Beside the physical layer benefit of up to a factor two in spectral efficiency, additional advantages are expected in higher network layers enabling new applications [1,2].

The major bottleneck in achieving FD wireless is strong crosstalk between the transmitter and receiver, referred to as self-interference (SI), see Figure 1. Recovering the (much weaker) desired signal necessitates SI *isolation* and *cancellation*. Cancellation uses knowledge of the transmit signal from various points in the TX chain to subtract SI in the RX chain (figure 1).

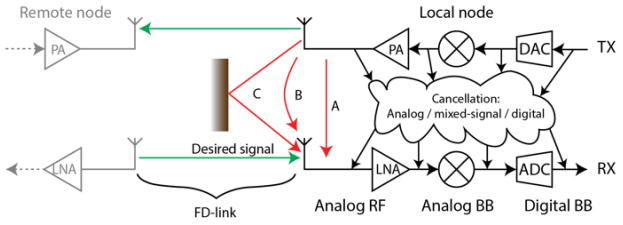

Figure 1: Generic view of a full-duplex link, subject to self-interference (SI) through electrical crosstalk (A), limited antenna isolation (B) and reflections by the environment (C). Cancellation of SI in the RX can be realized from various points in the TX.

In [3], the receiver part of a frequency agile SI-cancelling front-end was reported; its topology is shown in figure 2. A vector modulator (VM) downmixer simultaneously applies phase shifting, amplitude scaling and downmixing to a copy of the transmit signal, and subtracts it in the analog baseband for cancellation. The chosen resolution of the VM allows it to perform up to 27dB SI cancellation for a broad range of carrier frequencies from 0.15-3.5GHz; an external attenuator sets the full-scale of the canceller equal to the worst-case leakage expected from the chosen antenna solution. The mixer-first receivers are designed for high linearity to minimize RX distortion under strong SI, enabling more subsequent SI-cancellation in the digital domain.

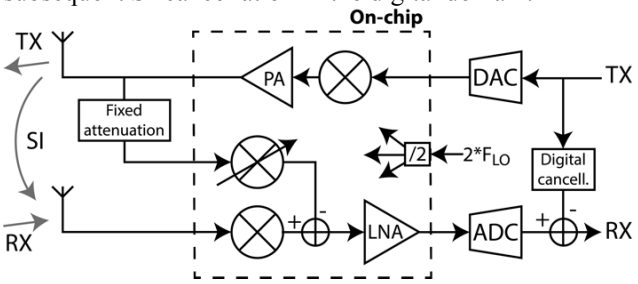

Figure 2: Topology of the SI-cancelling FD-front-end, in a system with added digital SI-cancellation. Note that TX, SI and RX occur *simultaneously* at *equal* frequencies.

In [3], up to 69dB SI-to-Noise-and-Distortion-Ratio (SINDR) is achieved at 27dB SI-cancellation in 16.25MHz. Hence the digital SI-cancellation potential is 69-27=42dB without RX noise and distortion limitation. Combined with a modest 20 dB antenna isolation, a link budget of 69+20=89dB is available at ~0 dBm TX power, enough for short-range links [3], provided that transmitter EVM and phase noise immunity are good enough [2]. This work complements the RX work of [3] and first addresses the co-integrated transmitter. Next, the phase noise benefits of clocking all three up- and down-conversion mixers from the same LO source are explored.

II. Transmitter

The implemented 65nm front-end is depicted in figure 3 and its differential transmitter structure is shown in figure 4. It consists of a four-phase sampling mixer, sampling its output on the gates of a class-A common source PA [4]. Whereas in [4], the design is promoted for FDD applications due to its low out-of-band noise potential, we

chose it for its high in-band accuracy (low 1/f noise and predictable distortion), which is important for full-duplex, as highly deterministic self-interference is more easily cancelled digitally. Choosing this transmitter architecture also has the benefit that it can be clocked with the same four-phase, non-overlapping full-swing clock signals readily available in the receiver. Frequency agile operation of both the TX and RX is possible at carrier frequencies from 0.15 to 3.5 GHz. AC-coupling between the sampling mixer and PA allows low drain / source voltages in the mixer, for reduced on-resistance. The PA is biased using a 5-bit R-2R DAC for tunable transconductance. Thick oxide cascodes enable biasing with RF choke inductors from a 2V supply (Vdd_PA).

Table I lists some key measured parameters. For 0 dBm TX power, its EVM is -40 dBc, allowing almost the 42 dB digital cancellation mentioned above. Bridging the 2dB gap by pre-distortion is part of ongoing research. The remainder of this paper discusses the more fundamental issue of phase noise.

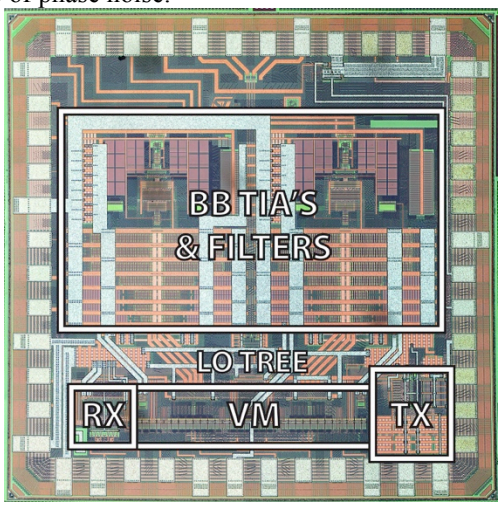

Figure 3: Chip photo of the 65nm design. The transmitter is located in the lower right of the front-end.

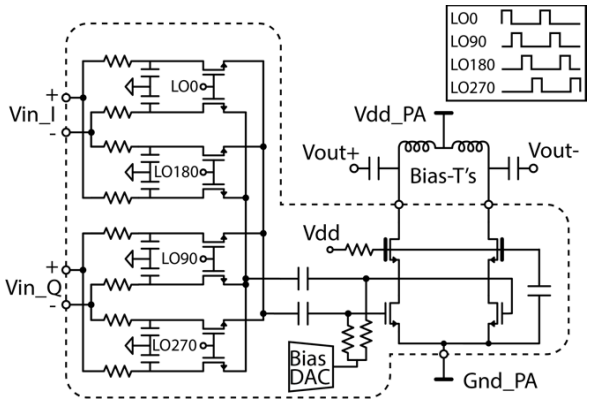

Figure 4: Transmitter topology: Four-phase sampling mixer and common source class-A PA with thick oxide cascodes. Dashed line = chip boundary. The clocks are shared with the RX.

TABLE I
TRANSMITTER SPECIFICATIONS @ 2.5 GHZ CARRIER FREQUENCY

Specification	Value
Output IP3	20.1 dBm
Image rejection ratio	38 dB (uncalibrated)
LO radiation	-49 dBm (uncalibrated)
Power consumption	108 mW from 2.0V (PA) 21 mW from 1.2V (LO)
Maximum single-tone output	12.4 dBm
Efficiency at max. output	13%
Operation frequency	0.05 – 3.5 GHz
EVM @ 0dBm 802.11a output	-40 dB

III. PHASE NOISE PERFORMANCE

Previous work on FD generally used off-the-shelf radios, specifically the WARP research platform [5, 6]. One particular topology, shown in figure 5, uses an additional upconverter chain for SI cancellation at the receiver input [6]. In [7], the authors observe that in this design, the combined amount of mixed-signal and digital cancellation never exceeds 35dB, leaving remaining SI far above the thermal noise floor. This is a result of using separate off-the-shelf radio IC's for both upconverters, each with their own PLL, generating -38dBc *uncorrelated* phase noise in the band of interest, inducing a combined noise floor of -35dBc that limits cancellation.

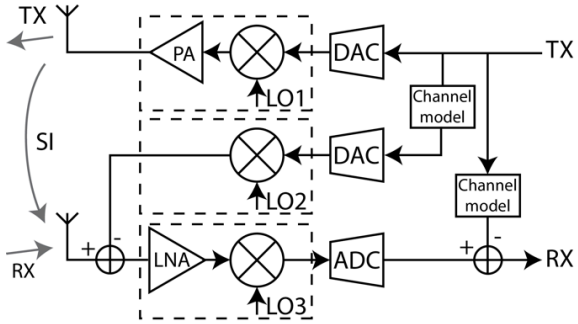

Figure 5: FD radio topology implemented in [6], using an additional upconverter for SI-cancellation at RF. All 3 up- and downconverters are separate transceivers with their own PLL.

In contrast, the integrated front-end in our work uses the same LO for the upconverter and both downconverters, which, ideally, would make the system insensitive to phase noise in the SI. We will now show that for short SI-paths, the RX noise floor is indeed hardly deteriorated by PN when using a PLL of the WARP platform. However, for long SI-paths via a reflective environment, the PN of the delayed SI becomes decorrelated from the RX clock [7]; we will evaluate this effect and examine its implications.

To exploit the maximum SINDR=69dB of our RX [3] and thus its maximum digital cancellation potential, the receiver should operate under its full 27 dB analog cancellation while receiving -18dBm SI [3]. For higher SI

powers, digital cancellation is impaired by SI-induced RX-distortion; for lower SI powers, dynamic range is limited by the RX noise floor. Hence, targeting the maximum link budget, the PN impact will be evaluated under 27dB analog cancellation of -18dBm SI at the receiver input. The remaining input-referred SI after analog cancellation will be -18dBm – 27dB = -45 dBm. The RX noise figure (NF_{DSB}) in its full bandwidth (50kHz - 12 MHz) is 11.7 dB (slightly more than reported in [3] since flicker noise is included down to 50kHz). Therefore, its input-referred DSB noise floor is -174dBm/Hz + $10*\log_{10}(24MHz)$ + 11.7dB = -88.5dBm. This leaves room for -45 - -88.5 = 43.5dB[1] of digital cancellation towards the noise floor. Therefore, the presence of e.g. -35 dBc uncorrelated phase noise between TX and RX can easily raise the noise floor and deteriorate the amount of achievable digital cancellation. The following experiments investigate if a common clock helps to prevent noise floor degradation due to phase noise present in the residual SI.

The measurement setup is shown in figure 6. Experiments were done at 2.5 GHz carrier frequency, requiring a 5 GHz LO. This LO is either generated by a generator or by an unmodulated carrier from the actual radio used in the WARP platform. The generator has better than -50 dBc PN, hardly degrading the RX noise floor, which lies at 43.5 dB below the residual SI. However, the WARP radio with its -38 dBc in-band PN is expected to significantly degrade the noise floor.

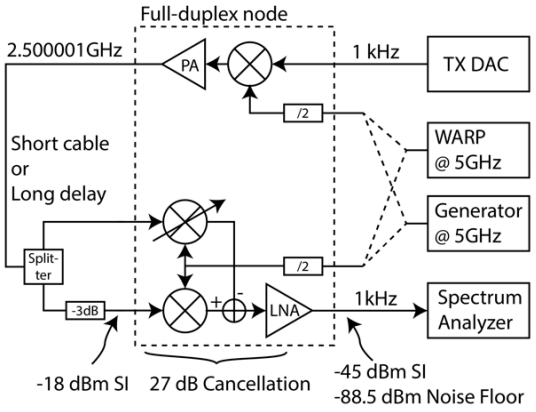

Figure 6: Simplified set-up used to measure the effect of correlated and non-correlated phase noise between TX and RX/VM, for short and long self-interference paths. The power levels are all referred to the RX input.

A very low offset-frequency single tone of 1 kHz is used from the TX. This permits filtering out TX imperfections like LO-radiation, image and distortion by AC-coupling toward the spectrum analyzer, allowing sensitive measurements of only the phase noise impact on the noise floor. In reality, such TX imperfections will also deteriorate cancellation, but since they are largely deterministic, they can be treated in the digital domain by e.g. calibration, pre-distortion and nonlinearity estimation [5], in contrast to phase noise.

Table II shows for short SI channels how the PN deteriorates the RX noise floor under cancellation, and Figure 7 shows the corresponding measured spectra. With un-correlated sources, the noise floor degrades by ~9.4 dB, and clearly shows the presence of the WARP phase noise profile. However, by virtue of correlated clocks, the noise floor is hardly affected by PN if TX and RX/VM share a single WARP clock source, but stays comparable to using a shared, low-PN generator.

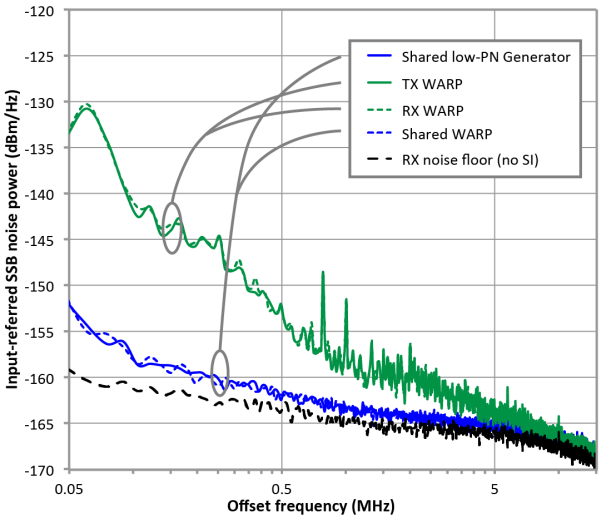

Figure 7: Measured input-referred noise spectra for the four clocking configurations with a short SI-path: A shared WARP clock shows comparable PN performance as a low-PN generator.

TABLE II
EFFECT OF PHASE NOISE ON RX NOISE FLOOR, SHORT SI PATH

TX clock	RX / VM clock	DSB noise figure	Noise floor degradation
Disabled	WARP	11.7 dB	-
Shared low-PN generator		13.0 dB	1.1 dB
Low-PN gen.	WARP	26.6 dB	9.3 dB
WARP	Low-PN gen.	20.2 dB	9.4 dB
Shared WARP		13.0 dB	**1.2 dB**

If the SI travels long distances, its phase noise may become decorrelated from that at the RX for larger offset frequencies (i.e. quick variations in LO phase), introducing a new, fundamental noise floor in the system that may limit digital cancellation [7]. An experiment was set up with an available delay line, providing again -18 dBm of SI at the RX input and 27 dB analog cancellation, but with 115ns of delay in the SI path. The results are shown in Figure 8 and Table III. The effect of PN

[1] Slightly more than the 42 dB mentioned earlier, since the influence of SI-induced distortion is omitted here for simplicity.

decorrelation is observed: clocking all upconverters from a shared WARP source does not bring the noise level down to that of a shared generator, but instead only offers 6.2 dB improvement compared to clocking one side with WARP, consistent with further analysis.

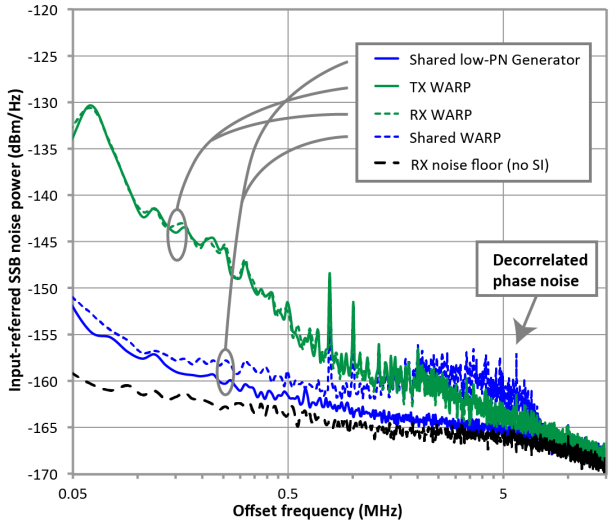

Figure 8: Measured input-referred noise spectra for the four clocking configurations with 115ns delay in the SI-path, resulting in phase noise decorrelation at high carrier offsets.

TABLE III
EFFECT OF PHASE NOISE ON RX NOISE FLOOR, LONG SI PATH

TX clock	**RX / VM clock**	**DSB noise figure**	**Noise floor degradation**
Disabled	WARP	11.8 dB	-
Shared low-PN generator		13.2 dB	1.2 dB
Low-PN gen.	WARP	19.5 dB	9.8 dB
WARP	Low-PN gen.	18.5 dB	9.5 dB
Shared WARP		15.6 dB	**3.3 dB**

However, this is a very pessimistic scenario: in a practical environment, a 115ns reflection will not return in the RX at such high signal strengths: Assuming a path-loss exponent of 2 in the SI path (corresponding to a perfect reflection against a flat metal surface), such a reflection would encounter 73.3 dB path loss. For a TX power of 0 dBm, the reflected SI would come in at -73.3 dBm, which is only 15.1 dB above the RX noise floor. Therefore, even if the phase noise were fully decorrelated, it would still be well below the noise floor. Although this is a discrete measurement point at 115 ns delay, further analysis shows that for a path loss exponent 2, no delay exists where decorrelated PN effectively raises the RX noise floor.

In conclusion, by virtue of a common clock for all mixers in the system, the phase noise arising from operation off a commercially available PLL with -38 dBc phase noise does not degrade the 89 dB link budget potential calculated previously.

IV. CONCLUSION

An integrated 0.15-3.5 GHz RF front-end with self-interference cancelling for in-band full-duplex wireless communication was described and measured. Its TX has -40dB EVM performance at 0dBm TX power, requiring only ~2dB improvement by e.g. pre-distortion to allow the full 89dB link budget potential of the system. The ability to clock the TX and RX from a shared clock offers increased immunity to phase noise compared to previous demonstrators based on WARP transceivers, allowing operation from the commercial WARP PLL with -38dBc phase noise. Decorrelation of the phase noise due to delays in the self-interference path was found not to deteriorate the system's overall link budget potential.

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