The Design of Encoding Architecture for UHF RFID Applications

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Introduction

Initially, RFID was being used to identify objects in the MIT robotics laboratory but was found to be useful for managing the supply chain [1]. The electronic product code (EPC) was then developed by the Auto-ID Center at MIT and is now being managed by EPCglobal Inc, which is a global not-for-profit standards organization commercializing the Electronic Product Code™ (EPC) and RFID worldwide. It is one important form of RFID used by retailers to manage the supply chain. EPC has standardized chip designs and protocols to enable the mass production of low-cost passive RFID tags in the 860-960 MHz range. EPC is a technology similar to the uniform product code (UPC) barcode identification used to provide information about the product. However, the EPC tag can be read at a distance and does not require line-of-sight aiming like the barcode system.

EPCglobal sought to create a single worldwide standard for the UHF RFID reader-tag air interface. This second-generation standard ("Gen 2") was developed in 2004 and became publicly available in 2005; it has also been submitted to the International Standards Organization (ISO) with the intention that it should become part of the ISO-18000 series of RFID standards, as ISO18000-6C [2]. Numerous vendors have announced upgrades for existing RFID readers, and new reader models, to support Gen 2 tags. Each RFID standard employs one modulation scheme for the Forward Link (reader-to-tag) and another for the Reverse Link (tag-to-reader).

According to the EPCglobal Gen2 standard protocol, there is a fundamental clock, known as the Backscatter Link Frequency (BLF), which specifies the pulse width of the shortest Reverse Link feature. There are then 4 permissible data encodings for the Reverse Link (tag-to-reader): FM0 (bi-phase space) baseband and 3 different Miller modulations of a BLF subcarrier. Miller-modulated subcarrier (MMS) is a more elaborate encoding. MMS provides more transitions per bit and so is easier to decode in the presence of noise, but is slower for the same tag BLF. Three different MMS schemes are available, Miller-2, Miller-4 and Miller-8. The number specifies how many BLF periods define a data symbol [3]. In this paper, The functionality of the Miller-modulated subcarrier (MMS), and FM0 encoding scheme are simulated using verilog hardware description language and implemented using FPGA technique. A comparison of the power performance of different coding architectures is also given.

The introduction of EPCglobal Gen2 standard protocol is presented in the next section. The design of encoding architecture for UHF RFID is described in Section 3. The simulation and power analysis results are provided in Section 4. Finally, we conclude the paper in Section 5.

EPCglobal Gen2 Standard Protocol

Class-1 Gen-2 tags use backscatter modulation to modulate the reader's RF carrier in the physical layer tag-to-reader link. The reader specifies the encoding format. The two formats are FM0 or a Miller-modulated subcarrier. FM0 encoding is for obtaining high read rates in

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low-noise environments and the Miller-modulated subcarrier encoding is for isolating tag responses into side channels of varying widths so that the reader can isolate responses [4]. In the reverse link (Tag-to-Reader), FM0 and three different Miller modulations methods are used for data encoding. Figure 1 illustrates the basic functions of the FM0 data coding. FM0 inverts the baseband value at the beginning of every bit period. The binary value of zero has a transition in the middle of the bit period. The binary value of one does not have a transition in the middle of the bit period [5]. A long string of FM0 data '0' symbols produces a square wave at BLF; a string of data '1' generates a square wave at BLF/2. For FM0 the data rate is equal to the BLF, and they therefore share the same allowable range, from 40 kbps to 640 kbps.

Figure 2 is the function of the Miller-modulated subcarrier. The Miller subcarrier encoding occurs a transition between two data '0' in sequence and also in the middle of a data '1' and the finally resulting waveform is multiplied by a square wave of M subcarrier cycles per bit, where M is two, four, or eight [6]. MMS provides more transitions per bit and so is easier to decode in the presence of noise, but is slower for the same tag BLF. Three different MMS schemes are available, Miller-2, Miller-4 and Miller-8. The number specifies how many BLF periods define a data symbol. For example, using the slowest BLF of 40 kHz, the data rate for Miller-8 is the BLF/8 = 5 kbps. At such a slow rate, to transmit a 96-bit EPC and 16-bit error check will take 22.4 mS, corresponding to less than 45 tag reads per second.

Encoding Architecture

According to the EPCglobal Gen 2 protocol, the two kinds of encoding architectures, FM0, and MMS are proposed. The design of FM0 encoding architecture is shown in Figure 3. The frequency divider divided the original clock signal frequency by 2, and will be processed as a clock signal to trigger the first register. And the encoder is still using the original clock signal for the trigger to conform the process of encoding can have a transition in the middle of cycle. The first register is used to save input data, after storage, data transmission will be entered into the encoder to encode. End of encoding, information will be stored in register and outputted the final result in sequence. The coding structure of MMS is similar to FM0. The frequency divider divided the original clock signal to trigger the first register which storage the input data. The encoder uses of the original clock as a trigger signal. The encoding result will be multiplied with subcarrier through XNOR gate. Figure 4 illustrates the MMS coding architecture.

Simulation Result

The coding architecture of FM0 and MMS described in previous session are implemented using verilog hardware description language. Figure 5 is the simulation results of the FM0 coding architecture. 'Clk' is the original signal to trigger encoder and the second register which saved the final results as shown on Figure 3. 'Clk_Out' is the signal which divides original clock signal frequency by 2. According to the operation principle of FM0, input pattern '11110000' will be encoded to '1100110010101010' and complete signal 'done' will be high.

In Figure 6, the simulation results conform to the operation principle of MMS. The original encoding information is presented on 'test_out'. The subcarrier signal, 'subcarrier_in', is multiplied with the original encoding information and displayed on 'out'.

The Synopsys PrimePower platform is applied to simulate power consumption with different input patterns on FM0 and MMS coding architectures. In Figure 7, there is maximum power consumption of FM0 when input pattern is '01010101_01010101', and the power is 3.367×10^{-5} W. The coding of MMS dissipated more power than FM0. When input pattern is '11111111_11111111', there is maximum power consumption on MMS M=2, 4, and 8. The power is 3.741×10^{-5} W, 3.993×10^{-5} W, 4.493×10^{-5} W, respectively.

Conclusion

Two different coding schemes including Bi-phase space (FM0) and Miller-modulated subcarrier (MMS) for Class 1, Gen 2 UHF RFID applications have been developed and correlated with the experimental results. The functionality of the Miller-modulated subcarrier (MMS) and FM0 designs are verified using verilog hardware description language. In addition, the simulation results for the power performance of these different encoding schemes are performed on PrimePower Synopsys platform.

Acknowledgments

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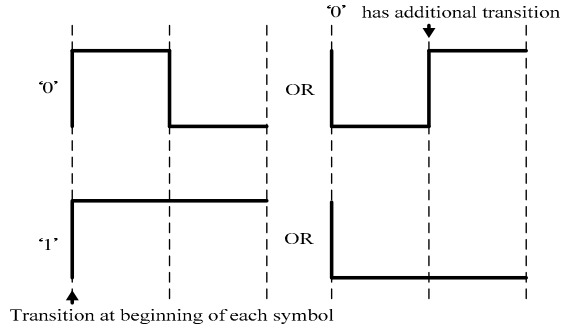

Figure 1. The Function of FM0 Coding

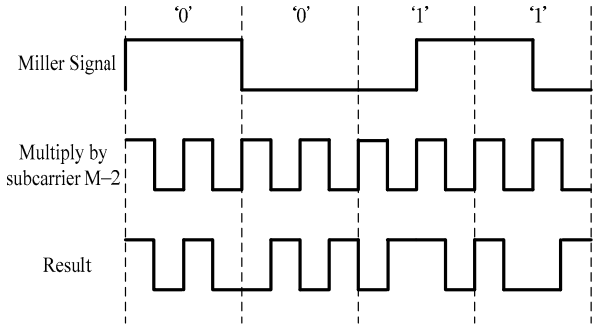

Figure 2. The Function of MMS Coding

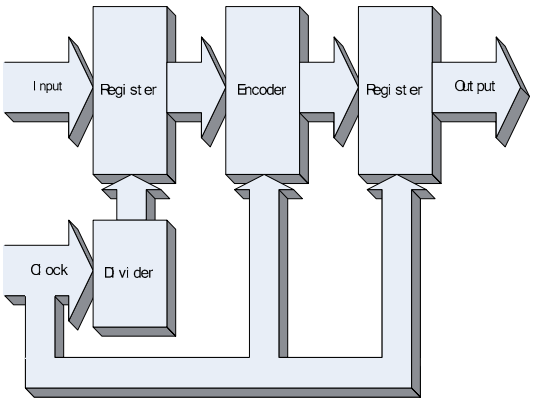

Figure 3. Data Coding Architecture of FM0

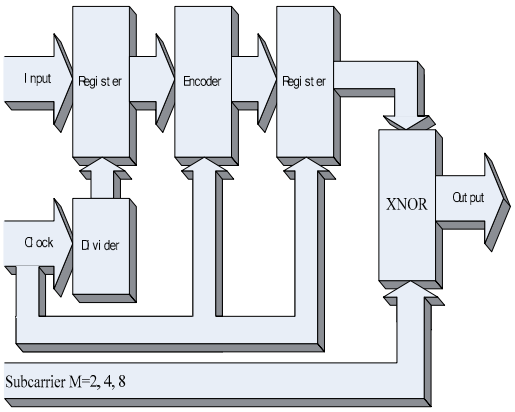

Figure 4. Data Coding Architecture of MMS

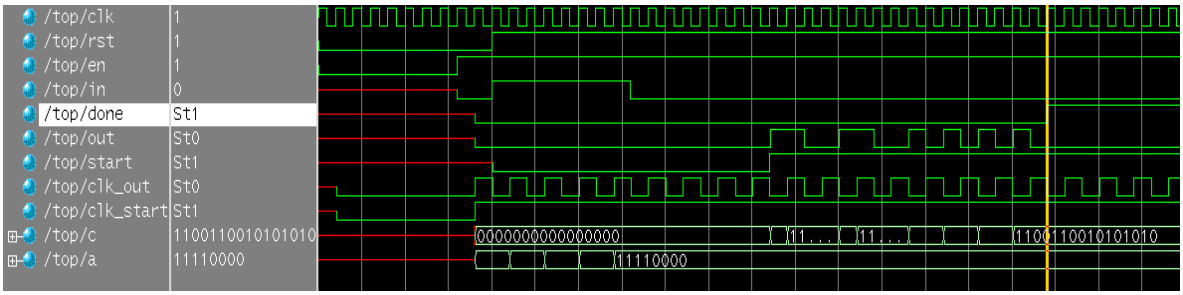

Figure 5. Simulation result of FM0

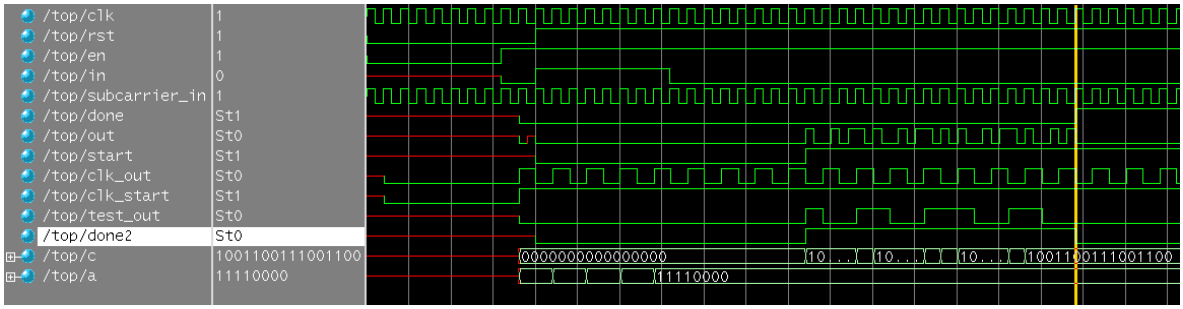

Figure 6. Simulation Result of MMS (M=2)

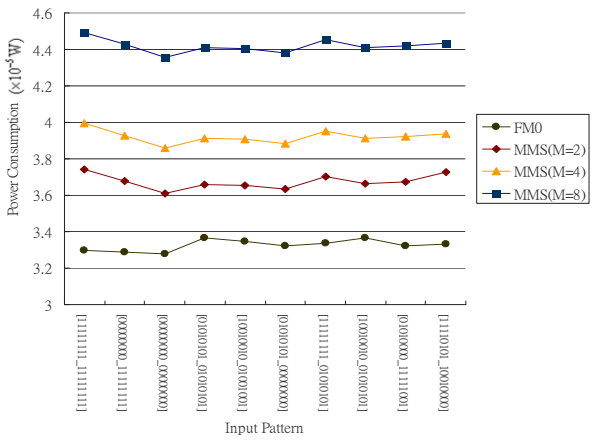

Figure 7. Power Consumption with Different Coding