

RF/Analog Self-Interference Cancellation Techniques: Challenges for Future Integrated Full Duplex Transceivers

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I. Introduction

Integration of discrete radios onto a single-silicon CMOS substrate [1]–[6], followed by commercialization of single-chip cellular, Bluetooth and WiFi radios [7]–[9], has shaped the wireless world that we live in today. Although integration of wireless transceivers with powerful micro-processors in very large System-on-Chip (SoC) are currently common place in consumer electronics, the demand for lower power consumption, higher effective data rates and higher network capacity continues to drive research on integrated radios. By some estimates, the demand for mobile data per volume area will increase 1000x over the next decade, with end-user data rates increasing by as much as 10-to-100x [10].

Numerous efforts over the last ten years have focused on methods to improve the data rate of mobile wireless devices. Research from diverse areas including communication theory, electromagnetics and circuit/device implementation techniques have shown significant progress towards increasing spectral efficiency and exploiting under-utilized spectrum to achieve higher data rates. However, these methods typically come at the expense of added radio complexity which implies higher costs and power consumption, as compared to existing systems. For example, Multiple-input Multiple-output (MIMO) radios increase throughput by exploiting spatial diversity offered by “massively” arraying transceiver elements. Millimeter wave (mm-Wave) bands above 30GHz have demonstrated multi-Gbps data rates [11] and will likely be better utilized with the evolution of 5th Generation (5G) wireless standards. However, these systems suffer from high path loss and unfavorable propagation characteristics, which implies more complex radio hardware (phased-array systems) that typically translates to higher power consumption. [12]

Full Duplex (FD) communication uses a single channel to both transmit and receive simultaneously and is another technique to achieve higher spectral efficiency, which could be used as a standalone solution, or as a way of

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complementing both MIMO and mm-Wave transceivers [13]-[15]. Compared to traditional Frequency Division Duplex (FDD) systems, which use dedicated channels to transmit and receive, FD radios combine the two channels (TX and RX) into one common TX/RX band, thus freeing up one of the two bands for another user, which ideally increases the spectral efficiency by 2x (Fig. 1). Compared to traditional Time Division Duplex (TDD) systems, where users only transmit or only receive at any given moment, FD systems increase the spectral efficiency up to 2x by transmitting and receiving simultaneously. The bands from 100MHz to 5GHz represents the most favorable characteristics for wireless communication, due to the relatively low path loss and the reasonably small size of components used to implement transceiver building blocks (antennas, LC tanks and transformers). However, these bands are completely occupied by communication applications that include emergency services (police and fire), cellular networks, media broadcast and WiFi, to name a few. The value of the bands below 10GHz was recently highlighted by an \$8billion acquisition of a 31MHz band around 600MHz frequency, by T-Mobile [16]. If FD communication could be applied to all bands below 10GHz, this would potentially translate to more than a trillion dollars in savings for carriers and end-users.

There are significant challenges when simultaneously transmitting and receiving on the same frequency, mainly the presence of a large interfering signal from the transmitter (TX) which is presented to the receiver (RX) input; this is often referred to as transmitter self-interference (SI). This self-interference will degrade the signal-to-noise ratio (SNR) at the back-end of the receiver, potentially eroding any improvement in spectral efficiency. Enabling a FD transceiver relies on cancellation techniques to suppress the TX SI. These cancellation methods find use in other applications including interference suppression in radar and cable modem systems. In fact, FD transceivers are currently used by commercially available cable modems with the advent of DOCSIS 3.1 [17].

This paper explores some of the opportunities and challenges surrounding FD transceiver implementations. Section II discusses recent advances in TX-to-RX isolation brought about by advances in air interface, RF/analog and digital cancellation subsystems found in FD transceivers. This is followed by a more in-depth look at an implementation example of a high performance two-point injection feedforward cancellation network that provides deep SI cancellation over wide bandwidth (BW) in Section III. A major challenge confronting the integration of FD radios on a single chip relates to the long delays associated with some of components of the reflected TX SI signal. This issue of TX SI cancellation for multiple delayed versions of the TX signal is explored in Section IV. This is then followed with a few concluding comments in Section V.

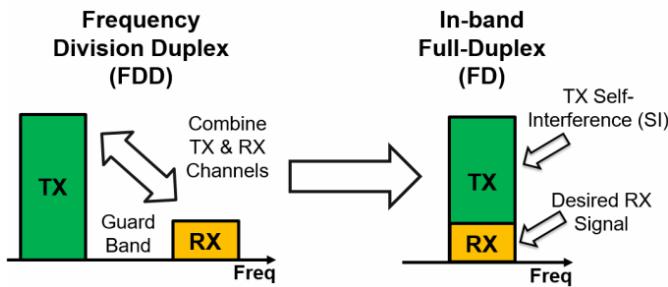


Fig. 1. Conceptual diagram illustrating the improvement in spectral efficiency in Full Duplex (FD) Communication as compared to more traditional Frequency Division Duplex (FDD).

II. Full Duplex System Overview

A key challenge in realizing an FD transceiver is the strong TX output signal which appears as an interference at the RX input of the same transceiver (

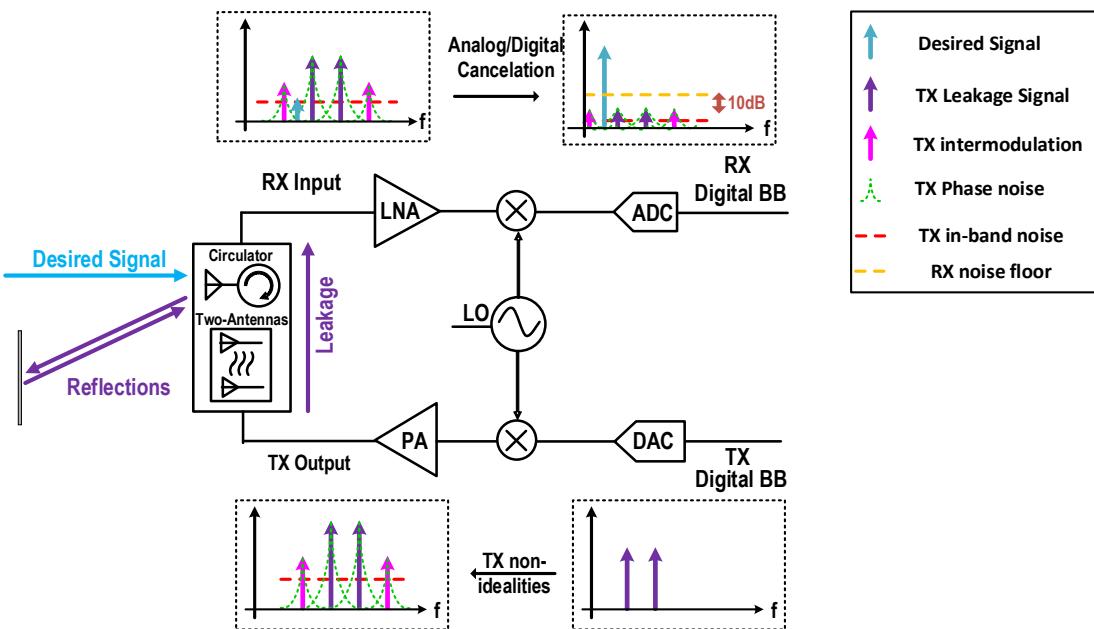


Fig. 2). Before the desired received signal is demodulated in the receiver's digital back-end, the interference should reside 10dB below the noise floor at the receiver back-end to limit the SNR degradation to 0.5dB. The SI at the TX output contains several non-idealities along with the linearly amplified and up-converted TX baseband input signal. First, the circuits used for up-conversion and amplification have a limited linearity which results in unwanted harmonics and intermodulation products in the TX spectrum. Also, the quantization noise of the TX digital-to-analog converter (DAC), in addition to the noise contributed by any active circuits along the TX signal path, contribute to broadband noise in the TX spectrum. Finally, the phase noise of the Local Oscillators (LO) used for up/down-conversion will potentially degrade the achievable SI cancellation [18].

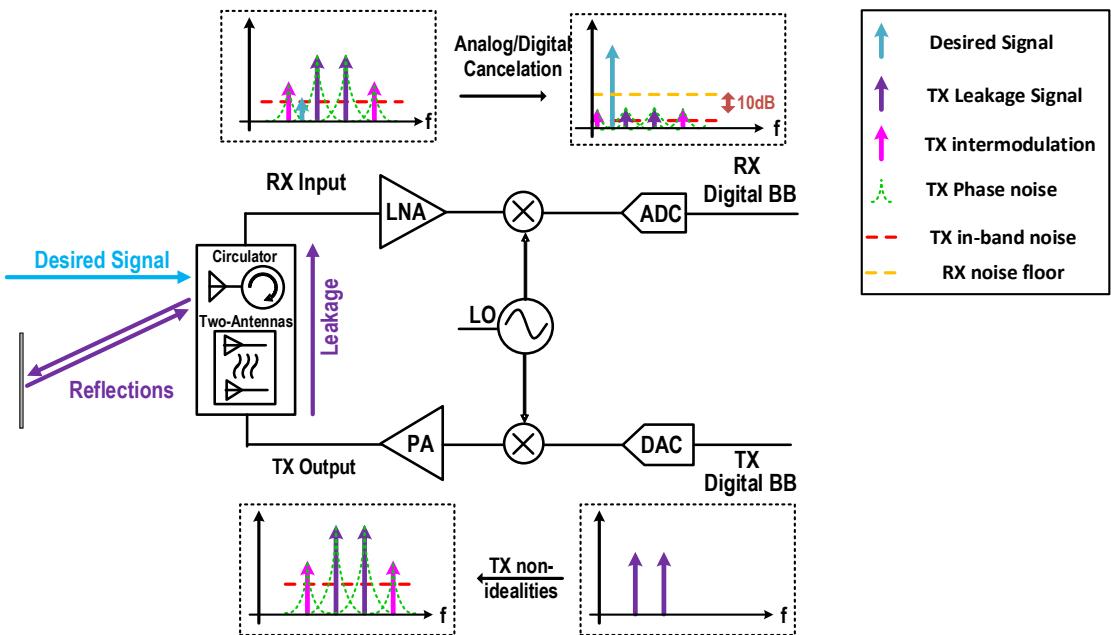


Fig. 2. TX leakage and reflections appear as self-interference in the RX of a full duplex transceiver. The SI signal and non-idealities generated in TX should be suppressed at least 10dB below the RX noise floor to have a minimal impact on RX NF.

The three basic components associated with the undesired TX Self Interference consists of, 1) the modulated carrier at the transmitter output, 2) the broadband noise generated by the TX signal path, and 3) interference generated by the nonlinearities in the transmitter resulting in intermodulation components and spectral regrowth. The flow of

TX SI in both transmit and receive signal paths is shown conceptually in

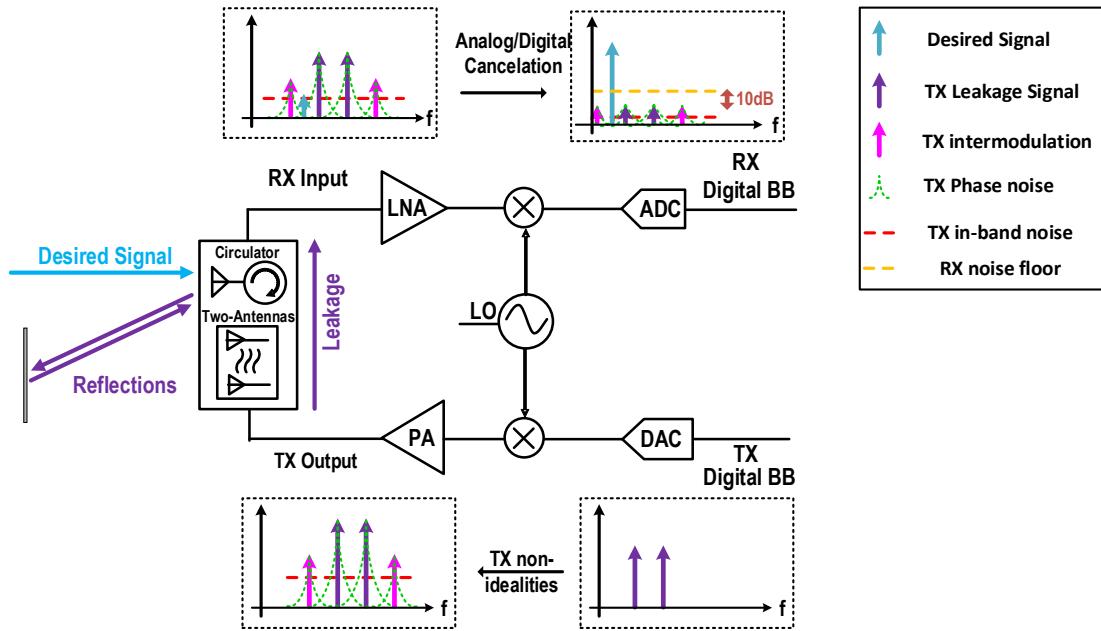


Fig. 2. To illustrate the impact of intermodulation around the carrier, two tones are shown as they pass through the transmitter and back to the receiver. This will become particularly important in future multicarrier systems where the in-band sub-carriers can inter-modulate with each other, creating distortion products around the signal bandwidth. This intermodulation then appears with both the TX noise, and the transmitted modulated signal to present a source of interference to the receiver. Thus, the challenge of TX SI cancellation is not only confined to simply canceling the modulated signal produced by the transmitter, but also the distortion and noise components generated along the TX signal path. This ultimately limits the amount of SI suppression that can be performed by using purely the digital backend as a reference source.

SI cancellation techniques can be generally divided into three domains: TX-to-RX air interface (multiple antennas, circulators and duplex filters), cancellation in the RF and analog front-end (AFE), and SI suppression using the digital back-end (DFE). Ultimately, the goal is to suppress as much of the TX SI (including the intermodulation, TX circuit noise and phase noise) before the desired received signal is demodulated at the receiver back-end. Future implementation of FD radios will likely accomplish this cancellation task by implementing cancellation functions in each of the three domains shown in Fig. 3. Each domain could contain multiple components which perform cancellation. For example, the radio AFE has multiple cancellation paths which tap off different points in the transmitter, from the baseband up to the PA output. Likewise, the output of the cancellation paths could be injected

into various points along the receiver. The radio air interface, often considered as the antenna(s) with a circulator or filter, will comfortably supply 20dB of TX-to-RX isolation before the TX SI hits the radio AFE input. From a receiver linearity performance perspective, it is better to provide some level of cancellation as close to the antenna as possible. Similarly, the origin of the cancellation path is influenced by which SI components are being suppressed. For example, if the noise and non-linearities generated by the TX are to be suppressed, the cancellation path should start later in the TX chain (ideally at the PA output). Finally, digital cancellation can be employed to suppress any residual carrier signal.

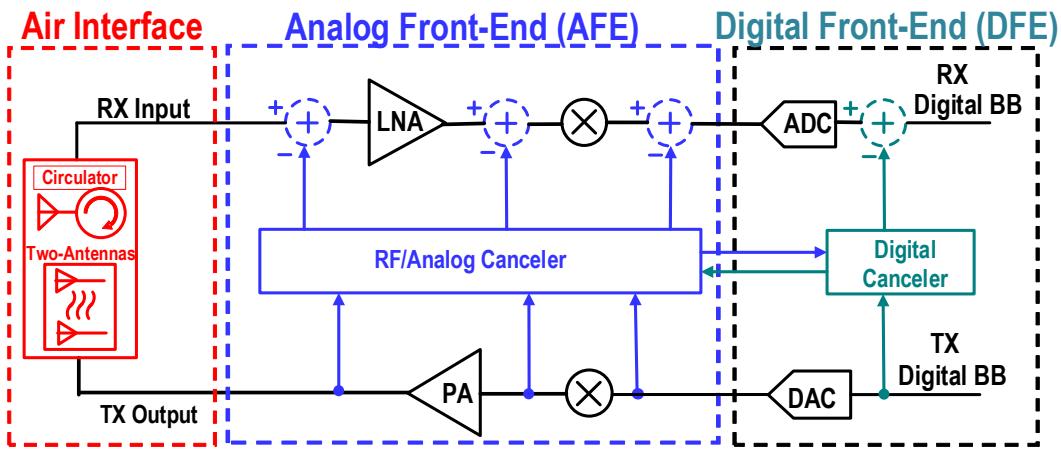


Fig. 3. Categorization of SI cancellation methods in FD transceivers: TX-RX air interface, RF and analog front-end (AFE) cancellation and digital cancellation in the digital back-end (DFE).

Different TX-to-RX isolation techniques can be found throughout the literature, e.g., two or more distanced antennas [19]-[22], dual-polarized or phased-array antennas [23]-[25] circulators [26]-[29] and electrical balance duplexers (EBD) [30]-[33] (Fig. 4). The TX-to-RX isolation in a two-antenna system depends on the antenna separation and the orientation of the antennas [34], [35]. Although using two antennas, one dedicated for the TX and the other for RX, could provide a higher TX-to-RX isolation by increasing their separation [24], this would also imply more space and a higher cost solution, which is undesirable for consumer handheld devices. An alternative strategy for the air interface of full duplex transceivers would be the use of a single antenna for both TX and RX, coupled with the use of a circulator which is a three-port device characterized by non-reciprocal paths that allows signals to flow in one direction (TX-to-antenna, antenna-to-RX, and RX-to-TX), while providing a high isolation in the reverse path (e.g. TX-to-RX, RX-to-antenna, and antenna-to-TX). As an example, ferrite circulators use magnetic materials [26] provide a wideband (>80MHz) TX-to-RX isolation with high TX power handling capability (>25dBm) and minimal

insertion loss (<0.3dB) [27]. However, these devices typically occupy a large footprint. Integrated CMOS circulators have been proposed recently which show significant promise [36]. It exploits the time-variance characteristic of N-path filters to break the on-chip reciprocity. A recent version of this device has the ability to handle +8dBm signal supplied by the TX [36].

An alternative implementation approach to realize a “circulator-like” function is an Electrical Balanced Duplexer (EBD) which is based on a hybrid transformer [32] (Fig. 4c). EBDs can be integrated with the rest of the transceiver on the same silicon substrate and show promise toward achieving very high linearity (>70dBm [37]), thus allowing their use with high-output power signals from a transmitter. However, EBDs suffer from a high inherent insertion loss [32] due to reciprocal properties which translate to a minimum insertion loss of 3dB in both the TX and RX signal paths. Also, similar to other single antenna FD systems, to maintain a high TX-to-RX isolation, the balancing impedance must be tuned dynamically in response to antenna impedance changes [38], where the tuning circuitry has the potential to degrade the linearity performance. The mentioned TX-to-RX isolation methods differ from each other in size, depth of suppression, isolation bandwidth, power handling capability, linearity and insertion loss, all of which are currently being explored by researchers in the RF community.

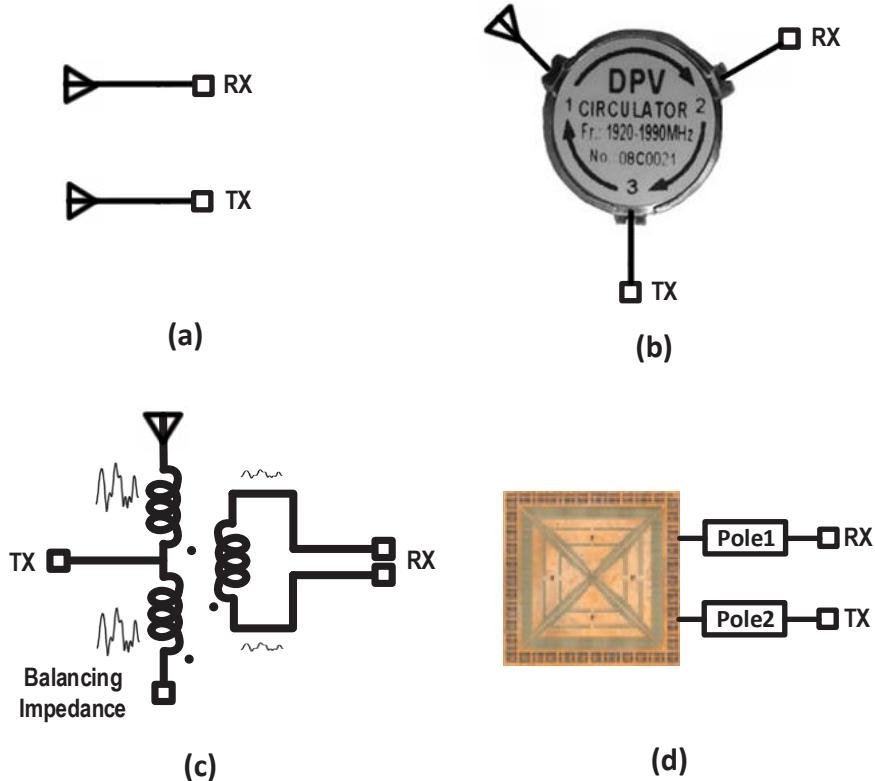


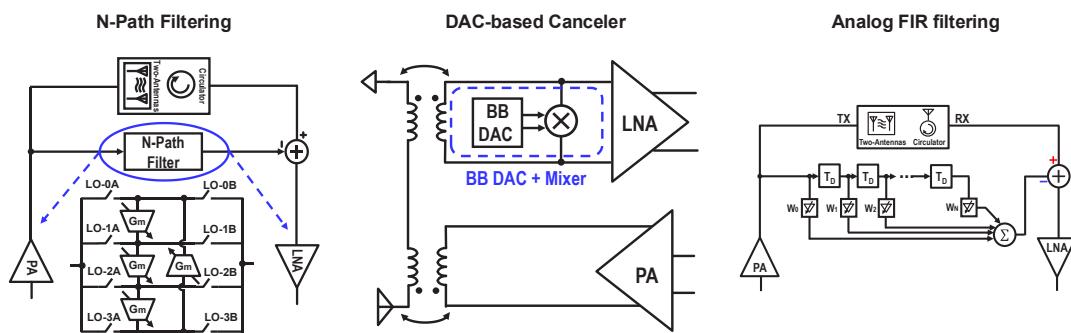
Fig. 4. Different TX-to-RX isolation methods. (a) Two antennas. (b) Circulator. (c) Electrical Balanced Duplexer [32]. (d) Dual-Polarized antennas [23]

There are a number of considerations which must be taken into account when implementing any circuitry to perform RF/analog cancellation. [39] In general, an ideal integrated TX SI canceler would possess the following characteristics:

- Introduce minimal noise in the RX signal path, particularly if the SI mitigation component is placed prior to the LNA.
 - Highly linear, especially any cancellation/filtering blocks post the PA.
 - Occupy minimal silicon area, implying minimum use of inductors and transformers.
 - Present negligible loading (high impedance) to the TX/PA output, which minimizes any output power loss and efficiency degradation.
 - Minimal sensitivity to packaging and EMI effects.

From the perspective of maximizing the TX-to-RX isolation, it is most beneficial to capture the entire TX spectrum as close to the antenna as possible (PA output) to include the modulated signal centered at carrier frequency, as well as the noise and non-linearities generated by the TX/PA. Likewise, the point of injection for the cancellation signal should be as close to the RX input as possible to reduce the required linearity and blocking performance of subsequent blocks in the RX chain. Therefore, to enhance the TX-to-RX isolation, some level of SI suppression should be performed between the TX output and RX input.

Numerous efforts have explored methods to mitigate TX leakage signals which track the SI over a broad bandwidth by synthesizing a frequency response in the cancellation path [40]. Feedforward cancelers , for example [41], [42], [29], copy the TX output and inject an amplitude-adjusted and phase-rotated signal into the RX signal path. In [22], a 2nd order G_m-C N-path filter was used to perform frequency domain equalization. An alternative method synthesizes an inverse leakage signal at the LNA input using a current DAC and up-conversion mixer [43]. However, for applications requiring high RX sensitivity, the DAC quantization noise will likely degrade the RX sensitivity. Other SI suppression techniques include passive vector modulator down-conversion mixers [44], baseband Hilbert transform equalization[45], integrated high-Q passive filters using bond-wires [46], transformer coupling [47], polyphaser filters [48], active bandpass sink filters [49], an LMS adaptive filter [50], a mixer-first FD LNA [51], harmonic-reject power amplifier to suppress out of band SI [52] and an LC phase-shift network [53]. However, these approaches typically rely on some resonant circuitry which delivers a relatively narrowband solution.



J. Zhou et al, ISSCC2015

S.Ramakrishnan et al, VLSI 2016

T. Zhang et al, ISSCC 2017

Fig. 5. Suggested techniques to perform wideband self-interference cancellation which include an N-path filter, DAC-based cancellation and analog FIR.

After TX SI cancellation is performed at the air interface and AFE, digital cancellation can be employed to further suppress the SI signal to the levels below the receiver noise floor. A sufficient ADC dynamic range is required to

capture the SI as well as desired signal, with enough resolution to cancel the former and demodulate the latter. Digital cancelers use the original transmitting data together with channel model estimates to cancel the TX residual signal in the RX baseband. These residual signals could originate from linear and non-linear parts of the TX signal, as well as signals generated in the circulator, canceler or RX due to the TX data. Several efforts achieve high digital cancellation particularly by accurately modeling the non-linearity of the TX signal path [54]-[58]. In [54], a general non-linear model which consider up to an 11th-order non-linearity of TX signal is used to achieve 48dB digital cancellation. In [55], a parallel Hammerstein model is used to address the non-linearity generated by a low-cost PA. It achieves 25dB linear digital cancellation and 8.5dB non-linear digital cancellation. In [56], three non-linearity cancellation techniques, reconstruction, auxiliary RX path and pre-calibration, were simulated for different wireless channel coherence times and compared to linear cancellation.

The achievable digital cancellation is limited by the TX and RX impairments such as TX/RX nonlinearities, DAC/ADC dynamic range, phase noise and environmental reflections. The effect of these impairments can be lumped into TX EVM which sets a high limit for achievable digital SI cancellation [24]. Note that it is impractical to cancel the TX in-band noise, TX phase noise and canceler circuitry noise only based on a cancellation signal derived from the baseband digital data, since they are independent of the baseband TX data.

In Table 1, a few commercial wireless standards have been analyzed in terms of RF/analog canceler requirements for FD operation without significant signal-to-noise ratio loss [59]-[61]. For each standard, channel bandwidth is extracted from the standard and practical numbers are assumed for the TX maximum output power and the RX noise figure. The required SI Suppression is calculated based on equation (1).

$$\text{Required SI Can} = \text{TX}_{\text{Power}} - \text{RX}_{\text{noisefloor}} + \text{Margin} \quad (1)$$

10 dB margin is assumed to calculate the values in table 1. As can be seen in the table, standards with higher TX output power and narrower channel bandwidths, require more SI cancellation. For example, cellular standards such as (LTE) require almost 140dB of SI cancellation, while Wi-Fi may demand as much as 125 dB and short-range standards such as Bluetooth only demand 115 dB of SI suppression.

Signal strength at different points along the RX chain depends on the achieved TX leakage suppression and the receiver gain distribution. To calculate linearity requirements for the TX, RX and RF canceler, achievable interface

isolation, digital linear and nonlinear cancellations and RF cancellation are assumed for an FD transceiver based on recent advances. Equations (2) – (4) are used to calculate the required linearity in terms of IIP3 for the TX, RX and RF canceler (assumed to be connected between TX output and RX input).

Required TX OIP3

$$\begin{aligned}
 &= 1.5 * TX \text{ max power} - 0.5 * (\text{Interface Isolation} + \text{RF Cancellation} \\
 &\quad + \text{Nonlinear Digital cancellation} - RX_{noisefloor} + \text{Margin})
 \end{aligned} \tag{2}$$

Required Canceller IIP3

$$\begin{aligned}
 &= 1.5 * TX \text{ max power} - 0.5 * (\text{Interface Isolation} \\
 &\quad + \text{Nonlinear Digital cancellation} - RX_{noisefloor} + \text{Margin})
 \end{aligned} \tag{3}$$

Required RX IIP3

$$\begin{aligned}
 &= 1.5 * (TX \text{ max power} - \text{Interface Isolation} - \text{RF cancellation}) \\
 &\quad - 0.5 * (\text{Nonlinear Digital cancellation} - RX_{noisefloor} + \text{Margin})
 \end{aligned} \tag{4}$$

The required linearity values in Table I are calculated based on an assumed interface isolation equal to 25dB, digital linear cancellation equal to 48dB [54], nonlinear digital cancellation equal to 20dB [54] and RF cancellation equal to 30dB [62] with the margin set to 10dB. As expected, cellular standards with higher maximum output power have higher linearity requirement compared to lower power standards. Also, it can be seen that the canceller has the stringent linearity requirement. Any non-linearity in TX output is suppressed by air interface, RF canceller and nonlinear digital cancellation in BB, so higher non-linearity levels at the TX output can be tolerated. The RX non-linearity requirement is relaxed due to the fact that the leakage signal power at RX input is suppressed by the air interface and the RF canceler. On the other hand, the signal power at the RF canceler input is very high since it is connected to PA output, and at the same time its output is connected to RX input. Thus, a modest nonlinearity generated at the RF canceler output will degrade the receiver SNR.

Table 1. SI Cancellation and linearity requirement for FD transceiver implementation of selected commercial standards.

Standard	BLE*	WiFi	GSM	WCDMA	LTE
Channel BW (MHz)	1.0	40.0	0.2	5.0	5.0
TX max power (dBm)	4.0	20.0	30.0	24.0	23.0
Assumed Rx NF (dB)	14.0	4.0	10.0	5.0	4.0
Receiver Noise Floor (dBm)	-100.0	-94.0	-111.0	-102.0	-103.0
Required SI suppression (dB)	114.0	124.0	151.0	136.0	136.0
Required Tx OIP3 (dBm)	18.0	34.0	44.0	38.0	37.0
Required Canceller IIP3 (dBm)	38.5	59.5	83.0	69.5	68.5
Required RX IIP3 (dBm)	-31.5	-10.5	13.0	-0.5	-1.5

*Power class II

+ Assumed to be connected between TX output and RX input

III. Example of Single Chip Full Duplex Transceiver

A transceiver with a dual-point injection feedforward canceler and electrical balanced duplexer is described in this section. This device achieves a deep SI cancellation (>70dB) over wide bandwidth (>40MHz) using three TX SI suppression blocks, Fig. 6.

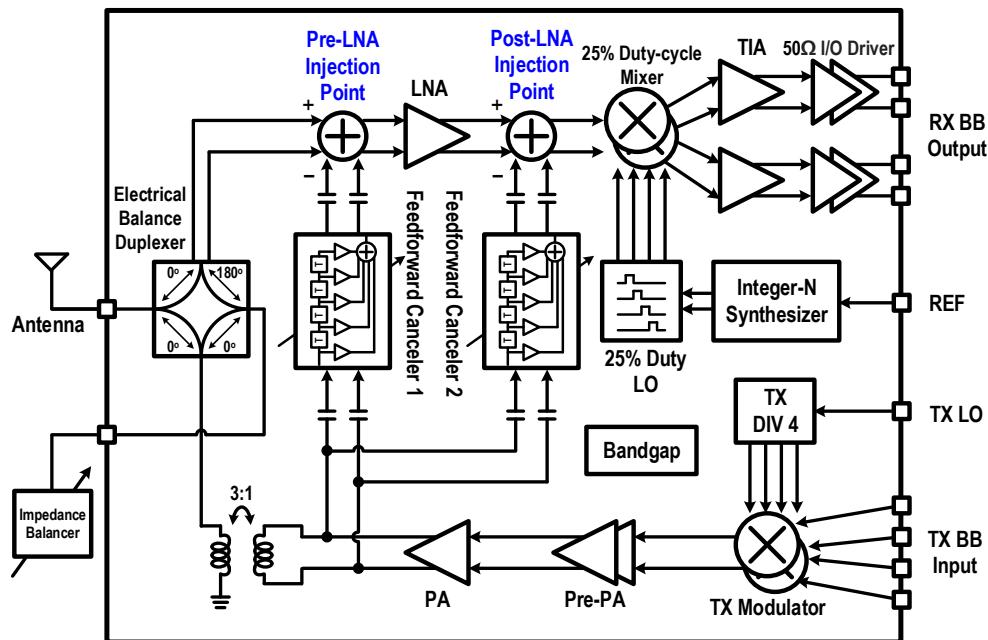


Fig. 6. Improved Dual-Injection Path Canceler with Electrical Balance Duplexer to allow both FD and FDD operation.

The first SI cancellation component that acts as the air interface is the electrical balanced duplexer, where the PA output current splits and flows into different directions toward the antenna port and impedance balancing port. The balancing impedance port should be connected to the same impedance as seen by the antenna port. Due to the

symmetry, current flows equally from the center tap in the two coils, emerging at the antenna and balance ports. The two coils generate equal magnetic flux with the opposite polarity effectively canceling each other in the secondary coil (RX side).

Two RF feed-forward analog cancelers, both of which have their inputs attached to the TX output matching network, further suppress the TX SI in the RX chain. The first RF canceler resides between the PA output and the LNA input, with the primary function of sufficiently reducing the TX SI power to prevent saturation in the RX front-end. The second RF canceler further suppress the remaining SI signal with an injection point at the LNA-RX downconversion mixer interface (Fig. 6). This relaxes the linearity demand on the RX downconversion mixers and filters in the analog BB and obviates the need for the complex I/Q auxiliary downconversion mixers and the analog FIR filters as in [29]. The filters in the RF feed-forward cancelers can be set to suppress the TX carrier and/or noise when in FDD mode, independent of the RX and TX carrier frequencies.

Each analog canceler is made up of a 5-tap analog FIR filter, where each tap includes a delay line and a variable gain amplifier (Fig. 6). Adding more taps to the FIR filter would increase the SI cancellation bandwidth, however it would also degrade the RX noise figure [63]. Passive RC-CR first-order all pass filter (APF) are used in each tap to generate the true-time delay. The variable gain amplifier (VGA) is implemented using inverter-based amplifier. Each of the VGA taps has 7-bit gain control with one additional bit that determines the signal polarity. An additional bit in the VGA will provide 6dB more dynamic range and better cancellation, however this also has the undesired effect of reducing the output impedance of the canceler by half, which loads the LNA input, thus increasing RX input insertion loss. A push-pull buffer stage was added between each tap delay to minimize the loading effects of later stages. The current outputs of different taps are summed with the AC signal coming from the RX input (Antenna) in the current domain.

The upconversion mixer, LO dividers/drivers, PA pre-driver and a class AB power amplifier form the TX chain. The RX signal path includes a Gm-based low noise amplifier (LNA) that converts the received signal into a current, a passive mixer followed by a baseband transimpedance amplifier (TIA) and An integer-N synthesizer. Both the integrated EBD and a transformer at the PA output, eliminate the need for off-chip RF components including a circulator and RF baluns. The balancing impedance is implemented off-chip for tunability purpose and to achieve a high linearity.

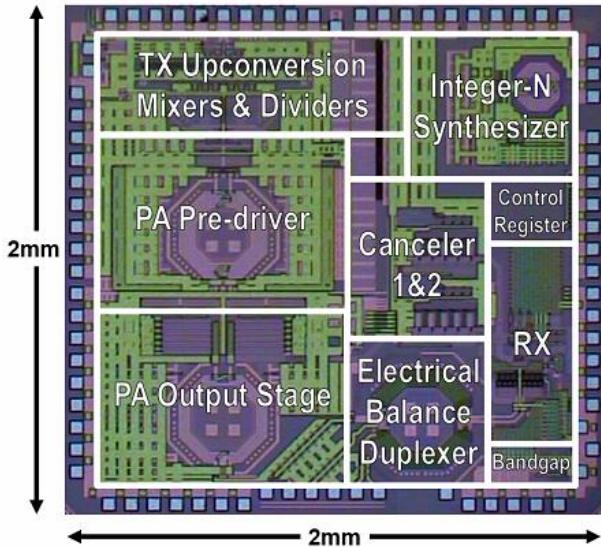


Fig. 7. Die photo of improved dual-injection path radio with EBD implemented in a 40nm TSMC CMOS process.

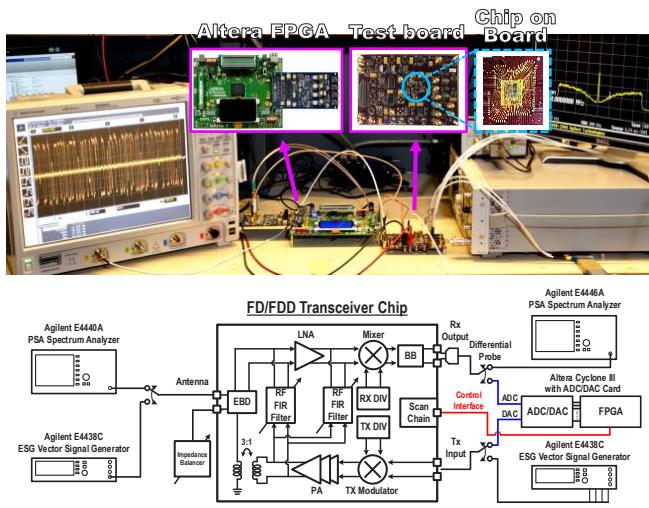


Fig. 8. Test setup which includes a FPGA board to emulate the digital baseband and perform real-time calibration.

A 1-to-3 transformer is placed after the PA, to translate the 50Ω impedance of the antenna down to 6Ω , which is the optimum resistance for the PA output. A 2-to-4 turns ratio EBD converts the single-ended input to a differential signal and provides the LNA noise matching (The LNA is implemented with a current-reuse Gm stage, which provides a current-mode output to drive the passive downconversion mixers. The feed-forward cancelers only cancel the differential mode TX SI and has no effect on any common mode leakage through the EBD. To provide a first-order

rejection of any common mode signals generated by the EBD, both PMOS and NMOS tail currents are utilized in the LNA [64].

This transceiver chip was fabricated in TSMC 6L 40nm LP CMOS process with a die size of 4mm² and consumes 106mW (w/o PA) (Fig. 7). The EBD occupies an area of 0.23mm² while both RF cancelers occupy an area of 0.12mm². To close the filter adaptation loop, an Altera Cyclone III FPGA with 14bit ADC/DACs operating at 100MHz is used to find optimal codes for the canceler weights in real time with a gradient descent algorithm (Fig. 8). The on-chip SI cancellation is tested by applying a 20/40/80MHz OFDM multicarrier 64QAM modulated signal, and 72.8/70.1/65.2dB difference in channel power (maximum 77.6dB from a single-tone sweep) is measured with an integration BW of 22/45/85MHz, respectively (Fig. 9). A more through description of this chip is given in [62], while the key data of this chip is summarized in Table 2.

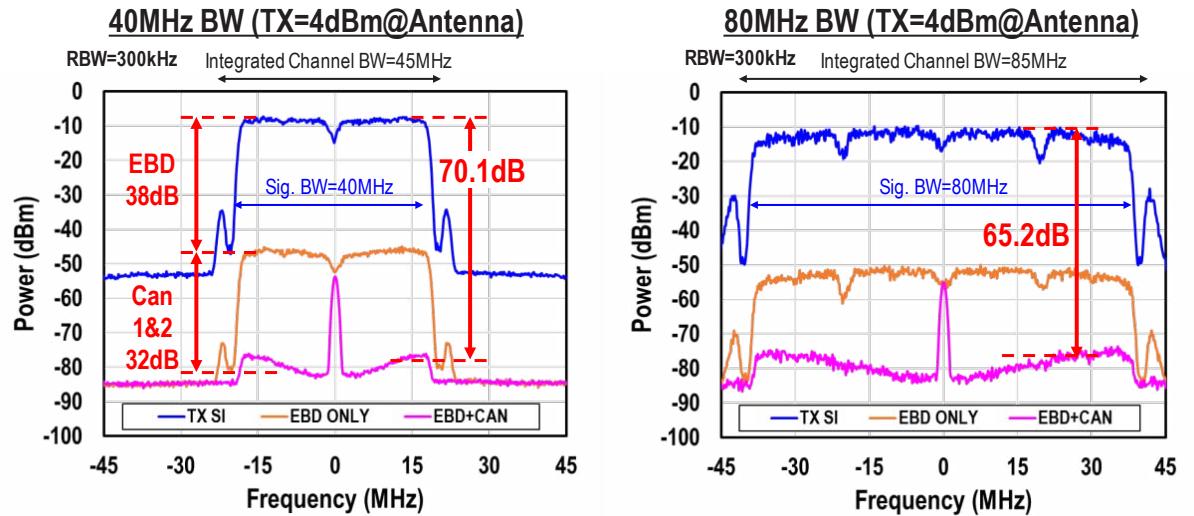


Fig. 9. Measured SI cancellation using IEEE 802.11 (OFDM multicarrier) sample packets with different bandwidths.

Table 2: Comparison of recently published Full Duplex transceivers and components, including circulators.

	S. Ramakrishnan RFIC' 2017 [43]	J. Zhou JSSC' 2015 [22]	N. Reiskarimian ISSCC' 2017 [36]	B. Liempd TMTT' 2017 [30]	I. Fabiano TMTT' 2017 [33]	V. Broek JSSC' 2015 [18]	T. Zhang JSSC' 2015 [39]	T. Zhang ESSCIRC' 2017 [48]	T. Zhang ISSCC' 2017 [29]	K. Chu ISSCC' 2018 [62]
Architecture	VM-downmixer	Frequency Domain Equalization	Duplexing LNA	EBD + SAW Filter	EBD + Rx	SIC VM-downmixer + Mixer-first RX	Transformer Coupling	Poly-phase Filter + Active Gm Stage	Dual-path + Adaptive Filter	EBD + Double-RF Adaptive Filter
Technology	65nm	65nm	65nm	0.18um SOI	28nm	65nm	40 nm	40 nm	40 nm	40 nm
Frequency Range (GHz)	0.15 - 3.5	0.8 - 1.4	0.61 - 0.975	0.7 - 1.0	1.7 - 2.1	0.15 - 3.5	1.8 - 2.4	2.4	1.7 - 2.2	1.6 - 1.9
TX SI	$\text{TX}_{\text{out-to-RX}_b}$ Iso. (dB)	N/A External Circulator	30-50 External Circulator Two-antenna	40° On-chip Circulator	50 On-chip EBD	40 On-chip EBD	25 Two-antenna	50 External Duplex Filter	20-30 External Circulator Two-antenna	30-35 External Circulator
	Total On-chip SIC Depth (dB) / BW (MHz)	64 / 20	20 / 25 (15) ^a	40 / 20	50 / 10 (SAW) 50 / 2 (EBD)	45 / 14	21 / 16	20 / 3.84	30 / 4	50 / 42
RX Gain (dB)	35	27 - 42	28	7.5	35	24	18	45	36	42
Noise Figure (dB)	3.6	4.8	6.3	7.6	6.7	10.3 - 12.3	5	4.5	4	8.0 (EBD 5.6)
SIC NF Degradation (dB)	3.4 ^b	1.1—1.5 (0.9-1.2) ^b	1.7	N/A	N/A	4	0.1	0.6	1.5	1.6
Canceler Area (mm²)	N/A	N/A	N/A	N/A	N/A	N/A	~ 0	0.015	0.349 (RF+BB)	0.12 (RF*2)
SI Circuitry Power (mW)	N/A	44 - 91 ^c	36 ^c	0 (passive)	0 (passive)	1 - 10	0 (passive)	0.25	11.5 (RF+BB)	14.3 (RF*2)
Canceler IIP3 (dBm)	N/A	N/A	N/A	N/A	N/A	21.5	N/A	15	36 (RF) / 34.5 (BB)	N/A
TX-ANT Path IIP3 (dBm)	N/A	N/A	30	58	50	N/A	N/A	N/A	N/A	N/A
Max TX Operating Power (dBm)	17	N/A	8	24	N/A	3.6	30	0	15	10
TX SI to RX LO Suppression (dB)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	10	11
Integrated TX Upconversion Path	No	No	No	No	No	No	No	No	No	Yes
Integrated PA	Yes	No	No	No	No	Yes	No	Yes	Yes	Yes
Integrated PLL	No	No	No	No	No	No	No	No	Yes	Yes
Active Area (mm²)	6.25	4.8	1.5	6.62	0.72	2	2.08	1.93	3.5	4

^a Measured with on-chip test structure. ^b Measured channel power difference with 20MHz 64QAM and 22MHz integration BW. ^c Measured channel power difference with 40MHz 64QAM and 45MHz integration BW. ^d Measured channel power difference with 80MHz 64QAM and 85MHz integration BW. ^e Averaged over 20MHz. ^f Antenna interface. ^g Calculated by the difference between system NF and RX NF. ^h Measurement with an antenna pair, 15MHz BW, 0.9-1.2dB NF deg. is with one filter, 25MHz, 1.1-1.5dB NF deg. is with two filters. ⁱ power including 0.47mW Gm cells and 44mW LO for one buffer.

IV. Future Full Duplex Radios – Confronting SI with Multiple Environmental Reflections

In a practical usage scenario, when full duplex transceivers are used in either an indoor or outdoor environment, there are multiple leakage paths from the TX output to RX input, where each leakage path has a different associated time delay. All the paths together form the total SI presented to the receiver. The first component of SI results from a direct coupling path through the board, or chip substrate. Because of the immediate vicinity of the transmitter relative to the receiver, this coupling path has the shortest delay to the receiver input, as compared to other SI components. The second large response is attributed to a quick reflection at the antenna interface, which is the result of an impedance mismatch between the antenna and its driver. The signal strength of the antenna reflection depends on the matching accuracy and varies as the antenna impedance changes due to the user interaction or environmental changes; e.g. as the handheld moves relative to the user's head, the antenna impedance varies as does the amplitude of the reflected SI. Finally, a third major component to the TX self-interference is attributed to what is commonly called “environmental reflections” which results from the TX signal reflecting off of nearby (several meters away) objects. The power, delay and channel response of these reflections depends on the propagation characteristics and the material

associated with the reflection. Although environmental reflections have lower power than the signals due to direct leakage and antenna mismatch, they could have much longer delays on the order of several hundreds of nano-seconds for a typical indoor environment [65].

To characterize the SI power as a function of time (i.e. delay), the leakage channel time delay profile should be characterized. [66], [35]. As an example, the environmental reflection power for a 0dBm signal at 2.4-2.5GHz through a discrete circulator (Meca Electronics #CS-2.500, 2.3-2.7GHz) was characterized with measurements in different environments (Fig. 10). The direct leakage path and antenna mismatch is combined together to form the first peak. There is a wide variation both in the amplitude and delay of various coupling paths including the antenna and environmental reflections. The longer delays are typically associated with the environmental reflections and naturally their power drops as their delay increases.

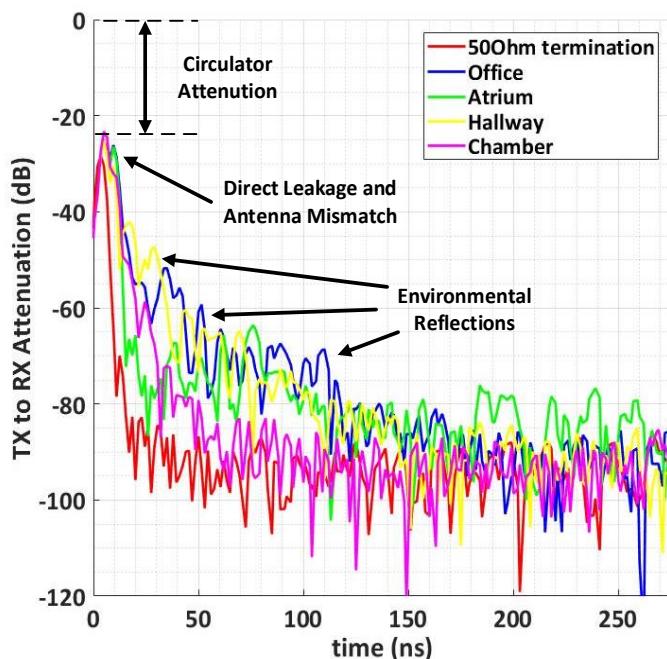


Fig. 10. Various reflections measured as a function of arrival time using a Meca Electronics #CS-2.500 circulator.

The measured attenuation over time can be used to derive the required RF/analog and digital SI cancellation as a function of time delay. The SI power at any instance of time is equal to the sum of TX_{power} and the attenuation. The required analog and digital SI cancellation is determined from the difference between the SI power and RX noise floor

plus the margin. This difference is plotted in

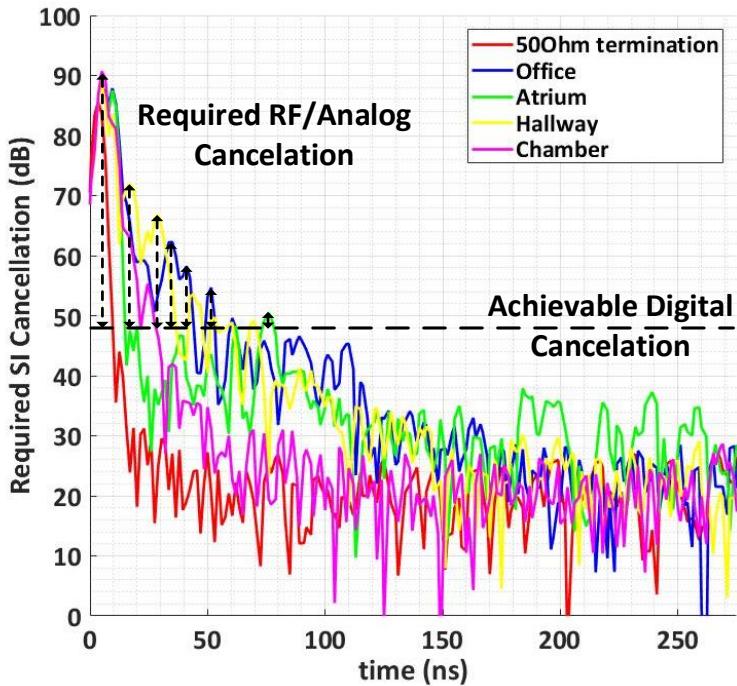


Fig. 11 for a TX power of 10dBm and a RX noise floor of -94 dBm. The required analog and digital cancellation is more than 90dB for leakage signal and drops for signals with longer delays.

$$\text{Required SI Can}(t) = \text{TX}_{\text{Power}} + \text{Attenuation}(t) - \text{RX}_{\text{noisefloor}} + \text{Margin} \quad (5)$$

In the digital domain, longer delays can be synthesized easier than in the analog domain by simply holding values in a digital memory. Therefore, delayed SI signals with longer delays are easier to address in digital domain. However, as discussed in section II, the maximum achievable digital cancellation is limited by TX/RX non-idealities. To achieve a delayed-SI cancellation beyond what is possible using the radio digital back-end, some level of cancellation in the AFE must be employed. The required AFE cancellation can be calculated by subtracting the achievable digital cancellation from the total required cancellation, assuming that the maximum cancellation which can be achieved by

the radio's digital baseband is 48dB [54] and the suppression is independent of time (

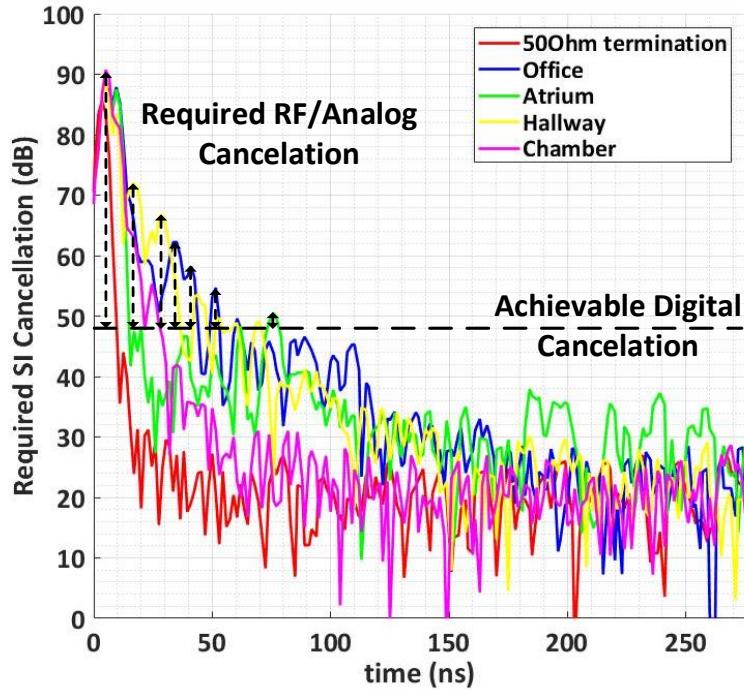


Fig. 11). Higher digital cancellation would relax the required AFE cancellation, given the condition that the receiver front-end does not go into saturation. The AFE described in Section II mainly targets SI resulting from short-delay reflections that have a higher power associated with them. However, the SI due to longer delayed environment reflections are more challenging to address in the AFE; mainly because synthesizing a longer delay on chip is less practical to implement.

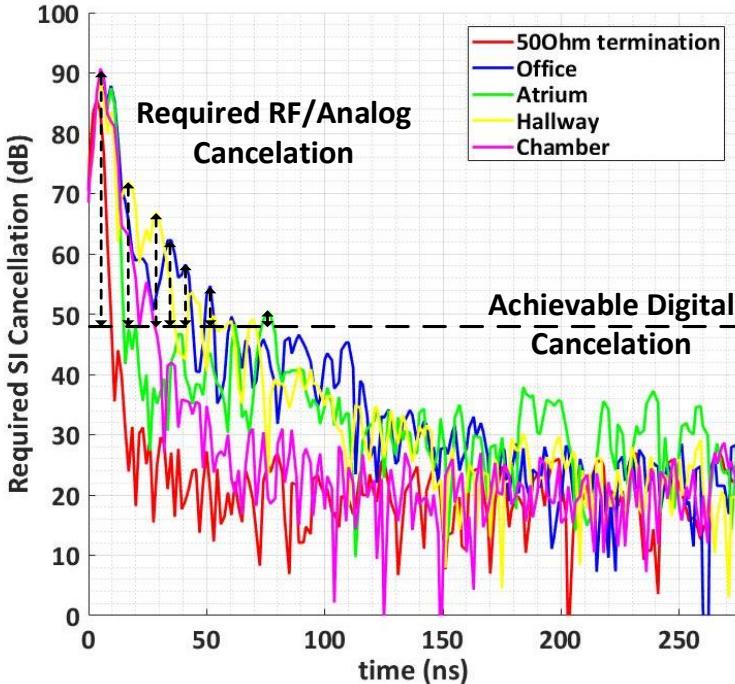


Fig. 11. Required SI cancellation for a transceiver with 20dBm TX output power and -94dBm sensitivity using the Meca Electronics #CS-2.500.

As mentioned in Section II, both the RF and the analog cancelers match the SI delay and amplitude, before injecting a cancellation signal in the RX signal path. So, the power or delay mismatch between the canceller path and the SI would decrease the AFE cancellation. To investigate the effect of delay mismatch, a model as shown in Fig. 12 is simulated. This model uses a single delayed (τ_e) version of TX output as the SI, while the canceler is a weighted sum of two fixed delays equal to τ_f and $\tau_f + T_c/4$, where T_c is the carrier period. The weights w_1 and w_2 are truncated to 12 bits and the input signal has 1/5/40MHz channel bandwidth centered at 2.4GHz. It can be seen in Fig. 12b that this *single-tap* architecture with two fixed delays, separated in time by 104ps, can provide 20/12/6dB cancellation for the 40MHz modulated SI with 2/5/10ns delay mismatch. The SI cancellation drops as the delay mismatch and signal bandwidth increases, i.e. the SI cancellation is inversely proportional to the ratio of delay mismatch over symbol time. This result is intuitive since delay mismatch over symbol time ratio determines the portion of time that both SI signal and canceler signal convey the same symbol information. The case of multi-tap cancelers and multiple delayed SI signals is examined in more detail in [67].

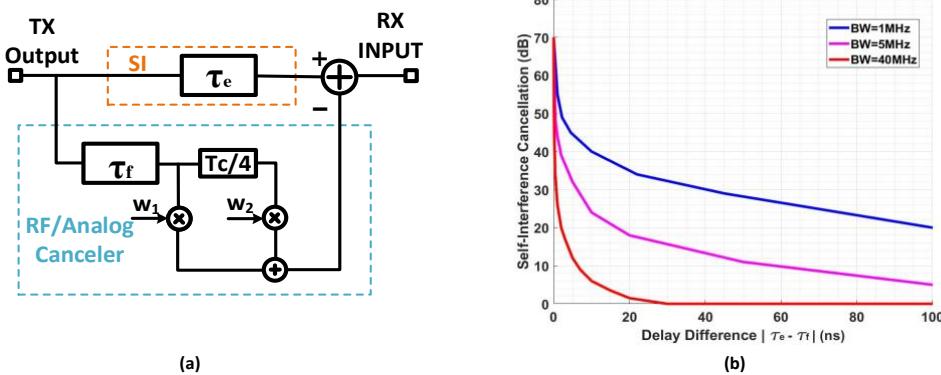
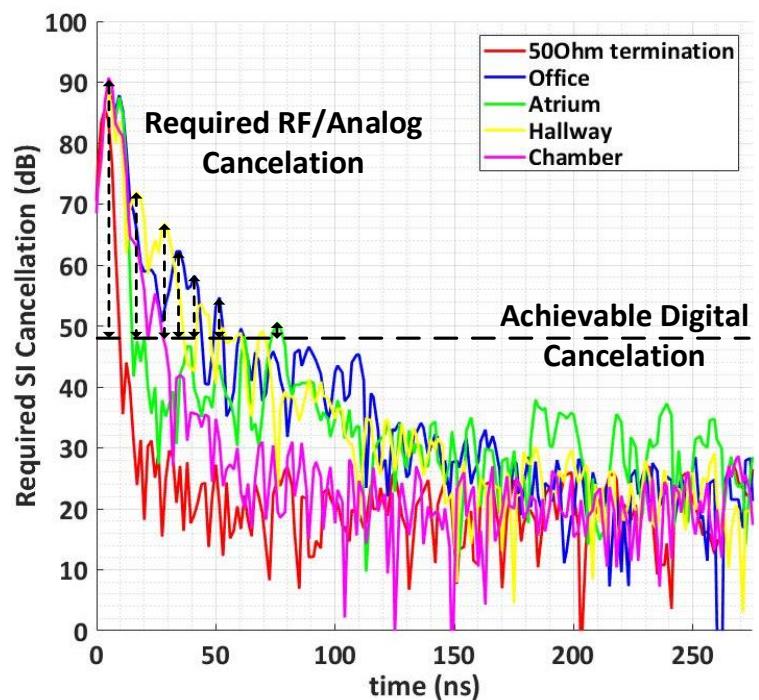


Fig. 12. (a) Block diagram of a single tap analog canceler with two fixed delays. (b) The effect of delay mismatch on SI cancellation for the analog canceler in (a).

For a 40MHz signal in Fig. 12b, the SI cancellation from the single-tap analog canceler falls faster than the



required AFE SI cancellation shown in

Fig. 11. Thus, a single tap canceler fails to achieve the required analog cancellation for every delayed SI. Instead, a multi-tap AFE canceler with different τ_f for each tap must be employed (Fig. 13.a). The total achievable analog and digital cancellation by the multi-tap system is shown conceptually in Fig. 13.b (black curve) where multiple copies of cancellation achieved with a single-tap canceler are added together and used to provide enough cancellation for a broad range of time delays. The τ_f associated with different taps are positioned in time to force the valleys of total cancellation contributed between each tap, to be above the desired cancellation (blue curve in Fig. 13). As mentioned

before, the required SI cancellation versus time is changing, i.e. more SI cancellation is required for stronger leakage with shorter delays as compared to SI with longer delays. From Fig. 13, it becomes self-evident that the time delays associated with various delays (differences in τ_f) are not uniform.

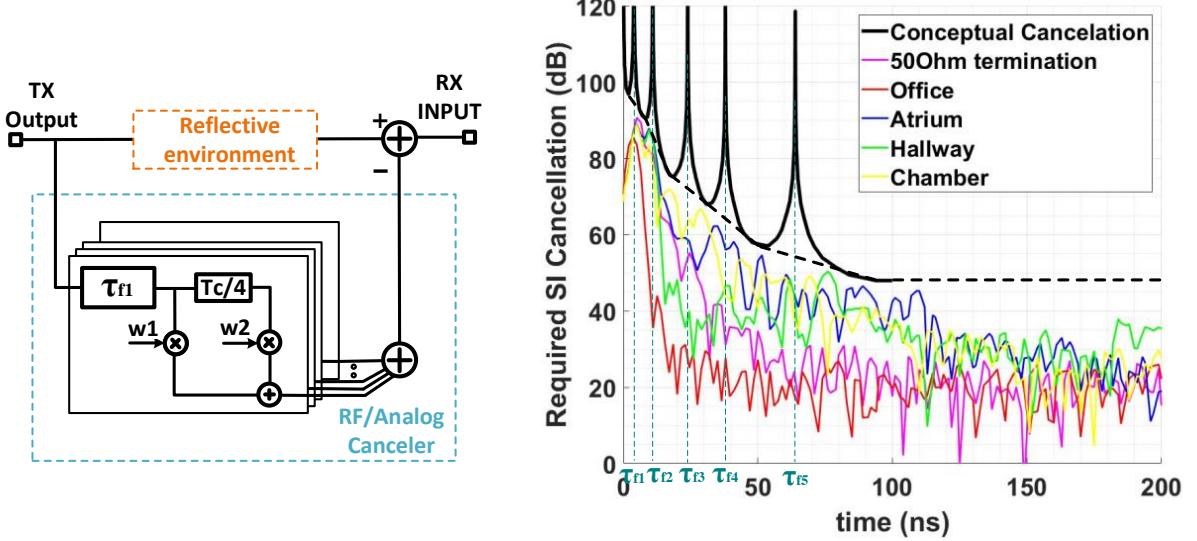


Fig. 13. (a) Multi-tap RF analog canceler with different τ_f associated with various taps. (b) Conceptual achievable SI cancellation for environmental reflection signals by using multi-tap AFE and DFE cancelers.

The need for a multi-tap RF/analog canceler with delays as long as tens of nano-seconds, highlights two challenges for future integrated FD transceivers. The first challenge relates to the implementation of long delays on chip. [54], [55] use PCB traces and/or cables to generate multi-nano-second delays which are impractical for integration on chip because of the physical component sizes. In [68] and [69] a Gm-C all-pass filter and LC delay lines are used respectively to generate sub-nano-second delays at GHz frequencies. However, the achieved delay (sub-nano-second) is far from the estimated requirement of 100ns. Switched capacitor circuits could be used to generate longer delays in analog domain [70], but non-idealities such as charge sharing, clock feed-through and noise must be addressed carefully. The second challenge relates to finding the optimal weights for different taps of the RF/analog canceler which produce an optimum cancellation in real time. As the number of filter taps required to cover a broader range of environmental delays increases, so does the number of weights associated with each tap. Thus, this makes the calibration of the AFE filter coefficients increasingly more complex and is becoming one of the grand challenges of future FD radio design.

V. Conclusion

This paper presents an overview of methods for TX SI cancellation towards FD integrated radios. An example of an integrated transceiver with 70dB SI cancellation over 40MHz bandwidth was described and shows promise with respect to achieving the level of performance required for FD operation, compatible with some commercial standards-based radios. The challenges presented by environmental reflections in a FD system and the SI cancellation requirements for longer delayed self-interference was explored. Although advancements have been achieved with respect to realizing integrated, single-chip Full Duplex radios, there are still significant problems which remain to be solved, particularly with respect to providing a comprehensive end-to-end receiver solution that includes SI suppression from the air interface to the radio digital back-end. RFIC design for new radio SoCs that include numerous techniques to improve power and spectral efficiency, will likely keep designers engaged for years to come!

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