AMD Versal™ Adaptive SoC: Introduction

2023.2

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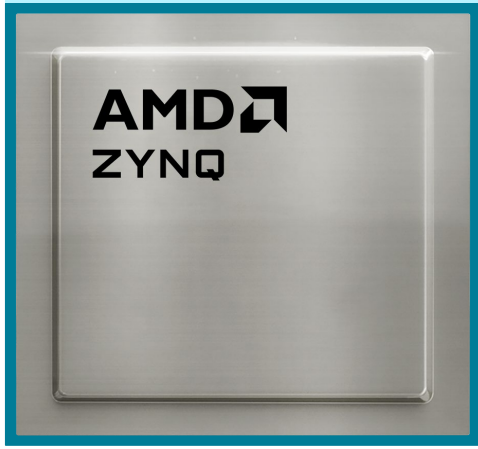
AMD Adaptive System on Chips (SoCs)

Select the right SoC from AMD's scalable portfolio

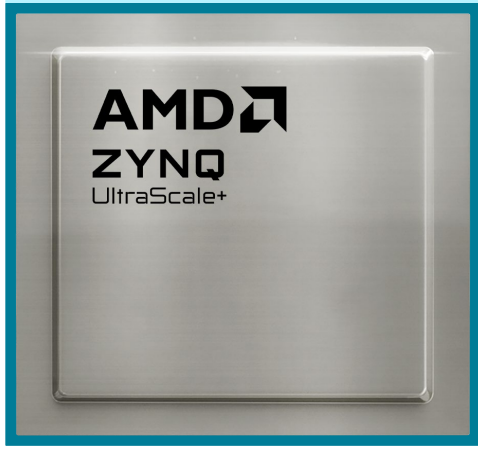
Zynq™ 7000 SoC



Cost-optimized scalable SoC platform

- Single or dual Arm® Cortex®-A9 cores
- 28nm 7 series programmable logic
- Up to 12.5G transceivers

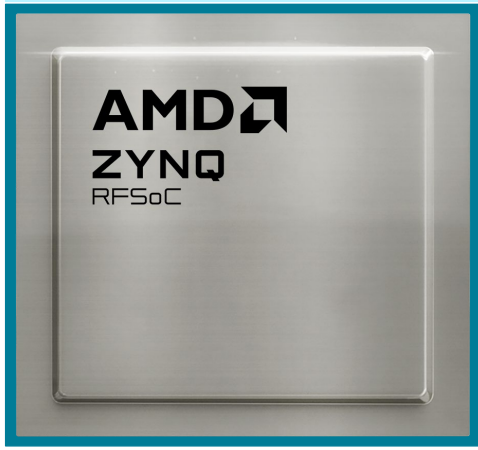
Zynq UltraScale+™ MPSoC



Industry's first heterogeneous adaptive SoC

- Dual or quad Arm Cortex-A53 cores
- Dual Arm Cortex-R5F core
- 16nm FinFET+ programmable logic
- Arm Mali™-400MP2 GPU
- H.264/H.265 video codec

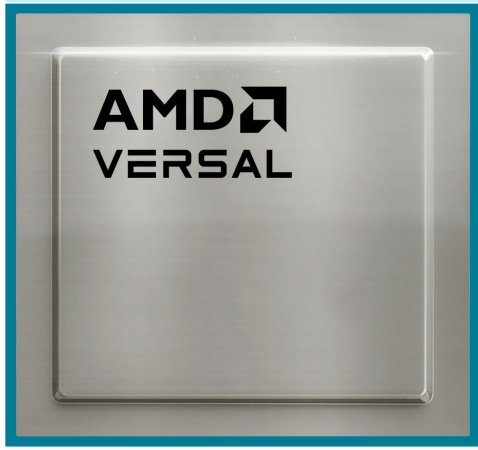
Zynq UltraScale+ RFSoC



Industry's first single-chip adaptive radio platform

- Quad Arm Cortex-A53 cores
- Dual Arm Cortex-R5F cores
- 16nm FinFET+ programmable logic
- Digital RF-ADC, RF-DAC, SD-FEC

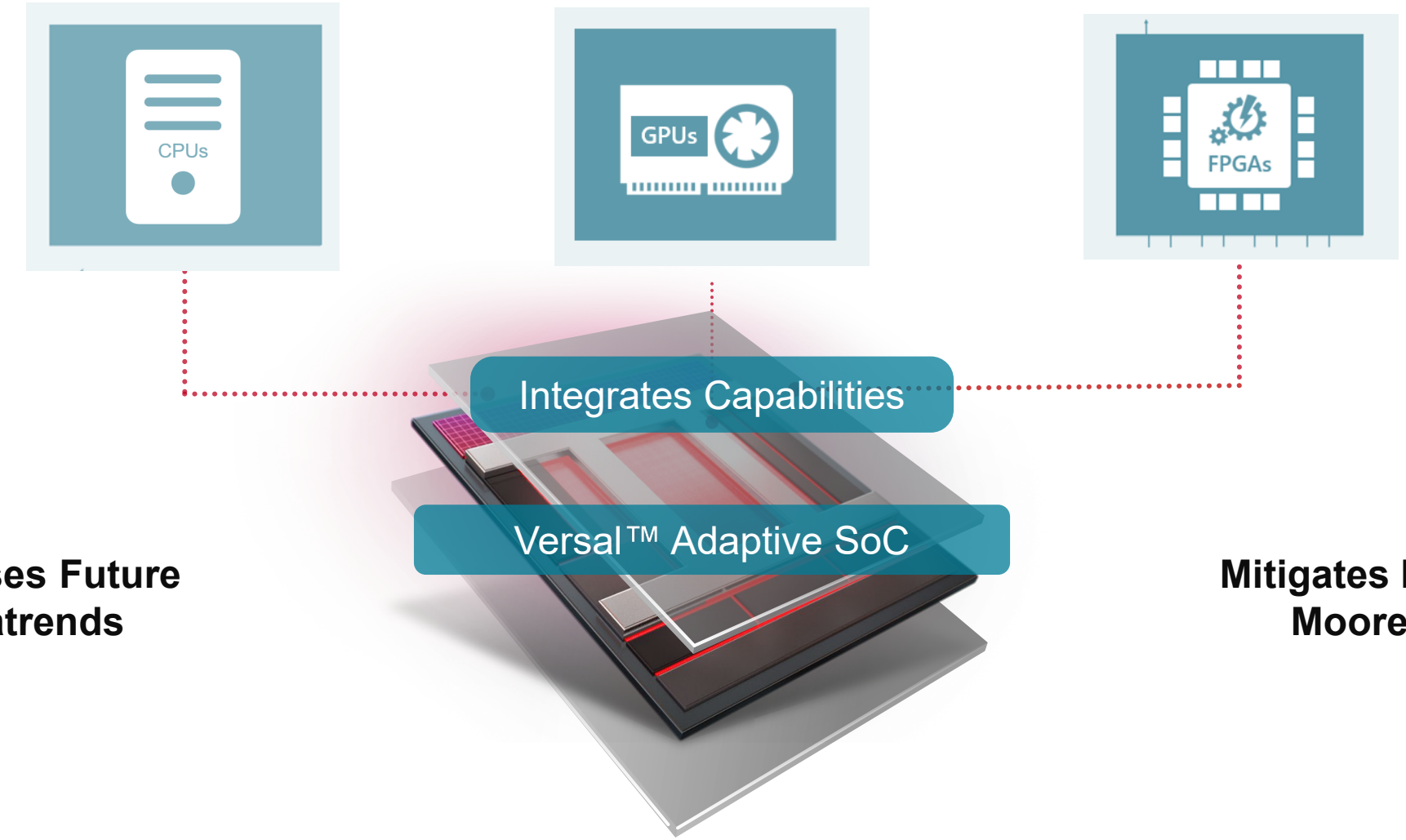
Versal™ Adaptive SoC



Adaptive SoC

- Dual Arm Cortex-A72 cores
- Dual Arm Cortex-R5F cores
- 7nm programmable logic
- DSP and AI Engines
- Programmable network on chip (NoC)

Versal Adaptive SoC



Addresses Future Megatrends

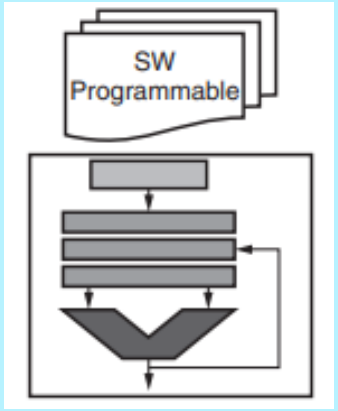
Mitigates Failures of Moore's Law

Heterogeneous Compute Architecture

Versal Adaptive SoC – Motivation

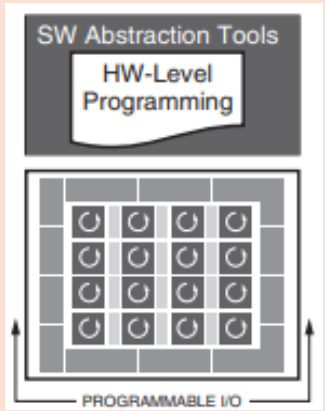
Versal adaptive SoC
✓ Delivers the best of all three

CPU



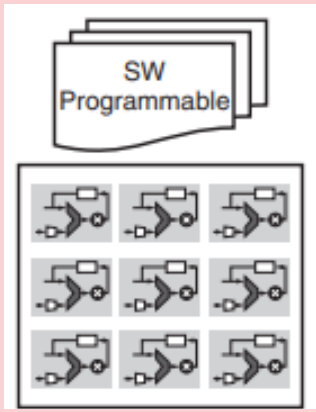
- Scalar, sequential processing
- Memory bandwidth limited
- Fixed pipeline, fixed I/O

FPGA



- Flexible parallel compute
- Fast local memory
- Custom I/O

Vector Processor



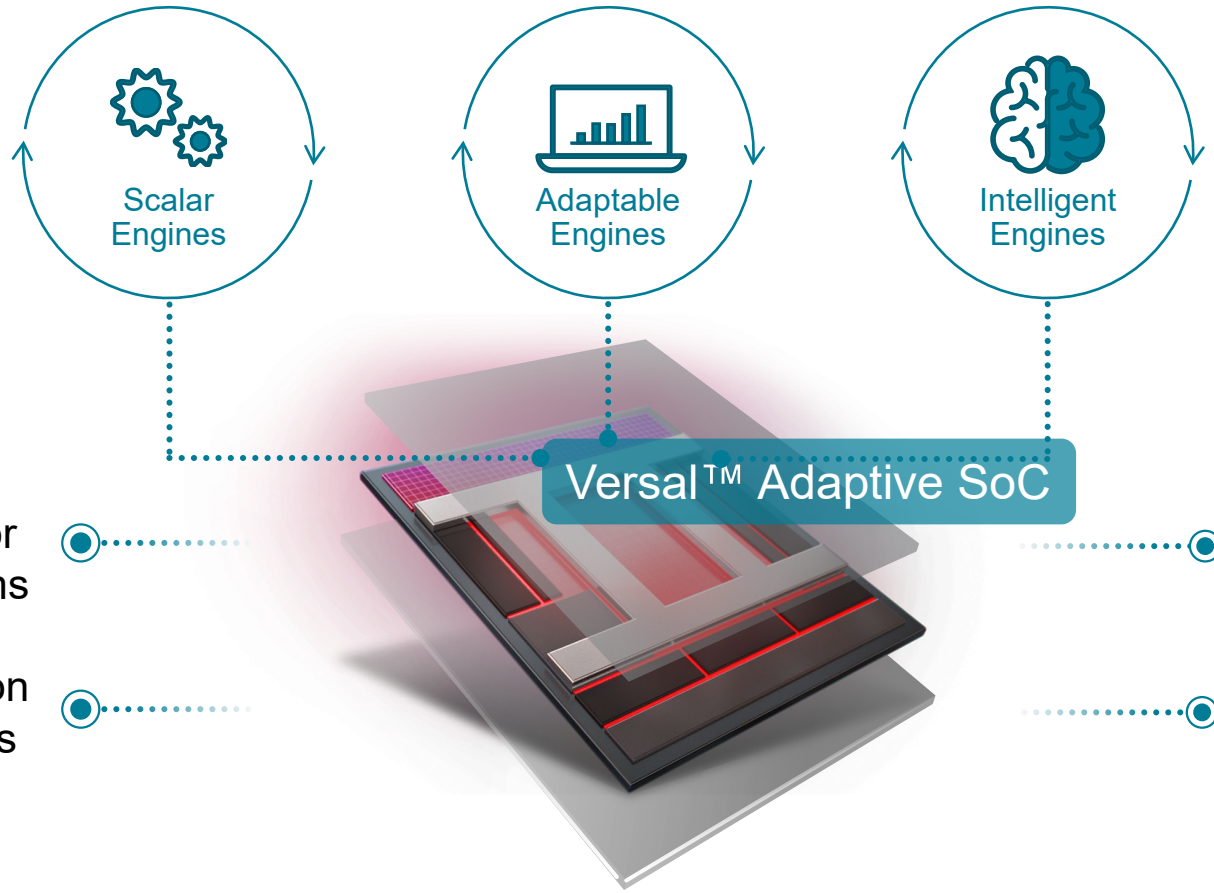
- Domain-specific parallelism
- High compute efficiency
- Fixed I/O and memory bandwidth

Scalar Engines ⟷ Adaptable Engines ⟷ Intelligent Engines

Integrated Software Programmable Interface

Heterogeneous Software Programmable Interface

Versal Adaptive SoC



- Customizable Memory Hierarchies
- NoC to Move Data
- Future Proof for New Algorithms
- Support for Common Standards
- Single Heterogeneous Platform for HW/SW Engineers
- Frameworks, Libraries, SW, Runtime Stack

Enables programming and optimization by data scientists and software and hardware developers

Versal Adaptive SoC

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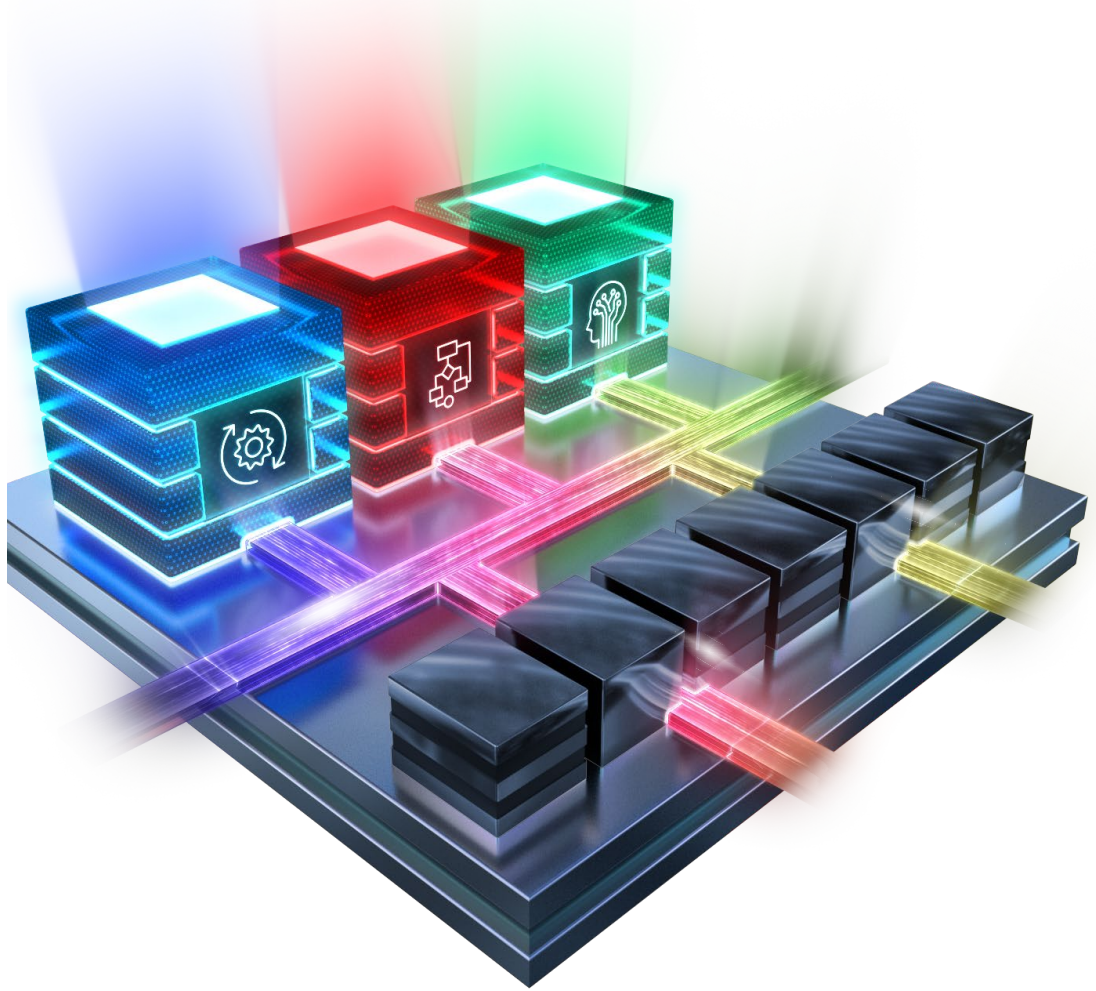
VERSAL

- Heterogeneous acceleration
  - For any application
  - For any developer
- TSMC 7 nm FinFET
  - Software programmability and domain-specific hardware acceleration with adaptability
- Six series of devices
  - Scalability and AI inference capabilities for diverse applications



Versal Architecture: Overview

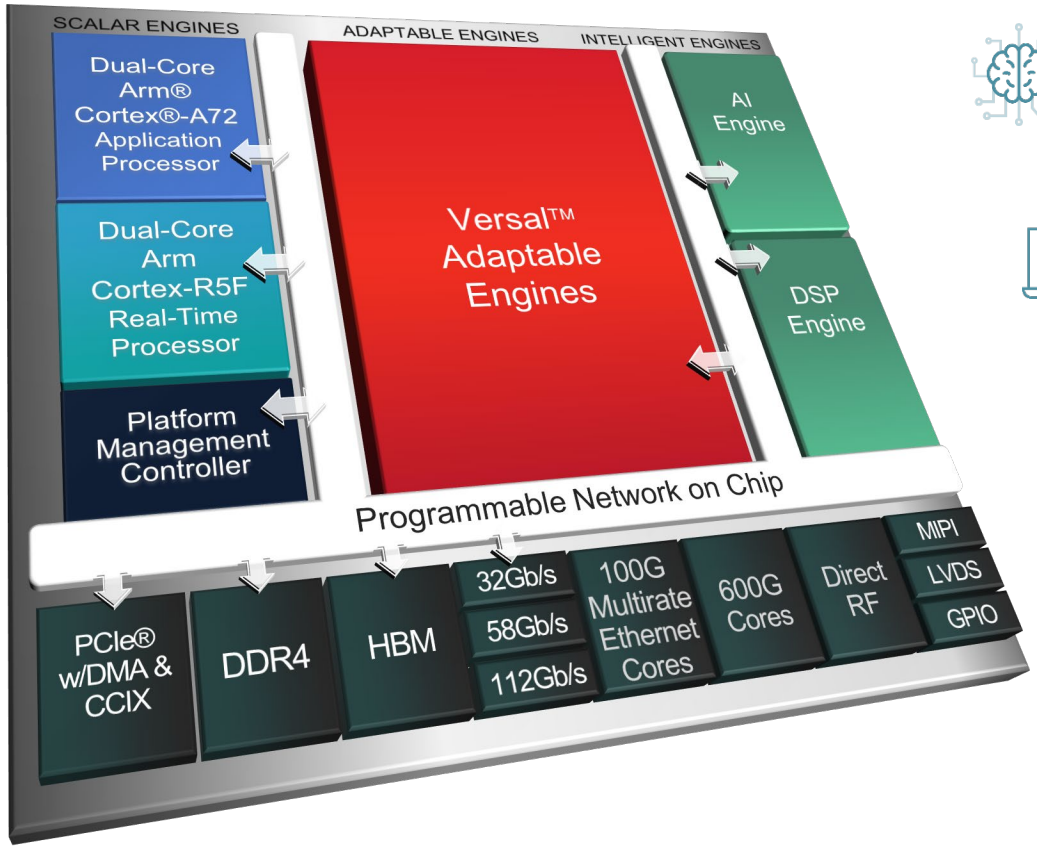
Adaptable Engines
- High compute density
- Voltage scaling for perf/watt

Scalar Engines
- Platform control
- Embedded edge compute

PCIe Gen5 & CCIX
- High PCIe and DMA bandwidth
- Cache coherency

DDR4 Memory
- 3200-DDR4, 4266-LPDDR4
- High bandwidth/pin

Transceiver Leadership
- Broad range, 32G → 112G
- 58G in mainstream devices



Intelligent Engines (DSP)
- AI compute
- Diverse DSP workloads

Programmable NoC
- Guaranteed bandwidth
- Efficiently moves data among portions of devices

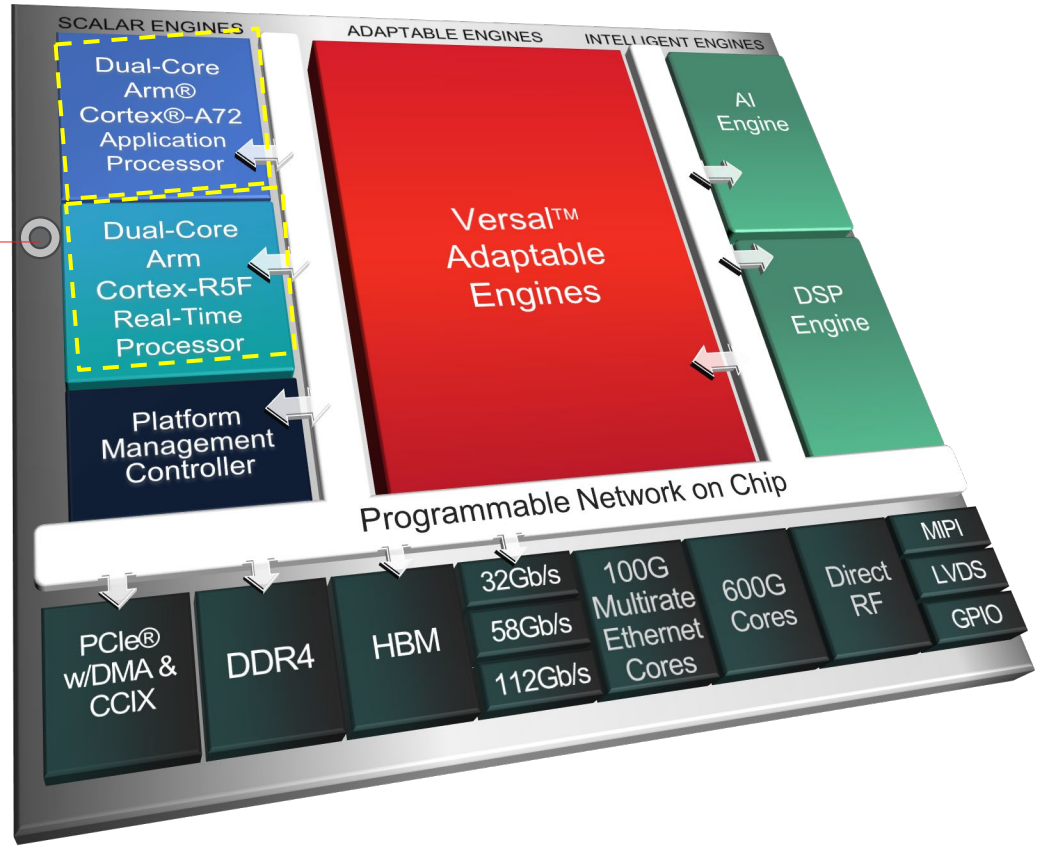
Protocol Engines
- 400G/600G cores
- Power optimized

Programmable I/O
- Any interface or sensor
- Includes 3.2Gb/s MIPI

Scalar Engines

Scalar Engines for Platform Management

- Execute complex algorithms and decision making
- Provide safety processing and redundancy for mission- and safety-critical applications
- Manage the entire platform
- Load each aspect of the Versal device and monitor status
- Support capability extension
  - PL-instantiated MicroBlaze™ processor



Scalar Engines

Application Processing Unit (APU)

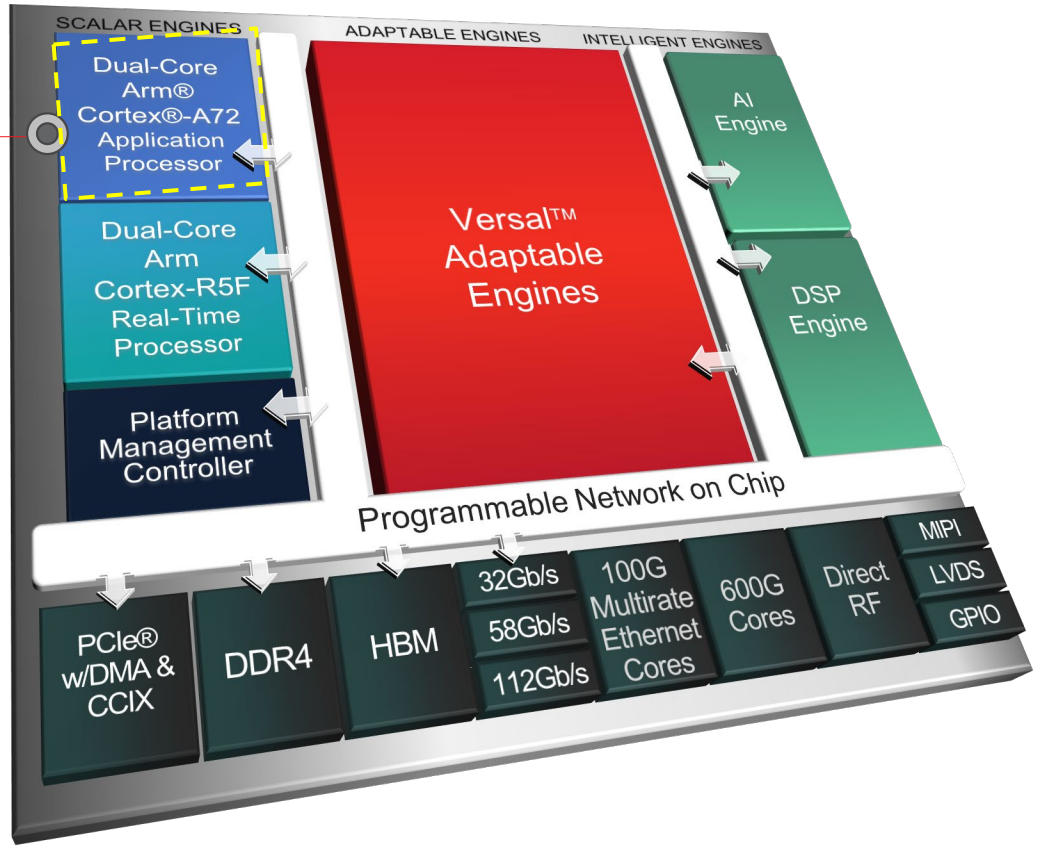
Based on Arm Cortex-A72 dual-core processor

- System memory management unit (SMMU)
- Cache coherent interconnect (CCI) unit
- Interface channels
- System peripherals

SMMU and CCI provide shared memory environment with PS, PMC, and PL processors

Features:

- Up to 1.7 GHz speed
- Armv8 architecture
- Up in seconds
- Supports Linux and bare-metal



Scalar Engines

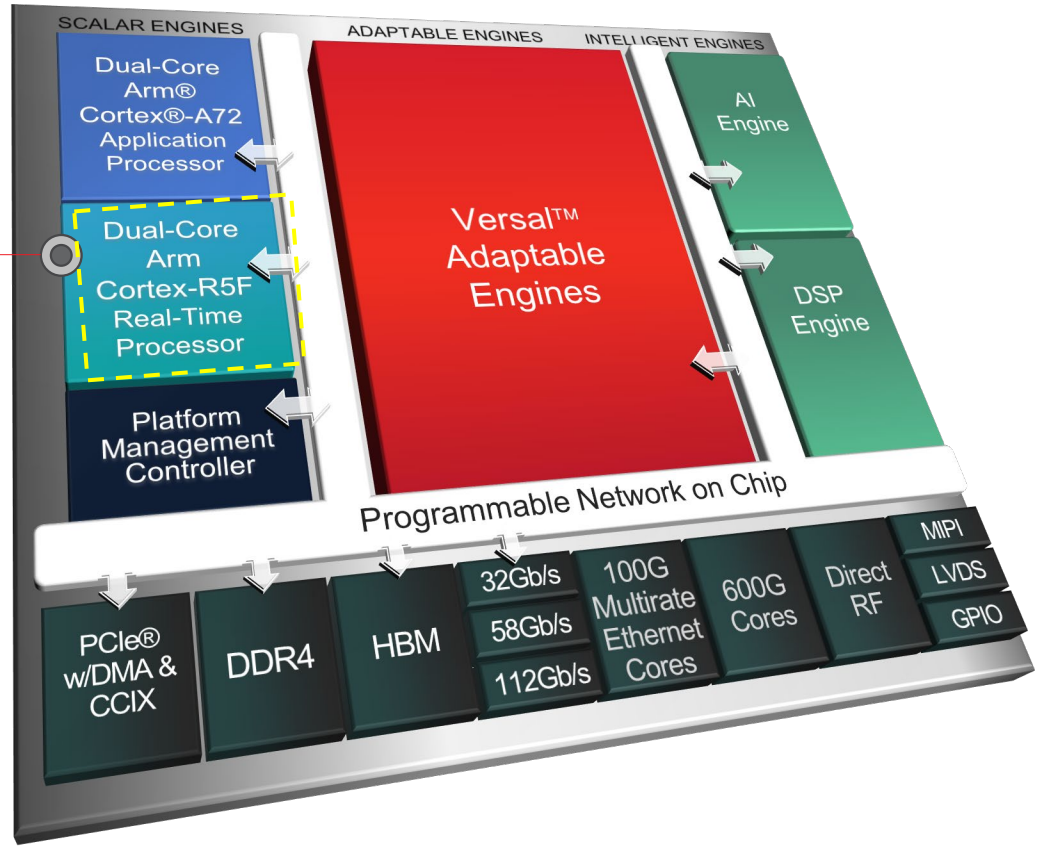
Real-time Processing Unit (RPU)

Based on Arm Cortex-R5F dual-core processor

- L1 caches
- Tightly coupled memories (TCM)
- Configured into dual-processor mode or lock-step mode

Features:

- Functional safety
- Split mode or lock step
- Low latency, determinism, and real-time control
- ASIL/SIL certifiable



Platform Management Controller (PMC)

Primary Functions

Device Configuration

- Initialization of the device
- Boot and configuration from a supported boot device
- Configure Adaptable Engines using CFI (configuration frame interface)

System Monitor

- Monitors system activity
- Responds to security and functional safety events
- Releases the PS from reset
- Provides system power and error management services

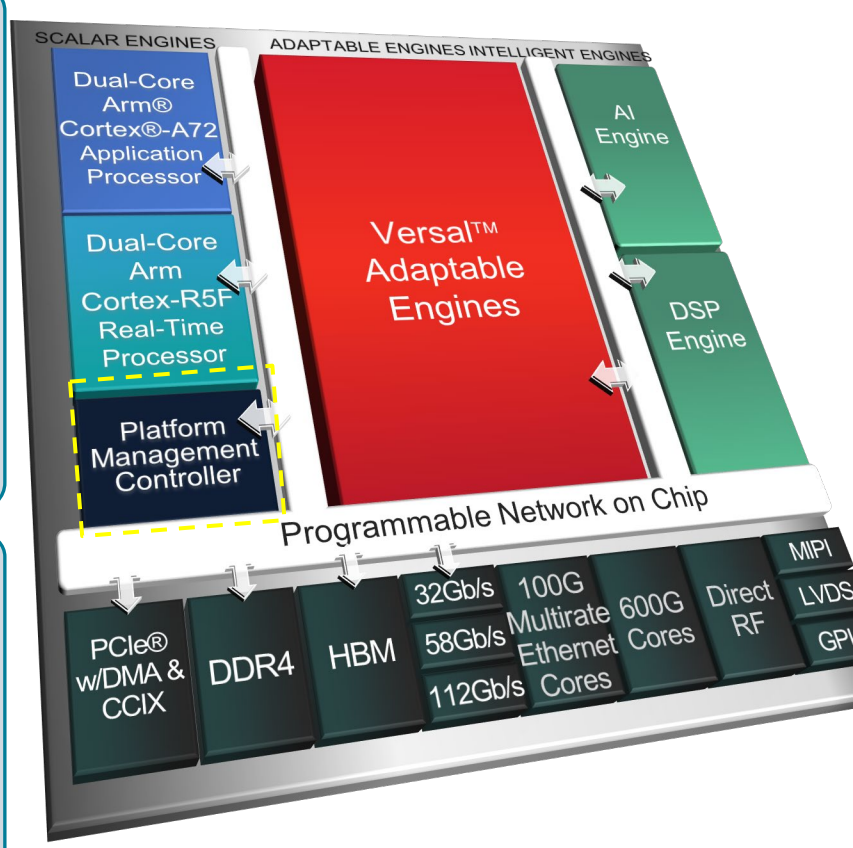
Security & Device Integrity

Security core functions

- Encryption and decryption
- Authentication
- Key management

Testing & Debugging

- Provides test and debug infrastructure
- Supports boundary scan and Arm® CoreSight™ trace and debug technology



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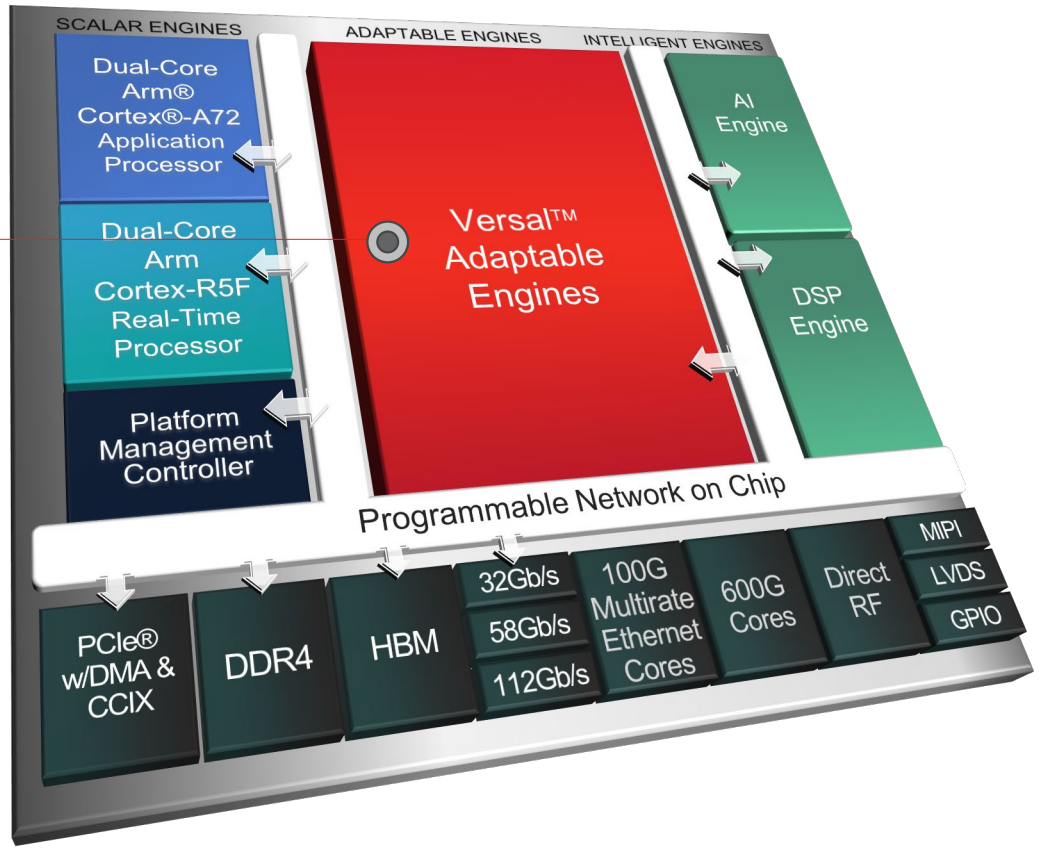
Adaptable Engines

Adaptable Hardware Engines – Programmable Logic

Millions of reconfigurable system logic cells

Support for parallel, pipelined and hybrid architectures

Wide variety of memory elements



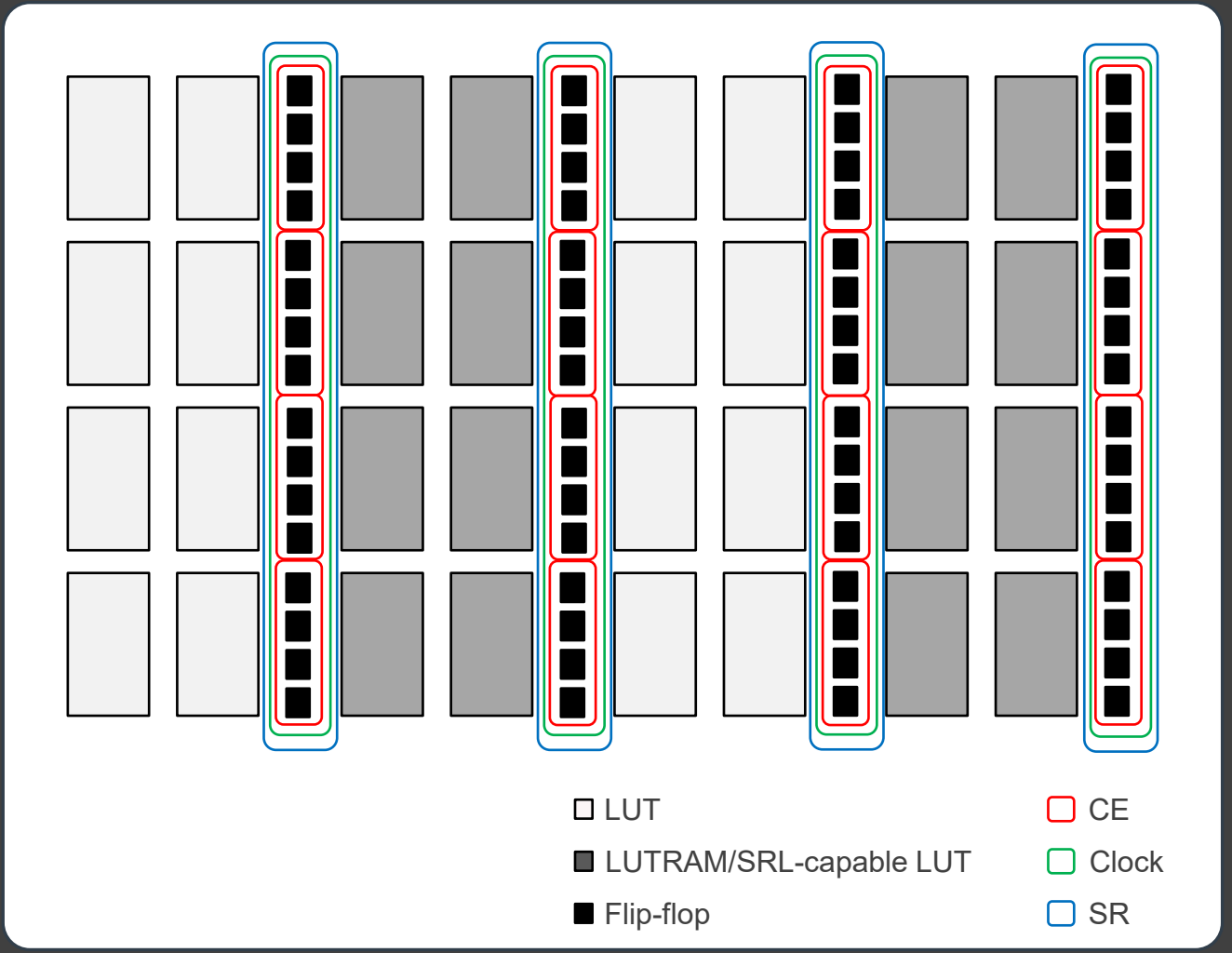
Configurable Logic Block

CLBs include logic and look-up tables (LUTs)

- Configurable into different combinations
  - To create special-purpose functions, processing units, and other entities

CLB contains:

- 32 LUTs and 64 slice flip-flops
- Arithmetic carry logic and multiplexers
- Control signals
  - 4 clocks, 4 set/resets, 16 clock enables
- 50% of the LUTs can be combined to form LUTRAM and shift registers
- Dedicated interconnect paths



Programmable I/O

XPIO

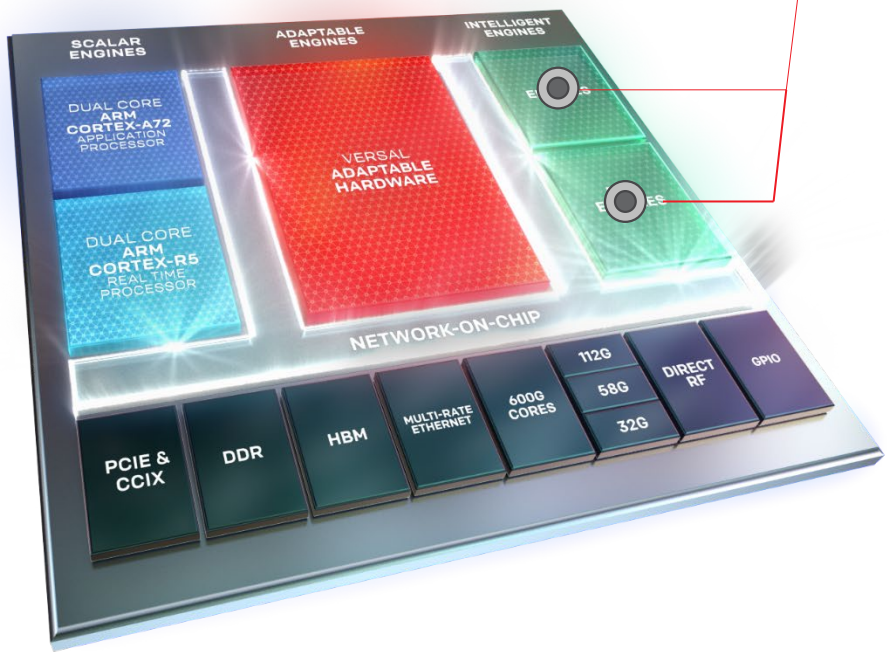
- High-performance XP I/O
- Dedicated logic
- Support for interfaces between 1.0V and 1.5V
- Grouped into 54-pin banks
- Each XPIO can use the XPHY

HDIO

- High-density HD I/O
- Support for interfaces from 1.8V to 3.3V
- Grouped into 22-pin banks with supporting resources for low-performance interfaces

- No overlapping voltages or I/O standards
- Support for low-speed SDR and DDR interfaces and coarse data alignment
- Input and output buffers support a range of single-ended and differential I/O standards
- Processor peripherals are routed to the MIO pins

Intelligent Engines



Wired communications, automotive, and consumer markets

AI Is Everywhere

Intelligent Engines for Diverse Compute

DSP Engines

High-precision, floating-point computation support

Offload additional functions for acceleration

AI Engines

High throughput, low latency, and power efficient

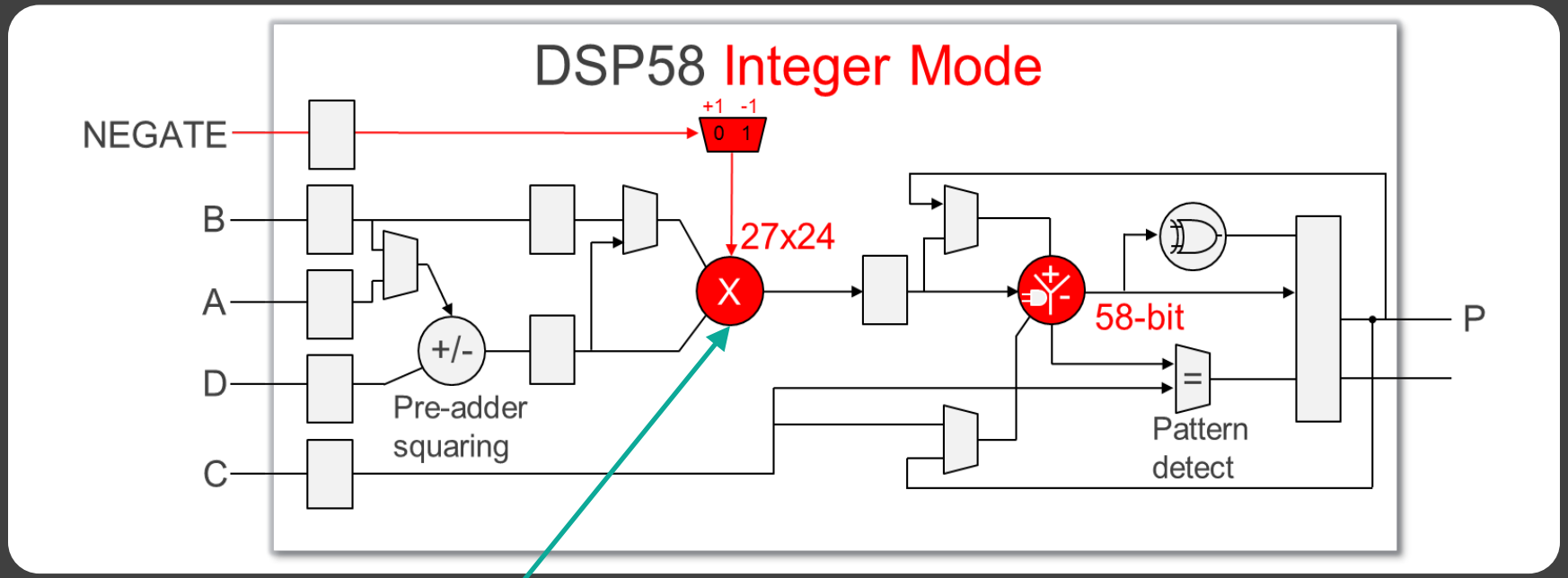
Ideal for AI inference and advanced signal processing

Array of VLIW processors with SIMD vector units

Instruction-level and data-level parallelism

Digital Signal Processing Capability

Combines high speed with small size for high performance and system design flexibility



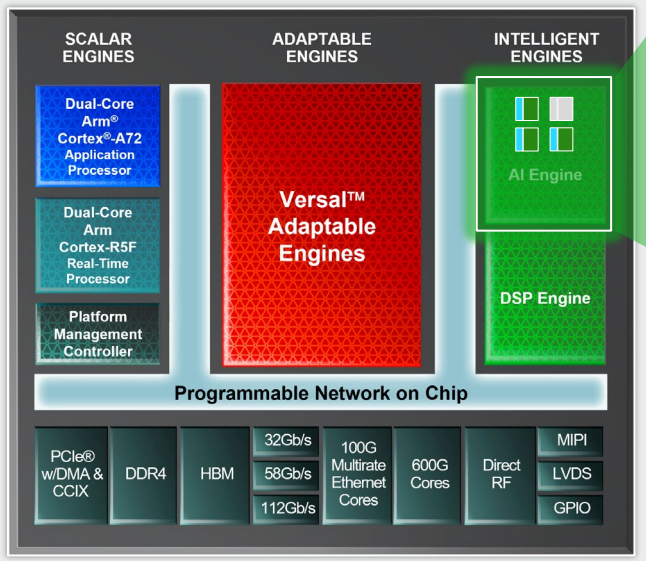
- Multiplier can be dynamically bypassed
- Two 58-bit inputs can feed a SIMD arithmetic unit
- Logic unit can generate a logic function on the two operands

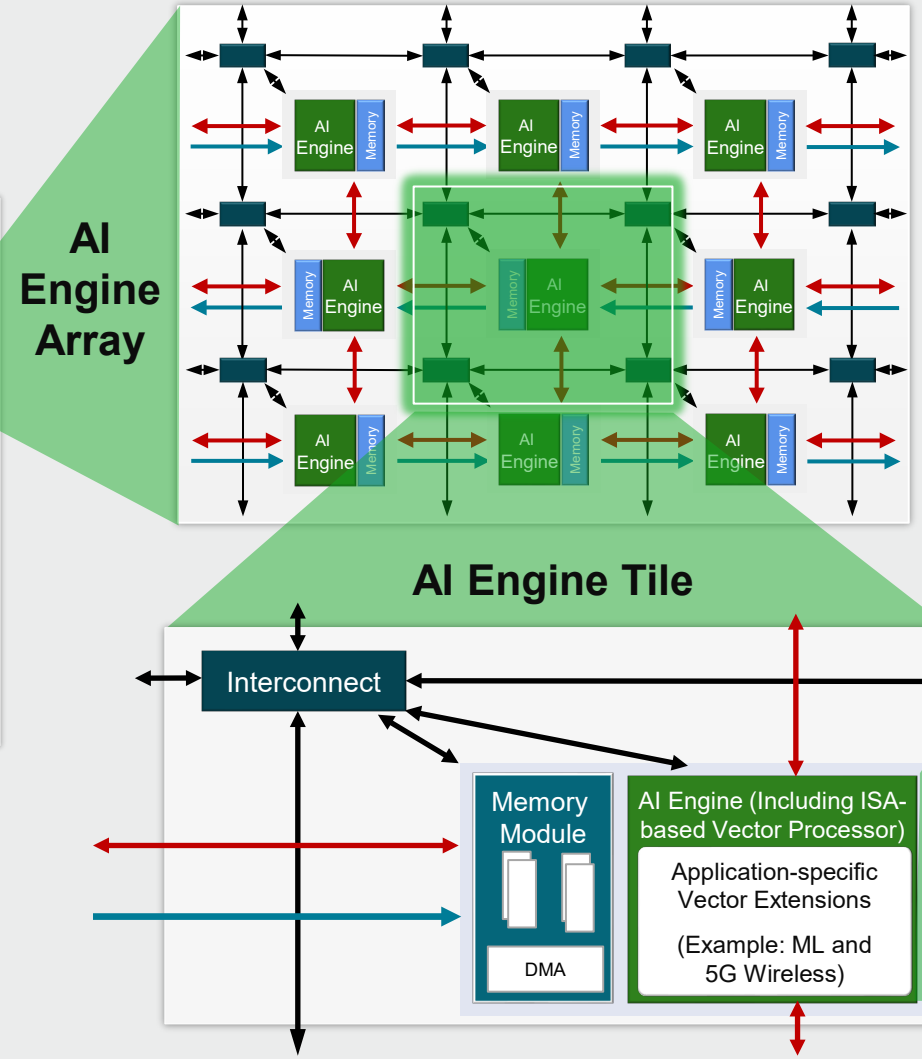
Supports a new negate function that enables a dynamic negate post multiplier

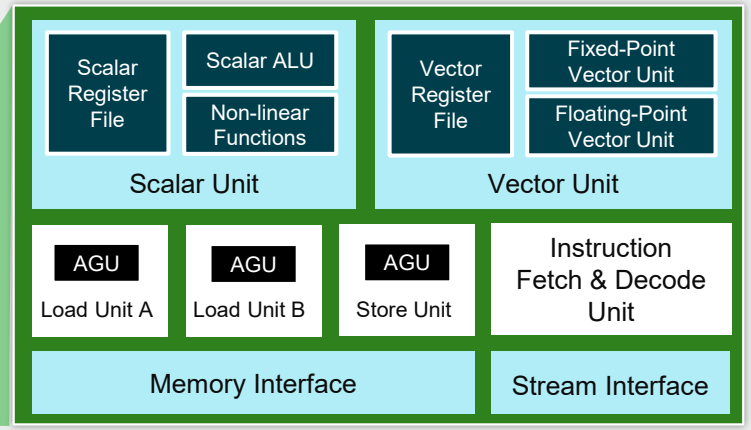
The DSP58 slice supports modes such as:

- Fixed point
- Int8 dot product
- Single precision floating point, and
- 18x18 complex multiply

AI Engine







- VLIW processor with 512-bit SIMD vector units (16x32. 64x8, …)
  - Application-specific vector extensions
    - Optimized for DSP, 5G, AI, ML, etc.
  - Hardened in 7nm @ 1 GHz
  - Software programmable (e.g., C/C++)

Memory Interface
Stream Interface
Cascade Interface

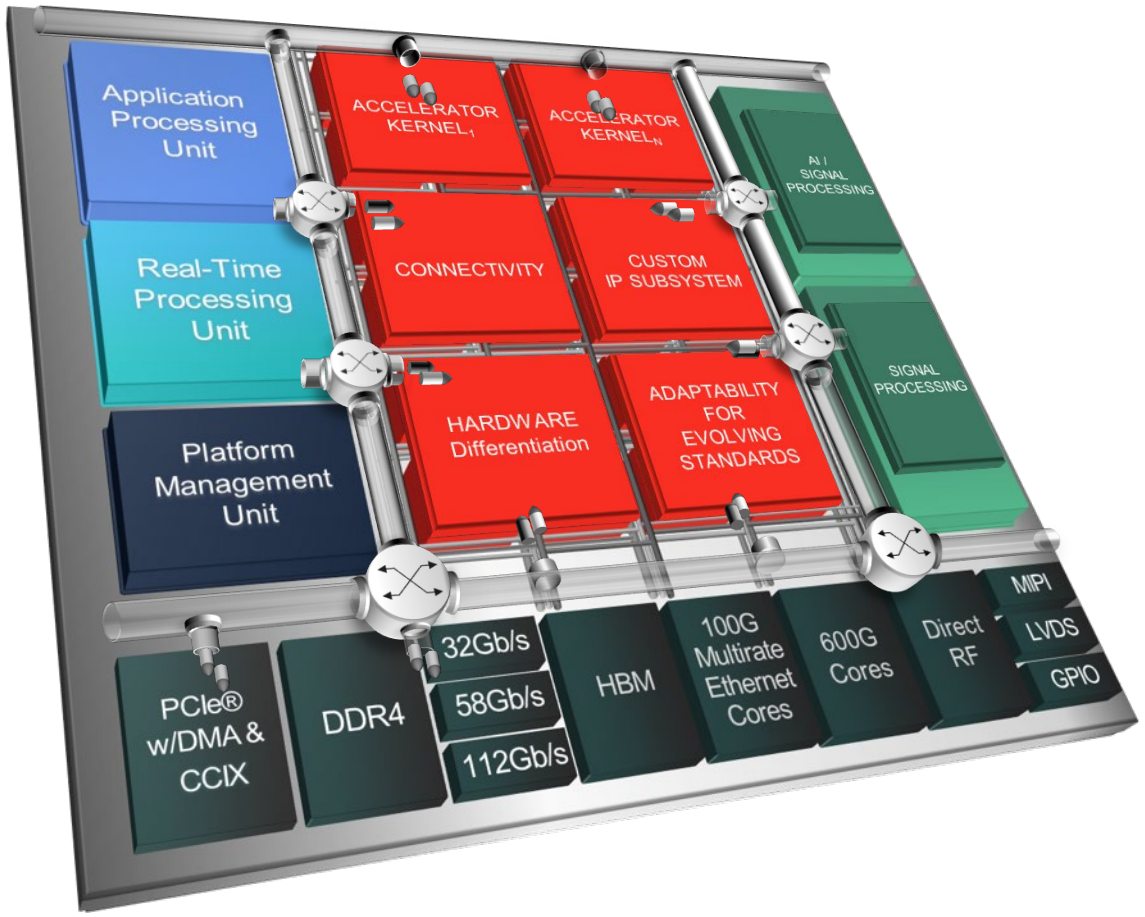
Programmable NoC: Bridging Engines & Hard IP

High-bandwidth, Terabit Programmable NoC

- Can be programmed for different data flows between high-speed I/Os and engines
- Can be prioritized between throughput, latency, and bit widths
- Guaranteed QoS (bandwidth vs. latency)

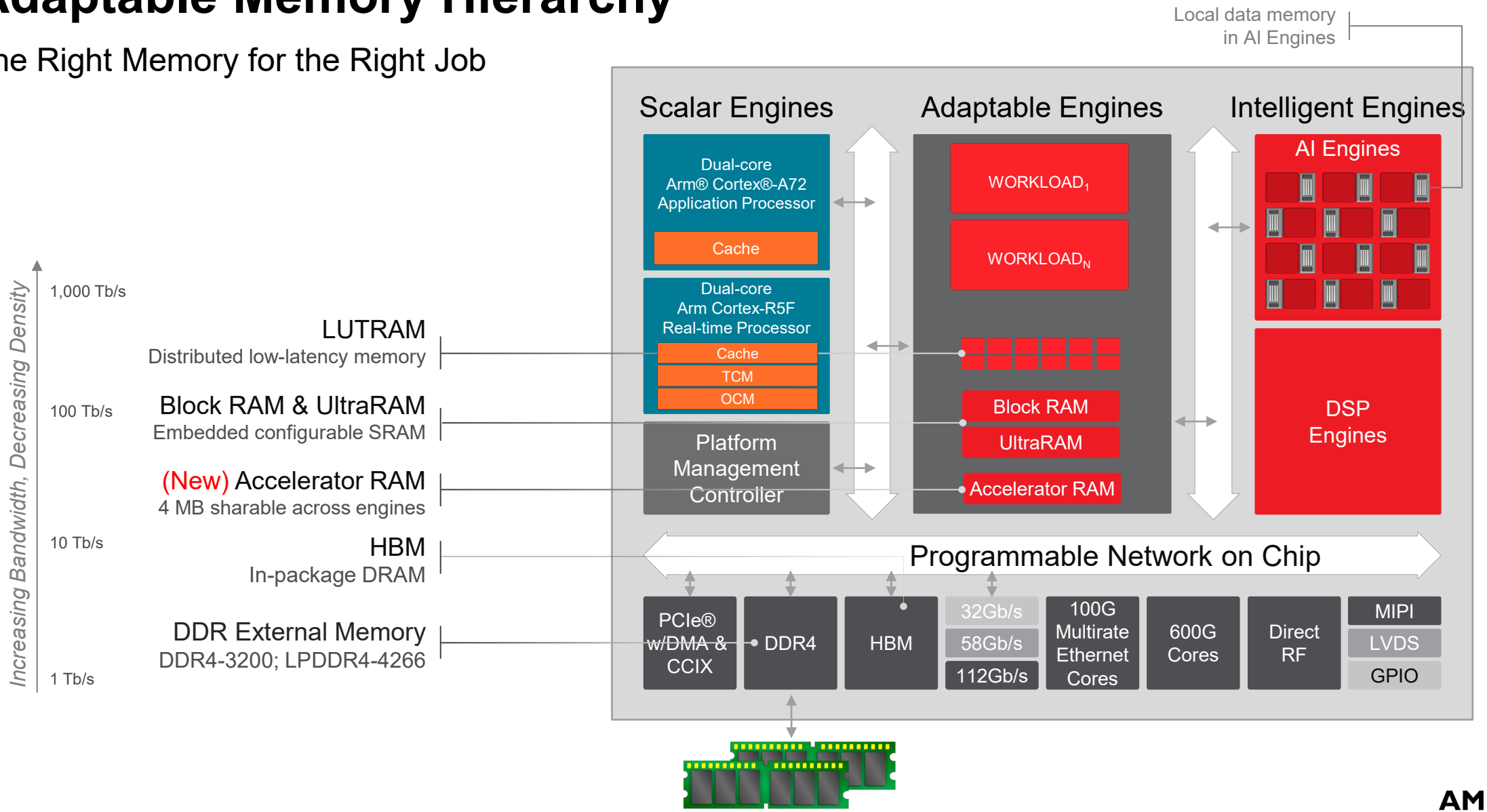
Eases IP and Kernel Placement

- Ability to compartmentalize the kernels with easy entry and exit points
- Ability to connect any master to any slave
- Configurable NoC is an AXI4-based network
- Hardened connectivity to the integrated memory controllers and PCIe core



Adaptable Memory Hierarchy

The Right Memory for the Right Job



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