TXV0106 6-Bit Fix Direction Low Skew, Low-Jitter Voltage Translator or Buffer

1 Features

- Supports up to 500Mbps for 1.65 V to 3.6 V
- Meets RGMII 2.0 timing specifications:
  - < 750 ps rise and fall time
  - < ± 5 % duty cycle distortion
  - < ± 400 ps channel to channel skew
  - Up to 250Mbps/channel
- Integrated 10 Ω damping output resistor to minimize signal reflections
- High drive strength (up to 12 mA at 3.6 V)
- Fully configurable symmetric dual-rail design
- Optimal signal integrity performance with 390ps peak-to-peak jitter for 1.8 V to 3.3 V
- Features V_{CC} isolation and V_{CC} disconnect
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22:
  - 2000-V Human-Body Model
  - 1000-V Charged-Device Model
- Low power consumption:
  - 10-μA maximum (25°C)
  - 20-μA maximum (–40°C to 125°C)
- Operating temperature from –40°C to +125°C

2 Applications

- Medium or short range radar
- ADAS domain controller
- HVAC controller design
- Machine vision camera
- Rack sever motherboard
- IP telephone

3 Description

The TXV0106 is a 6-bit, dual-supply fixed-direction low-skew, low jitter voltage translation device. This device can be used for redriving, voltage translation and power isolation when implementing skew sensitive interface, such as RGMII between Ethernet MAC and PHY. The Ax I/O pins and enable pin ($\overline{OE}$) are referenced to V_{CCA} logic levels, and Bx I/O pins are referenced to V_{CCB} logic levels. This device has improved channel-to-channel skew, duty cycle distortion and symmetric rise or fall timing for applications requiring strict timing conditions.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, thus preventing damaging current backflow through the device when it is powered down.

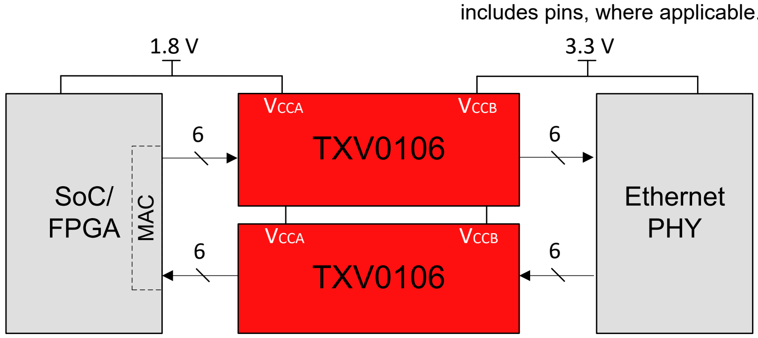
The V_{CC} isolation feature is designed so that if either V_{CC} supply is at or near 0 V both ports will switch to a high-impedance state. This feature enables power isolation for communications across multiple MACs and PHYs, and is beneficial in situations where MACs and PHYs are powered up asynchronously preventing current backflow between devices.

The TXV0106 transmits data in a fixed direction from the A bus to the B bus. When $\overline{OE}$ is set to High, both Ax and Bx pins will be forced into a high-impedance state. See *Device Functional Modes* for a summary of the operation of the control logic.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TXV0106	BQB (WQFN, 16)	3.5 mm × 2.5 mm

(1) For more information see, Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TXV0106 in RGMII Applications

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4 Pin Configuration and Functions

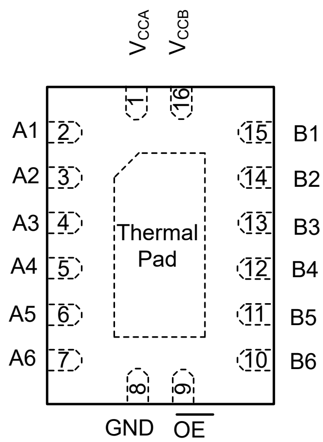


Figure 4-1. BQB Package, 16-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
V_{CCA}	1	—	A-port supply voltage. 1.8 V ≤ V_{CCA} ≤ 3.6 V.
A1	2	I/O	Input/output A1. Referenced to V_{CCA}.
A2	3	I/O	Input/output A2. Referenced to V_{CCA}.
A3	4	I/O	Input/output A3. Referenced to V_{CCA}.
A4	5	I/O	Input/output A4. Referenced to V_{CCA}.
A5	6	I/O	Input/output A5. Referenced to V_{CCA}.
A6	7	I/O	Input/output A6. Referenced to V_{CCA}.
GND	8	—	Ground.
$\overline{OE}$	9	I	Output Enable. Pull to GND to enable all outputs. Pull to V_{CCA} to place all outputs in high-impedance mode. Referenced to V_{CCA}.
B6	10	I/O	Input/output B6. Referenced to V_{CCB}.
B5	11	I/O	Input/output B5. Referenced to V_{CCB}.
B4	12	I/O	Input/output B4. Referenced to V_{CCB}.
B3	13	I/O	Input/output B3. Referenced to V_{CCB}.
B2	14	I/O	Input/output B2. Referenced to V_{CCB}.
B1	15	I/O	Input/output B1. Referenced to V_{CCB}.
V_{CCB}	16	—	B-port supply voltage. 1.8 V ≤ V_{CCB} ≤ 3.6 V.
Thermal pad		—	Thermal pad. Can be grounded (recommended) or left floating.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	4.6	V
V_{CCB}	Supply voltage B		–0.5	4.6	V
V_I	Input Voltage[(2)]	I/O Ports (A Port)	–0.5	4.6	V
		I/O Ports (B Port)	–0.5	4.6	
		Control Inputs	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state[(2)]	A Port	–0.5	4.6	V
		B Port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state[(2) (3)]	A Port	–0.5	V_{CCA} + 0.5	V
		B Port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	$V_I < 0$	–50		mA
I_{OK}	Output clamp current	$V_O < 0$	–50		mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 [(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) [(1)]

				MIN	MAX	UNIT
V_{CCA}	Supply voltage A			1.65	3.6	V
V_{CCB}	Supply voltage B			1.65	3.6	V
V_{IH}	High-level input voltage	Data Inputs (Ax, Bx), $\overline{OE}$ (Referenced to V_{CCI})	V_{CCI} = 1.65 V - 3.6 V	V_{CCI} x 0.7		V
V_{IL}	Low-level input voltage	Data Inputs (Ax, Bx), $\overline{OE}$ (Referenced to V_{CCI})	V_{CCI} = 1.65 V - 3.6 V		V_{CCI} x 0.3	V
I_{OH}	High-level output current		V_{CCO} = 1.65 V - 1.95 V		–8	mA
	High-level output current		V_{CCO} = 2.3 V - 2.7 V		–9	mA
	High-level output current		V_{CCO} = 3 V - 3.6 V		–12	mA
I_{OL}	Low-level output current		V_{CCO} = 1.65 V - 1.95 V		8	mA
	Low-level output current		V_{CCO} = 2.3 V - 2.7 V		9	mA
	Low-level output current		V_{CCO} = 3 V - 3.6 V		12	mA
V_I	Input voltage			0	3.6	V
V_O	Output voltage	Active State		0	V_{CCO}	V
		Tri-State		0	3.6	
Δt/Δv	Input transition rise and fall time				5	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port. V_{CCO} is the V_{CC} associated with the output port.

5.4 Thermal Information

THERMAL METRIC[(1)]		TXV0106 BQB (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.5	°C/W
Y_{JT}	Junction-to-top characterization parameter	4.5	°C/W
Y_{JB}	Junction-to-board characterization parameter	41.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	20.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics app report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A) –40°C to 125°C			UNIT
					MIN	TYP	MAX	
V_{IL}	Data Input_Negative threshold	Data inputs, $\overline{OE}$	1.65 V - 3.6 V	1.65 V - 3.6 V			0.3× VCCA	V
V_{IH}	Data Input_Positive threshold	Data inputs, $\overline{OE}$	1.65 V - 3.6 V	1.65 V - 3.6 V	0.7× VCCA			V
V_{OH}	High-level output voltage [(3)]	I_{OH} = –8 mA	1.65 V	1.65 V	1.1			V
		I_{OH} = –9 mA	2.3 V	2.3 V	1.8			V
		I_{OH} = –12 mA	3 V	3 V	2.4			V
V_{OL}	Low-level output voltage [(4)]	I_{OL} = 8 mA	1.65 V	1.65 V			0.27	V
		I_{OL} = 9 mA	2.3 V	2.3 V			0.23	V
		I_{OL} = 12 mA	3 V	3 V			0.26	V
I_I	Input leakage current	Data Inputs (Ax, Bx) $V_I = V_{CCI}$ or GND	1.65 V - 3.6 V	1.65 V - 3.6 V	–1		1	µA
I_{off}	Partial power down current	A Port or B Port V_I or V_O = 0 V - 3.6 V	0 V	0 V - 3.6 V	–5		3.6	µA
		A Port or B Port V_I or V_O = 0 V - 3.6 V	0 V - 3.6 V	0 V	–5		3.6	
I_{OZ}	Tri-state output current [(5)]	A or B Port: $V_I = V_{CCI}$ or GND $V_O = V_{CCO}$ or GND $\overline{OE} = V_{IH}$	3.6 V	3.6 V	–5		5	µA
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	1.65 V - 3.6 V	1.65 V - 3.6 V			14	µA
			3.6 V	0 V			11	
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	0 V	3.6 V	-1			µA
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	1.65 V - 3.6 V	1.65 V - 3.6 V			14	µA
			3.6 V	0 V	–1			
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	0 V	3.6 V			11	µA
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	1.65 V - 3.6 V	1.65 V - 3.6 V			22	µA
C_i	Control Input Capacitance	V_I = 3.3 V or GND	3.3 V	3.3 V			3.9	pF
C_{io}	Data I/O Capacitance	$\overline{OE} = V_{CCA}$, V_O = 1.65V DC +1 MHz -16 dBm sine wave	3.3 V	3.3 V			2.7	pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) Tested at $V_I = V_{IH}$.
(4) Tested at $V_I = V_{IL}$.
(5) For I/O ports, the parameter I_{OZ} includes the input leakage current.

5.6 Switching Characteristics, V_{CCA} = 1.8 ± 0.15 V

Minimum and maximum limits apply over the recommended temperature range at C_L = 15 pF and 250Mbps, unless otherwise indicated.

PARAMETER		FROM	TO	B-Port Supply Voltage (V_{CCB})									UNIT
				1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	1.5		4.8	1.2		3.5	1.2		3.0	ns
t_{dis}	Disable time	$\overline{OE}$	B	3.5		7.0	3.0		5.5	3.6		6.5	ns
t_{en}	Enable time	$\overline{OE}$	B	1.2		4.0	1.0		3.0	1.0		2.6	ns
t_{SKO}	Output channel-to-channel skew (1)	A	B	-450		450	-300		300	-330		330	ps
T_R	Rise time (2)	A	B	0.49		1.35	0.40		0.95	0.35		0.80	ns
T_F	Fall time (2)	A	B	0.45		1.35	0.35		0.95	0.35		0.80	ns
Duty Cycle	Duty cycle variation	A	B	47	50	56	47	50	54	47	50	54	%
T_{R_5pF}	Rise time (2) (3)	A	B	0.28		0.75	0.22		0.55	0.19		0.45	ns
T_{F_5pF}	Fall time (2) (3)	A	B	0.27		0.75	0.20		0.55	0.18		0.40	ns
t_{SKO_5pF}	Output channel-to-channel skew (1) (3)	A	B	-300		300	-270		270	-310		310	ps
Duty Cycle _5pF	Duty cycle variation (3)	A	B	47	50	54	47	50	54	47	50	54	%
$t_{jit(pp)}$	Peak-to-peak jitter (250 Mbps 2^{15}- 1 PRBS input)	A	B	160		450	130		335	120		390	ps

(1) Skew parameter also includes jitter
(2) Rise and fall time is measured at 20% - 80%
(3) Parameters tested under RGMII input transition (≤ 2 ns/V) rise and fall time. C_{LOAD} = 5 pF

5.7 Switching Characteristics, V_{CCA} = 2.5 ± 0.2 V

Minimum and maximum limits apply over the recommended temperature range at C_L = 15 pF and 250Mbps, unless otherwise indicated.

PARAMETER		FROM	TO	B-Port Supply Voltage (V_{CCB})									UNIT
				1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	1.5		4.2	1.2		3.0	1.1		2.5	ns
t_{dis}	Disable time	$\overline{OE}$	B	3.6		6.5	2.7		5.0	3.6		6.0	ns
t_{en}	Enable time	$\overline{OE}$	B	1.2		3.5	1.0		2.5	0.9		2.0	ns
t_{SKO}	Output channel-to-channel skew (1)	A	B	-330		330	-200		200	-200		200	ps
T_R	Rise time (2)	A	B	0.50		1.4	0.40		1.0	0.35		0.80	ns
T_F	Fall time (2)	A	B	0.45		1.4	0.35		1.0	0.30		0.80	ns
Duty Cycle	Duty cycle variation	A	B	47	50	55	47	50	53	47	50	53	%
T_{R_5pF}	Rise time (2) (3)	A	B	0.25		0.75	0.20		0.55	0.15		0.45	ns
T_{F_5pF}	Fall time (2) (3)	A	B	0.25		0.76	0.2		0.55	0.15		0.45	ns
t_{SKO_5pF}	Output Channel-to-channel skew (1) (3)	A	B	-210		210	-160		160	-180		180	ps
Duty Cycle _5pF	Duty cycle variation (3)	A	B	48	50	53	48	50	52	48	50	52	%
$t_{jit(pp)}$	Peark-to-peak jitter (250 Mbps 2^{15}- 1 PRBS input)	A or B	A or B	120		370	100		300	90		360	ps

(1) Skew parameter also includes jitter
(2) Rise and fall time is measured at 20% - 80%
(3) Parameters tested under RGMII input transition (≤ 2 ns/V) rise and fall time. C_{LOAD} = 5 pF

5.8 Switching Characteristics, V_{CCA} = 3.3 ± 0.3 V

Minimum and maximum limits apply over the recommended temperature range at C_L = 15 pF and 250Mbps, unless otherwise indicated.

PARAMETER		FROM	TO	B-Port Supply Voltage (V_{CCB})									UNIT
				1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	1.2		3.8	1.2		2.7	1.1		2.3	ns
t_{dis}	Disable time	$\overline{OE}$	A	2.7		7.0	2.7		7.0	2.7		7.0	ns
t_{en}	Enable time	$\overline{OE}$	A	0.75		4.0	0.75		4.0	0.75		4.0	ns
t_{SKO}	Output channel-to-channel skew (1)	A	B	-310		310	-190		190	-160		160	ps
T_R	Rise time (2)	A	B	0.50		1.3	0.40		1.0	0.35		0.80	ns
T_F	Fall time (2)	A	B	0.45		1.3	0.35		1.0	0.35		0.80	ns
Duty Cycle	Duty cycle variation	A	B	46	50	54	48	50	53	48	50	52	%
T_{R_5pF}	Rise time (2) (3)	A	B	0.30		0.80	0.20		0.55	0.15		0.45	ns
T_{F_5pF}	Fall time (2) (3)	A	B	0.25		0.80	0.20		0.60	0.20		0.45	ns
t_{SKO_5pF}	Output channel-to-channel skew (1) (3)	A	B	-230		230	-130		130	-140		140	ps
Duty Cycle _5pF	Duty cycle variation (3)	A	B	48	50	53	48	50	52	48	50	52	%
$t_{jit(pp)}$	Peark-to-peak jitter (250 Mbps 2^{15}- 1 PRBS input)	A or B	A or B	115		390	75		330	75		330	ps

(1) Skew parameter also includes jitter
(2) Rise and fall time is measured at 20% - 80%
(3) Parameters tested under RGMII input transition (≤ 2 ns/V) rise and fall time. C_{LOAD} = 5 pF

5.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

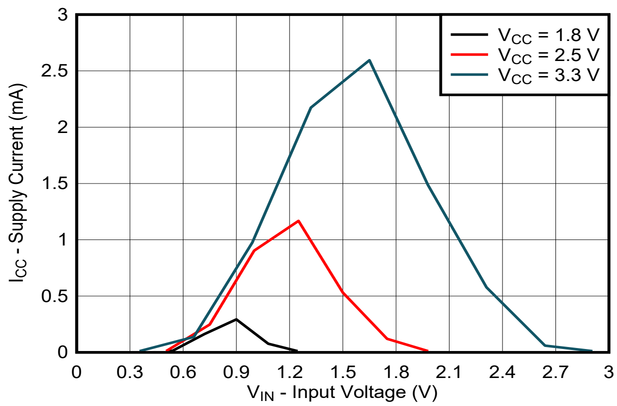


Figure 5-1. Supply Current vs Input Voltage Supply (Rising)

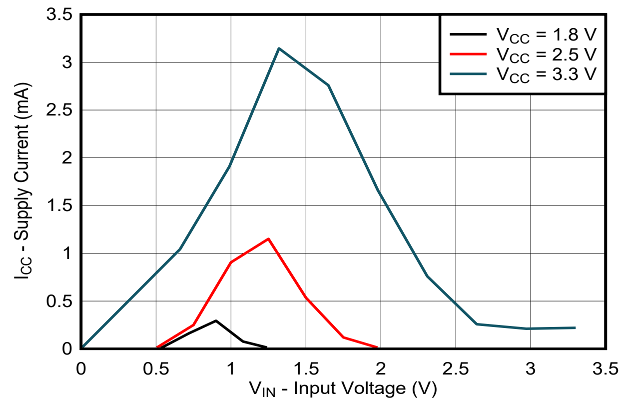


Figure 5-2. Supply Current vs Input Voltage Supply (Falling)

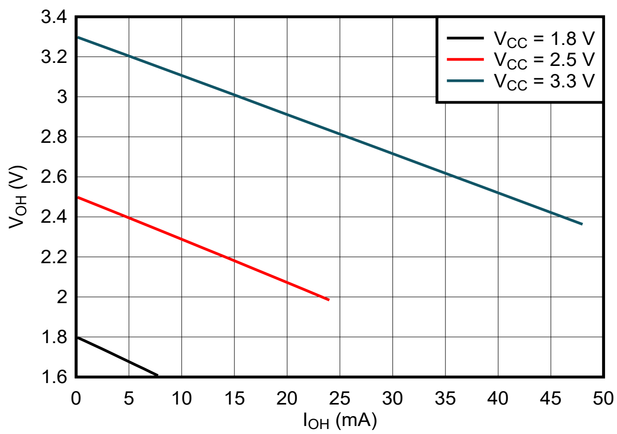


Figure 5-3. Output Voltage vs Current in HIGH State

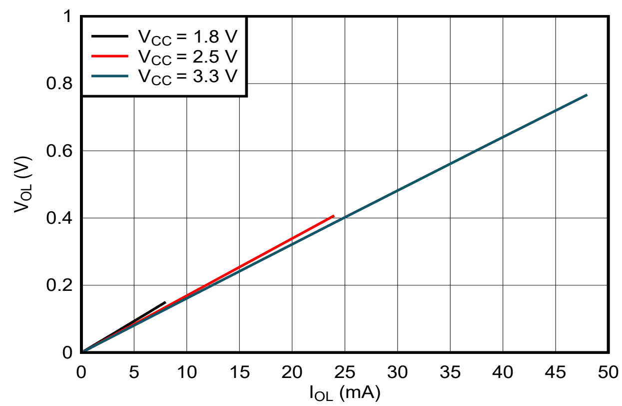


Figure 5-4. Output Voltage vs Current in LOW State

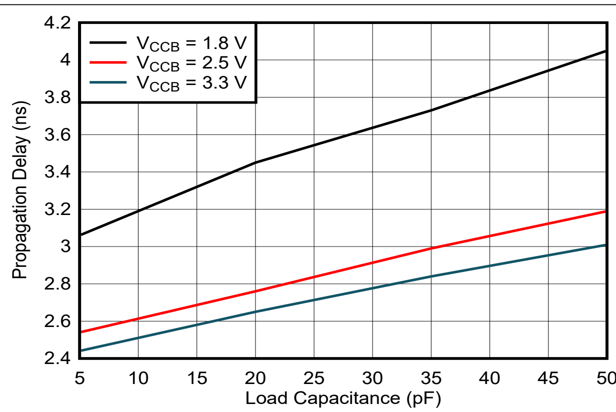


Figure 5-5. Propagation Delay, T_{PLH} vs Load Capacitance (V_{CCA} = 1.8 V)

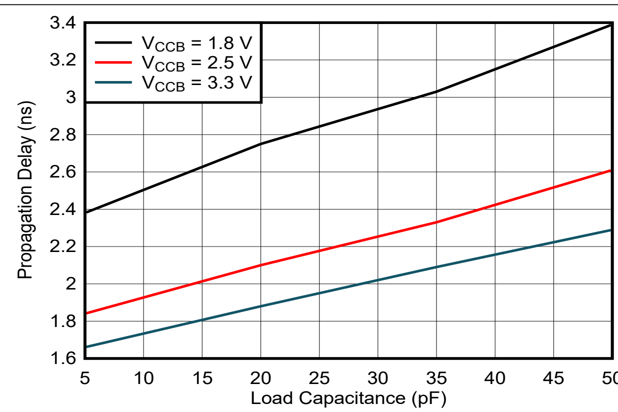


Figure 5-6. Propagation Delay, T_{PLH} vs Load Capacitance (V_{CCA} = 2.5 V)

5.9 Typical Characteristics (continued)

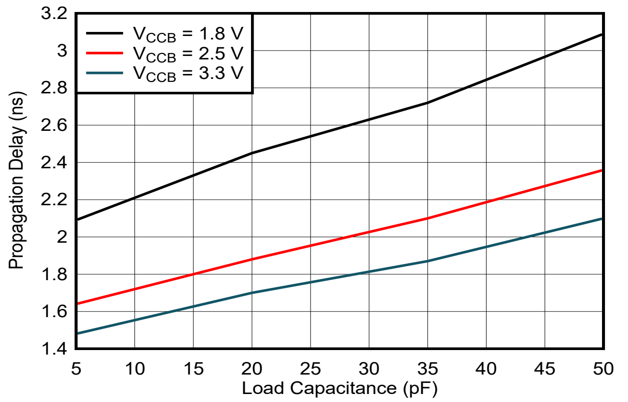


Figure 5-7. Propagation Delay, T_{PLH} vs Load Capacitance (V_{CCA} = 3.3 V)

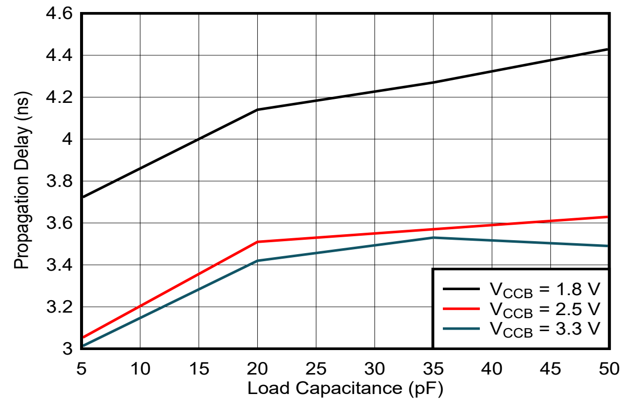


Figure 5-8. Propagation Delay, T_{PHL} vs Load Capacitance (V_{CCA} = 1.8 V)

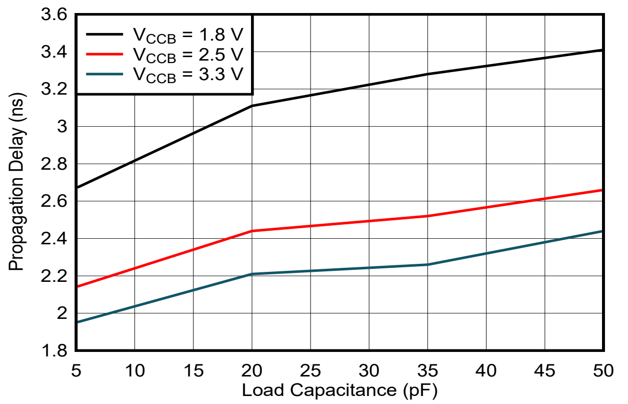


Figure 5-9. Propagation Delay, T_{PHL} vs Load Capacitance (V_{CCA} = 2.5 V)

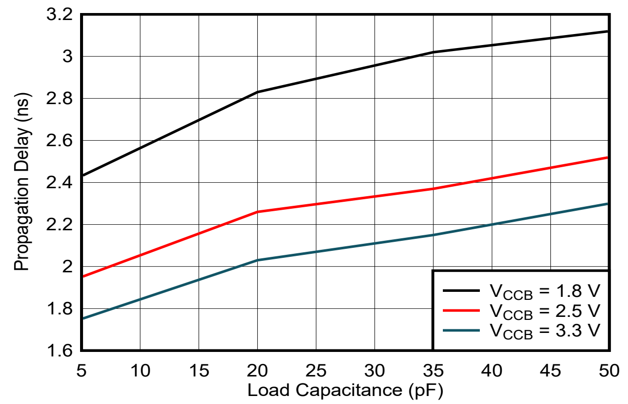


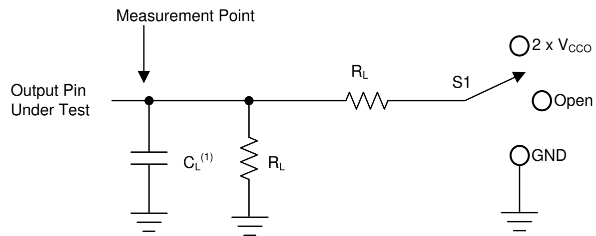
Figure 5-10. Propagation Delay, T_{PHL} vs Load Capacitance (V_{CCA} = 3.3 V)

6 Parameter Measurement Information

6.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- Z_O = 50 Ω
- $\Delta t/\Delta V \leq 1$ ns/V

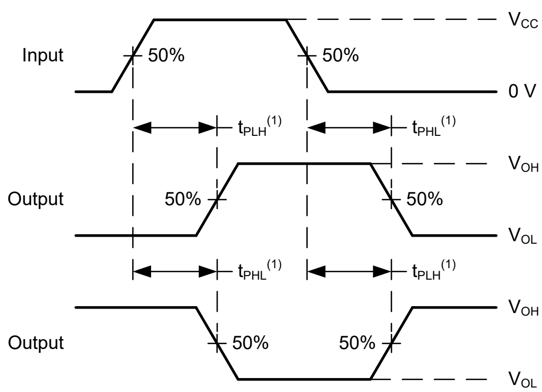


A. C_L includes probe and jig capacitance.

Figure 6-1. Load Circuit

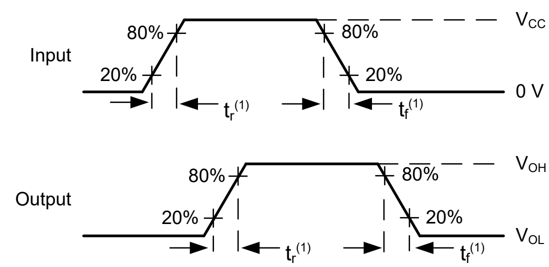
Table 6-1. Load Circuit Conditions

Parameter		V_{CCO}	R_L	C_L	S_1	V_{TP}
t_{pd}	Propagation (delay) time	1.65 V – 3.6 V	2 kΩ	15 pF	Open	N/A
t_{en}, t_{dis}	Enable time, disable time	1.65 V – 3.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.15 V
t_{en}, t_{dis}	Enable time, disable time	1.65 V – 3.6 V	2 kΩ	15 pF	GND	0.15 V



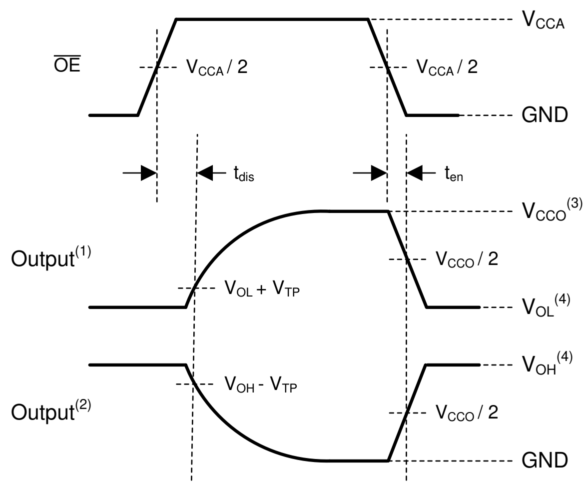
1. The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 6-2. Propagation Delay



1. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 6-3. Input Transition Rise and Fall Rate



A. Output waveform on the condition that input is driven to a valid Logic Low.
B. Output waveform on the condition that input is driven to a valid Logic High.
C. V_{CCO} is the supply pin associated with the output port.
D. V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

Figure 6-4. Enable Time and Disable Time

7 Detailed Description

7.1 Overview

The TXV0106 is an 6-bit translating transceiver that uses two individually configurable power-supply rails. The device is operational with both V_{CCA} and V_{CCB} supplies as low as 1.65 V and as high as 3.6 V. Additionally, the device can be used as a buffer with V_{CCA} = V_{CCB}. The Ax port is designed to track V_{CCA}, and the Bx port is designed to track V_{CCB}.

The TXV0106 device is designed for asynchronous communication between data buses, and transmits data in a fixed direction from the A bus to the B bus. The output-enable input ($\overline{OE}$) is used to disable the outputs so the buses are effectively isolated. The output-enable pin ($\overline{OE}$) of the TXV0106 is referenced to V_{CCA}. To enable the high-impedance state of the level shifter I/Os during power up or power down, the $\overline{OE}$ pin should be tied to V_{CCA} through a pullup resistor.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry prevents excessive current from being drawn from or sourced into an input, output, or I/O while the device is powered down.

7.2 Functional Block Diagram

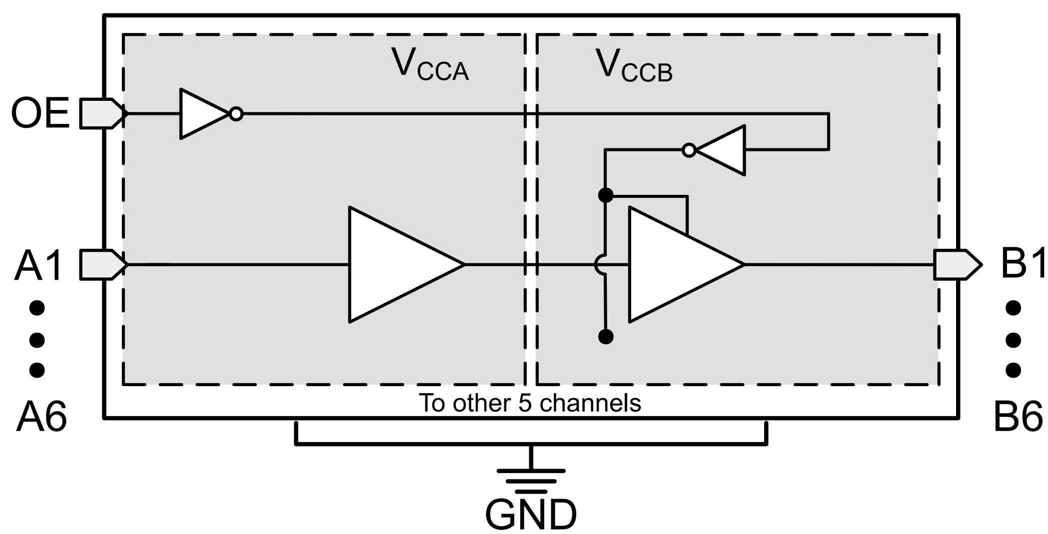


Figure 7-1. Functional Block Diagram of the TXV0106

7.3 Feature Description

7.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

7.3.2 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

7.3.3 V_{CC} Isolation and V_{CC} Disconnect ($I_{off\text{-}float}$)

This device has 2 features (V_{CC} Isolation and V_{CC} Disconnect) which helps in preventing current backflow in case the device is powered down unexpectedly. V_{CC} Isolation: when one of the supplies is kept at (or goes to) zero during normal operation, no current will be consumed by the supply that is maintained. This scenario forces all I/Os to be High-Z. V_{CC} Disconnect: when one of the supplies is left floating (disconnect) after ramping up, the I/Os are forced into High-Z without consuming any current from the maintained supply. In both cases, the I/Os will enter a high-impedance state when either supply (V_{CCA} or V_{CCB}) is <100 mV or left floating, while the other supply is still connected to the device. The following figure shows more information.

The maximum supply current is specified by I_{CCx}, while V_{CCx} is floating, in the *Electrical Characteristics*. The maximum leakage into or out of any input or output pin on the device is specified by $I_{off(float)}$ in the *Electrical Characteristics*.

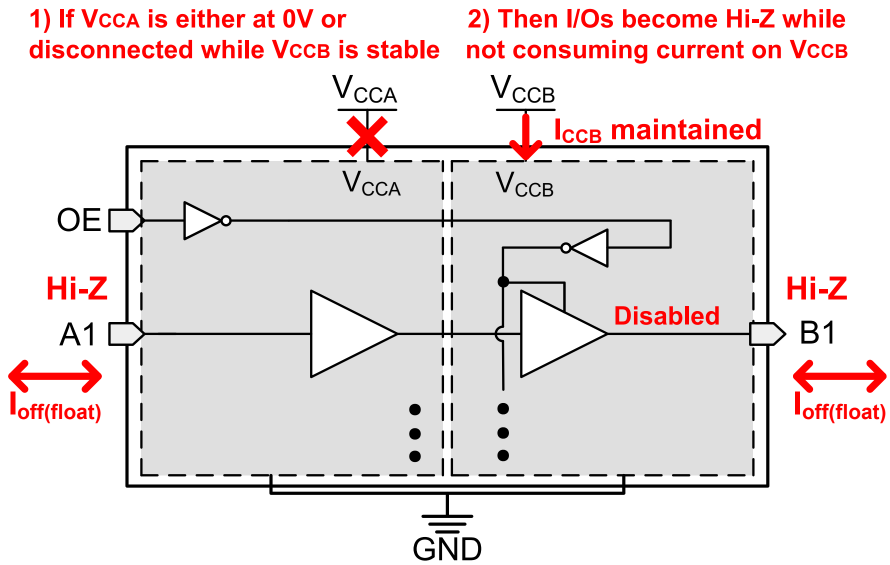


Figure 7-2. V_{CC} Disconnect and V_{CC} Isolation Feature

7.3.4 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

7.3.5 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in Figure 7-3

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

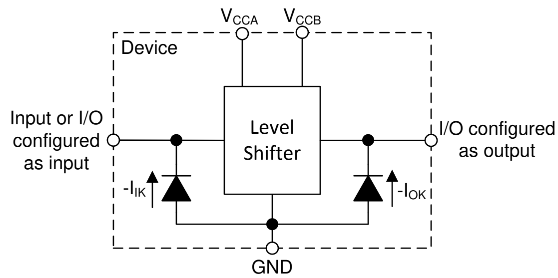


Figure 7-3. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.6 Fully Configurable Dual-Rail Design

Both the V_{CCA} and V_{CCB} pins can be supplied at any voltage from 1.65 V to 3.6 V, making the device an excellent choice for translating between any of the voltage nodes (1.8 V, 2.5 V, and 3.3 V).

7.3.7 Supports High-Speed Translation

The TXV0106 device can support high data rate applications. The translated signal data rate can support up to 500Mbps when the signal is translated from 1.65 V to 3.6 V. For the device to meet RGMII 2.0 timing specifications (rise or fall time, skew, and duty cycle distortion) the data rate will need to be lowered to 250Mbps.

7.3.8 Integrated Damping Resistor and Impedance Matching

The TXV0106 features a 10 Ω integrated damping resistor to help minimize signal reflections on the rising and falling edges. If impedance matching with a 50 Ω load is required, then a series resistor will be needed. Since the output impedance of the device will vary with the output voltage (V_{CCB}), Table 8-1 provides the recommended resistor values needed to impedance match a 50 Ω load

Table 7-1. Series Resistor Values for 50 Ω Impedance Matching

Output Voltage (V_{CCB})	1.8 V	2.5 V	3.3 V
Series Resistor	25 Ω	30 Ω	32 Ω

7.4 Device Functional Modes

Table 7-2. Function Table

CONTROL INPUTS (1)	PORT STATUS		OPERATION
$\overline{OE}$	A PORT	B PORT	
L	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active and should be kept at a valid logic level.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TXV0106 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXV0106 device is an excellent choice for use in applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 500Mbps when device translates a signal from 1.65 V to 3.6 V.

8.2 Typical Application

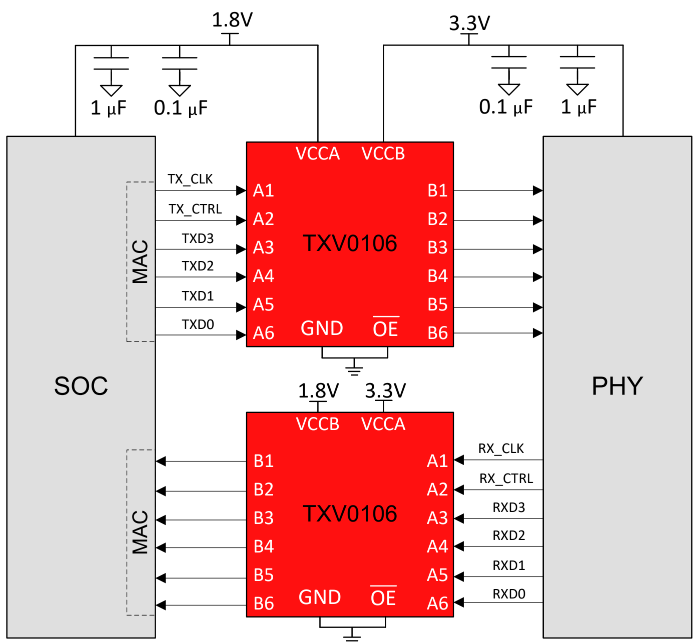


Figure 8-1. RGMII Application (Interfacing between MAC and PHY)

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.65 V to 3.6 V
Output voltage range	1.65 V to 3.6 V
Frequency	125 MHz
Load Capacitance	5 pF
Input Transition Rise/Fall Time	< 2 ns/V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range:
  – Use the supply voltage of the device that is driving the TXV0106 device to determine the input voltage range. For a valid logic-high, the value must exceed the positive-going input-threshold voltage (V_{t+}) of the input port. For a valid logic low the value must be less than the negative-going input-threshold voltage (V_{t-}) of the input port.
- Output voltage range:
  – Use the supply voltage of the device that the TXV0106 device is driving to determine the output voltage range.
- RGMII timing:
  – For the TXV0106 to meet RGMII timing specifications, parameters like frequency, C_{LOAD} and input rise/fall transition have to be met. Ensure each channel does not exceed a maximum frequency of 125 MHz, use a C_{LOAD} no greater than 5 pF, and use an input rise or fall transition no greater than 2 ns/V.

8.2.3 Application Curves

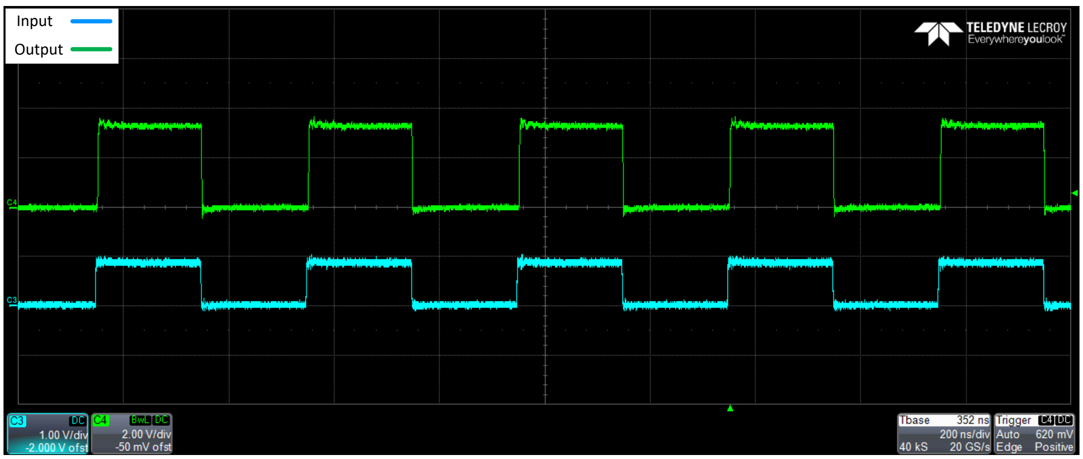


Figure 8-2. Up Translation (1.8 V to 3.3 V) C_{LOAD} = 15 pF at 2.5 MHz

8.3 System Examples

8.3.1 Solving Power Sequencing Challenges with the TXV0106

The TXV0106 not only solves voltage mismatch between interfaces but also solves power sequencing challenges. In some Ethernet applications, you may have a multi-core RGMII system with an Ethernet switch Figure 8-3. In other applications, you may have a standard Ethernet interface with one MAC and PHY. In either case, it is necessary to power up each device properly. This will prevent the I/O pins from powering up before the core blocks, which can cause in-rush current during power up or bus contention and other malfunctions.

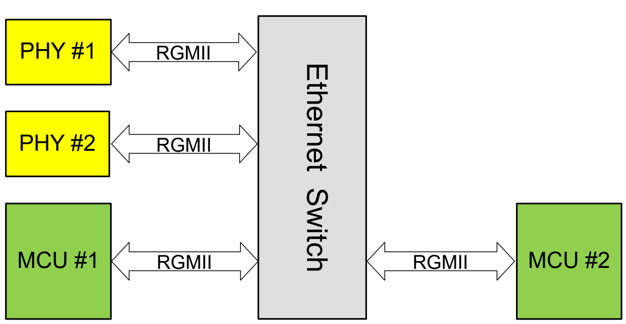


Figure 8-3. Multi-Core RGMII Communication

Low Dropout (LDO) devices are a common way to power up devices, but they do not provide any power sequencing features. As can be seen in Figure 8-4, before the 1.8 V can be applied to the MAC, the input of the LDO will need to come up first. This will result in the PHY powering up which can lead to in-rush current flowing into the MAC I/O pins.

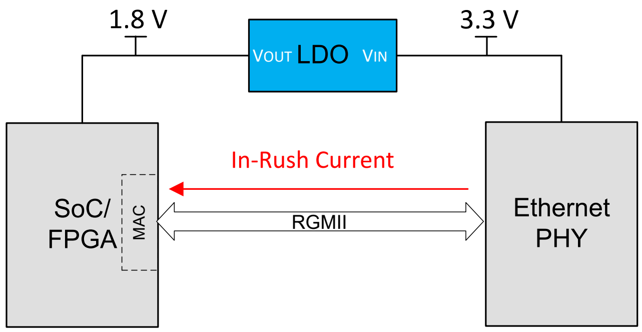


Figure 8-4. Residual Current Flowing Into MAC I/O Pins After PHY is Powered Up

With the TXV0106 supporting the $I_{off\text{-}float}$ feature, in-rush current from improper power sequencing can be prevented. When either power supply pin is at 0 V or below 100 mV, the I/O pins become high impedance until both pins go above 100 mV. The high impedance state will prevent any in-rush current from flowing to the opposite side.

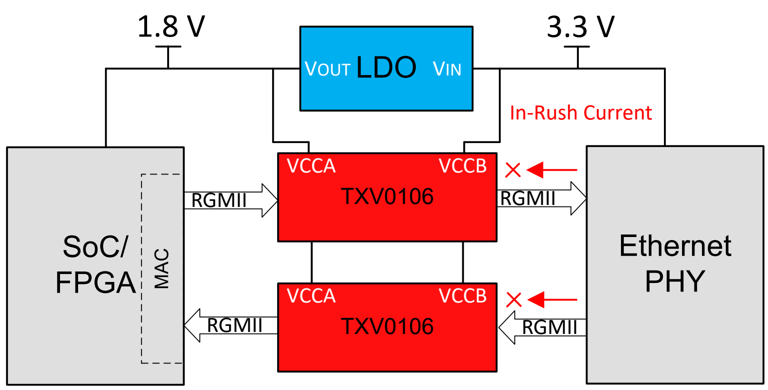


Figure 8-5. Using the TXV0106 for Power Isolation

For additional information on the TXV0106 and power isolation use cases, see the *Solving Power Sequencing Challenges for Ethernet RGMII Communications* application note.

8.4 Power Supply Recommendations

The TXV0106 uses two separate configurable power supply rails, V_{CCA} and V_{CCB}. The A port and B port are designed to track V_{CCA} and V_{CCB}, respectively, allowing for low-voltage fixed translation between any of the 1.8-V, 2.5-V and 3.3-V voltage nodes.

The output-enable $\overline{OE}$ input circuit is designed to be supplied by V_{CCA}. When the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To put the outputs in a high-impedance state during power up or power down, tie the $\overline{OE}$ input pin to V_{CCA} through a pullup resistor and do not be enable it until V_{CCA} and V_{CCB} are fully ramped and stable. The current-sinking capability of the driver determines the minimum value of the pullup resistor to V_{CCA}.

8.5 Layout

8.5.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines such as:

- Use short trace lengths to avoid excessive.
- Use bypass capacitors on the power supply pins and place them as close to the device as possible.
- A 0.1-μF bypass capacitor is recommended, but transient performance can be improved by having both 1-μF and 0.1-μF capacitors in parallel with the smallest value capacitor placed closest to the power pin.
- The high drive capability of this device creates fast edges into light loads. Routing and load conditions should be considered to prevent ringing.

8.5.2 Layout Example

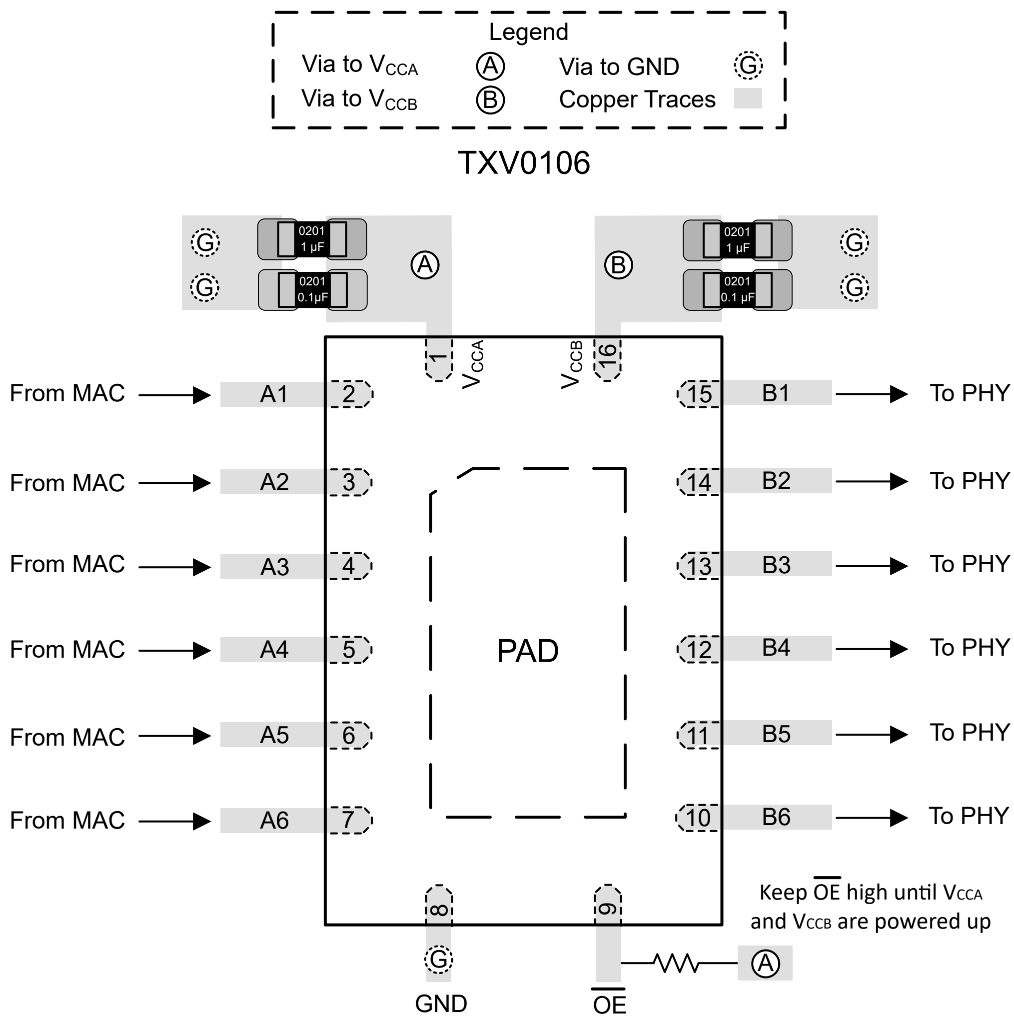


Figure 8-6. Layout Example – TXV0106

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Solving Power Sequencing Challenges for Ethernet RGMII Communications* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
December 2023	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXV0106BQBR	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TV106	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

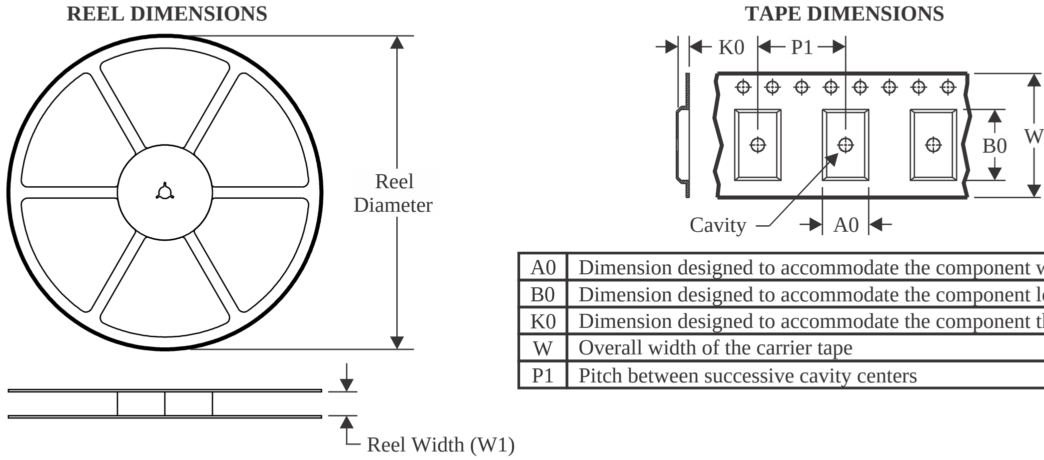
OTHER QUALIFIED VERSIONS OF TXV0106 :

- Automotive : TXV0106-Q1

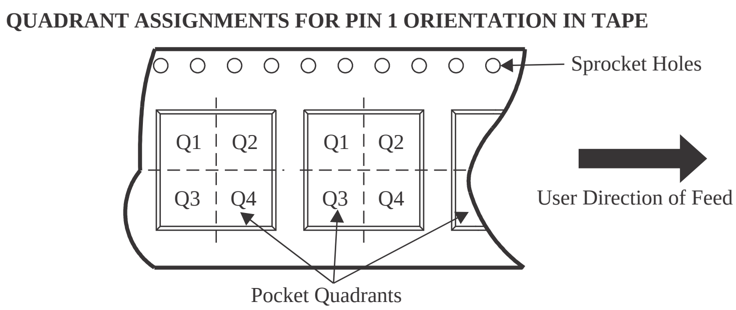
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



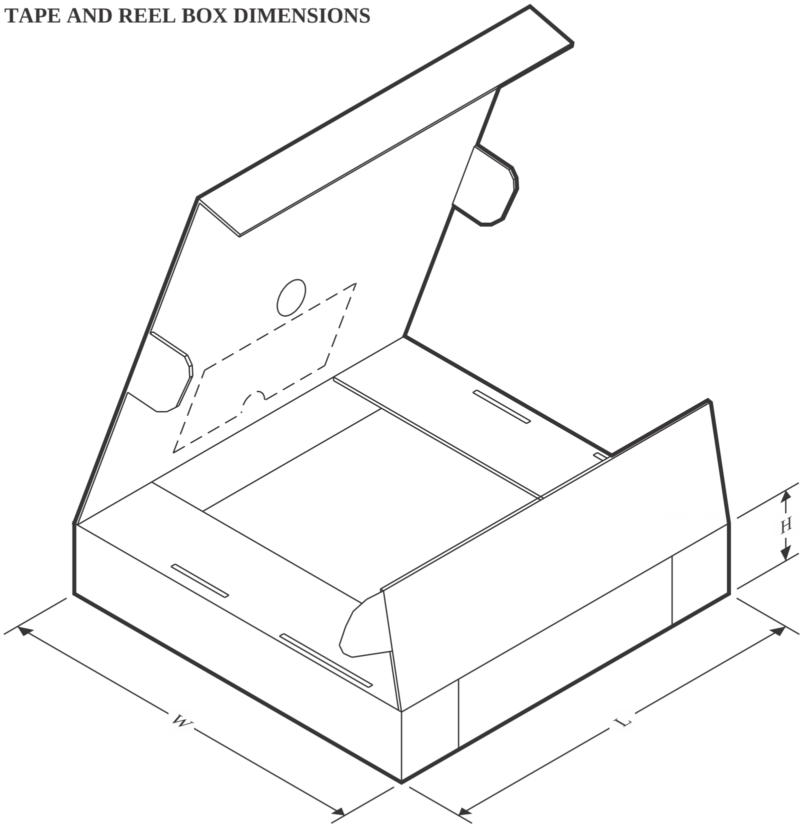
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXV0106BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXV0106BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0

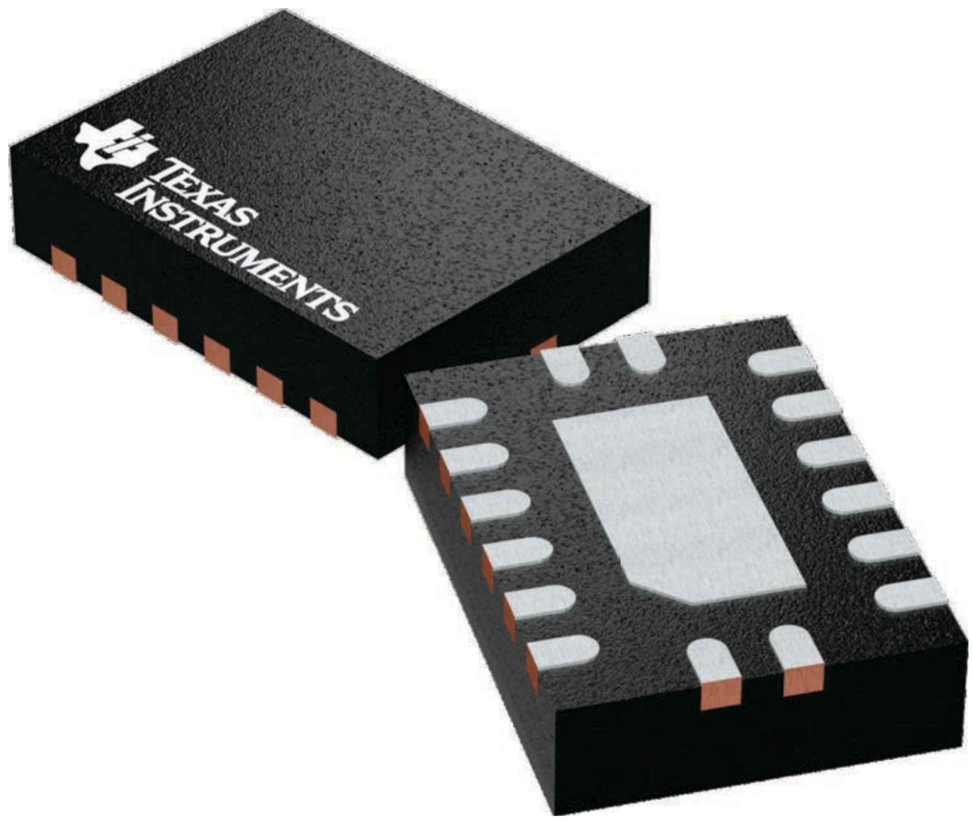
BQB 16

WQFN - 0.8 mm max height

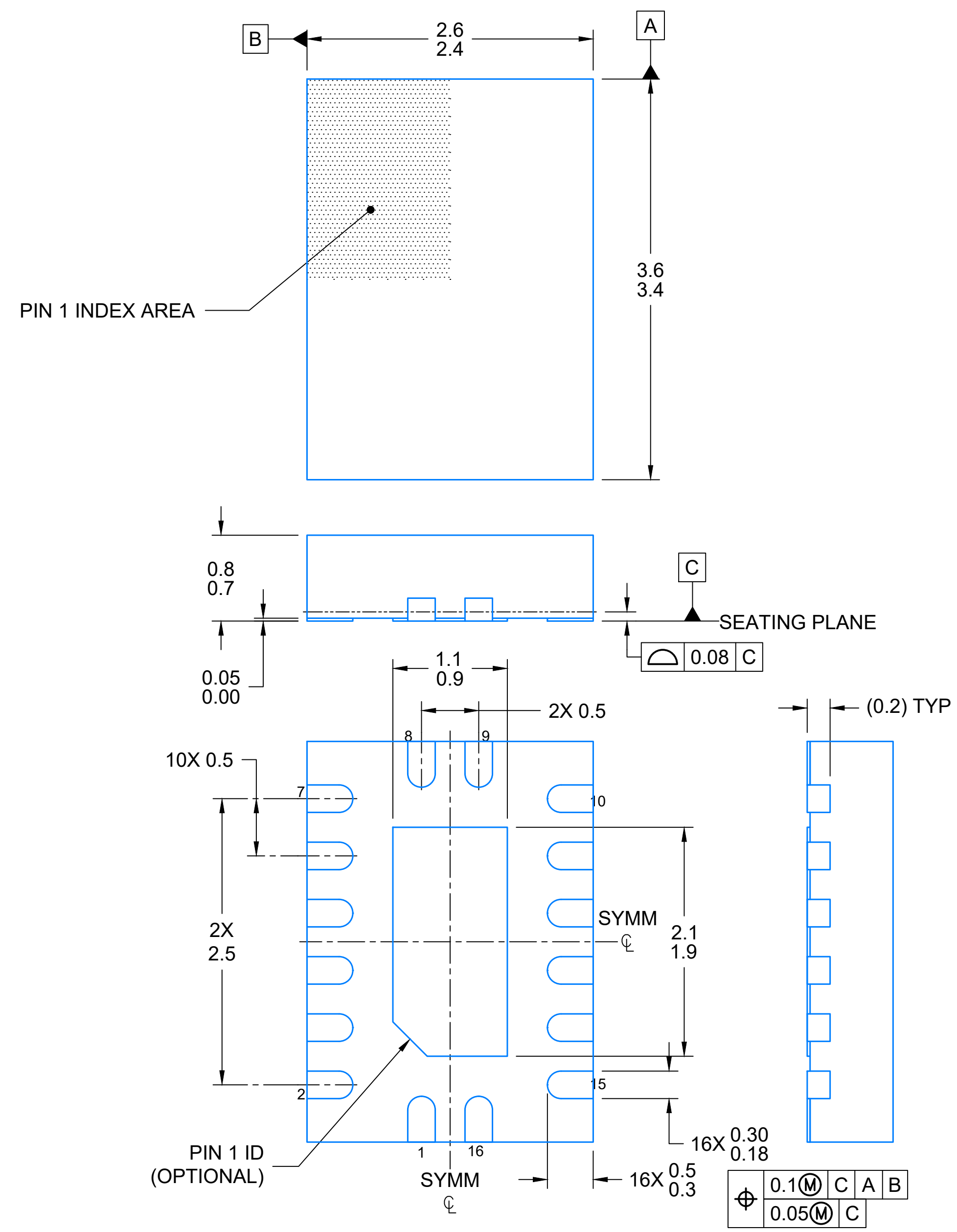
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

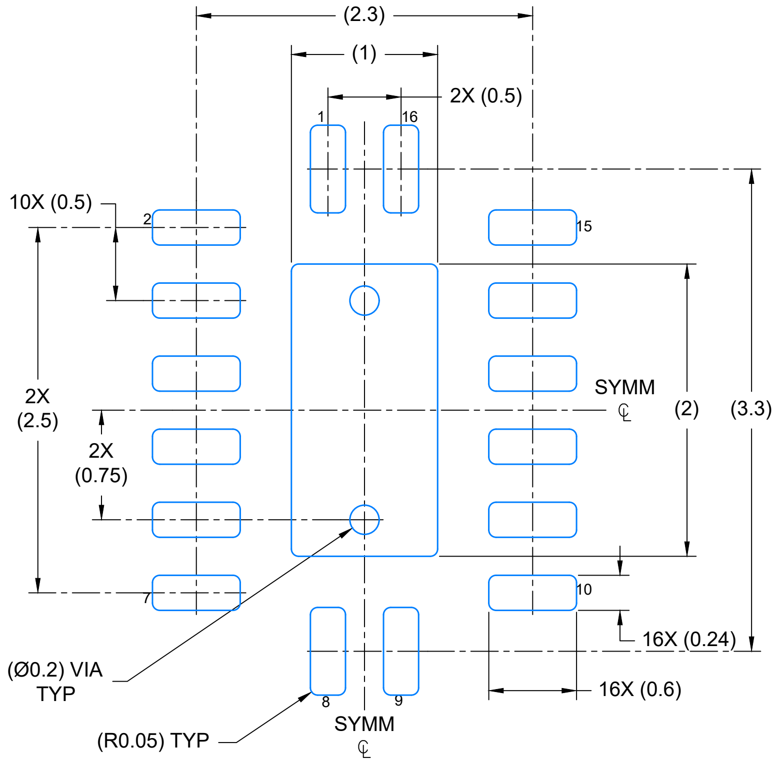


4226161/A

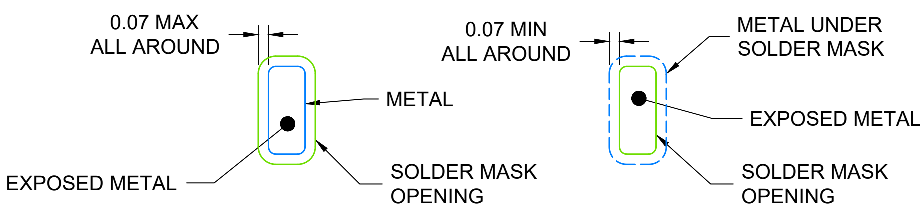


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

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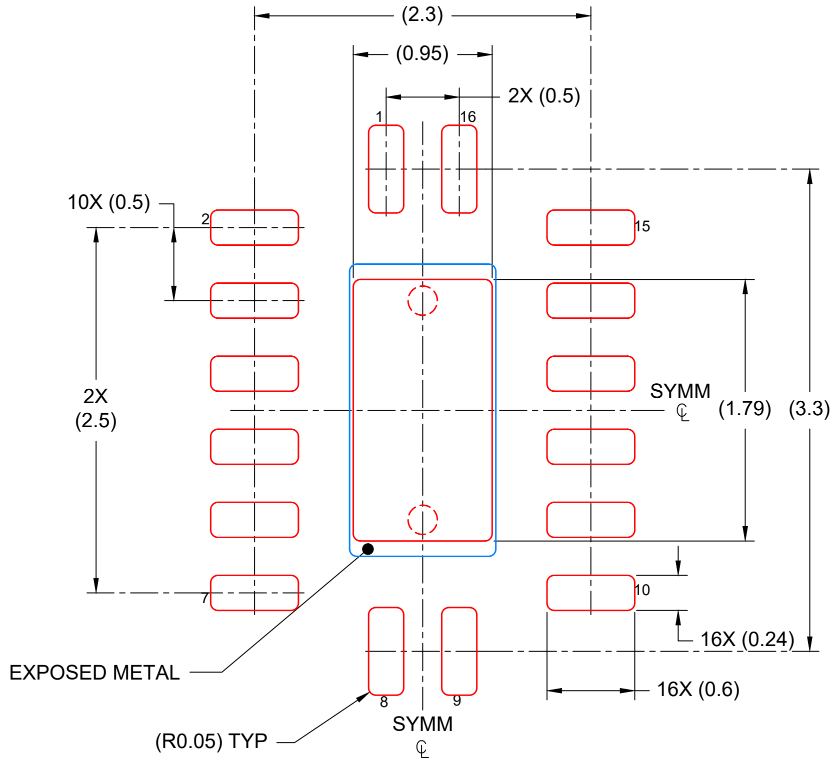
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265