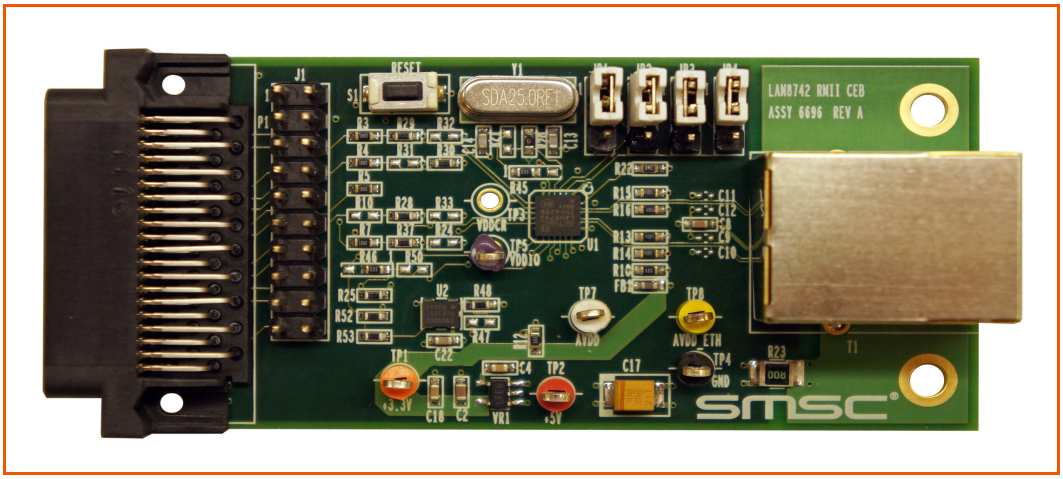
EVB8742 Evaluation Board User Manual



USER MANUAL

1 Introduction

The LAN8742A is a low-power, 10BASE-T/100BASE-TX physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3 and 802.3u standards. The LAN8742A supports communication with an Ethernet MAC via a standard RMII interface.

The EVB8742 is a PHY Evaluation Board (EVB) that interfaces a Reduced Media Independent Interface (RMII) MAC controller to the LAN8742A Ethernet RMII PHY via a 40-pin connector. The LAN8742A is connected to an RJ45 Ethernet jack with integrated magnetics for 10/100 connectivity. A simplified block diagram of the EVB8742 can be seen in Figure 1.1.

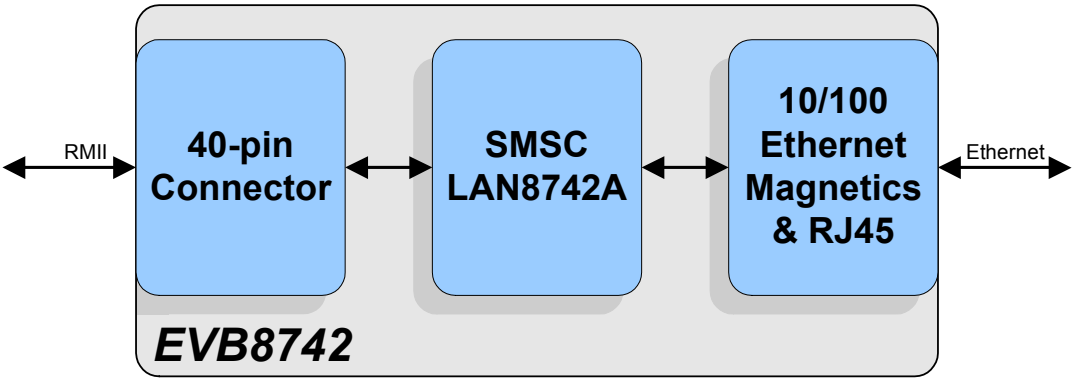


Figure 1.1 EVB8742 Block Diagram

1.1 References

Concepts and material available in the following documents may be helpful when reading this document. Visit www.smsc.com for the latest documentation.

- SMSC LAN8742A Datasheets
- AN 25.3 Migrating from the LAN8710A/LAN8720A to the LAN8740/LAN8741/LAN8742
- AN 8.13 Suggested Magnetics
- SMSC LAN8742A Evaluation Board Schematics

2 Board Details

This section includes the following EVB8742 board details:

- Power
- Configuration
- Mechanicals

2.1 Power

2.1.1 +5V Power

Power is normally supplied to the EVB8742's +3.3V regulator externally via the +5V power pins of the 40-pin connector. If desired, the EVB8742 can be powered without +5V present on the 40-pin connector (P1) by supplying +5V to the TP2 (red) test point with ground connected to the TP4 (black) test point.

Note: Before connecting an external power supply to TP2, ensure power is not present on the 40-pin connector's +5V pins. Connecting +5V simultaneously via the 40-pin connector and TP2 may result in permanent damage to the board.

2.1.2 VDDIO Power

The LAN8742A's VDDIO power may be supplied at a voltage other than +3.3V by depopulating resistor R12 and supplying +1.6V to +3.6V externally via test point TP5 (purple), with ground connected to the TP4 (black) test point.

Note: Before connecting an external power supply to TP5, ensure that resistor R12 has been removed. Connecting an external power supply to TP5 while resistor R12 is populated may result in permanent damage to the board.

2.1.3 +1.2V Power

The LAN8742A's internal +1.2V regulator can be optionally disabled. Refer to Section 2.2.4, "Internal +1.2V Regulator Configuration (REGOFF)," on page 7 for additional information.

2.2 Configuration

The following sub-sections describe the various board features and configuration settings. A top view of the EVB8742 is shown in Figure 2.1.

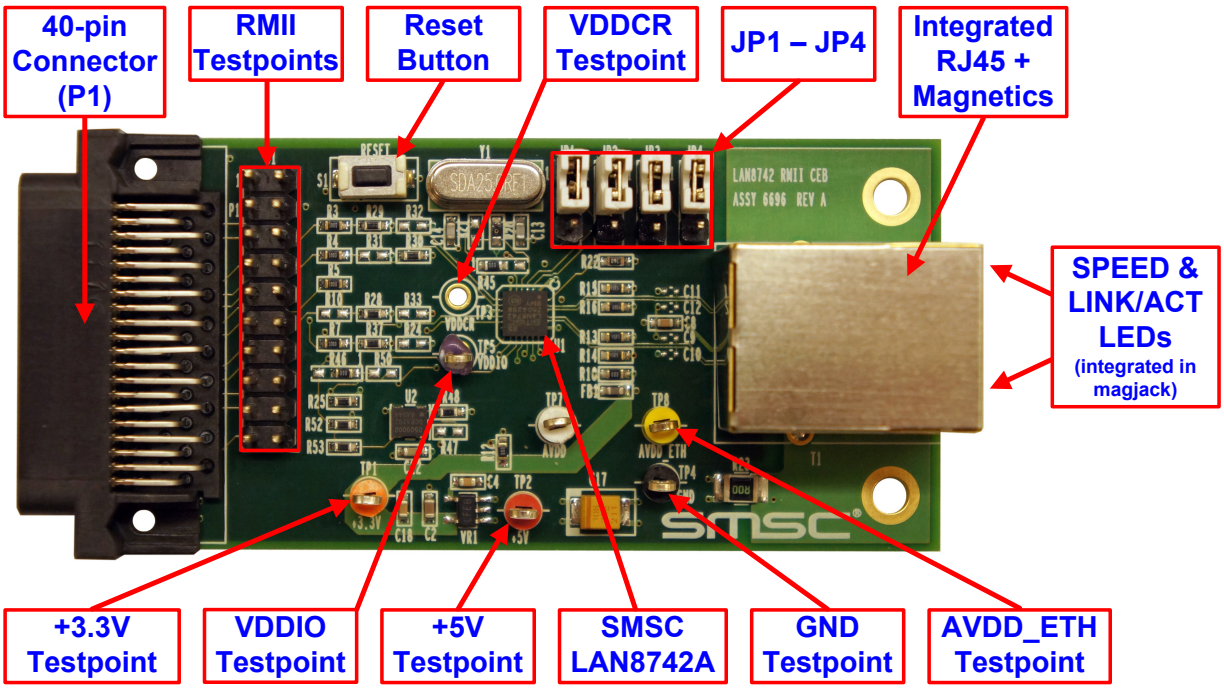


Figure 2.1 Top View of the EVB8742

2.2.1 PHY Address Configuration

The EVB8742 allows the user to configure the default PHY address at power-up via the PHYAD[0] configuration strap. Table 2.1 details the proper configuration required for each PHY address value. By default, PHYAD[0] is configured to a value of “0”.

Table 2.1 PHYAD[0] Resistor Configuration

PHYAD[0]	PHYAD[0] PULL-UP/DOWN RESISTORS	
	R24	R37
0 (Default)	*Depopulate*	**Populate**
1	**Populate**	*Depopulate*

2.2.2 Reset Mode Configuration

The EVB8742 can be configured to reset into a specific mode of operation at power-up via the MODE[2:0] configuration straps. Table 2.2 details the proper configuration required for each mode. By default, all EVB8742 MODE[2:0] straps are configured to a value of “1”.

Note: For additional details on each mode of operation, refer to the LAN8742A datasheet.

Table 2.2 MODE[2:0] Resistor Configuration

MODE[2:0]	MODE[2:0] PULL-UP/DOWN RESISTORS					
	MODE2		MODE1		MODE0	
	R28	R33	R29	R32	R30	R31
000 10BASE-T Half Duplex Auto-neg disabled	*Depopulate*	**Populate**	*Depopulate*	**Populate**	*Depopulate*	**Populate**
001 10BASE-T Full Duplex Auto-neg disabled	*Depopulate*	**Populate**	*Depopulate*	**Populate**	**Populate**	*Depopulate*
010 100BASE-TX Half Duplex Auto-neg disabled	*Depopulate*	**Populate**	**Populate**	*Depopulate*	*Depopulate*	**Populate**
011 100BASE-TX Full Duplex Auto-neg disabled	*Depopulate*	**Populate**	**Populate**	*Depopulate*	**Populate**	*Depopulate*
100 100BASE-TX Half Duplex Auto-neg enabled	**Populate**	*Depopulate*	*Depopulate*	**Populate**	*Depopulate*	**Populate**
101 Repeater mode	**Populate**	*Depopulate*	*Depopulate*	**Populate**	**Populate**	*Depopulate*
110 Power Down mode	**Populate**	*Depopulate*	**Populate**	*Depopulate*	*Depopulate*	**Populate**
111 (Default) All capable. Auto-neg enabled	**Populate**	*Depopulate*	**Populate**	*Depopulate*	**Populate**	*Depopulate*

2.2.3 Clocking and nINT/REFCLKO Pin Configuration (nINTSEL)

The nINT and REFCLKO functions share a common LAN8742A pin. This pin can operate in two functional modes: nINT (Interrupt) Mode and REFCLKO Mode. The nINTSEL configuration strap is used to select one of these two modes.

Additionally, the EVB8742 allows clock source selection in nINT mode, resulting in the three modes of operation detailed in Figure 2.2. In nINT mode, the clock can be sourced from the partner device or via the on-board 50MHz oscillator. In REFCLKO mode, the clock can only be sourced from the 25MHz on-board clock source. The EVB8742 must be properly configured for each mode as detailed in Table 2.3.

Note: The nINTSEL configuration strap shares functionality with LED2. Therefore, LED2 may function active-high or active-low depending on the nINTSEL configuration. For additional information on the functionality of the nINT/REFCLKO and LED2/nINTSEL pins, refer to the LAN8742A Datasheet and LAN8742A schematics.

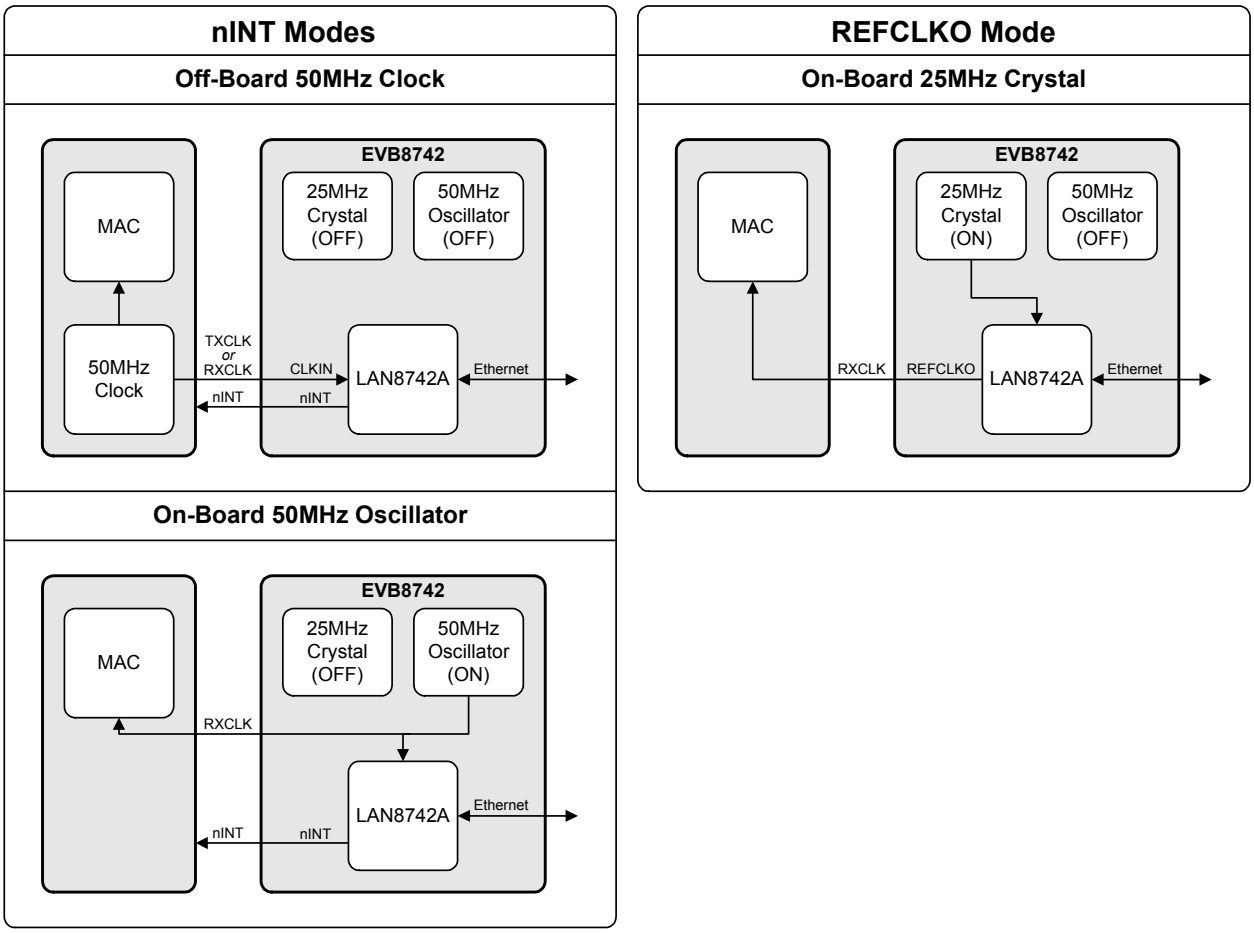


Figure 2.2 EVB8742 nINT & REFCLKO Modes of Operation

Table 2.3 nINT/REFCLKO Modes Resistor Configuration

FUNCTIONAL MODE		RELATED RESISTORS							
		R20	JP3,JP4	R45	R46	R47	R48	R49	R50
nINT Mode Off-Board 50MHz Clock (Note 2.1)	via TXCLK	*Depopulate*	*Depopulate 1-2* **Populate 2-3**	*Depopulate 1-2* *Depopulate 2-3*	*Depopulate 1-2* *Depopulate 2-3*	*Depopulate*	**Populate**	**Populate**	**Populate**
	via RXCLK	*Depopulate*	*Depopulate 1-2* **Populate 2-3**	*Depopulate 1-2* **Populate 2-3**	*Depopulate 1-2* **Populate 2-3**	*Depopulate*	**Populate**	*Depopulate*	**Populate**
nINT Mode On-Board 50MHz Osc.		*Depopulate*	*Depopulate 1-2* **Populate 2-3**	*Depopulate 1-2* **Populate 2-3**	*Depopulate 1-2* **Populate 2-3**	**Populate**	*Depopulate*	*Depopulate*	**Populate**
REFCLKO Mode On-Board 25MHz Crystal (Default)		**Populate**	**Populate 1-2** *Depopulate 2-3*	**Populate 1-2** *Depopulate 2-3*	**Populate 1-2** *Depopulate 2-3*	*Depopulate*	**Populate**	*Depopulate*	*Depopulate*

Note 2.1 The off-board 50MHz clock can be routed to the CLKIN pin of the LAN8742A via the TXCLK or RXCLK pin of the 40-pin connector. The related resistors must be populated as shown for each mode.

2.2.4 Internal +1.2V Regulator Configuration (REGOFF)

The LAN8742A provides the ability to disable the internal +1.2V regulator. When the regulator is disabled, an external +1.2V must be supplied to the VDDCR pin (via TP3). Configuration of the internal regulator is controlled by the REGOFF configuration strap. The EVB8742 must be properly configured for each mode as follows:

Internal +1.2V Regulator Enabled (Default EVB8742 Mode)

- Depopulate the 2-3 positions of JP1 and JP2.
- Populate the 1-2 positions of JP1 and JP2 to pull-down the REGOFF strap (enable regulator).

Internal +1.2V Regulator Disabled

- Depopulate the 1-2 positions of JP1 and JP2.
- Populate the 2-3 positions of JP1 and JP2 to pull-up the REGOFF strap (disable regulator).

Note: The REGOFF configuration strap shares functionality with LED1. Therefore, LED1 may function active-high or active-low depending on the REGOFF configuration. For additional information on the LED1/REGOFF pin and the disabling of the internal 1.2V regulator (power sequencing requirements, etc.), refer to the LAN8742A Datasheet and LAN8742A schematics.

2.2.5 LEDs

Table 2.4 LEDs

REFERENCE	COLOR	INDICATION
LED1	Green	Link/Activity Active when the PHY has established a valid link with a link partner and blinks when activity is detected.
LED2	Yellow	Speed Active when a 100BASE-TX link has been established. Inactive when a 10BASE-T link has been established or during line isolation.

Note: LED1 and LED2 are located inside the RJ45 connector. LED1 and LED2 may function active-high or active-low depending on the configuration of the REGOFF and nINTSEL straps, respectively. Refer to the LAN8742A Datasheet and LAN8742A schematics for additional information.

2.2.6 Test Points

Table 2.5 Test Points

TEST POINT	DESCRIPTION	CONNECTION
TP1	+3.3V Test Point (Orange)	+3.3V
TP2	+5.0V Test Point (Red)	+5.0V
TP3	+1.2V VDDCR Test Point (Unpopulated) (Note 2.2)	+1.2V
TP4	Ground Test Point (Black)	Ground
TP5	VDDIO Test Point (Purple)	+3.3V (Note 2.3)
TP7	AVDD Test Point (White)	AVDD
TP8	AVDD_ETH Test Point (Yellow)	AVDD_ETH

Note 2.2 VDDCR is the internal +1.2V regulated output. When REGOFF is enabled, the internal 1.2V regulator is disabled. In this case, an external 1.2V regulator must be supplied to test point TP3.

Note 2.3 The LAN8742A's VDDIO power may be supplied externally at a voltage other than +3.3V as described in Section 2.1, "Power," on page 3.

2.2.7 System Connections

Table 2.6 System Connections

PLUG/HEADER	DESCRIPTION	PART
T1	RJ45 with Integrated LEDs	Pulse J0011D01BNL
J1	2x10 RMII Header **Note:** Refer Table 2.7 to for a full pin list	Adam Tech PH2-20-U-A
P1	40-pin Female Connector **Note:** Refer Table 2.8 to for a full pin list	Tyco 5173278-2

Table 2.7 J1 - 2x10 RMII Header Pinout

HEADER PIN	DESCRIPTION	HEADER PIN	DESCRIPTION
1	+3.3V	11	nINT (Note 2.6)
2	VDDIO	12	TXCLK (Note 2.7)
3	nRST	13	TXEN
4	No Connect	14	Ground
5	MDC	15	TXD0
6	MDIO (Note 2.4)	16	Ground
7	RXD1/MODE1	17	TXD1
8	RXD0/MODE0	18	Ground
9	RXER/PHYAD0	19	CRS_DV/MODE2
10	RXCLK (Note 2.5)	20	Ground

Note 2.4 Resistor R11 acts as a pull-up on the MDIO pin. In most situations, the MAC circuitry provides this pull-up and R11 is not required.

Note 2.5 The functionality of pin 10 depends on the configured mode of operation. Pin 10 will be driven by REFCLKO in the REFCLKO mode of operation. In the nINT on-board 50MHz oscillator mode, pin 10 will be driven by the EVB8742's on-board 50MHz oscillator. In the nINT off-board 50MHz clock mode, pin 10 is either unconnected (50MHz clock provided by the partner device via the TXCLK pin) or used to provide the 50MHz clock to the CLKIN pin of the LAN8742A. Refer to Section 2.2.3, "Clocking and nINT/REFCLKO Pin Configuration (nINTSEL)," on page 6 and the LAN8742A schematic for additional information.

Note 2.6 The functionality of pin 11 depends on the configured mode of operation. Pin 11 will be driven by nINT in the nINT modes of operation. In the REFCLKO modes of operation, pin 11 will be unconnected. Refer to Section 2.2.3, "Clocking and nINT/REFCLKO Pin Configuration (nINTSEL)," on page 6 and the LAN8742A schematic for additional information.

Note 2.7 When configured for nINT off-board 50MHz clock mode via TXCLK, pin 12 is connected to the XTAL1/CLKIN pin of the LAN8742A. Pin 12 is unconnected in all other modes of operation. Refer to Section 2.2.3, "Clocking and nINT/REFCLKO Pin Configuration (nINTSEL)," on page 6 and the LAN8742A schematic for additional information.

Table 2.8 P1 - 40-Pin Female MII Connector Pinout

PIN	DESCRIPTION	PIN	DESCRIPTION	PIN	DESCRIPTION	PIN	DESCRIPTION
1	+5V	11	No Connect	21	+5V	31	GND
2	MDIO	12	TXCLK (Note 2.9)	22	GND	32	GND
3	MDC	13	TXEN	23	GND	33	GND
4	No Connect	14	TXD0	24	GND	34	GND
5	No Connect	15	TXD1	25	GND	35	GND
6	RXD1	16	No Connect	26	GND	36	GND
7	RXD0	17	No Connect	27	GND	37	GND
8	RXDV	18	No Connect	28	GND	38	GND
9	RXCLK (Note 2.8)	19	CRS	29	GND	39	GND
10	RXER	20	+5V	30	GND	40	+5V

Note 2.8 The functionality of pin 9 depends on the configured mode of operation. Pin 9 will be driven by REFCLKO in the REFCLKO mode of operation. In the nINT on-board 50MHz oscillator mode, pin 9 will be driven by the EVB8742's on-board 50MHz oscillator. In the nINT off-board 50MHz clock mode, pin 9 is either unconnected (50MHz clock provided by the partner device via the TXCLK pin) or used to provide the 50MHz clock to the CLKIN pin of the LAN8742A. Refer to Section 2.2.3, "Clocking and nINT/REFCLKO Pin Configuration (nINTSEL)," on page 6 and the LAN8742A schematic for additional information.

Note 2.9 When configured for nINT off-board 50MHz clock mode via TXCLK, pin 12 is connected to the XTAL1/CLKIN pin of the LAN8742A. Pin 12 is unconnected in all other modes of operation. Refer to Section 2.2.3, "Clocking and nINT/REFCLKO Pin Configuration (nINTSEL)," on page 6 and the LAN8742A schematic for additional information.

2.2.8 Switches

Table 2.9 Switches

SWITCH	DESCRIPTION	FUNCTION
S1	Reset switch	When pressed, triggers a board reset.

2.3 Mechanicals

Figure 2.3 details the EVB8742 mechanical dimensions.

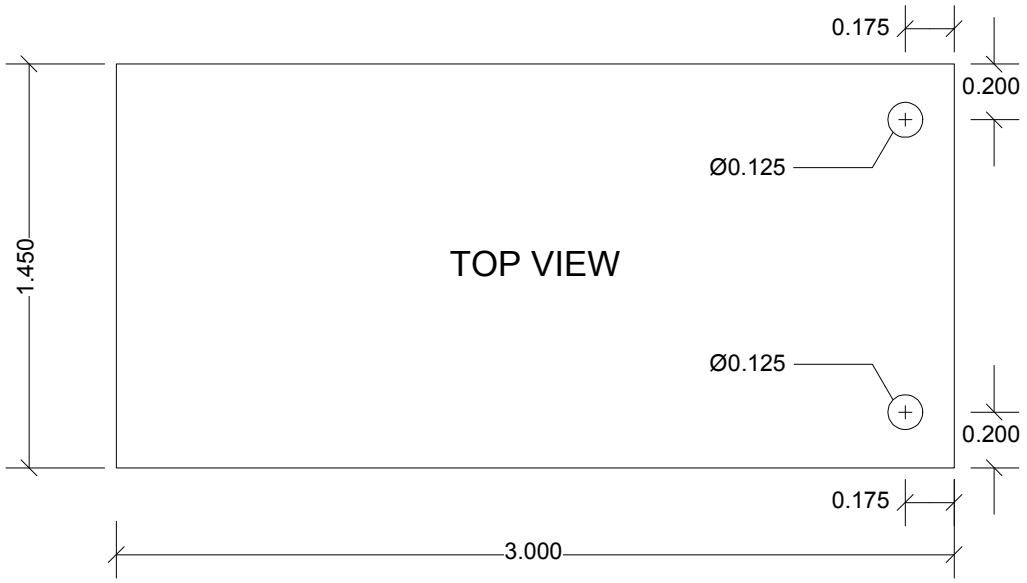


Figure 2.3 EVB8742 Mechanicals

3 User Manual Revision History

Table 3.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.0 (04-29-13)	All	Initial release.