

# An Energy Efficient CMOS Sub-THz Interconnect with Surface Plasmonic Converter and Oscillator

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## ABSTRACT

Free-space EM-wave based GHz interconnect suffering significant loss and narrow bandwidth cannot be deployed as low-power and dense I/Os for future network-on-chip (NoC) integration of many-core and memory. This paper proposes an energy-efficient and low-crosstalk sub-THz (0.1T-1T) I/O using surface-plasmonic based interconnects and oscillator in CMOS. By introducing sub-wavelength periodic corrugation structure onto transmission line with gradient groove, the surface-plasmonic is established to propagate signal that is strongly localized on surface of top-layer metal wire. A mode conversion from guided wave to surface wave is carefully designed considering low loss and efficient impedance/momentum matching at mm-wave to THz frequencies. As such, significant power saving and cross-talk reduction can be observed with high communication bandwidth. In addition, a low phase noise surface-plasmonic oscillator with high- $Q$  resonator is also proposed. The phase noise is -116dBc/Hz at 10MHz offset under 0.7V power supply by consuming only 3.5mW power. As designed in 65nm CMOS, the results have shown that the proposed surface-plasmonic I/O interface achieves 25Gbps data rate and 0.01pJ/bit/mm energy efficiency at 140GHz carrier frequency over 20mm dual surface-plasmonic channels.

## Keywords

CMOS; Terahertz; surface plasmon polariton; transmission line; converter; oscillator; metamaterial; I/O.

## 1. INTRODUCTION

Future high performance computers require wideband on-chip communication between microprocessor cores and memory. In order to realize a network on-chip (NoC) with 1000 of cores, it requires supporting wide bandwidth on-chip communication (>20Gbps) with low energy consumption (<0.1pJ/bit/mm).

RF-interconnect (RF-I) is a competitive solution owing to its low latency and large bandwidth [1]. In contrast to traditional voltage

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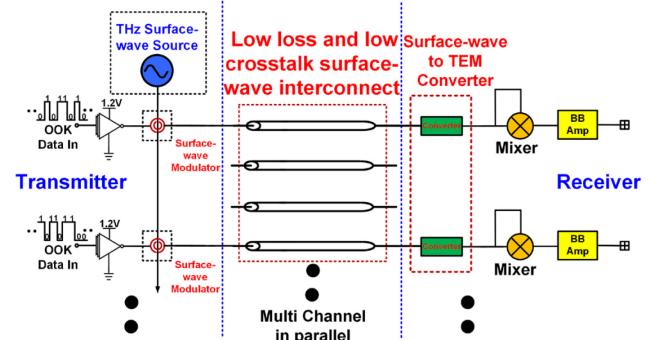
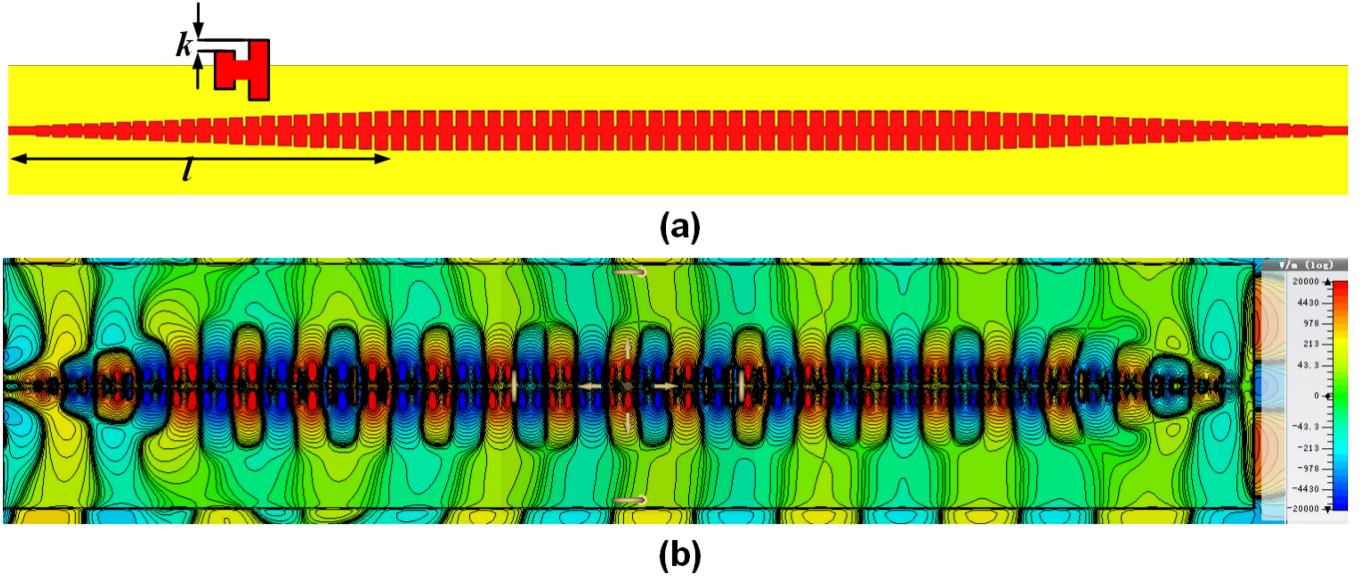


Fig. 1 The proposed multi-channelled on-chip I/O transceiver with: 140GHz surface-plasmonic oscillator, SRR-based modulator [6], surface-plasmonic interconnects (including mode converter and surface-plasmonic T-lines based channel), self-mixing mixer and multi-stage baseband (BB) amplifier.

signaling in baseband [2-4], RF-I basically transmits electromagnetic (EM) wave along the transmission line (T-line). The distinction of individual “0” and “1” can be simply achieved by ASK modulation. Compared to optical on-chip communication by optical I/O link, the RF-I building blocks can be all built in CMOS with carrier frequency already scaled up to millimeter-wave and sub-THz frequency region [5, 6]. Recent works have demonstrated multi-channelled RF-I to leverage much larger bandwidth utilization. However, the CMOS BEOL used in fine-pitch silicon interconnect for RF-I are highly field-delocalized at high frequencies, resulting in large channel loss and narrow bandwidth. Moreover, in order to fulfill certain BER requirement, the data rate will be ultimately limited by the low phase noise of on-chip oscillator at THz frequencies.

This paper explores the realization of CMOS multi-channelled I/O by *surface-plasmonic* interconnects (including T-lines and converter) and oscillator at sub-THz, to achieve high data rate with high energy efficiency. The CMOS 140GHz surface-plasmonic I/O transceiver architecture is shown in Fig. 1, which accommodates multiple sub-THz TRx links in parallel. The contributions of this work are summarized as follows:

- Proposed a surface-plasmonic T-line converter on the basis of spoof surface plasmonic polariton (SPP) with periodic groove on metal film. As such, the propagation of surface-confined EM-wave mode is adapted to the curvature of the surface. By introducing gradient grooves, mode conversion between conventional TEM and the surface mode could be efficiently



**Fig. 2 (a)** The proposed SPP T-line with mode converter structure featured by smoothly gradient grooves, while parameter  $k$  denotes the gradient factor, **(b)** the simulated  $E_x$  component evaluated at the  $xy$  plane demonstrating the mode evolution by the proposed converter structure.

achieved with low loss within compact area. Due to low loss and wide bandwidth when using surface-plasmonic as signal traces, significant power reduction can be achieved with no additional equalization circuit that is required for free EM-wave based RF-I.

- Introduced an on-chip passive surface-plasmonic resonator which evolves from a stacked split-ring-resonator (SRR) [6] structure. By simultaneously incorporating the sub-wavelength grooves into the SRR, electrical field ( $E$ -field) is more tightly confined achieving better  $Q$ -factor of resonance. The residue electric dipole is strongly suppressed while the magnetic dipole is enhanced, leading to less electromagnetic loss at sub-THz. One 140GHz oscillator is designed by employing the proposed surface plasmonic resonator, demonstrating low phase noise (-116dBc/Hz at 10MHz offset) with only 3.5mW power consumption.

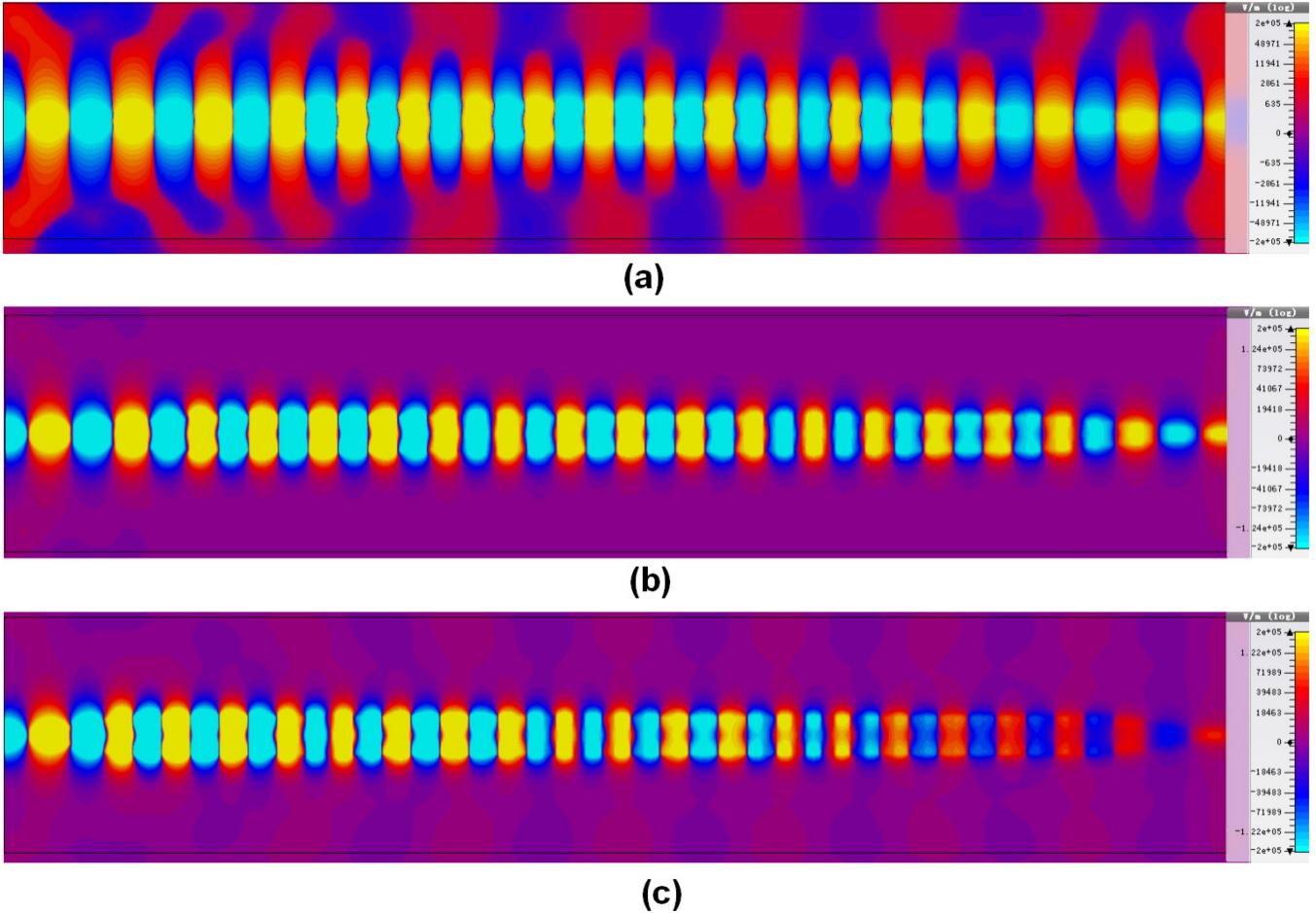
As such, with wideband low loss and high conversion efficiency of channels, and low phase noise of surface-plasmonic oscillator, the sub-THz I/O transceiver is designed in 65nm CMOS with 25Gbps data rate communication and 0.01pJ/bit/mm efficiency, better than all existing on-chip interconnect. In the remaining of the paper, the surface-plasmonic interconnects will be presented in section II, while the surface-plasmonic oscillator is introduced in section III. The whole sub-THz surface-plasmonic I/O design is revealed in section IV with results. The paper is concluded in section V.

## 2. SURFACE-WAVE INTERCONNECTS

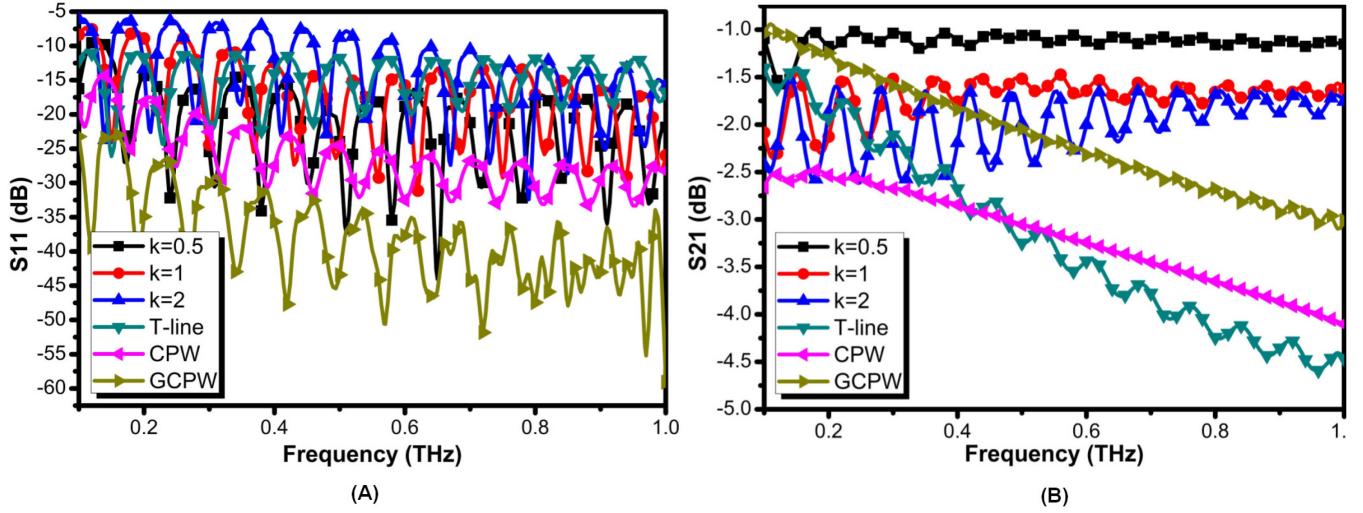
The sub-THz interconnect based channel in this paper works with the surface-wave. Due to the negative permittivity behavior, surface plasmon polaritons (SPP) is one special electromagnetic wave (surface-wave) locally confined onto the metal/dielectric interface, propagating in parallel to the interface with exponentially decaying in the direction perpendicular to the interface. By introducing sub-wavelength periodic corrugation structure into the T-line, surface-waves can be excited to propagate signals with strong field confinement at frequencies up to THz [5]. As such, one can achieve the minimum EM-coupling or loss to substrate and also to neighbor wires in surface-wave mode than the use of the

traditional free-space TEM-wave mode. Previous work has demonstrated the wideband low loss transmission by surface-plasmonic interconnect as silicon channel with minimized channel crosstalk at mm-wave to THz frequency in CMOS [5].

Mode conversion from the surface wave back to conventional TEM wave is generally required for further data processing at the Rx side. Both impedance and momentum must be matched at the interface in order to obtain high conversion efficiency. Fig. 2(a) shows the mode conversion structure proposed in this work, in which the periodic sub-wavelength grooves form the surface-wave T-line delivering highly confined surface-wave, while the grooves depth gradually evolve to realize momentum matching at the mode conversion interface. The periodical pitch  $d$  of the surface plasmonic converter is chosen as 15 $\mu\text{m}$  to create strong field confinement at sub-THz region, and the groove gap  $a$  is 2.4 $\mu\text{m}$  with line width of 5 $\mu\text{m}$ , to ensure the propagation length larger than 20mm at 140GHz [5]. Note that the  $E$ -field confinement is strongly dependent on the groove depth  $h$ , so the gradient groove technique provides a simple yet efficient way to maintain high efficiency of conversion and transmission. Considering that the coplanar waveguide (CPW) structure proposed by our previously work consumes too much of silicon area [7], the plasmonic structure should be therefore simplified by omitting the CPW part, while the line width  $w$  needs to be tuned accordingly to maintain impedance matching at low frequencies. With the line width of 5 $\mu\text{m}$ , the reflection coefficient could reach -10dB and below [7]. More importantly, the mode conversion can be still realized by the gradient groove, which is easy to implement on-chip. Such a design is depicted in Fig. 2(a) with the bottom copper metal M1 as the ground plane as well. Here, the conversion efficiency depends only on the gradient factor  $k$  and line width  $w$ . Fig. 2(b) illustrates the  $E$ -field ( $E_x$  component) distribution for the simplified version evaluated in the  $xy$  plane at 2THz. As observed, the  $E_x$  component starts with small amplitude but gradually increases to its maxima over a long distance transmission. At the TEM wave injection interface, the structure degenerates to a microstrip line whose impedance is mainly governed by the line width while it supports quasi-TEM waves with a wave vector  $k_0$  (wave vector in the free



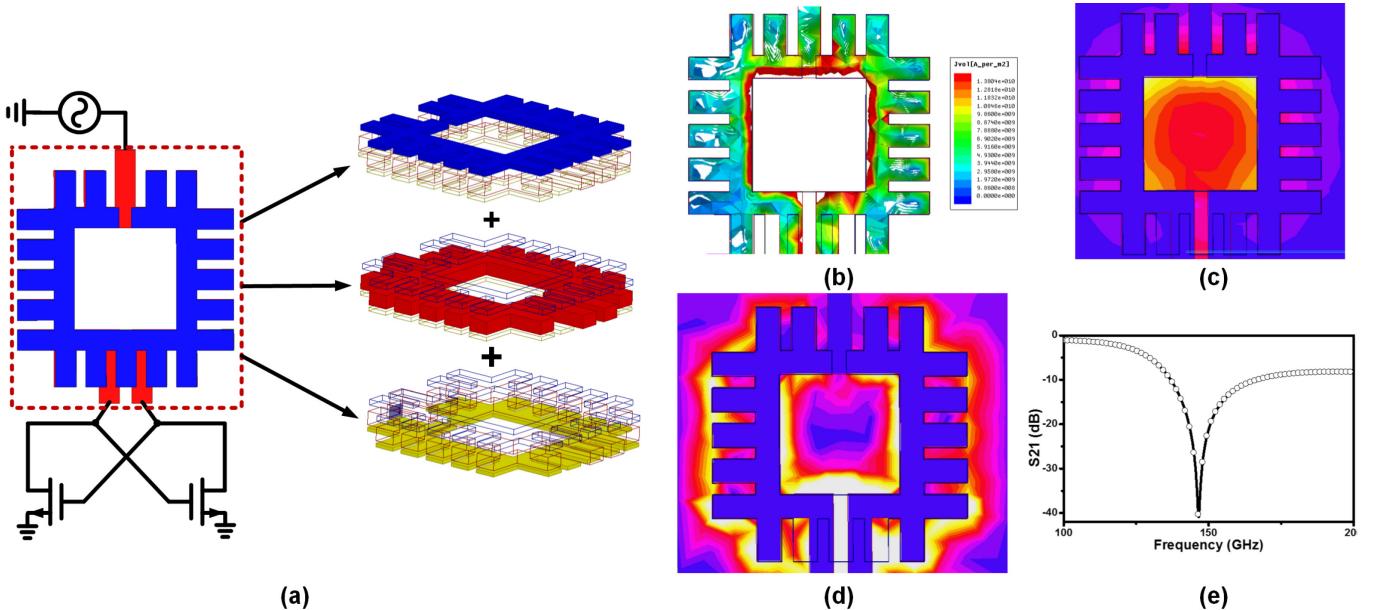
**Fig. 3** (a) The simulated near-field result of  $E_y$  component evaluated at the  $xy$  plane for the proposed SPP T-line with gradient groove converter structure: (a)  $k=0.5\mu\text{m}$ , (b)  $k=1\mu\text{m}$ , and (c)  $k=2\mu\text{m}$ .



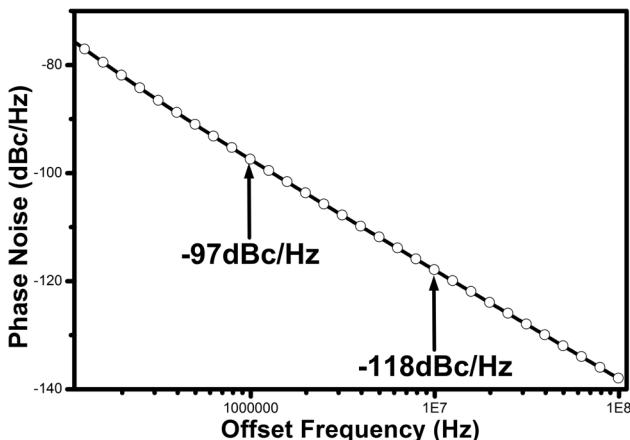
**Fig. 4** Simulated input reflection coefficient ( $S_{11}$ ) of the designed on-chip SPP T-line with converter for different  $k$  with  $d = 12.4 \mu\text{m}$ ,  $a = 2.4\mu\text{m}$ ,  $w = 5\mu\text{m}$ , and (b) simulated transmission coefficient ( $S_{21}$ ) of the designed on-chip SPP T-line with converter for different  $k$ . Conventional waveguide T-line (microstrip), CPW and grounded planar waveguide (GCPW) are incorporated as well for comparison.

space). As the guided modes are bounded to either the metal surface or surrounding ground, the low frequency transmission is expected to be degraded. By gradually enlarging the groove depth  $h$ , the

quasi-TEM modes are smoothly transformed to the bounded mode with larger  $k_x$ , and the resulting  $E_x$  component significantly demonstrates the tight confinement of SPPs. The SPP modes are



**Fig. 5** (a) The proposed sub-THz surface-plasmonic oscillator, (b) current density, (c)  $M$ -field (d)  $E$ -field distribution of the proposed surface-plasmonic resonator, (e) insertion loss the surface-plasmonic resonator demonstrating huge reflection at resonance.



**Fig. 6** The simulated phase noise of the proposed surface-wave oscillator at 140GHz.

now highly localized by the grooves with short decaying length, and propagate with low loss. The receiving part simply decreases the groove depth in a linear manner, so that the bounded modes are converted back to quasi-TEM modes for receiving by subsequent  $50\Omega$  system.

To see how the gradient factor  $k$  impacts the conversion efficiency, Fig. 3 illustrates the  $E$ -field distribution at the  $xy$  plane ( $E_z$  components). With  $k=2$  ( $\mu\text{m}$ ), the grooves seem to have an abrupt change that leads to larger loss compared to gentle evolution of groove. With  $k=0.5$ , the surface-plasmonic T-line smoothly converted the conventional TEM mode (guided mode) to the bounded mode with low loss and hence longer propagation length. Fig 4(a) illustrates the simulated reflection coefficient ( $S_{11}$ ) for various T-line structures. The reflection and transmission of the proposed surface-plasmonic T-line and three dominant on-chip interconnect structures, namely, T-line, CPW and GCPW, all have been designed and optimized for mm-wave to THz applications. All conventional structures supporting quasi-TEM modes clearly demonstrates wideband impedance matching up to 500GHz.

However, the plasmonic waveguides with abrupt gradient  $k$  suffers from large reflection, while a smaller  $k$  such as  $0.5\mu\text{m}$  provides sufficient low reflection over wideband. As such, by simply tuning the gradient factor  $k$  the on-chip plasmonic waveguides can avoid the use of GCPW as conversion. With broadband impedance matching, the transmissions could be fairly compared. First, as shown in Fig. 4(b), the plasmonic waveguide suffer from a slightly increase of loss in the low frequency region mainly due to impedance mismatch, as expected. For example, the case with  $k=1$  for the plasmonic design has an insertion loss of around  $-1.5\text{dB}$  at 400GHz, while it degenerates to  $-2.3\text{dB}$  with large ringing for the design with  $k=2$ , as expected. For  $k=0.5$ , however, the insertion loss is only  $-1\text{dB}$  at 400GHz, demonstrating high conversion efficiency. For  $k>1$ , the two designs experiences similar results as they both encounter impedance mismatch at same extent in the low frequency region. It is interesting to note that, the transmission of plasmonic waveguide are not necessarily better than conventional counterparts, while they are obviously much better as frequency goes up, as long as impedance/momentum matching attained. With slower gradient increment in the conversion part, the transmission efficiency is found to be better over a very broad band. These observations demonstrate the wideband low loss transmission by SPP T-line even with TEM wave injection and receiving. The proposed SPP T-line with converters demonstrates high and flat transmission coefficient from 400GHz to 1THz, and no transmission degradation found in high frequency region. Among traditional waveguide the CPW structure has relatively lower loss compared to CPW and T-line as it inherently acquires better field restriction among grounds. However, it is sensitive to skin and proximity effects at high frequencies for which the current density is large with severer Ohmic loss. The current tends to crowd on the metal surface with more energy radiated outward into the dielectric. These in turn show the leaky field confinement of conventional waveguide structures and therefore they are not desired in sub-THz.

### 3. SURFACE-PLASMONIC OSCILLATOR

To omit the mode converter at the Tx side, the source generator is desirably constructed by surface-plasmonic components. The

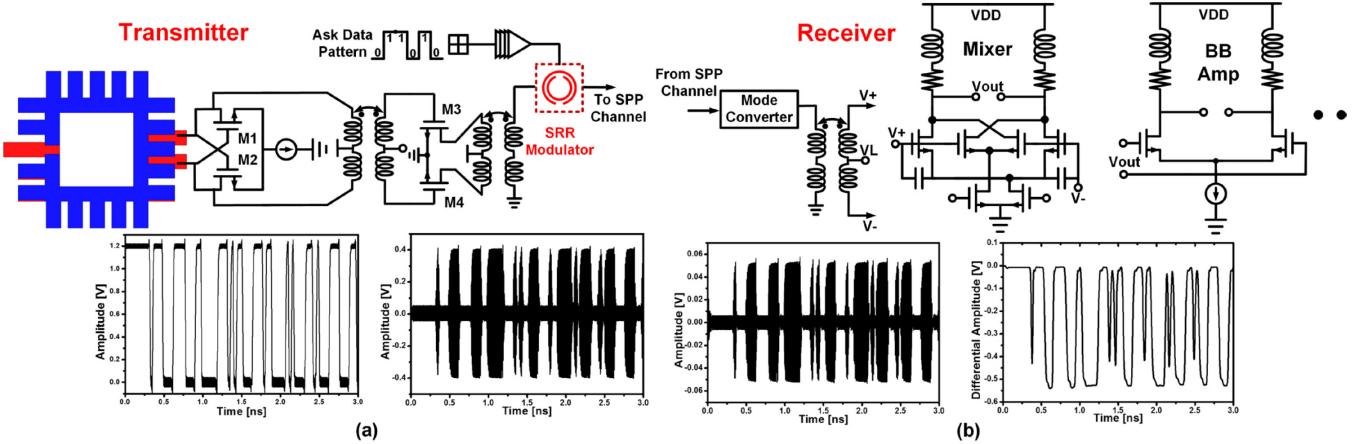


Fig. 7 TRx architecture: (a) the transmitter by using ASK modulation and the simulated time-domain waveform, and (b) receiver architecture and simulated time-domain waveform.

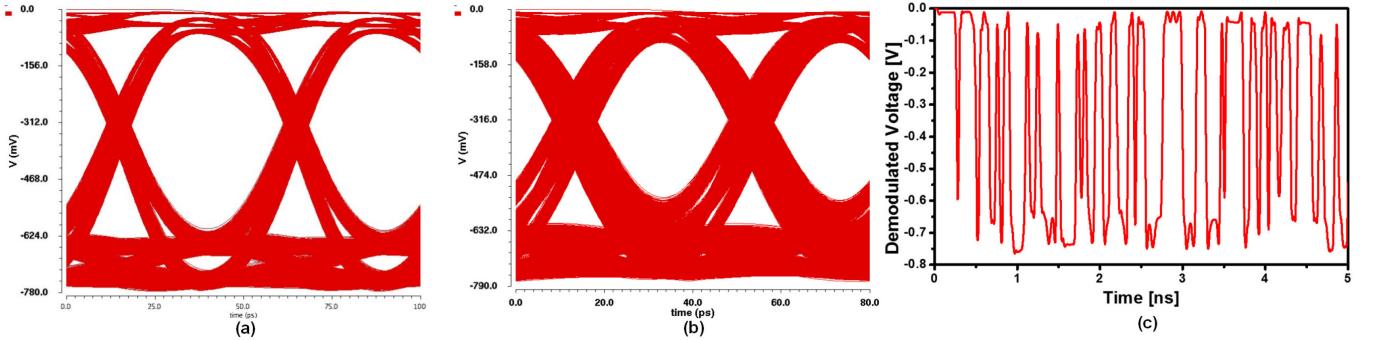


Fig. 8 The simulated eye diagrams of (a) 20Gbps dual channel surface-wave I/O, (b) 25Gbps dual-channels surface-wave I/O, (c) recovered waveform for 25Gbps dual-channels I/O.

stacked split-ring-resonator (SRR) structure, as proposed in [6], demonstrates electric dipole suppression as well as magnetic dipole enhancement, showing potential to be incorporated with TM-polarized surface-plasmonic structures.

$Q$  factor is the key issue in the design of sub-THz oscillator. It determines not only the start-up condition but also the phase noise of oscillator. Traditional resonators have high loss as their resonance rely on excitation of TEM mode. Considering that electrical dipole is very sensitive to frequency with high loss due to skin effect at THz frequencies, we can consider magnetic metamaterial which stores EM energy by magnetic field. One special example is the single SRR structure, which is similar to a commonly-used inductor. Such device stores magnetic energy through the geometry center. Its equivalent circuit can be modeled by  $LC$  resonator model. Since electrical dipole can also be excited across the SRR lanes, its  $Q$  factor will not be improved compared to traditional transmission line based resonator. To overcome this limitation, we need to strongly suppress electric dipole while enhance magnetic dipole. The proposed resonator evolves to a stacked SRR structure as shown in Fig. 5(a). Similar to SPP T-line in which TM polarization is proposed, to achieve the enhancement of magnetic field storage, more single SRR unit-cell can be stacked to reinforce magnetic plasma resonance. The stacked SRR structured is shown in this figure, and the equivalent circuit [6] indicates a magnetic plasma region. Inside this region the incoming EM signal will be perfectly reflected. While the top level SRR is fed by THz source, the bottom SRR will be excited by induced magnetic field. As their current flows are in opposite directions, the induced electrical dipole will be suppressed while the induced magnetic dipole will be enhanced. And therefore, the stacked SRR

mainly relies on magnetic field to store EM energy. As such, it should be feasible to combine both surface-wave transmission line and surface-wave resonator to enhance the magnetic energy storage at mm-wave and beyond in CMOS. Such a novel architecture is shown in Fig. 5(a). Again, the resonator structure is based on the stacked SRR resonator, while its lanes have been shaped by arrays of periodic grooves around the structure. In that sense, the fundamental property of high  $Q$  SRR resonator still remains while the magnetic energy propagation is realized in the form of surface-wave. The electrical field inside stacked SRR resonator will be strongly attenuated, and the excitation can be provided by cross-coupled pair in CMOS. As only surface-wave can exit along the structure, the cross-couple pair now delivers surface-wave.

The current distribution of stacked SRR is shown in Fig. 5(b). As observed, compared to single SRR structure the induced body current is effectively suppressed. This means that a large portion of electric dipole is neutralized by the stacked SRR structure. Fig. 5(c) confirms the magnetic metamaterial nature of the stacked SRR structure. It can be also shown that the effective permeability is negative around the plasma frequency [6], which cannot be achieved by traditional transmission line based resonator. Fig. 5(d) depicts the  $E$ -field distribution around the structure. Clearly, the  $E$ -field is now mainly localized by the periodic grooves, demonstrating a basic property of surface-wave transmission. In the procedure of optimization, the  $E$ -field should be tightly confined by the grooves without leakage to the SRR lane body. Fig. 5(e) further proves that the stacked SRR attains a strong signal reflection at around 140GHz with narrow bandwidth, which is important to achieve high  $Q$ . We also note that the proposed stacked SRR structure does not occupy more silicon area. However, the electric

resonance of conventional SRR structure can be excited across the SRR lane and hence the body current is induced. In addition, the body current is not uniformly distributed. This will increase the effective resistance over the ring, converting more EM energy into heat. As such, single SRR structure cannot improve  $Q$  factor at (sub)-THz. With MOS width of 15um, only 0.7V V<sub>DD</sub> is required to power up the 140GHz oscillator, achieving -116dBc/Hz at 10MHz offset with only 3.5mW power consumption as shown in Fig. 6.

## 4. SUB-THZ SURFACE-PLASMONIC I/O

### 4.1 Sub-THz I/O Transceiver

Fig. 7 shows the TRx implementation in 65nm CMOS. The Tx contains a 140GHz fundamental surface-plasmonic VCO, an *LO* buffer and the SRR-based modulator. Transformers are extensively employed to save silicon area, impedance transformation while providing individual biasing for each functional blocks. Note that transformer conveys EM energy by magnetic storage as well, and a mode conversion is not necessary here. The surface-plasmonic interconnect including conversion part is 20mm long, which is slightly higher than the propagation length for groove depth of 12μm [5]. The 50Ω impedance criteria is not necessary when driving the *LO* buffer since the rail-to-rail swing of fundamental oscillator will completely toggle the buffer output that drives the modulator with high swing. The Rx side contains a self-mixing mixer and three stages baseband amplifier. Mm-wave technique such as inductive peaking is deployed for wider bandwidth so that sharp data transition can be detected. The simulated Tx/Rx waveform of the modulated/demodulated data is shown in Fig. 7 as well. To demonstrate the field confinement of the proposed surface-plasmonic interconnect, dual channels in parallel are presented here with 2.4μm separation which already poses great crosstalk issue for conventional T-line based interconnects. The recovered data and the corresponding eye diagram of 25Gbps communication by surface-plasmonic interconnect are shown in Fig. 8, which presents clearly horizontal/vertical eye opening. As observed, channel crosstalk barely affects high speed communication at 25/25Gbps. It is clear that the proposed sub-THz surface-plasmonic interconnect is immune to channel electromagnetic crosstalk, which is important for densely on-chip wireline communication with high data rate.

### 4.2 Performance Comparison

Recent state-of-art I/O interfaces are summarized with comprehensive performance comparison all implemented in CMOS technology. Firstly, compared with [4], the proposed surface-plasmonic interconnect has at least 10dB crosstalk reduction, leading to over 196% improvement of efficiency. Besides, equalization technique by DFE can hardly support data rate higher than 20Gbps without full-rate clock and data recovery [2-4]. What is more, the total power consumption of the proposed transceiver is less than 8mW which is smaller than RF-I transceiver demonstrated in [1] mainly due to the low loss of surface-plasmonic interconnect and the low power of proposed oscillator. The noticeable improvement on energy can be in part attributed to crosstalk reduction as well. The energy efficiency of the proposed transceiver is even higher than optical-I transceiver [9], which has typical supply voltage of ±20V in driver with large dynamic power consumption during on/off switching. In the proposed sub-THz transceiver design, the surface-plasmonic modulator can be directly driven by on-chip sub-THz oscillator with a nominal voltage (1.2V) and hence low power is consumed.

## 5. CONCLUSION

Using surface-plasmonic interconnects and fundamental oscillator at 140GHz, one multi-channeled I/Os interface is proposed in 65nm CMOS technology. The surface-plasmonic interconnect is able to localize EM energy into the periodic groove by exciting the surface wave with mode conversion to match both impedance and momentum to the conventional guided wave with low loss within wideband. Thus the surface-plasmonic T-lines can strongly attenuate mutual crosstalk with no additional power-hungry circuits for equalization. In addition, the proposed surface-plasmonic resonator combines the merit of stacked SRR resonator and surface-wave interconnect to boost the TM-polarized ability of magnetic resonance at sub-THz frequencies. The  $Q$ -factor could be effectively enhanced by suppressing radiation loss. One 140GHz oscillator is designed by incorporating the proposed surface-plasmonic resonator, demonstrating -116dBc/Hz phase noise at 10MHz offset with only 3.5mW power consumption under 0.7V supply. It is also shown that the proposed sub-THz I/O can communicate 25Gbps with 0.01pJ/bit/mm energy efficiency over 20mm surface-plasmonic channel, exhibiting great potential for the future high performance NoC.

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