Fine-Grain Reconfigurable Logic Cells Based on Double-gate CNTFETs

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ABSTRACT
This paper presents 2-input cells designed to perform reconfigurable operations in nanometric systems exploiting the ambipolar property of double-gate (DG) carbon nanotube (CNT) FETs. Previous work [1] described a dynamic logic cell generating only 14 functions instead of 16 normally performed by the multiplexer-based logic part of a CLB (Configurable Logic Block) of an FPGA for 2-inputs.
In this work, a reconfigurable 2-input dynamic logic cell designed using DG-CNTFET devices is able to achieve the whole set of 16 functions exploiting a specific correlation between input and configuration signals to offer full functionality over the previous version. We also built a reconfigurable 2-input static logic cell which performs 16 functions. Both cells demonstrate a significant reduction in circuit complexity with respect to conventional CMOS-based reconfigurable cells for equivalent functionality. Compared with a 2-LUT, the dynamic cell improves the time delay by a factor of 2X to the detriment of 2X increase in power consumption, while the static logic cell shows an improvement of 2X both in terms of power consumption and time delay.

Categories and Subject Descriptors
B.6.1 [**Logic Design**]: Design style –*Combinational logic, logic arrays*. B.7.1. [**Integrated Circuits**]: Types and Design styles – *advanced technologies, gate arrays*.

General Terms
Performance, Design.

Keywords
ambipolar double-gate devices, static logic, CNTFETs, dynamic logic, advanced technologies.

1. INTRODUCTION
Technology scaling and consequent design complexity have led to increasing difficulties to satisfy constraints concurrently on development costs, time to market and volume manufacturing for physically optimized ASICs.
To counteract these problems different solutions have emerged; while some design teams focus on new methods and tools to facilitate ASIC design, others choose to implement logic in reconfigurable technology such as FPGA. In fact, since their inception, reconfigurable computing architectures are igniting a revolution in *general-purpose* processing; their use might lead to characteristics - such as high-performance, energy efficiency, and flexibility - not achieved by other forms of computing. With so many facilities, this has become an exciting and promising research area. Among several reconfigurable architectures, the Field Programmable Gate Array (FPGA) technology is the most widespread. This conventional reconfigurable technique uses multiplexer-based logic cells to enable switching between previously defined memory cells and the output, using the data inputs as control for the multiplexers. In addition, complete reconfigurability is ensured through the association of reconfigurable interconnect networks between individual cells. This level of reconfigurability is however costly in terms of power, area and speed – all of which are an order of magnitude worse than a physically optimized cell with no reconfigurability.
The aim of this work is to improve on the performance envelope of reconfigurable cells through the use of emerging technologies such as double-gate (DG) carbon nanotube (CNT) FETs. In fact DG devices, with four accessible terminals, open the way to solutions specifically exploiting the additional terminal for reconfigurability purposes. For silicon DG-MOS transistors for example, reconfigurability can be achieved by modulating the threshold voltage of individual transistors via the back-gate [2].
In previous work [1], we proposed area- and power-efficient reconfigurable cells based on emerging devices with incomplete operator sets (i.e. where the number of achievable functions is less than 2^c, where c represents the number of possible combinations of data inputs, itself related to the number of inputs n by $c=2^n$).
In this work, we exploit the ambipolar property of DG-CNTFETs to realize new reconfigurable cells, demonstrating a significant reduction in circuit complexity with respect to conventional CMOS-based reconfigurable cells for equivalent functionality; and improved performance over previous versions of incomplete operator set DG-CNTFET based cells, in terms of the number of achievable logic functions. In fact, the previously designed CNT_DRC_7T cell [1] can achieve 14 logic functions but cannot access the XOR/XNOR functions. The work described here is of a reconfigurable 2-input cell which performs 16 functions, exploiting a specific correlation between input and configuration signals for the missing functions in CNT_DRC_7T. Furthermore, we also describe a 10-transistor, reconfigurable static-logic 2-input cell (CNT_SRC_10T) which performs 16 functions with the advantage of not requiring any phased clock signals or clean supply voltages as compared to dynamic-logic cells.
We begin by presenting the technological hypotheses (section 2). In section 3, we describe the 2-input cell which performs 16 functions based on dynamic-logic and the specific correlation between input and configuration signals to access XOR/XNOR functions; we evaluate and compare different correlations. In

GLSVLSI'11, May 2–4, 2011, Lausanne, Switzerland.

section 4, we present a reconfigurable static-logic 2-input cell (CNT_SRC_10T) which performs 16 functions and we estimate their performance metrics. Both cells performance were discussed and compared with a 2 inputs Look-Up-Table (2-LUT) in sections 5 and 6.

2. TECHNOLOGICAL HYPOTHESES

The idea of using a second gate (polarity gate, PG) to set device polarity in ambipolar double-gate (DG) FETs has opened the way to a new generation of in-field programmable devices. In this paper, we explore all three states of the device (N-type, P-type or off). To validate the concepts, we consider the use of a DG-CNTFET. The compact model presented in [1], written in Verilog-A and extending a unipolar model to double-gate functionality, was used for all simulations throughout this paper. It reflects the ambipolar characteristics of DG-CNTFETs and shows an adaptability to improve channel mobility and control of the off-state.

Several techniques to manufacture such in-field programmable CNTFETs have been proposed in the literature where ambipolar DG-CNTFETs can have one top- and one back-gate [3] or, by applying the self-alignment technique [4], two top-gates [5].We also suppose that the technology is based on aligned semiconducting CNTs [6], with metal interconnections defined by CMOS-compatible lithography steps.

A sample device cross-section with the layout was presented in [7]. The gate G turns the device on or off, in the same way as the regular gate of a MOSFET; the polarity gate PG controls the device polarity setting to N- or P-type with a positive (+V) or negative (-V) voltage, respectively. The device is in the off-state (whatever the voltage on gate G) if the polarity gate is set to 0V. The symbol for this ambipolar DG-CNTFET in-field programmable CNTFET is shown in Fig 1.

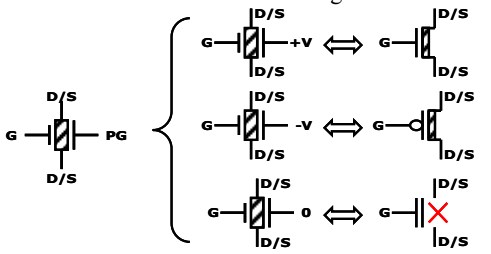

Figure 1. DG-CNTFET device symbol and configurations

3. 2-INPUT DYNAMIC-LOGIC RECONFIGURABLE CELL

The previously designed reconfigurable 14-function DG-CNTFET logic gate, on which this work is based, is shown in figure 2. This logic gate consists of seven DG-CNTFET transistors organized in two stages: the logic function stage and the follower/inverter stage. The three states (+1V, -1V, 0) of the back gate voltages (V_{bA}, V_{bB} and V_{bC}) determine whether transistors T_{c1}, T_{c2} and T_{c3} operate as n-type, p-type or OFF devices.

The cell has two data inputs, three configuration inputs, four clock inputs, and one output:

- The two Boolean data inputs are designated A and B, and the logic values correspond to the supply voltage values: 0V and 1 V.
- The three control inputs determine the overall logic function realized by the cell. These signals are used as back gate voltages for each transistor and as such are +1V for n-type configuration, -1V for p-type configuration and 0V for switched off configuration.
- The four clock inputs are due to the dynamic logic style used in this cell, and the two stages. Each cell must be precharged (first stage to 0V, second stage to +1V) with PC_1 and PC_2, then evaluated (conditional charge or discharge for the first and second stages respectively) based on the state of the inputs and configuration voltages with EV_1 and EV_2.
- The output of the cell, Y, is defined between 0V and +1V.

In this cell, 14 logic functions can be achieved, as shown in table I. The missing functions are the XOR and XNOR functions.

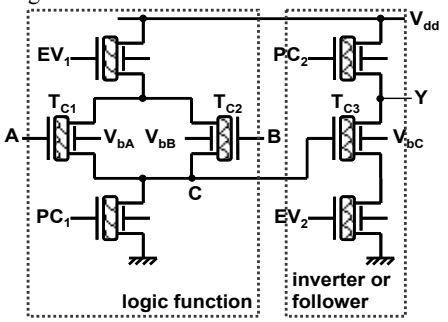

Figure 2. Dynamically reconfigurable dynamic logic cell (DRLC_7T)

TABLE I. 3-INPUT CONFIGURATIONS FOR DRLC_7T WITH 3 LOGIC LEVELS (+V, 0, -V) AND CORRESPONDING 14 BASIC BINARY LOGIC FUNCTIONS

V_{bA}	V_{bB}	V_{bC}	Y
+V	+V	+V	$\overline{A+B}$
+V	+V	-V	$A+B$
+V	0	+V	$\overline{A}$
+V	0	-V	A
-V	-V	+V	$A \bullet B$
-V	-V	-V	$\overline{A \bullet B}$
+V	-V	+V	$B \bullet \overline{A}$
+V	-V	-V	$A+\overline{B}$
0	+V	+V	$\overline{B}$
0	+V	-V	B
0	0	0	T
0	0	-V	$\perp$
-V	+V	+V	$A \bullet \overline{B}$
-V	+V	-V	$\overline{A}+B$

3.1.General concept

The missing functions are the XOR and XNOR functions. To solve this, we can exploit a specific correlation between input signals and configuration signals. In the CNT_DRC_7T cell, configuration is achieved via control signals then used to directly fulfil a logic function with two inputs and one output, such that there is no dependency or correlation between input signals and

control signals. In this work, we define a correlation and additional circuitry that enables the CNT_DRC_7T to access the XOR/XNOR functions.

We suppose that we aim to perform the XOR function at the output node (C) of the first stage of the CNT_DRC_7T.

The truth table of the XOR function is shown in figure 3(a) with the four possible combinations of input signals A and B. For each case, in the right hand columns corresponding to V_{bA} and V_{bB}, we show the set of identified combinations among the original control signal set which generate the required output logic level in the presence of the considered combination of input signals. A certain level of symmetry can be identified in these combinations. In other words, we aim to exploit the dynamic reconfigurability of the CNT_DRC_7T cell to set the actual function of the cell to one which will give the same output as an XOR/XNOR for a given input combination. The work thus centres on the identification of such a data-dependent correlation and generation of a corresponding circuit enabling this dynamic reconfiguration. This approach is possible since the reconfiguration to a surrogate function is at a fine-grain logic level and requires no latency for reconfiguration.

A	B	A⊕B	V_{bA}	V_{bB}
0	0	0	0	0
			0	+V
			+V	0
			+V	+V
0	1	1	-V	0
			-V	+V
			-V	-V
			0	+V
			+V	+V
1	0	1	0	-V
			+V	-V
			-V	-V
			+V	0
			+V	+V
1	1	0	0	0
			0	-V
			-V	0
			-V	-V

(a)

Cor1

V_{bB}= 0
V_{bA}= -V when B=1
V_{bA}= +V when B=0

Cor2

$V_{bA}=V_{bB}= \overline{A \bullet B}$

Cor3

$V_{bA} = \overline{B}$
$V_{bB} = \overline{A}$

(b)

Figure 3. XOR truth table with corresponding control signal combinations (a), Extracted correlations (b)

3.2.Correlation identifcation and corresponding circuits

3.2.1 Correlation I (Cor1)

As shown in figure 3 (b), a first correlation (Cor1) can be identified from the XOR truth table: V_{bA}=-V when B=1 and V_{bA}=+V when B=0, while V_{bB}=0. Hence, the XOR function can be achieved with respect to the following condition:

$V_{bB}=0,\ V_{bA}=\{-V \text{ if } B=1 \mid +V \text{ if } B=0\}$

The condition still holds if we exchange V_{bB} with V_{bA} and B with A.

The corresponding circuit, as implementation of this algorithm, is shown in figure 4. It is composed of an inverter and a switch; the inverter is used to correlate B and V_{bA}. Using the switch we can operate in normal mode if S='0' (CNT_DRC_7T → 14F) or in XOR/XNOR mode if S='1', by combining the inverter with the basic CNT_DRC_7T.

The circuit was designed and simulated using Cadence/Spectre, and validates the theoretical study. The additional structure uses 4 transistors (2T for the switch and 2T for the inverter).

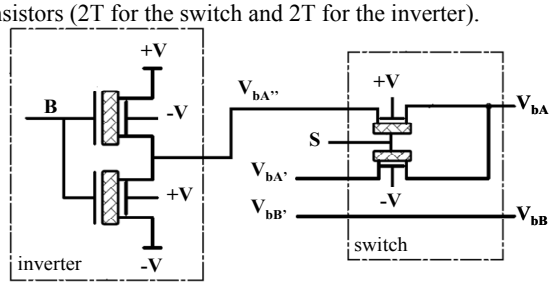

Figure 4. Corresponding circuit for Cor1

3.2.2 Correlation II (Cor2)

An additional observation of the truth table with different combinations of control signals indeed shows a second correlation between input signals and control signals.

As shown in figure 3 (b), if we constrain $V_{bA}=V_{bB}$= (A NAND B), we will also achieve the XOR function.

The circuit implementation (Figure 5) is composed of two stages:

- A NAND function taking A and B as inputs and only one output.
- A switch composed of 4 transistors (2 with n-type and 2 with p-type): the purpose of the switch is to make the cell work either in the normal mode of the (CNT_DRC_7T → 14F) if S='1'or in the XOR/XNOR mode if S='0'.

The circuit was designed and simulated using Cadence/Spectre, and validates the theoretical study. The additional structure uses 8 transistors (4T for the switch and 4T for the NAND function).

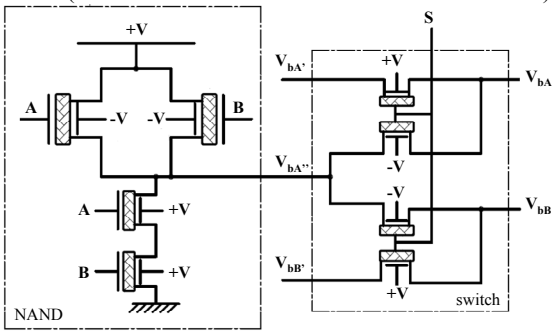

Figure 5. Corresponding circuit for Cor2

3.2.3 Correlation III (Cor3)

A final possibility for correlation could also be V_{bA}= ⌐B and V_{bB}= ⌐A, as shown in figure 3 (b). This correlation circuit uses the same switch needed for Cor2 and utilizes two parallel inverter gates rather than a NAND gate. The same number of transistors is required as correlation II. The corresponding correlation circuit is presented in figure 6.

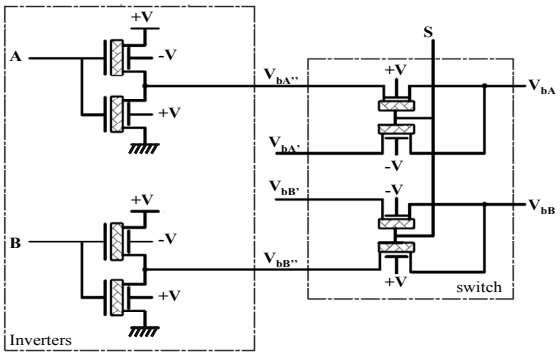

Figure 6. Corresponding circuit for Cor3

3.3.Comparison of the three correlations

To compare the efficiency of the 3 proposed techniques enabling the CNT_DRC_7T to have access to XOR/XNOR functions, we carried out a comparative study of performance metrics as shown in table II.

The following table represents an estimation of performance metrics (power consumption and time delay) from detailed electrical simulations, of the basic cell CNT_DRC_7T combined with the circuitry of each correlation at a frequency of 1GHz with equal rise and fall time of 20ps, and a load capacitance of 100aF. The supply voltage was 1V and clock and data inputs were single polarity (i.e. '1'=1V, '0'=0V) for Cor2 and Cor3. For Cor1, the supply voltage and clock and data inputs were full rail (i.e. '1'=1V, '0'=-1V).

Cyclic simulations were carried out to establish average power consumption and time delay over all data combinations.

We also illustrate in the table the number of transistors and the voltage dynamic required by each correlation circuit.

TABLE II COMPARISON OF AVERAGE VALUES OF CORRELATIONS METRICS

	Time delay(ps)	Av.Power (nW)	# additional transistors	Voltage dynamic (V)
Cor1	1.5	686	4	(-1, +1)
Cor2	5.5	235	8	(0, +1)
Cor3	5.5	287	8	(0, +1)

The disadvantage of correlation I (Cor1) is that the data input B has a voltage dynamic of {0V, +1V}, whereas the output of the inverter in the additional circuit has a dynamic of {-1V, +1V}. For this reason, simulations for the correlation I (Cor1) were carried out with a supply voltage, clocks and data inputs which are full rail (i.e. +V=1V, V_0=-V). We could also use an *open drain* approach typically used to change logic levels if we choose to work with a single rail circuit but this would lead to increased circuit complexity and static power consumption.

As a result of using a voltage dynamic of {-1V, +1V}, the power consumption has dramatically increased more than 2X compared to the use of other correlations. Although the Cor1 circuit consumes more, it has a better time delay, 4X faster than Cor2 and Cor3 since the current flow is much higher. One additional benefit of this correlation is the use of a low number of additional transistors; it uses only 4 additional transistors representing half the number of transistors used by other correlations.

Concerning Correlation 2 (Cor2) based on NAND cell, and Correlation 3 (Cor3) based on Inverter cells, simulations show that the time delay is the same and the power consumption of the Inverter-based correlation (Cor3) cell is slightly higher. In fact, both correlations demonstrate similar reduced power consumption, compatible voltage dynamic of {0V, +1V} and slight increase in the time delay of the basic CNT_DRC_7T cell (5ps). Of course, the essential disadvantage of these two correlations is the high number of additional transistors required.

For a compromise between dynamic voltage compatibility, reduced power consumption and robustness of the circuit, the most suitable solution among the three correlations seems to be Cor2 which uses the NAND gate with minimum power consumption and a voltage dynamic of {0V, +1V}.

4. 2-INPUT STATIC-LOGIC RECONFIGURABLE CELL

4.1.Description of the static logic cell

The static-logic reconfigurable 16-function DG-CNTFET logic gate, designed in this section (abbreviated CNT_SRC_10T), is shown in figure 7. This logic gate consists of 10 DG-CNTFET transistors organized in two stages: The first performs an elementary logic operation; the second propagates or inverts the result depending on its configuration mode; follower or inverter.

The three states (+V, -V, 0) of the back gate voltages of transistors (TC1…TC10) determine whether transistors operate as n-type, p-type or OFF devices.

The cell has two data inputs, 9 configuration inputs, and one output:

- The two Boolean data inputs are designated A and B, and the logic values correspond to the supply voltage values: 0V and 1V.
- The 9 control inputs determine the overall logic function realized by the cell. These signals are used as back gate voltages for each transistor and as such are +1V for n-type configuration, -1V for p-type configuration and 0V for switched off configuration.
- The output of the cell, Y, is defined between 0V and +1V.

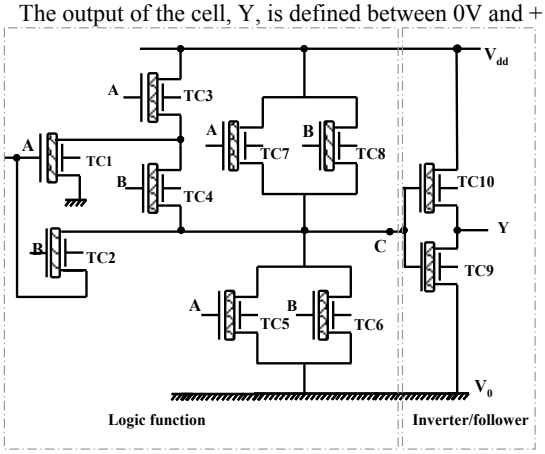

Figure 7. Dynamically reconfigurable static logic cell (CNT_SRC_10T)

In fact, the cell is mainly based on complementary static logic and works almost in the same way as conventional static CMOS; the logic function stage is based on pull-up network and pull-down network. For example, to perform the OR function in the output; transistors TC3 and TC4 are configured as p-type (PG=-V), TC5

and TC6 are configured as n-type (PG=+V) and the output stage is configured as an inverter. All other transistors are switched-off (PG=0).

Table II shows the configuration of every transistor within the cell for each of the 16 performed functions.

TABLE III. 9-INPUT CONFIGURATIONS FOR CNT_SRC_10T WITH 3 LOGIC LEVELS (+V, 0, -V) AND CORRESPONDING 16 BASIC BINARY LOGIC FUNCTIONS

TC1 TC2	TC3	TC4	TC5	TC6	TC7	TC8	TC9	TC10	Function
0	-V	-V	+V	+V	0	0	-V	+V	$\overline{A+B}$
0	-V	-V	+V	+V	0	0	+V	-V	$A+B$
0	+V	-V	-V	+V	0	0	+V	-V	$\overline{A}+B$
0	+V	-V	-V	+V	0	0	-V	+V	$A \bullet \overline{B}$
0	-V	+V	+V	-V	0	0	+V	-V	$A+\overline{B}$
0	-V	+V	+V	-V	0	0	-V	+V	$B \bullet \overline{A}$
0	-V	+V	0	0	+V	-V	-V	+V	T
0	-V	+V	0	0	+V	-V	+V	-V	$\perp$
0	+V	+V	-V	-V	0	0	-V	+V	$A \bullet B$
0	+V	+V	-V	-V	0	0	+V	-V	$\overline{A \bullet B}$
0	0	0	+V	0	-V	0	+V	-V	A
0	0	0	+V	0	-V	0	-V	+V	$\overline{A}$
0	0	0	0	+V	0	-V	-V	+V	$\overline{B}$
0	0	0	0	+V	0	-V	+V	-V	B
+V	-V	-V	0	0	0	0	-V	+V	$\overline{A \oplus B}$
+V	-V	-V	0	0	0	0	+V	-V	$A \oplus B$

Transistors TC1 and TC2 are used only to fulfil XOR/XNOR functions when they are combined with TC3 and TC4 to form Wang's XOR presented in [8]. They are configured as n-type transistors or switched-off, which is why only one control signal is required for both of them.

We mention that the choice of the most suitable structure to implement the XOR/XNOR functions is a crucial step to build the static logic cell with the better performance envelope. Different designs were presented in the literature for XOR gates, but as for many digital designs, implementation in pass-transistor logic (PTL) has been shown to be superior in terms of area, timing, and power characteristics to static CMOS [8][9]. In our case, Wang's XOR structure, showed in figure 8, is the most suitable to be integrated in the whole cell design while keeping a reduced transistor count.

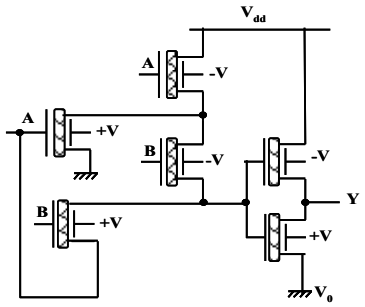

Figure 8. Inverter-based XOR (Wang's XOR)

4.2.Characterization of the static logic cell

To characterize the performance metrics (power consumption and time delays) of the static logic cell CNT_SRC_10T, we used the same simulation conditions presented in (3.3). We also show in table IV the number of configuration points (memory cells) required by the reconfigurable cell.

TABLE IV. AVERAGE VALUES OF CNT_SRC_10T METRICS

delay (ps)	Av power (nW)	# transistor	Config points	Functions
6.5	100	10	9	16

The CNT_SRC_10T cell works almost in the same way as conventional static CMOS (pull-up network and pull-down network). Consequently, it inherits the efficiency of this logic style to implement simple monotonic gates, such as NAND/NOR and AOI/OA, with only a few transistors.

For non-monotonic gates, such as XOR/XNOR such logic requires more complex circuit realizations. As a solution to this issue, the cell is able to switch to one of the simplest XOR/XNOR structures (Wang's XOR), and retain the simplicity and efficiency of the reconfigurable cell for the whole set of 16 functions. The flexibility of the cell makes it power efficient with a minimum number of transistors which means improved integration density at the layout level.

However, the principle disadvantage of the cell is the high number of configuration signals which increase the number of memory points needed.

In the next section, a more detailed comparison of the cell with conventional reconfigurable cells will be presented.

5. PERFORMANCE EVALUATION

In this section, a comparison is made between three different reconfigurable structures, all of them based on CNTFET technology (the same DG-CNTFET model is used).

In fact, we will summarize the performance metrics of the two new designed cells presented in this work and extend the comparison to conventional reconfigurable structures based on multiplexers usually utilized in FPGA.

In other words, the comparison is carried between:

- CNT_DRC_7T cell with the best correlation (Cor2) based on a dynamic logic dynamic logic.
- CNT_SRC_10T with the static logic
- 2-bit LUT (Look-Up-Table) based on Pass-Transistor MUXs (figure 9).

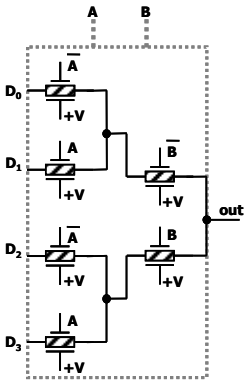

Figure 9. 2-LUT structure

For a fair comparison between the three reconfigurable structures, the same simulations conditions (presented in 3.3) have been used.

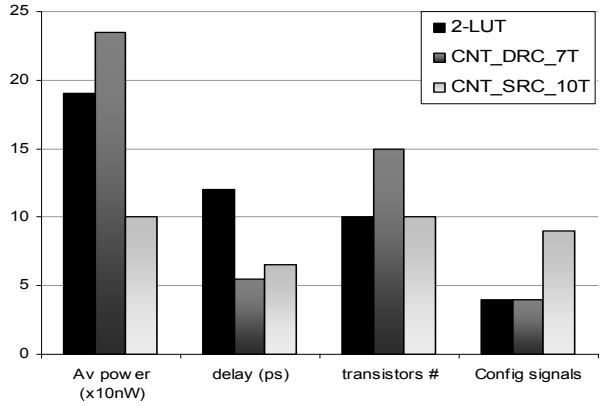

Figure 10. Comparison of the three reconfigurable structures

6. DISCUSSION

Concerning power consumption, simulations show that the dynamic logic cell CNT_DRC_7T is power hungry, an expected result, which is usually linked to the dynamic logic style. However, it offers the best time delay which attains an improvement of 2X compared to a 2-LUT structure. To make the CNT_DRC_7T cell capable of achieving XOR/XNOR functions a penalty at transistor count was observed (1.5 X compared to other cells transistor count). For control signals it needs the same number required by conventional 2-LUT structure.

We notice that CNT_SRC_10T is 2X faster and also 2X power efficient compared to the 2-LUT with the same number of required transistors. The disadvantage of the CNT_SRC_10T is of course the number of configuration lines which is relatively high since each transistor needs its own control signal.

We mention that the 2-LUT structure uses a pass-transistor style with few transistors and small input capacitances, those two advantages are partially undone by the need for swing restoration circuitry often added with this logic style. With other logic styles, the 2-LUT will need much more transistors and so the new designed cells will be more advantageous.

In spite of its attractive high-speed, the dynamic logic cell is no viable candidate for low-power application, worsening further its vulnerability to internal signal races and noise margins leading to degraded circuit robustness.

We mention that in addition to the remarkable improvement in power consumption and time delay, since the CNT_SRC_10T is a static logic cell, it is expected to inherit the ease-of-use and robustness of complementary CMOS [10].

In this study, we did not compare the new cells performance to that of Si MOSFETs because any quantitative results would depend to a large extent on the quality of the device model used. However, we highlighted the improvement that these new structures, exploiting the back-gate of the DG-CNTFET, could provide.

7. CONCLUSION

We have described and evaluated two Fine-Grain reconfigurable logic cells based on DG-CNTFETs. Both cells specifically exploit the ambipolar property of this emerging device to reduce efficiently the time delay or/and the power consumption over conventional CMOS-based reconfigurable cells. While the first designed cell is based on a fast dynamic-logic style exploits specific correlations between input and configuration signals to furnish complete set of 16 functions over previous version [1], the second cell is based on a static-logic offering a maximum of power consumption efficiency and reduced transistor count.

8. REFERENCES

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