Analysis of Universal Logic Gates Using Carbon Nanotube Field Effect Transistor

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ABSTRACT
Due to extraordinary physical and electrical properties, carbon nanotubes have become one of the most promising technologies that might someday pick up where conventional CMOS devices leave off. This paper details analysis of power and delay performance of carbon nanotube field effect transistor- based universal logic gates (NAND and NOR gates). Though electrolyte-gated carbon nanotube field effect transistor have exhibited the highest performance than top-gated and back-gated carbon nanotube field effect transistor, the work demonstrates that energy delay product and switching time performance of 30nm channel length top-gated carbon nanotube field effect transistor - based NAND gate is much better than 20nm channel length electrolyte-gated carbon nanotube field effect transistor technology. As the performance of p type carbon nanotube field effect transistor is better than n type carbon nanotube field effect transistor, 30nm channel length top-gated carbon nanotube field effect transistor-based NOR gate is 4% faster than corresponding NAND gate and its energy delay product is 46% lesser than that of NAND gate.

Categories and Subject Descriptors
B 7.1 VLSI (very large scale integration)

General Terms
Design, Verification.

Keywords
Carbon nanotube field effect transistor, NAND gate, NOR gate, CMOS.

1. INTRODUCTION
The steady reduction in the dimensions of transistors on ICs, according to Moore's law has been the main force behind the regular leaps in the level of performance of silicon ICs over the past four decades. However, no one expects those leaps to go on forever due to scaling problems. Because as the channel length is reduced to increase the speed of operation and the number of components per chip, the short-channel effects, tunneling effect (due to too thin gate insulation), additional heat dissipation, interconnects problems etc. problems arise. So it is not possible to reduce the size further. Hence now it is necessary to adopt new material or technology which preserve a lot of what's good about existing silicon technology and also able to cope up with problems associated with physical limits continuing improvement trends further. The other material such as Ge, SiGe, III-V compound semiconductors and new devices like ultra-thin body fully depleted SOI MOSFETs, FinFets etc have numerous new challenges. The better solution would be carbon nanotube technology.

The number of remarkable electrical as well as mechanical properties of CNTs that are superior for electronic devices and rarely found all in one single material, made CNTs promising structure for digital as well as non-digital applications (storage media for batteries, different sensors etc.). CNT bundles can outperform copper for long intermediate and global interconnects. Semiconducting CNTs are better option as channel for field effect transistor (FET). These carbon nanotube field effect transistors (CNTFETs) can avoid performance degradation problems in Si-transistors due to channel length reduction. The digital logic gates made from CNTFET perform in better manner than CMOS logic devices.

This paper mainly evaluates area, power and delay performance of CNTFET-based NAND and NOR gate using Automatic Logic to Layout tool for Carbon Nanotubes (ALLCN). Section 2 briefs idea about properties and basic structure of CNTs. Section 3 describes design of CNTFETs and their types. Section 4 deals with analysis of NAND and NOR gate and experimental results. Section 5 concludes the paper.

2. BASICS OF CARBON NAOTUBES
Sumio Iijima of NEC Corp in Tokyo first discovered CNTs in 1991. They are basically hollow cylinders with diameters ranging from 1 nm to 50 nm and length, over 10 μm and consist of only carbon atoms in the form of graphite**.** Graphene, the basic material of CNT, is a single sheet of graphite, consisting of sp^2-hybridized atoms arranged in a hexagonal lattice, as shown in Figure 1. A nanotube can be viewed as a single layer or multilayer of graphene sheet rolled into a seamless cylinder [5].

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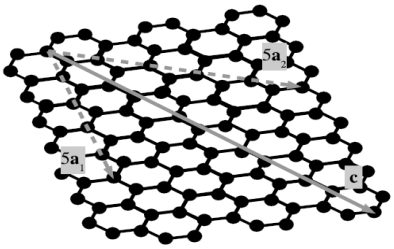

Figure 1. Hexagonal lattice of a graphene sheet with chiral vector in a carbon nanotube (solid arrow).

Accordingly there are two types of nanotubes: single-wall nanotube (SWNT) that is made up of a single layer of graphene sheet**,** and multiwall nanotube (MWNT) that consists of multiple shells, as shown in Figure 2 a) and b) respectively.

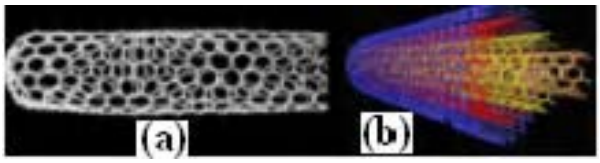

Figure 2. Structure models of nanotubes a) SWNT b) MWNT

2.1 Electronic Structure: Metallic and Semiconducting Nanotubes

To characterize the way in which the tube is rolled up one uses the chiral (or rollup) vector c, which points around the circumference of a CNT describing what unit cell of the graphene lattice is mapped onto itself by rolling up the sheet. As illustrated in Figure 1 using the basis vectors a1 and a2 the chiral vector is given by c = na1 + ma2, written simply as (n, m) and the diameter d of a CNT is calculated as the length of c divided by π:

$$d = \frac{|\mathbf{c}|}{\pi} = \frac{\sqrt{(n\mathbf{a}_1 + n\mathbf{a}_2)^2}}{\pi} = \frac{\sqrt{3}a\sqrt{n^2 + nm + m^2}}{\pi} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(1)$$

Where a is the length of the carbon-carbon bond (1.42°A).

The choice of n and m determines the electronic properties of a CNT. The chirality of a CNT is measured by its chiral angle θ, which is the angle between a1 and c. Figure 3 shows two types for CNT: Figure 3(a) shows a "armchair" or metallic tube with chiral angle, θ = 30° and indices (n, n). Figure 3(b) shows a "zigzag" or semiconducting tube with indices (n, 0) and a chiral angle of θ = 0°.

Figure 3 also shows schematic view of the band structures near the Fermi level (marked by the plane defined by the hexagon). The black hexagons represent the plane of the Fermi level in 2D momentum space. Near the Fermi level the conduction band (grey) and valence band (yellow) in graphene are cone shaped with the cones' apices meeting at the Fermi-energy.

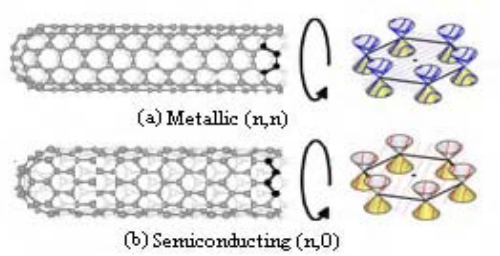

Figure 3. Types of CNTs and Schematic view of the band structures: (a) Metallic (b) Semiconducting [5].

When rolling up the graphene into a CNT another quantization condition is imposed onto this band structure, essentially cutting slices out of the band structure. Depending on the chirality of the particular CNT, if these slices pass through the apices of the cones (blue slices) in Figure 3 (a), the CNT is metallic; otherwise (red slices) in Figure 3 (b), the CNT is semiconducting. In semiconducting nanotubes, the diameter of the tube affects the band gap of the material. By changing the diameter of the CNTs, it is possible to produce devices with any band gap from 0 (a metallic nanotube) to more than 1 electron volt (~ band gap of silicon) and all gap values in between. This feature allows to make devices that turn on and off at different voltages, which we can tailor for different applications.

2.2 Characteristics of Nanotubes

The unique properties of CNTs due to their 1-D character and the peculiar electronic structure of graphite [1, 3, 4] and the fact that, its diameter can be controlled by chemistry and not by conventional fabrication techniques may make them the natural successor to silicon microelectronics.

2.2.1 Electrical Properties: CNTs have low electrical resistance due to ballistic transfer. The low scattering probability, strong chemical bonding and extraordinary thermal conductivity allows metallic CNTs to withstand extremely high current densities up to ~ 10^9 A/cm^2. The low scattering probability and high mobility results in high ON current (more than 1 mA/μm) in semiconducting carbon nanotube field effect transistor (CNTFET). The fact that there are no dangling bond states at the surface of CNTs allows for a much wider choice of gate insulators (with high dielectric constant) beyond the conventional SiO_2 and thickness below 1nm without any additional gate leakage. The 1D electron confinement and full depletion in the nanoscale diameter of the SWNTs should lead to suppression of short-channel effects in transistor devices. It is possible to dope CNTs to improve electronic, vibrational, chemical and mechanical properties [7]. The boron doped SWNT acts as p-type nanoconductor and as n-type when doped with N. When MWNTs are doped with boron or nitrogen they become metallic.

2.2.2 Mechanical Properties: CNTs have very high Young's modulus (0.40 TPa to 4.15 TPa for MWNTs and of the order of 5 TPa for SWNTs). They are extraordinary stiff and strong [6], remarkably flexible and resilient. MWNTs can be bent repeatedly through large angles (up to ~110^0) without undergoing catastrophic fracture, despite the occurrence of kinks.

2.2.3 Optoelectronic Properties: Under proper biasing condition CNT transistor can emit and detect light [2].

3. CARBON NAOTUBE FIELD EFFECT TRANSISTOR

A first CNTFET was created nearly in 1998 at Delft University and in IBM laboratory [2], separately. A silicon wafer was covered with a thick silicon-dioxide film. Then gold or platinum electrodes fabricated on it as the source and drain of FET and a single CNT positioned as a channel between two electrodes, as shown Figure4. The heavily doped underlying silicon wafer served as the gate electrode. The transistor action occurs at the contact points between the metal electrodes and the CNT, where the contact between the two dissimilar materials sets up an energy barrier that prevents electrons from crossing between the metal electrode and the semiconducting nanotube. Increasing the gate voltage thins the barrier and turns the nanotube transistor on. The performance degradation problems in Si-transistors due to channel length reduction can be avoided. Table 1 shows how CNTFETs are better than Si-MOSFETs.

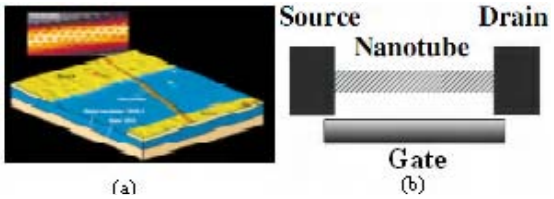

Figure 4. (a) An early prototype CNTFET, inset [left] is a highly magnified scanning tunneling microscope image of a nanotube (b) CNTFET Schematic

The first developed CNTFET is back-gated transistor. Further improvements in structure resulted in development of top gated, electrolyte-gated CNTFET [8-14]. The schematic of top-gated and electrolyte-gated CNTFETs are shown in Figure 5 (a) and (b) respectively.

A back-gated CNTFET uses the heavily-doped silicon wafer itself as the gate, while the gate of a top-gated CNTFET is patterned over the gate oxide which covers the CNT channel. For an electrolyte-gated CNTFET, the role of the gate is played by a droplet of an electrolyte connected to an electrochemical electrode. Similar to CMOS technology, by controlling the gate voltage, the CNTFET can be turned "on" and "off." Take a p-type CNTFET as an example. When the gate voltage is above the threshold voltage, there is high on-current through the CNT channel. However, when the gate voltage is below the threshold voltage, the leakage current in the channel is very low. Among the three types of CNTFETs, electrolyte-gated CNTFETs have exhibited the highest performance to date, but their device structure is hard to integrate into chips. On the other hand, compared with back-gated CNTFETs, top-gated CNTFETs have higher transconductance and on-current.

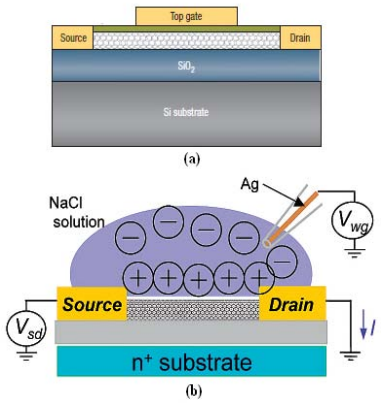

Figure 5. Schematic of (a) top-gated CNTFET (b) Electrolyte-gated CNTFET

Moreover, top gated CNTFETs have the advantage that the gate voltage of each CNTFET can be separately controlled. Hence it is mostly used for application of digital circuit design such as inverter, NAND gate, NOR gate, memory element etc. ALLCN uses device structure of a top-gated Schottky Barrier CNTFET in standard cell design. Top-gated CNTFETs exhibit high performance for both n-type and p-type CNTFETs with transconductance as high as 10-30μS per tube, 10^5 to 10^6 on/off current ratio, 8-25μA on-state current, and 70-130mV/dec subthreshold swing.

4. PERFORMANCE ANALYSIS OF NAND AND NOR GATE

4.1 Tools and Software for CNT-based Devices

ALLCN [16] is the main software tool used for analysis of logic gates which automatically performs logic-to-layout synthesis for CNTFET based circuits. To obtain layout of any circuit, first it is necessary to obtain its logic implementation. For larger circuits a logic synthesis tool, such as SIS [15], can be used. The logic synthesis output, which contains a gate-level netlist, is input to ALLCN directly [16]. ALLCN then maps the netlist to the standard cells and performs placement and global routing. Based on the global routing results, a symbolic detailed router is called to finish routing. When routing is done, symbolic routing results are translated into real physical metal layers. Then the circuit layout is ready to be displayed in a layout window. At the same time, the corresponding SPICE [17] model or switch-level circuit model can be extracted from the layout containing interconnect parasitic parameters. Simulations for timing, power, etc can be performed using SPICE or switch level simulator.

4.2 Experimental Results

The NAND gate and NOR gate have been designed using ALLCN and their performance is evaluated by Spice. To design any logic gate or combinational logic circuit the .blif file is given as an input to Sis. Sis then generates .netblif file. This file acts as input file for ALLCN and after processing generates .mag file which is used to display the layout in magic window. After extracting the magic file, ext file is formed. This is used by Spice for power, delay performance evaluation.

Figure 6 and 7 shows layout of NAND and NOR gate respectively. Whereas output plot and power dissipation graph of NAND and NOR gate are shown in Figure 8, 9, 10, 11 respectively.

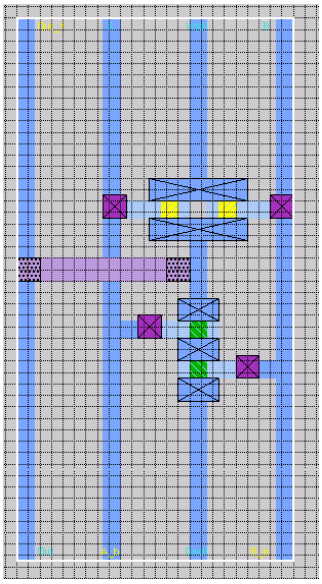

Figure 6. Layout of NAND gate

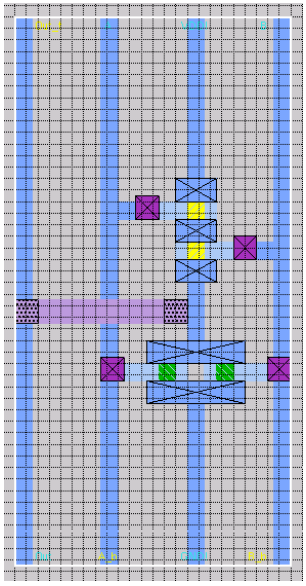

Figure 7. Layout of NOR gate

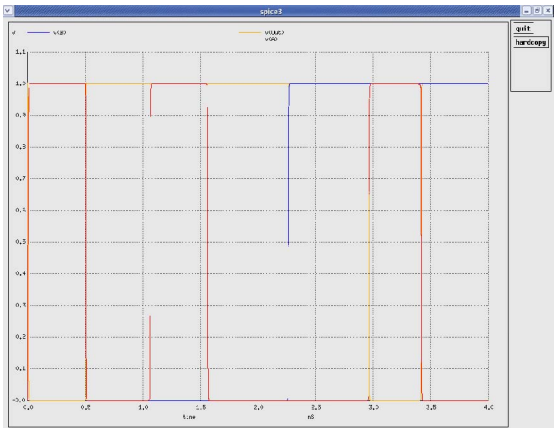

Figure 8. Output Characteristic of CNTFET based NAND gate

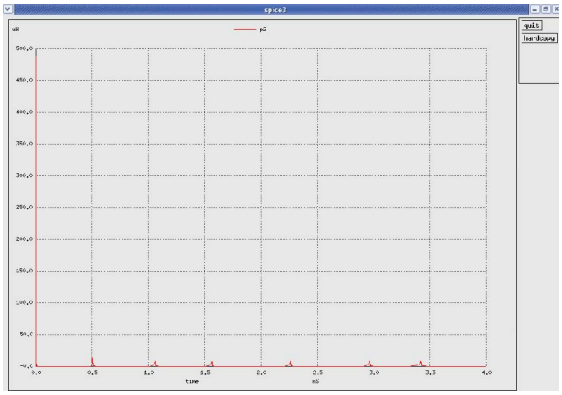

Figure 9. Power performance plot of CNTFET based NAND gate.

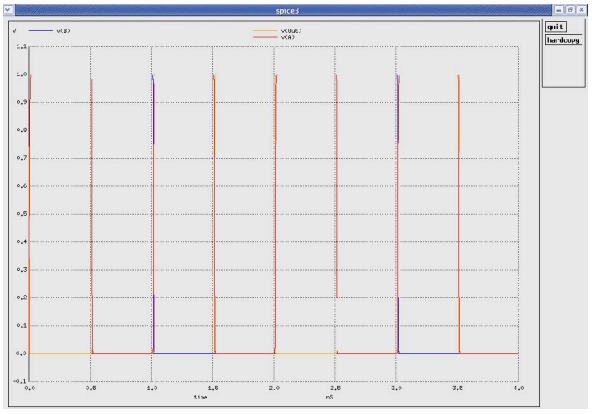

Figure 10. Output Characteristic of CNTFET based NOR gate

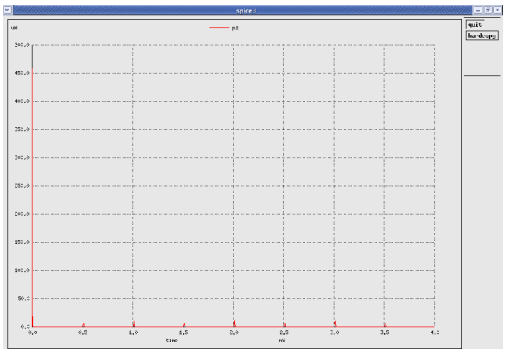

Figure 11. Power performance plot of CNTFET based NOR gate

Following table 1 shows switching time and energy delay comparison of NAND gate designed with Si [17] as well as CNTFET technology. Table 2 shows comparison of CNTFET based NAND and NOR gate.

Table 1. switching time and energy delay comparison of NAND gate

Technology	Switching Time (ps)	Energy delay product (10^{-24} J-s)
180nm	87.8	2.87
130nm	76.5	0.612
100nm	52.5	0.315
65nm	57	0.268
45nm	54	0.140
20nm channel length electrolyte-gated CNTFET technology	10.3	4x 10^{-4}
30nm channel length top-gated CNTFET technology	0.52635	3.6x10^{-6}

Table 2. Comparison of 30nm channel length top-gated CNTFET based NAND and NOR gate

Gate	Area (μm2)	Energy delay product (10^{-30} J-s)
NAND	0.228	3.6
NOR	0.228	2.45

5. CONCLUSION

The result shows that 30nm channel length top-gated CNTFET-based NAND gate is better than other NAND gates whereas 30nm channel length top-gated CNTFET based NOR gate shows 46 % energy delay product improvement over 30nm channel length top-gated CNTFET based NAND consuming same area.

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