Novel CNTFET-based Reconfigurable Logic Gate Design

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ABSTRACT

This paper describes a dynamically reconfigurable 8-function logic gate (CNT-DR8F) based on a double-gate carbon nanotube field effect transistor (DG-CNTFET). The design is based on a property specific to this device: ambivalence, enabling p-type or n-type behavior depending on the back-gate voltage. Using available models, CNT-DR8F is proposed, simulated and analyzed at 20GHz operation. We also give an example functional block (full adder) to show how to construct logic circuits based on the association of physically identical reconfigurable logic cells.

Categories and Subject Descriptors

B.6.1. [**Logic Design**]: Design Styles – *combinational logic, logic arrays.* B.7.1. [**Integrated Circuits**]: Types and Design Styles – *advanced technologies, gate arrays.*

General Terms

Performance, Design.

Keywords

Double-gate CNTFET, dynamically reconfigurable logic.

1. INTRODUCTION

Reconfigurable computing is recognized today as the main way to achieve high performance systems on chip in the context of mask costs projected to move above the $10M mark in 2010. Such systems can cover a wide range of applications and outperform programmable architectures while requiring a single set of masks. Current reconfigurable systems however are inefficient in terms of number of devices used to realize a single function.

CNTFET benchmarking figures against state-of-the-art planar and nonplanar Si logic transistors have shown that the high mobility, achievable current density, theoretical transition frequency and I_{on}/I_{off} ratio make these devices highly suitable for logic applications [1]. Specific CNTFET characteristics have also recently been used in the development of multiple-valued logic [2] and single transistor XOR gates [3].

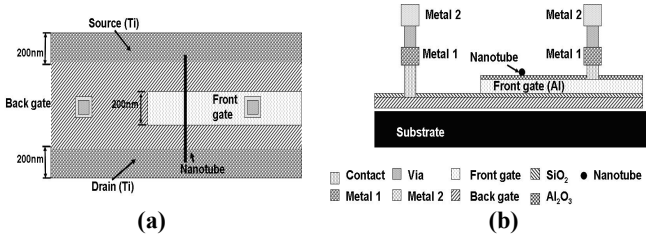
This paper aims to show how the ambivalence property of DG-CNTFETS can be used to build a dynamically reconfigurable 8-function logic gate (CNT-DR8F) that offers fine-grain reconfigurability not available with MOSFET technology, at comparable or better speed and power figures.

DAC 2007, June 4–8, 2007, San Diego, California, USA.

2. RECONFIGURABLE 8-FUNCTION LOGIC GATE (CNT-DR8F)

The double-gate CNTFET was proposed in [4] to improve channel mobility and control of the off-state in CNTFETs. It is built by placing a metal front gate terminal (Al) under the nanotube between the source and the drain (Figure 1). The voltage of the silicon back gate $V_{gs\text{-}bg}$ influences the behavior of the device in the following way:

- when $V_{gs\text{-}bg}$ is sufficiently negative (some hundreds of mV), the device functions like a p-type FET with a negative threshold voltage
- when $V_{gs\text{-}bg}$ is sufficiently positive (some hundreds of mV), the device functions like an n-type FET with a positive threshold voltage
- when $V_{gs\text{-}bg}$ is floating, the sub-bands with the contacts are not affected by the bias of the front gate, and the device is in the off state with a very weak current (I_{off}<100fA).



(a) **(b)**

Figure 1. DG-CNTFET (a) top view [4] (b) Cross-section view

This characteristic can be used to build a dynamically reconfigurable 8-function logic cell (CNT-DR8F). This cell is composed (Figure 2) of 7 DG-CNTFETs in two logic stages (logic function and follower/inverter). The polarities (n-type/p-type) of the individual devices T_{C1}, T_{C2} and T_{C3} are controlled by the corresponding back-gate bias voltages V_{bgA}, V_{bgB} and V_{bgC}, as previously explained. There are 7 inputs and 1 output:

- two boolean data inputs A and B (logic levels represented by the supply voltage values 0V and 1V);
- three control inputs to configure the circuit to one of eight basic binary operation modes as indicated in Table 1 (along with the average total simulated power consumption figures at 250MHz and 20GHz operation) - V_{bgA}, V_{bgB}, V_{bgC} (back-gate bias voltages are -1V for p-type polarity and 1V for n-type polarity);

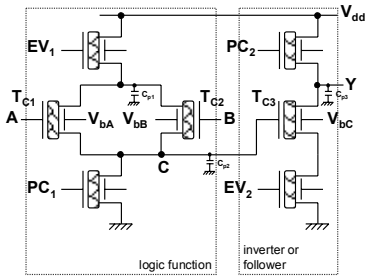


Figure 2. Schematic of the CNT-DR8F

- a four-phase clocking signal set consisting of two pre-charge inputs PC_1, PC_2 and two evaluation inputs EV_1, EV_2. The signals are non-overlapping as in classical CMOS dynamic logic gates;
- circuit output Y.

Table 1. Configuration codes and their logic functions

V_{bgA}	V_{bgB}	V_{bgC}	Y	Power (nW) @20GHz	Power (nW) @250MHz
+V	+V	+V	$\overline{A+B}$	895.7	32.2
+V	+V	-V	$A+B$	848.6	31.29
-V	-V	+V	$A \bullet B$	725.7	25.89
-V	-V	-V	$\overline{A \bullet B}$	686	24.98
+V	-V	+V	$\overline{A}B$	874.6	32.26
+V	-V	-V	$A+\overline{B}$	834.8	31.33
-V	+V	+V	$A\overline{B}$	828.3	31.93
-V	+V	-V	$B+\overline{A}$	788.1	31.1

An example explains how this logic gate works. When V_{bgA}=V_{bgB}=V_{bgC}=1V, CNTFETs T_{C1}, T_{C2} and T_{C3} (as shown in Figure 2) are all configured as n-type FETs. When PC_1 is enabled, the first logic stage is pre-charged, and the voltage of the internal node C (V_C) is discharged to 0V. Then, when EV_1 is enabled, if either of the data inputs A or B is equal to logic "1", the first stage evaluates its output such that the internal node C is set to logic "1". Then, PC_2 is enabled (pre-charge of the second logic stage), and the output Y is charged to logic "1"; and when EV_2 is enabled, the output is evaluated and Y is evaluated at logic "0". It can thus be seen that for V_{bgA}=V_{bgB}=V_{bgC}=1V, the CNT-DR8F cell is configured as a NOR operator.

Simulation was realized using a compact model [5] verified against results from the literature, and parasitic capacitances extracted from arbitrary design rules using those of a DGMOS technology and DG-CNTFET publications [4]. It should be noted that as this is prospective work, no technology as yet exists to build this circuit, although a single DG-CNTFET has been fabricated and characterized.

To build a more complex gate with CNT-DR8F, the logical function has to be translated into a combination of 2-input elementary terms. The translation of an n-input complex gate into a combination of 2-input Boolean gates leads to a pipeline architecture. For example, a full adder is composed of two operators: a sum gate (3-input XOR) and a carry generator. Figure 3 shows the whole structure of the full adder whose latency time is 7.5ns at 250MHz operation.

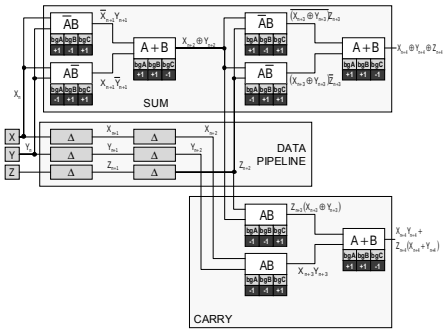


Figure 3. Schematic of the pipelined full adder using associations of CNT-DR8F gates

The full adder consists of 9 CNT-DR8F, which are physically the same but with different reconfiguration codes. This is a first step towards the use of the CNT-DR8F for the realization of a conventional function in platform-based system. Quantitative comparisons with advanced CMOS structures are part of the next steps of this work. Looking further ahead, CNT-DR8F can be dynamically reconfigured in pipelined reconfigurable circuits to realize far more complex functions. However, interconnect reconfigurability issues still have to be addressed.

3. CONCLUSION

In this paper, a dynamically reconfigurable 8-function logic gate (CNT-DR8F) using DG-CNTFETs was introduced, and from first layout and simulations we have estimated its power consumption and transient parameters. CNT-DR8F has been considered as a universal reconfigurable cell enabling the synthesis of any Boolean function, showing the possibility to realize dense, regular and highly reconfigurable circuits in platform-based system on chip design.

4. ACKNOWLEDGMENTS

This work was funded by the French Ministry of Research under Nanosys ("Programme ACI Nanosciences").

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