Ambipolar double gate CNTFETs based reconfigurable Logic cells

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ABSTRACT

This paper presents 2-input cells designed to perform reconfigurable operations in nanometric systems exploiting the ambipolar property of double-gate (DG) carbon nanotube (CNT) FETs. Previous work [12] described a dynamic logic cell generating only 14 functions instead of 16 normally performed by the multiplexer-based logic part of a CLB (Configurable Logic Block) of an FPGA for 2-inputs.

In this work, a reconfigurable 2-input dynamic logic cell designed using DG-CNTFET devices is able to achieve a more complete set of functions by exploiting sum of products (SOP) and product of sums (POS) to express logic functions. We also demonstrated that a static logic version can be derived from this dynamic cell. Simulations reveal improvement factor of 3X in terms of delay and 23% of decrease in power consumption compared with the previous work [12]. When compared with 16nm-CMOS Technology, DG-CNTFET cells (dynamic logic and static logic style) showed a comparable PDP with a slight increase in area.

Categories and Subject Descriptors

B.7.1 [**Hardware**]: Integrated Circuits – *Types and Design Styles.*

General Terms

Performance, Design

Keywords

Ambipolarity, Carbone nanotubes, Reconfigurable Logic, CNTFET, double gate

1. INTRODUCTION

Scaling the CMOS technology into nanometer regime requires innovative approach in overcoming a number of physical limits while maintaining performance improvements. Devices with structure different from the conventional single gate MOSFET are more and more investigated by technologists and designers. The most promising concept in this direction is the double gate MOSFET.

In fact, four-terminal devices with independent double gate show to be a common border between two basic cornerstones in nanodevice-based circuits: on one hand it responds to the device level expectations with appreciative benchmark figures against Si-CMOS transistors [1] [2]. On the other hand it shows a potential to provide novel logic blocks and elaborate innovative techniques for digital design circuits thanks to their specific intrinsic properties which deliver significant benefits. With independent double gate devices the overheads imposed by reconfigurability can be reduced or hidden to an extent where it becomes possible support complex data path architectures with homogeneous fine-grained organization [3-4].

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O'connor et al have proved the faculty of four terminal devices to offer a new paradigm to fine-grain reconfigurability by exploiting the additional terminal in two different technologies; first with using 6 DG-MOS transistors (FinFETs), a cell capable of achieving 8 functions was designed in [5]. Here, reconfigurability is enabled by modulating the transistor threshold voltages via the back gates. Second, the ambipolarity behaviour of DG-CNTFETs has been exploited to construct logic cells with various logic styles [6] [7]. Also, other design teams studied the impact of such reconfigurable cells at the architectural level [8][9][10][11] and showed that in addition to improved speed, power and area these new structures offer regularity, symmetry and especially provide the in-field reconfigurability.

Although the DG-CNTFET reconfigurable cells designed in [12] [13] showed area- and power-efficient figures of merit, they suffer from i) logic level degradation, ii) incomplete operator sets (i.e. the number of achievable functions is less than 2^{2^n} functions with n is the number of inputs, iii) dynamic-logic based cell without the possibility to derive a static-logic version iv) immature DG-CNTFET compact model to evaluate the logic circuits.

In this work, all these issues are tackled and a simpler reconfigurable logic cell without logic level degradation is proposed. It can be an attractive alternative to previous designed cells [12] [13]. A static logic cell is also derived. Both cells are validated and evaluated based on a recent compact model device. The paper begins by describing, in section 2, device principles, a DG-CNTFET device, and characteristic parameters for modeling. Then, in section 3 we introduce the novel 2-input reconfigurable cell with its two versions (dynamic logic and static logic). In section 4, we present an evaluation of both cells and comparative simulations with a 16nm low-power CMOS technology, while in section 5 we discuss the performances and the improvements brought by the new cells. Section 6 is the conclusion.

2. DEVICE CHARACTERISTICS

For conventional unipolar Si-CMOS devices, the p-type or n-type behaviour is determined during fabrication. But, original ambipolar conduction behaviour has appeared in many post-silicon devices; they conduct both electrons and holes, showing a superposition on n- and p-type behaviours.

The ability to select the polarity (p- or n-type) in field by using a second back-gate, polarity gate [7] [9] [10] [11], has inspired

some design teams to exploit Double-Gate ambipolar devices to build novel logic circuits showing significant gains in area, power, and performance. In [14], Yang and Mohanram have generalized the design principles of ambipolar electronic and presented new designs and applications. In this paper, we explore the ambipolar behavior through all three states of the device (N type, P-type or off) as it was reported recently in [15] for the most advanced DG-CNTFET compact model available in literature. Figure 1 describes the generic behavior of the ambipolar DG-FET.

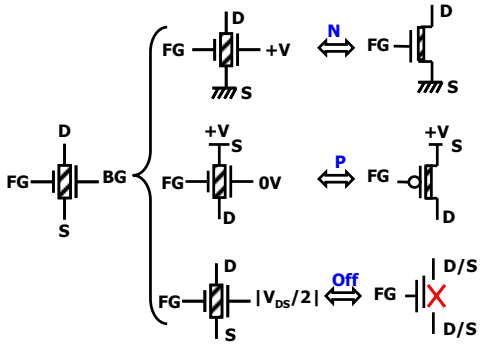


Figure 1 DG-CNTFET device. Symbol and configurations

The front gate FG turns the device on or off, in the same way as the regular gate of a MOSFET; while the back-gate BG controls the device polarity setting to N- or P-type with a positive (V_{BG}-V_S= +V) or negative (V_{BG}-V_S= -V) voltage, by permitting electrons or holes respectively to enter into the nanotube. The device is in the off-state (whatever the voltage on gate FG) if the back gate voltage is set midway between drain and source voltages. The symbol and the corresponding configurations for this in-field programmable DG-CNTFET are shown in Figure 1.

Careful technology engineering (e.g. gate materials, layer thicknesses) is required to ensure that both gates of the DG-CNTFET will achieve the desired functionality over the correct range of voltages.

While this work is expressed through DG-CNTFETs, the main specific FET device characteristic required is that of controllable (double-gate) ambipolarity. It is expected that the circuit techniques described in this paper are also valid using other devices with this property, such as double-gate transistors based on silicon nanowires recently published in [16] or potentially in the future on graphene.

2.1 DG-CNTFET technology

At present, various types of CNTFET devices have been produced experimentally, but there is no standard CNTFET process. In many works using CNTFET devices [6] [7], realistic and CMOS-compatible process flow steps have been suggested to manufacture such a device. A prior work, presented the structure of a DG CNTFET based on aligned semiconducting CNTs [17], applying the self-alignment technique [18] and using two top gates [19], as well as potential hybrid integration with CMOS technology and consequently with metal interconnections defined by CMOS-compatible lithography steps. In this work, the same hypotheses are kept, except that the structure used here does not have two top-gates, but a top-gate and a back-gate in order to be more faithful to the compact model used later for simulations. Figure 2(a), reported from a recent work [20] using the same compact model, shows the structure of the CNTFET with double gates. The front gate FG turns the device on or off, in the same way as the regular gate of a MOSFET; while the back-gate BG controls the device polarity setting to N- or P-type with a positive (V_{BG}-V_S= +V) or negative (V_{BG}-V_S= -V) voltage, respectively. The layout for this in-field programmable CNTFET is shown in Fig 2(b).

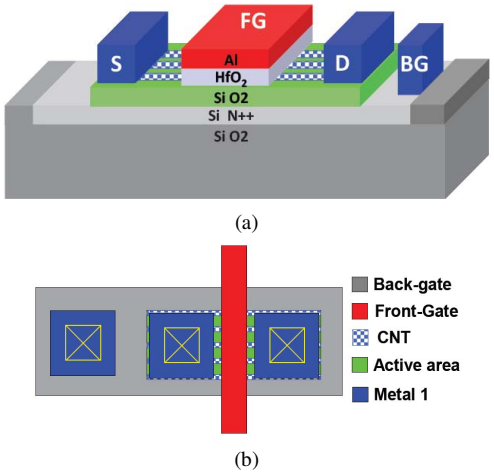


Figure 2 DG-CNTFET device [20]. Cross-section (a), device layout (b)

2.2 DG-CNTFET compact model

In prior works [6] [7] [12] [13] simulations were carried out with the model presented in [21] which is limited to thermionic transport without taking into account the coupling between the FG and BG and does not include SB (sub-band) modeling or BTBT (band-to-band tunneling). Recently, a more accurate model has been presented in [15]. To the best of our knowledge; it represents the first physically accurate model of a DG CNTFET with efficient convergence and simulation speed compatible with circuit design. The compact model is detailed in [15], where it was shown to include the most significant mechanisms such as the SB at the metal–nanotube interface, charge and electrostatic modeling, BTBT effect, and quasi-ballistic transport. Furthermore, the comparison of the model with measurements from two technologies published in literature; a DG CNTFET from IBM [22] and a DG CNTFET from Stanford University (used as a MOS-like CNTFET) [23], showed the accuracy of the compact model on different technology configurations since the values of the extracted parameters are close to those in the available technologies. We point out that the parameters of the model presented in [15] have been tuned to fit with the device structure suggested for this work in figure 2. More details are shown below (2.3 device parameters).

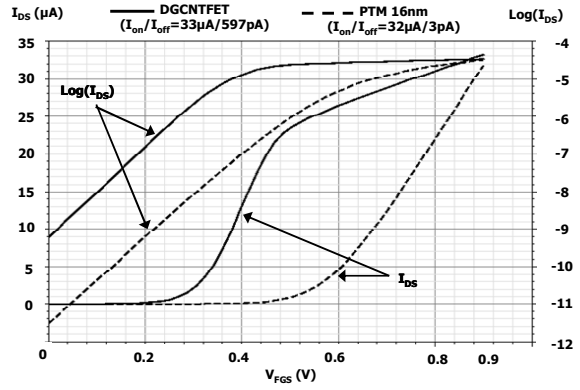
2.3 Device parameters

All simulations to characterize the ambipolar DG-FETs based cells are founded on the technological assumptions and the physical compact model for the DG-CNTFET device detailed in this section. We also aim to drive a comparative study with conventional CMOS circuit structures using identical device models. That's why, for silicon CMOS technology; we use a 16nm low power (LP) Predictive Technology Model (PTM) [24]. Since we aim to obtain quantitative comparisons, it is further necessary to calibrate the CMOS transistor width to match the on-current performance of the DG-CNTFET, for both types of transistor (p-type and n-type). Table 1 shows the parameters used for the DG CNTFET compact model as presented in [15] and the tuned length/width of the predictive model. Figure 3(a) (resp. figure3(b)) shows the I_D/V_{GS} characteristic of the DG-CNTFET

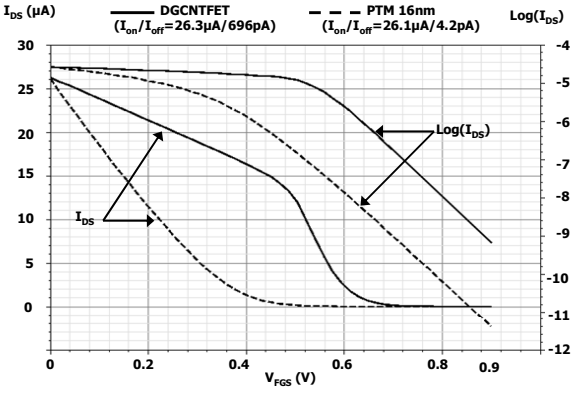
model and the 16nm LP PTM model for n-type (resp. p-type) configuration, where V_{GS} varies between 0V and +0.9V, while V_D=0.9V (resp. V_S=0.9V) and V_S=0V (resp. V_D=0V). It is worth noticing that for equal I_{on}, the DG-CNTFET leakage current is over two orders of magnitude higher than that of the 16nm LP PTM transistor, mainly due to the lower threshold voltage (V_{th}) by about 0.2V.

Table 1. DG-CNTFET and CMOS transistor parameters

Parameters	DG-CNTFET	16nm LP PTM
Drain access channel length	50nm	0nm
Source access channel length	50nm	0nm
Inner channel	20nm	16nm
Width	50nm	56nm (n-type) 90nm (p-type)
Number of nanotubes	12	-
Diameter of 1 nanotube	0.86nm	-
Supply voltage	0.9V	0.9V
Chirality (n,m)	(11,0)	-



(a)



(b)

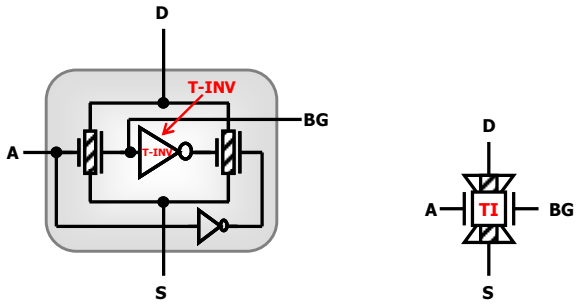
Figure 3 I_{DS}/V_{GS} characteristics. n-branch (V_{BG}-V_S = +V = +0. 9V) (a) ; p-branch (V_{BG}-V_S = -V = -0. 9V) (b)

3. Two-input reconfigurable logic cells based on DG-CNTFETs

In this work, the PG reconfigurability and associated states (N-type, P-type, off-state) are used to build a reconfigurable 2-input logic cells, using the PG signal as a configuration signal with a constant voltage. The first cell operates in a dynamic-logic style using DG-CNTFET devices and is able to achieve the whole set of 16 functions (except for the "true" (unconditional "1") function); the second cell is derived from the first one and operates in a complementary static-logic style and achieves the whole set of 16 functions (except for the "true" and "false" functions). In addition, we describe a necessary DG-CNTFET transmission gate structure to eliminate logic level degradation within the designed cells.

3.1 DG-CNTFET Transmission gate block

The reconfigurable cell, based on dynamic logic, essentially requires a network of transmission gates to propagate logic levels with no degradation and for a wide range of data and control voltage combinations. To obtain full swing in all configurations, we use a transmission gate formed by two CNTFETs in parallel controlled by complementary signals, both for data on the front gate and for control on the back (polarity) gate. While the data is a binary signal (such that complementarity requires a simple inverter), the control is a ternary signal and requires a ternary inverter (T-INV). The structure of the transmission gate, capable of switching between all three states (n-type, p-type and OFF) is shown in figure 4(a) and is abbreviated as "TI" in the associated symbol shown in figure 4(b).



(a) (b)

Figure 4 DG-CNTFET transmission gate: structure (a), symbol (b)

T-INV controls the back-gate of the parallel DG-CNTFET and operates according to {+V→0V, +V/2→+V/2, 0V→+V}. The structure of the T-INV is shown in figure 5; it is composed of two transistors and two resistors of 100kΩ each. This value is the result of tradeoff within a range of values giving acceptable ternary noise margins; with increasing resistance comes higher delay and area, and lower power consumption and dependency on DG-CNTFET channel resistance.

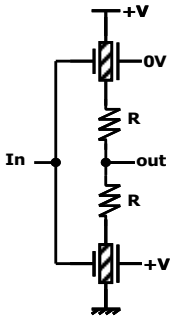


Figure 5 T-INV structure

3.2 2-input reconfigurable dynamic logic cell

Every Boolean function can be written in canonical form as a sum of products, i.e. minterms (SOP) or as a product of sums, i.e. maxterms (POS). While the possible minterms for a two-variable function f(A,B) are: A∧(¬B), (¬A)∧B, (¬A)∧(¬B), A∧B, the maxterms are: AV(¬B), (¬A)VB, (¬A)V(¬B), AVB.

For this two-variable function f(A,B), (2^{2^2}=16) functions can be obtained. On one hand, the majority of all 16 functions are realizable by using one maxterm, or a product of 2 maxterms. On the other hand, the remaining functions for which more than 2 maxterms are required (A∧(¬B), (¬A)∧B, (¬A)∧(¬B), A∧B) can be mapped using a single minterm. The main idea in this work is to express output functions in a reconfigurable cell as a POS or a SOP through the ambipolarity of DG-CNTFET and using the form which *requires the lowest number of transistors*.

Figure 6 illustrates the transistor level implementation of the single-stage dynamically reconfigurable cell abbreviated as POS-DRLC since the cell is basically built according to a POS form. TI1 and TI2 of the function path are placed in parallel (wired OR) to form a first maxterm, while TI3 and TI4 form the second maxterm. Both structures are connected in series (wired AND) to enable the potential use of the product of both maxterms. Further, by switching OFF one of the two TI structures in each maxterm (i.e. TI2 / TI3 or TI1 / TI4) the other transistor pair will form a structure of two transistors in series. In this way, functions in minterm form can also be implemented. The cell may thus achieve 15 basic binary operations (Table 2). The "true" function is missing, because the function path is a pull-up network and cannot be made unconditionally conducting.

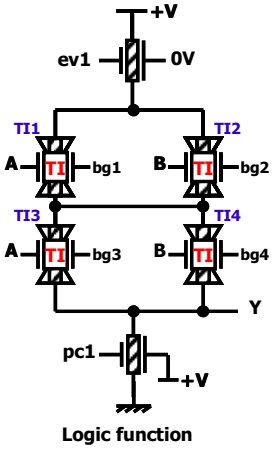


Figure 6 POS based dynamically reconfigurable dynamic logic cell POS-DRLC

The dynamic-logic cell (DRLC) uses 4 transmission gates and 2 transistors and realizes the whole set of functions (except for the "true" (unconditional "1") function) by exploiting the possibility to express a function as a POS or as SOP *(promoting the form which needs fewer transistor count*) using the same circuit.

The implementation of this cell requires single polarity inputs (i.e. 0V for logic "0" and +V for logic "1"), to avoid additional inverters and dual rail interconnects. In the case of complemented inputs, DG-CNTFETs and corresponding TI structrues can be configured to p-type using the corresponding PG voltage (0V). In this cell, there are ten inputs and one output:

- two boolean data inputs A and B (where the logic levels are represented by the supply voltage values 0V and +V).
- four control inputs $bg_{\{1\text{-}4\}}$ to configure the circuit
- a two-phase clock signal set consisting of 1 precharge input pc1 and 1 evaluation input ev1. The signals are non-overlapping as in classical CMOS dynamic logic gates
- circuit output "Y"

An example explains how this logic gate works; When (bg_1=+V, bg_2=+V, bg_3=+V, bg_4=+V), structures TI1, TI2, TI3 and TI4 as shown in Fig. 6 are all configured as n-type FETs. When pc1 is enabled, the output node is discharged to 0V. Then, when ev1 is enabled, if either of the data inputs A or B is equal to logic "1", the output node Out is charged to +V. The simulation results of DRLC_6T in this configuration (OR function) are shown in Fig. 7.

These circuit signals are illustrated in figure 7, showing a cyclic simulation of the POS-DRLC circuit in the OR configuration.

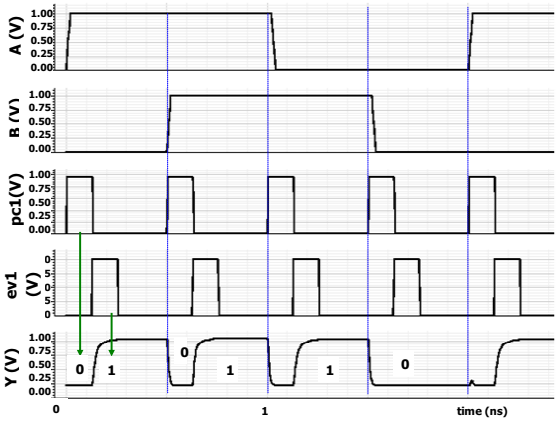


Figure 7 Simulation results for POS-DRLC in OR configuration

The available basic binary operations and the associated configuration PG voltage combinations are shown in Table 2.

Table 2. POS-DRLC configuration table

bg1	bg2	bg3	bg4	Y
0V	V/2	V/2	0V	¬(A∨B)
+V	+V	+V	+V	(A∨B)
0V	+V	0V	+V	(¬A)∨B
+V	0V	+V	0V	A∨(¬B)
0V	V/2	V/2	+V	(¬A)∧B
+V	V/2	V/2	0V	A∧(¬B)
+V	V/2	V/2	+V	A∧B
0V	0V	0V	0V	¬(A∧B)
V/2	0V	V/2	0V	¬B
V/2	+V	V/2	+V	B
+V	V/2	+V	V/2	A
0V	V/2	0V	V/2	¬A
+V	0V	0V	+V	¬(A⊕B)
+V	+V	0V	0V	A⊕B
V/2	V/2	V/2	V/2	⊥
INACCESSIBLE				T

3.3 2-input reconfigurable static logic cell

The dynamic structure showed an attracting flexibility to switch between wired OR and wired AND. Almost the whole set of functions has been achieved. However, due to variations dynamic solutions (in general) are at a disadvantage. Also, a designer must guess the penalty that should be paid (power and delay) for making such a solution work properly. That's why; a static logic cell is derived from the POS-DRLC, by duplicating the pull-up network to achieve the complementary static logic composed of pull-up network and pull down network. In the same way as dynamic logic cells, TI structures are used for both networks, so no logic degradation is observed independently from the type of the structure (n, p, off) and its placement in the cell (pull-up or pull-down).

Figure 8 illustrates the transistor level implementation of the complementary static logic dynamically reconfigurable cell abbreviated as CSL-DRLC. The cell may thus achieve 14 basic binary operations (Table 3). Functions "true" and "false" are missing.

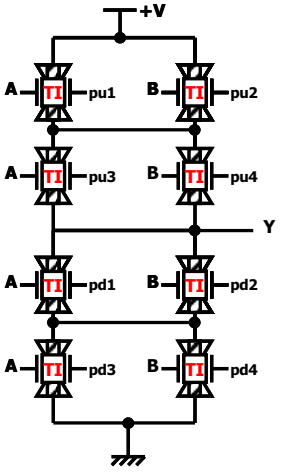


Figure 8 Complementary static logic dynamically reconfigurable logic cell CSL-DRLC

Table 3. CSL-DRLC configuration table

pu1	pu2	pu3	pu4	pd1	pd2	pd3	pd4	Y
0V	V/2	V/2	0V	+V	+V	+V	+V	¬(A∨B)
+V	+V	+V	+V	0V	V/2	V/2	0	(A∨B)
0V	+V	0V	+V	+V	V/2	V/2	0V	(¬A)∨B
+V	0V	+V	0V	0V	V/2	V/2	+V	A∨(¬B)
0V	V/2	V/2	+V	+V	0V	+V	0V	(¬A)∧B
+V	V/2	V/2	0V	0V	+V	0V	+V	A∧(¬B)
+V	V/2	V/2	+V	0V	0V	0V	0V	A∧B
0V	0V	0V	0V	+V	V/2	V/2	+V	¬(A∧B)
V/2	0V	V/2	0V	V/2	+V	V/2	+V	¬B
V/2	+V	V/2	+V	V/2	0V	V/2	0V	B
+V	V/2	+V	V/2	0V	V/2	0V	V/2	A
0V	V/2	0V	V/2	+V	V/2	+V	V/2	¬A
0V	0V	+V	+V	+V	0V	0V	+V	¬(A⊕B)
+V	0V	0V	+V	0V	0V	+V	+V	A⊕B
INACCESSIBLE								⊥
								T

4. Performance evaluation

4.1 Benchmarks

Our study concerns reconfigurable structure built with two different logic styles (dynamic logic and static logic). That's why, to make the comparison as fair as possible, we compare the reconfigurable dynamic logic cells designed in this work POS-DRLC with a 16nm CMOS-based multiplexer with 4 inputs and one output. It is build according to a dynamic-logic style with the same structure arrangement used with the CNT technology cells (2 non-overlapping clocks, pull-up function path block). The reconfigurability of this cell is achieved by swapping between different combinations of the 4 inputs data (D_1, D_2, D_3, and D_4) in the same way as the operation principle of a Look up table (LUT). It is abbreviated as DL-MUX 4:1 (Dynamic Logic MUX 4:1). Also the cell designed in [12] and represented in figure 9 is taken as a benchmark, since we suppose that the dynamic cell designed in this work is a better version of it.

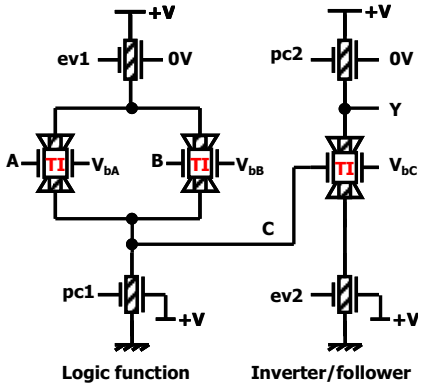


Figure 9 DRLC_7T reconfigurable dynamic logic cell [12]

Concerning the comparison of the reconfigurable static logic cell (CSL-DRLC) designed in this work; we handle two reconfigurable CMOS-based logic cells. Both use the same principle of reconfiguration in LUTs. The first is a complementary static logic multiplexer with four inputs and one output, it is abbreviated as "CSL-MUX 4:1". The second has also a static logic structure but it is built with transmission gates (pass transistor logic). It is abbreviated as "TG-MUX 4:1.

4.2 Simulations and results

We suppose that there is no difference in rise and fall times for inputs A and B. We ran simulations with a frequency f=250 MHz and equal rise and fall times (40ps) for input signals (A, B) with a capacitive load output of FO4. Input signals (A, B) had a pulse width of (1/2f) and a period of (1/f). The supply voltage was 0.9V according to the table 1 of devices parameters, data inputs were single rail (i.e. +V=0.9V, V_0=0V). For the dynamic logic cells, the same conditions were kept for the two inputs (A, B) and we suggested that non-overlapping clocks signals, have equal rise and fall times (10 ps), a period equal to (1/4f) and a pulse width of (1/16f).

Cyclic simulations using Spectre™ were carried out to establish mean power consumption and worst-case time delay over all data combinations and function configurations. Figures 10 and 11 show the overall simulation results for power consumption "P", time delay "TD", power-delay product "PDP" and the active area "AREA" (i.e. sum of all channel areas W*L), for dynamic logic cells and static logic cells respectively.

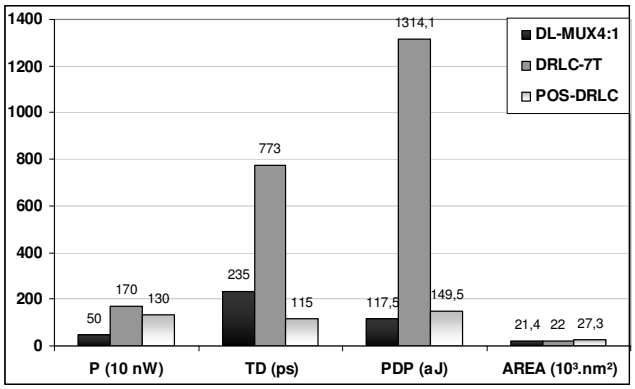


Figure 10 Average values comparison of reconfigurable dynamic logic cells

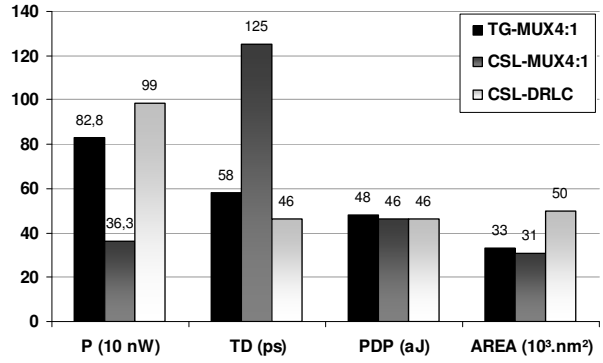


Figure 11 Average values comparison of reconfigurable static logic cells

5. Discussion

In this work, transmission gates are used instead of single transistors within functions path. The use of such transmission gates structures ("TI" structures) was indispensable ; i) to solve logic level degradation, ii) to insure the proper working of DG-FET inside functions paths and iii) to allow a correct switching between the three configuration state (n, p, off) since this depends on V_S, V_D and V_{BG}. The utilization of such structures has proved an efficiency to resolve these three problems and simulations showed very clean waveforms. However, to build one DG-FET transmission gate needs two transistors in parallel and two inverters. That's why this will decrease the number of transistors and consequently the area. In addition, more gates mean more power consumption. In fact, DG-CNTFET cells showed power consumption ~2-3X higher 16nm CMOS technology. This is due to two main reasons; the first is the high number of gates needed by using transmission gates instead of single transistors as we explained earlier, the second reason is related to the DG-CNTFET device itself; Actually, figure 2 illustrating the I_{DS}/V_{FGS} characteristics of both model devices used for our simulations with an equal I_{on}, explain clearly the worse power consumption of the DG CNTFET compared to the PTM 16nm. This is mainly due to the lower threshold voltage (V_{th}) of DGCNTFET compared to the PTM 16nm. Power consumption (P) depends on static leakage current $I_{leakage}$, also dependent on V_{th} $\{I_{leakage} \propto e^{-C \times Vth}\}$ and P depends as well on Short-circuit current $\{I_{SC} \propto (\beta.\tau_{in}/12.V_{DD}).(V_{DD}- 2.V_{th})^3.f\}$. The V_{th} of the DG-CNTFET is 2X smaller than that of 16nm CMOS technology, that's why with the cubic correlation with I_{SC} the difference of power consumption between logic gates, is elevated. Nevertheless, the low V_{th} is a mixed blessing factor since it offers an improvement between 2 to 3X concerning the time delay when compared with 16nm CMOS technology. With 2-3X increase in power consumption and 2-3X improvement in time delays, the PDP of both technologies is shown to be the same in figure 10 for static logic style but it is still higher with dynamic logic style.

However, if we compare the proposed dynamic logic cell in this work with the DRLC-7T from [12], it is clear that the POS-DRLC cell offers the minimum power consumption and it is also single-stage structure which has a direct impact on time delay and latency compared to a two-stage cell (DRLC-7T). The shortcoming of this cell is the inability to fulfil the "true" function but it is still have access to the XOR and XNOR functions, which are not available in the prior work [12].

To summarize, it seems that the new cell (POS-DRLC) furnish better results compared to the reconfigurable dynamic cells presented in previous works [7] [12] [13]. Furthermore, it offered the possibility to derive a static logic cell (CSL-DRLC) which showed an equal or better PDP compared to conventional 16nm-CMOS reconfigurable static logic cells regardless of the doubled number of configuration points required.

6. CONCLUSION

We have described and evaluated Fine-Grain reconfigurable logic cell based on DG-CNTFETs. The cell is inspired from product of sums (POS) to express logic functions and specifically exploiting the ambipolar property of DG-CNTFETs to furnish more complete set of functions over previous versions [12] [13]. Better performance and power consumption are also achieved. Moreover, a static version can be derived.

With a decreased time delay and increased power consumption, the DG-CNTFET cells showed a comparable PDP, when compared to a CMOS technology with a higher area because of the use of transmission gates instead of single transistors.

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