An Approach to Ternary Logic gates using FinFET

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ABSTRACT
Ternary logic has been evolved from binary logic due to its many advantages as it is energy efficient, less complex and faster speed for serial transfer. Due to these technological advancements ternary circuits have attracted many researchers to implement ternary circuits. In digital system, NOT, NOR and NAND are of importance as they are the main building blocks of many complex arithmetic and logic circuits. In this paper, we discuss the basic ternary gates and some circuits implemented by using FinFET. An extensive simulation is performed for all the gates and circuits using Tspice Simulator. FinFET is being adapted instead of traditional MOSFET because of its captivity over the drawbacks occurred during narrowing to nanometer scale. Results obtained have expected functionality of each gate and circuits, additionally there is enhancement in performance parameters.

Keyword
Multi Valued Logic; Ternary Logic; Ternary Gates; FinFET

1. INTRODUCTION
Since the era of semiconductors evolution from designing the integrated circuits for computers to mobile phones, it follows the Moore's Law. Semiconductor manufacturing foundries have been trying to meet the demand of customers by introducing as small as possible process node using FET technology. As approaching to the sub nanometer regime there tend to occur problem of leakage current and short channel effect which increases with the density. While moving down to sub nanometer range, it was not able to provide the gain as previous regime. Till then planar FET have reached the end of its life span but the semiconductor industries have found the alternative approach with FinFETs.

Complementary Metal Oxide Semiconductor(CMOS) has been ruling the semiconductor industries since decades to implement MVLsystems. The two levels binary logic performance is limited due to interconnect which occupy large area in VLSI chip. The ternary logic or radix 3 of MVL has three levels 0, 1,2 for balanced ternary logic and -1, 0 and 1 for unbalanced ternary logic. Binary system requires more number of digits as compared to ternary system. As a result more functions can be executed such as arithmetic and logical with higher speed and smaller number of computational stages. The proposed research aims on exploring advantages of FinFET for the design and simulation of Ternary gates and circuits. Ternary Inverter and basic gates are implemented using FinFET and some of their parameters are compared with the previous work . Some arithmetic and logic circuits are also implemented and their desired output is gained. The next section presents the structure of FinFET. Its advantages from Ternary prospective are also discussed. Section 3 presents a brief review of MVL(Ternary Logic).Section 4 details the proposed Ternary circuit designs and approach of basic gates and essential circuitries. It must be noted that other Ternary gates can further be designed using the TNAND and TNOR gates. The simulation results are illustrated in section 5, which also include rigorous timing analysis and analysis of Power Delay Product [PDP]. Then there is a section of parameters valued analyzed and compared with the previous work paper which concludes its benefits. Section 7 concludes the paper with the conclusion and discussion.

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2. FinFET
FinFET was first developed byCheming Hu and colleagues at University of California Berkely. It is a transistor designed to overcome Short channel Effect such as Drain Induced Barrier Lowering(DIBL) that is encountered while going down to sub-micron level.Short Channel effect make harder for the transistor to turn it off by stopping the flow of carriers through the channel This is done when it is hard to control the voltage on a gate electrode. The solution to this is by raising the channelabove the surface of the wafer instead of creating the channel just below the surface, it is possible to wrap the gate around up to three of its sides, providing muchgreater electrostatic control over the carriers within it [9].Figure 1 shows the structure of FinFET with SOI wafer as a basic platform, a thinfilm of silicon having thickness TSI is patterned on it. The gate shawls around the fin. The channel isformed perpendicular to the plane of the wafer.

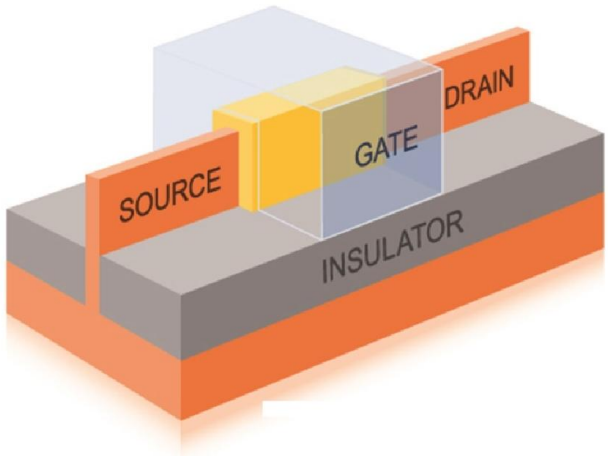

Figure 1.Structure of FinFET

Now, the key difference between FinFETbased design and that using conventional planar devices is that the freedom to choose the device's drive strength is reduced,especially for devices that are close to the minimum size. Drive strength can only be

improved during layout by adding more fins. The effective width of the devicebecomes quantized, and the quantization effect is worse for smaller transistors for which the next step up from the minimumsizedevice is one that is twice as wide. Inaddition, the minimum number of fins may be two in practical manufacturing processes. This is due to the self-alignedspacer processes that are used to create fins attight pitches – each sacrificial spacer element that is deposited creates a pair of fins.

At any one technology node the FinFET has several advantages over its planar counterpart including, but not limited to:

- Having excellent control of short channel effects in submicron regime, making transistors still scalable.
- Much Lower off-state current compared to bulk counterpart.
- Promising matching behavior
- Very good electrostatic control of the channel, meaning the channel can be "choked off" more easily. FinFETs boast a near ideal subthreshold behaviour (associated with leakage), something that's not easy to achieve in planar technology without considerable effort.
- High integration density, 3D, dueto vertical channel orientation delivers more performance per linear "w" than planar even after the isolation dead area between the fins is taken into account.

3. Ternary Logic

The performance of two levels binary logic is limited due to interconnectswhich occupy a large area on a VLSI chip. In a VLSI circuit, approximately 70percent of the area is devoted to interconnection, 20 percent to insulation, and 10percent to device [8].Powerful Arithmetic circuit has supported binary logic up till now. However, there are many disadvantages in binary compatible circuits such as interconnections and pin-out problems. The solution to this incorporating more logic levels than only to in binary (0 and 1).Ternary logic are functions, when third value is added to binary logic. Example shows ,15 = 1111 in binary and 120 in ternary100 = 1100100 in binary and 10201 in ternary which shows that less bits contains more value.Here 0,1and 2 denote the values as false, undefined, and true, respectively. Any n variable {X1,... ,Xn} ternary functionf(X) is defined as a logic function mapping {0, 1, 2}n
to {0, 1, 2}, where

$$X = \{X1, \ldots, Xn\}.$$

The basic operations of ternary logic can be defined as follows, where[5]

$$Xi, Xj = \{0, 1, 2\}:$$

$$Xi + Xj = \max\{Xi, Xj\}$$

$$Xi \bullet Xj = \min\{Xi, Xj\}$$

$$Xi = 2 - Xi. \quad (1)$$

Here + and • denotes OR, AND respectively and – represents subtraction.

By the perspective of theory, multivalued circuits should have below advantages over binary logic:Numbers of connection inside the chip is reduced in MVL as each wire transmits more information as compared to binary. Complexity of circuit is decreased as each MVL element process more information.As large chip contains more pins, the ON and OFF connections are reduced with the use of MVL logic.As the transmitted information per unit time is increased the speed of serial information will be faster. The ternary logic level is represented in two different ways: Balanced and Unbalanced. Balanced ternary logic level system has both positive and negative values in it, that has add mathematical advantages in numerical representation and in arithmetic operationsover the simple ternary logic system.

4. Ternary Circuit Design

4.1.1 Ternary Inverter

The fundamental part of most logic is Inverter and other of them are NAND and NOR gates which are constructed according to their structure. The same is valid for radix-3(ternary)and higher of them. Hence, when an efficient design of ternary inverter is implemented it results in enhancement of overall performance. Inverter is a great driver with its operation as well has a great driving capability. Ternary logic has three ways to define inverter as STI,PTI and NTI .PTI and NTI are binary inverters as they give two levels "0" and "2" at output. However, STI is the most efficient inverter, which generates real ternary logic at the output. Ternary inversion for the three types of inverter is defined by equation [12].

$$\boldsymbol{Xt} = \begin{cases} \boldsymbol{t} & , \boldsymbol{if\ x = 1} \\ \boldsymbol{t - X} & , \boldsymbol{if\ x \neq 1} \end{cases} \quad (2)$$

Where the value of ***t*** in above equation is 2 for PTI, 1 for STI and 0 for a NTI [12].

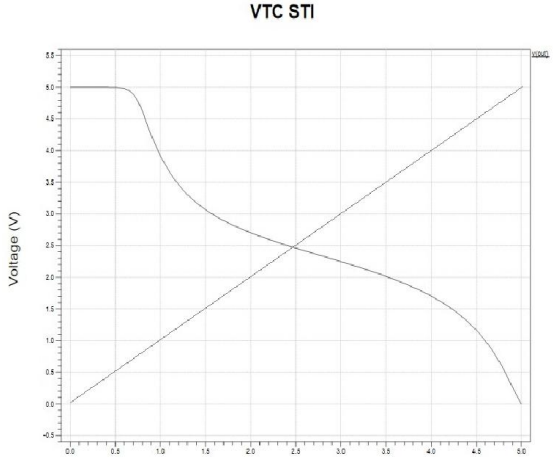

Figure 2.VTC of STI

The Fig.2 depicts the Voltage Transfer Curve [VTC] of the STI. Three states corresponding to logic level 0, 1 and 2 are clearly seen.

4.1.2 Ternary AND and NAND gates

Input A and B are given and Y and Z output are taken where Y is AND output and Z is NAND output. Here Y is minimum value of input signal and Z is inversion of Y value. These are the basic gates for building any further circuit. NOR and OR gates are also designed like same as this.

$$Y = [MIN\ (A, B)]$$

$$Z = INVERSE\ [MIN\ (A, B)]$$

Table 1. Truth Table of Ternary NAND and AND

A	B	Y	Z
0	0	0	2
1	0	0	2
2	0	0	2
0	1	0	2
1	1	1	1
2	1	1	1
0	2	0	2
1	2	1	1
2	2	2	0

4.1.3 Ternary Decoder

T-decoder (1to3) is a basically ternary combinational logic circuit with one-input and three-output, It converts ternary to unary functions for an input x.

Response of the ternary decoder to the input x is given [12] :

$$Xk = \begin{cases} 2, if\ x = k \\ 0, if\ x \neq k \end{cases} \quad (3)$$

Where, k = 0, 1, 2; which represents to higher voltage level-2, middle voltage level-1, and lower voltage level-0

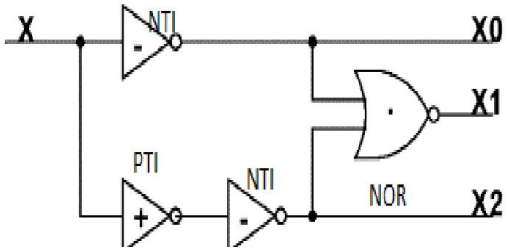

Figure 2.Ternary Decoder Schematic

4.1.4 Ternary Half Adder

The main function of the decoder is that when we give input to the decoder any one ofthe line is selected out of the three lines. Now in Half-Adder we give input X and Y totwo different decoder now the output of the decoders is first feed into the ternary logicAND gates to generate different terms, which is further passed into the two input ORgates which generates the Sum-Of –Product (SOP) terms. Here the output of theternary buffer gate is B now the final output of the ternary one-bit multiplier isgenerated by two SOP input with OR gate, out of which one of the input is fromTernary buffer and other is from the previous OR gate.

$$\textbf{Sum} = X2Y0 + X1Y1 + X0Y2 + 1 \cdot (X1Y0 + X0Y1 + X2Y2)$$
$$\textbf{Carry} = 1 \cdot (X2Y1 + X2Y2 + X1Y2)$$

The main function of ternary Half-Adder is to addition of two input (X and Y) andproduces two result out of which one bit is sum and other is carry.

Table 2. Truth Table of Half Adder

X	Y	SUM	CARRY
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

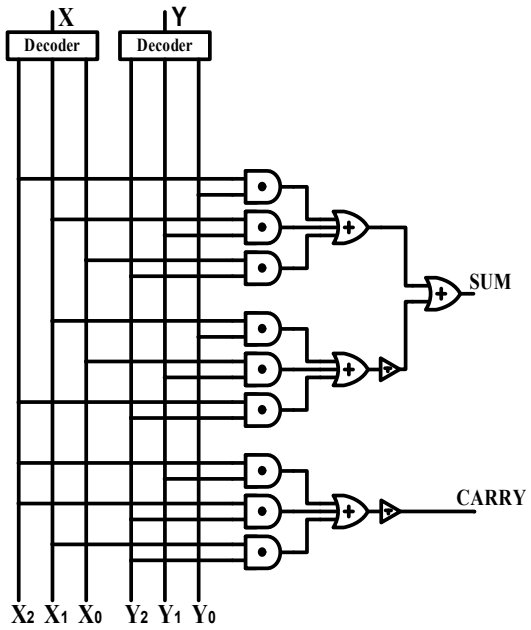

Figure 3.Ternary Half Adder

5. Simulation Result

In this section we discuss the simulation result of basic Ternary gates and Decoder. Tspice is used for simulation purpose and MOSFET model LEVEL 57 (**BSIM3SOI)** is taken into consideration. BSIMSOI is an international standard model for silicon-on-insulator (SOI) circuit design and it works similarly as FinFET device, thus this model is taken into consideration. The outputs of NTI, PTI, STI ,some basic gates,Ternary Decoder and Ternary Half Adder are observed as per their truth table described above. Here voltage level is 5V at 120 nm technology, as all the basic gates and circuit are implemented in ternary using FinFET device ,it is hard to develop it in below 120nm , once gates are implemented in this technology , we can try it on below technologies.

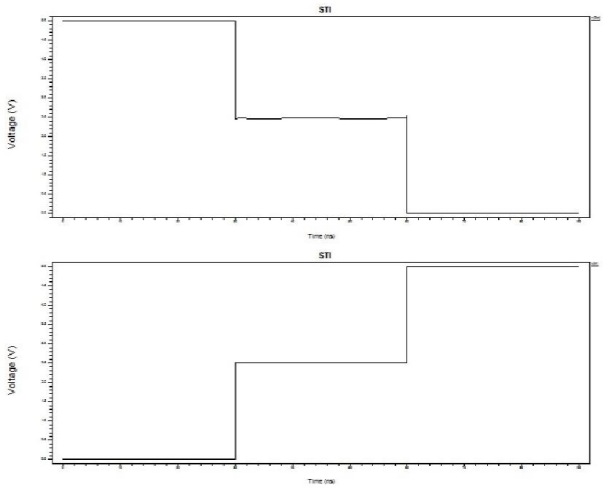

Figure 4.Input and Output waveforms of STI

Above Figure 4 describes the output and input waveform of ternary inverters. Here the operating voltage level is 5V, as it is expected to provide better fan in while implementing it for higher level designs. Inverter is the fundamental and primary part of any circuit. While implementing the designs withternary logic, it results in less computational steps.

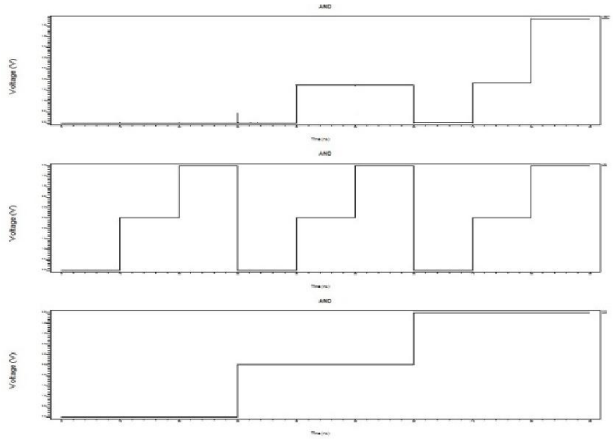

Figure 5.Input and Output waveforms of TAND

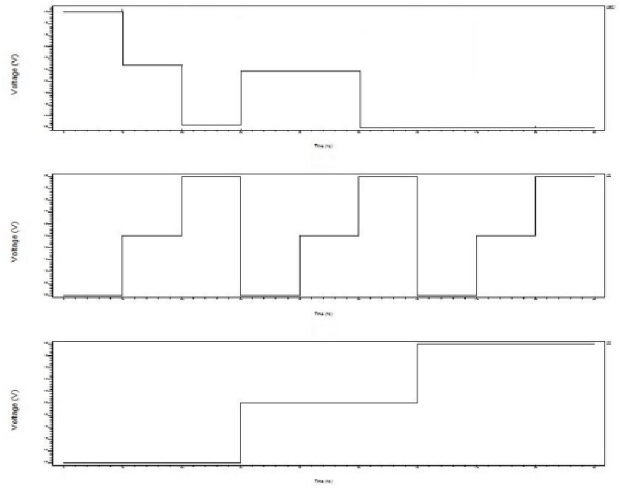

Figure 6.Input and Output waveform of TNAND

Figure 5 and 6 describes the input and output waveform of TAND and TNAND gates. These are the basic gates for any designs.

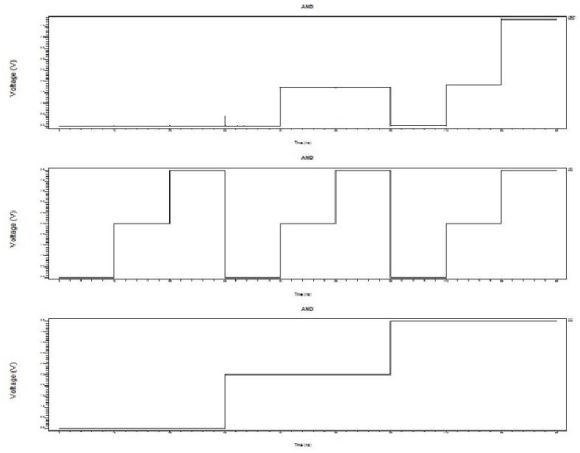

Figure 7.Input and Output waveform of TNOR

Above figure 7 shows the waveform for TNOR gates, by inverting this out output TOR gate can be produced and desired output can be gained

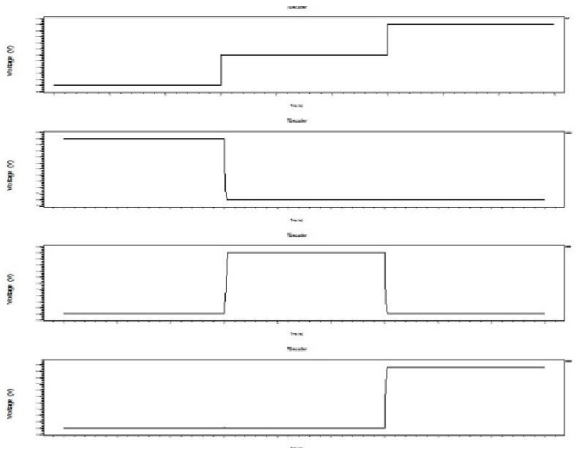

Figure 8.Input and Output waveform of Decoder

Figure 8 shows the waveform of Decoder, to implement any circuit ahead Decoder is needed.

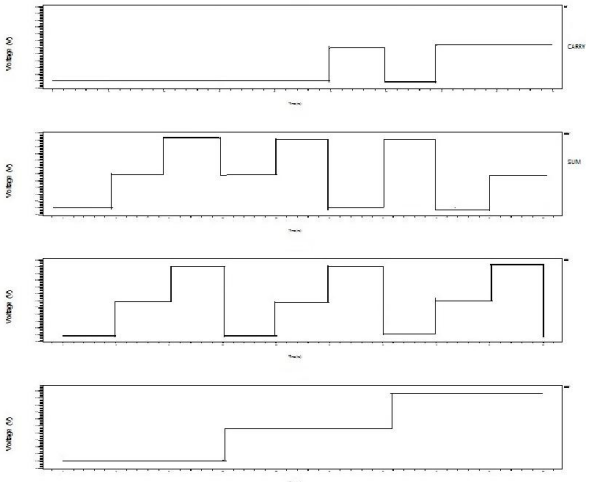

Figure 9.Input and Output waveform of Half Adder

Above figure shows the waveform of Half Adder, where two inputs are given and desired output is gained as sum and carry.

6. Result Analysis

Some parameters have been analyzed while simulating inverter and basic gates and there values are displayed. Table 3 shows the parameters and there readings of each design. These simulations are carried on T-spice tool and waveforms are displayed on W-edit. Power Delay Product (PDP) is the figure of merit to determine the quality of a digital gate.

Table 3. Parameters value of FinFET based Ternary gates

	Delay(sec)	Power Dissipation(W)	PDP (J)
STI	1.13e-12	8.00e-07	9.04e-19
PTI	3.00e-08	1.03e-06	3.11e-14
NTI	6.64e-14	8.78e-07	5.83e-22
TNAND	4.00e-08	1.87e-06	7.51e-14
TAND	5.00e-08	1.21e-06	6.08e-14
Half Adder	7.67E-09	1.95E-09	1.28E-17

Table 4. Comparison of average power consumed by TAND and TNAND

	Power Dissipation(W)	Ref[13]
TNAND	1.87e-06	0.191e-03
TAND	1.21e-06	0.213e-03

Table 4 describes the comparison of power dissipation of gates with some previous designs which are implemented in ternary logic.

Table 5. Comparison of average power consumed by STI

Ref [4]	Ref [11]	Proposed STI
0.7e-06	1.9e-06	8.00e-07

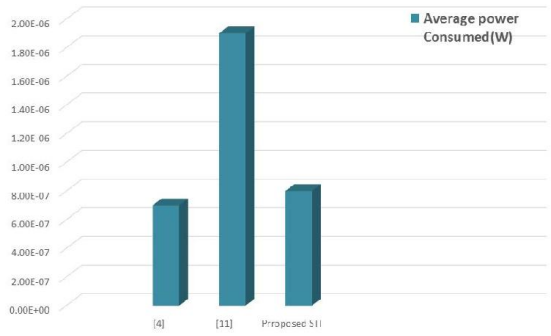

Figure 10.Graphical view of Avg Power consumed by STI

Table 5 describes the comparison of average power consumed of STI with some previous designs and its graphical representation is shown in figure10. Here it is observed that the Proposed STI consumes lessamount of power than other.

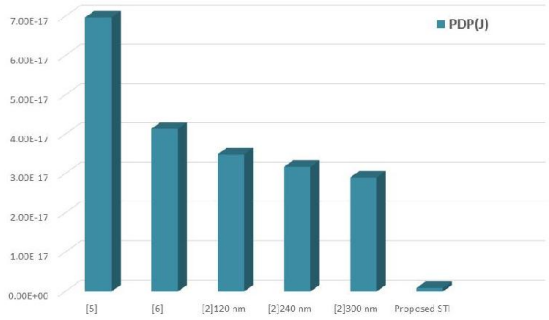

Figure 11.Graphical view of PDP for STI

Figure 11.Shows the Power Delay Product of STI, compared by different modelsand the proposed one. Here it is observed that the Proposed STI consumes lessamount of power than other.

Table 6. Comparison of PDP product of HA

Ref [12]	Ref [1]	Proposed HA
0.411e-15	0.543e-15	0.128e-16

Above table 6 describes the comparison of PDP product of Half Adder with the previous work done on CNTFET using Ternary logic.

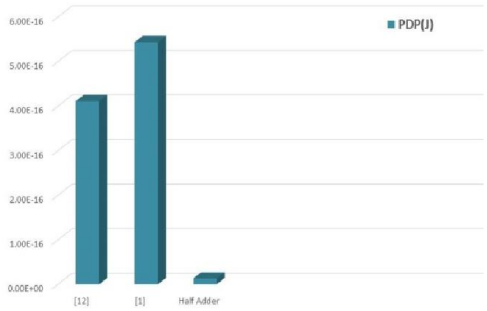

Figure 12.Graphical view of PDP for Half Adder

As observed from above comparison it is concluded that PDP product by HalfAdder is much less than the other referenced work. Now as few of the gates and circuits parameters are compared with previous, it can be concluded that the overallefficiency and other prospects of power consumption are enhanced.

7. CONCLUSION

As nowadays CMOS is been scaled down to Nano meters there occurs manydrawbacks as Short channel effect, Drain Induced Barrier Lowering(DIBL) and hot electron effect. An extensive simulation of all the designed gates is carried out using TSPICE

circuit simulator. The results demonstrate expected functionality of the proposed gates and an additional improvement in the performance parameters is also achieved .FinFET has great controllability over short channel effect thus makingit as a booming technology replacing CMOS. Proposing basic gates ,Arithmetic and Logic Circuits based on Ternary Logic using FinFET can be reliable because by Using TernaryLogic, it is possible to accomplish simplicity & energy efficiency in modern digital design. Here many parameters are compared and desired output andcalculations conclude that Circuits using FinFET and ternary is efficient than theprevious designs.

8. REFERENCES

[1] A.P. Dhande ,V. T. Ingole*" Design And Implementation Of 2 Bit TernaryALU Slice* "3 RD INTERNATIONAL CONFERENCE: SCIENCES OF ELECTRONIC, TECHNOLOGIES OF INFORMATION ANDTELECOMMUNICATIONS",2005

[2] Akbar Doostaregan , Mohammad Hossein Moaiyeri, KeivanNavi and OmidHashemipour " *On the Design of New Low- Power CMOS StandardTernary Logic Gates*" IEEE COMPUTER SOCIETY,2010.\

[3] Aqilah binti Abdul Tahrim , Michael Loong Peng Tan "*Design andImplementation of a 1- bit FinFET Full Adder Cell for ALU in SubthresholdRegion*" IEEE-ICSE2014 Proc,2014.

[4] ArijitRaychowdhury*, Student Member, IEEE,* and Kaushik Roy*, Fellow,IEEE "Carbon-Nanotube-Based Voltage-Mode Multiple-Valued LogicDesign*" IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 4,NO. 2, MARCH 2005

[5] H.T. Mouftah and I. B. Jordan, "Integrated circuits for ternary logic," InProc. international symposium on multiple valued logic, 1974, pp. 285-302.

[6] H. T. Mouftah and K.C. Smith, "Injected voltage low-power CMOS for 3-valued logic," IEE Proc. G, vol. 129, no. 6, pp. 270-272, Dec. 1982.

[7] Jamil Kawa, Andy Biddle"FinFET :The promises and challenges " An article fronm Synopsys Insight, Issue 3, 2012

[8] J.T. Butler, *Multiple-Valued logic in VLSI*, IEEE Computer Society Press

[9] Mary Ann White" What makes FinFET so compelling" An article by new electronic 08 oct,2013

[10] Michael C. Wang "*Low Power, Area Efficient FinFET Circuit Design"*Proceedings of the world Congress on Engineering and ComputerScience,2009.

[11] RichaSaraswat ,ShyamAkashe and ShyamBabu" *Designing andSimulation of Full Adder Cell Using FinFET Technique*"IEEE,2012.

[12] Sheng Lin, Yong-Bin Kim ,Fabrizio Lombardi " *CNTFET –Based TernaryLogic Gates and Arithmetic Circuits*" IEEE TRANSACTIONS ONNANOTECHNOLOGY,2011.

[13] V.T. Gaikwad, P.R. Deshmukh "*Design of CMOS Ternary Logic Familybased on Single Supply Voltage* "International Conference On PervasiveComputing(ICPC),2015