Modeling Noise Transfer Characteristic of Dynamic Logic Gates

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ABSTRACT

Dynamic noise analysis is recently gaining more attention as a definitive method to overcome glaring deficiencies of static noise analysis. Exact dynamic noise analysis requires modeling of both injected noise and propagated noise. In this paper, we have developed a strategy to study the noise propagation problem. An efficient analytical formula has been derived to accurately model the noise waveform transfer characteristic of dynamic CMOS logic gates. Experiments have shown that the maximum error in peak propagated noises of the proposed model is less than 10%.

I. INTRODUCTION

Static noise analysis, where inputs and outputs of the logic gates are assumed to be DC signals, is studied extensively in the literature [1]-[2]. However, static noise analysis can be very pessimistic. Input noises with very short duration may not cause significant voltage change in gate output even if the input noise peak is greater than the static noise margin of the gate [3]. With the continuous technology scaling, we are heading towards the scenario that static noise analysis will flag too many false errors causing unnecessary design revisions and sacrifices in other design metrics like area, speed and power consumption to resolve the false noise violation.

Dynamic noise analysis considers not only the noise peak but also the duration of the noise [4]-[5]. In general, entire time-varying waveforms of the noises are modeled. For proper analysis of dynamic noises in a circuit, the noise waveform at each node should be first obtained. The total noise at a node is the combination of, 1) injected noise at the present node, and 2) noise from previous stage, referred to as propagated noise. The majority of previous research works on signal integrity have discussed the noise injection modeling problem. The modeling of the noise propagation phenomena or the cell noise waveform transfer characteristic, is not yet well studied.

In this paper, we describe an efficient method to model gate noise waveform transfer characteristics that can be used in a dynamic noise analysis tool. The accuracy of the proposed model is verified by comparing with SPICE simulation results.

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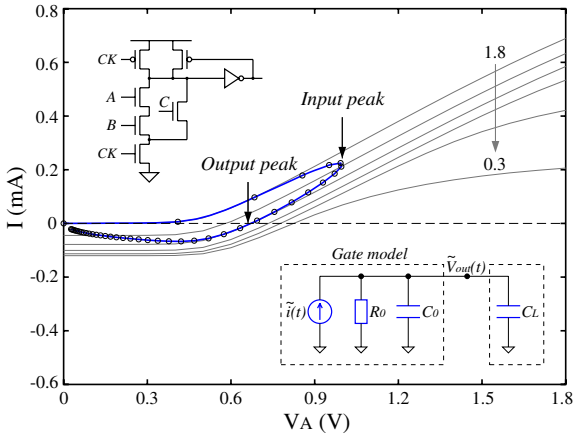

Fig. 1. Dynamic logic gate modeling.

II. NOISE TRANSFER CHARACTERISTIC MODELING

A. Gate modeling

The schematic of a typical dynamic logic gate is illustrated in the top left inset of Fig. 1. The grey curves in Fig. 1 show the I-V characteristic of the gate with various output voltage values. The dark curve in the figure illustrates the locus of operating points of a typical input noise. The input noise waveform reaches peak at the right end of the locus curve and the output noise drop is maximized when the curve intersects the x-axis.

As shown in the bottom right inset of Fig. 1, we model the PMOS keeper with a resistor of value R_0 and the parameter C_0 is used to measure the intrinsic capacitance of the gate. We then model the pull-down n-network as a voltage controlled current source and assume the current has a simple linear dependency on input voltage when the input voltage exceeds a threshold voltage V_T: $\widetilde{I}(t) = k(\widetilde{V}_{in}(t) - V_T)$, where the tilde mark refers to the deviation of the measures from their nominal values. In all, our simple circuit model consists of four parameters: transconductance k, threshold voltage V_T, holding resistance R_0, and intrinsic capacitance C_0.

B. Noise waveform modeling

We model the input noise waveform using a multiple-pole approximation: $\widetilde{V}_{in}(t) = a_0 + \sum_{i=1}^{N}\left(a_i \cdot e^{-p_i t}\right)$, where p_i's and a_i's are poles and residues, respectively, a_0 is the DC compo-

TABLE I

EXTRACTED PARAMETERS AND MODEL ERRORS IN PEAK NOISE.

Cell (In)	V_T (V)	k (mA/V)	R_0 $(K\Omega)$	C_0 (fF)	Avg err (%)	Max err (%)
nand2 (A)	0.504	0.536	6.65	4.47	2.42	8.73
nand2 (B)	0.521	0.605	7.78	6.80	3.25	8.41
nor2 (A/B)	0.561	0.390	7.26	4.73	2.38	8.10
aoi21 (A)	0.493	0.518	6.65	6.14	3.10	8.36
aoi21 (B)	0.521	0.614	7.80	7.62	3.17	8.18
aoi21 (C)	0.563	0.393	7.37	6.03	2.28	7.95

nent of the input noise, and in practice N is usually a small positive integer. Those modeling parameters can be obtained for an arbitrary noise waveform using Padé approximation. This multiple-pole formula is able to accurately model noise waveforms.

Based on the proposed gate model and the noise waveform model, we have derived a closed-form formula for the output noise waveform:

$$\widetilde{V}_{out}(t) = \begin{cases} 0 & t \le t_1 \\ kR_0\big(\Phi(t) - \Phi(t_1)e^{-(t-t_1)/\tau}\big) & t_1 < t \le t_2 \\ \widetilde{V}_{out}(t_2)\cdot e^{-(t-t_2)/\tau} & t > t_2 \end{cases} \quad (1)$$

where $\Phi(t) = (a_0 - V_T) + \sum_{i=1}^{N}\big(a_i/(1-p_i\tau)\big)e^{-p_i t}$, τ equals $R_0(C_0+C_L)$, and (t_1, t_2) is the timing window when the input noise voltage exceeds the threshold voltage V_T.

C. Noise sensitivity

We define the DC *noise sensitivity* $S_{dc}(t)$ of a gate as the partial derivative of output noise with respect to the DC component of the input noise, a_0. This DC noise sensitivity under the multiple-pole waveform approximation has the following simple form.

$$S_{dc}(t) = -kR_0\big(1 - e^{-(t-t_1)/\tau}\big). \quad (2)$$

Similarly, we can define the AC *noise sensitivity* $S_{ac}(t)$, which measures the sensitivity of the output noise with respect to the AC component of the input noise, and we have derived the following formula.

$$S_{ac}(t) = -kR_0\sum_{i=1}^{N}\frac{e^{-p_i t} - e^{-p_i t_1 - (t-t_1)/\tau}}{1 - p_i\tau}. \quad (3)$$

In circuit design applications, the DC noise sensitivity is useful for noises caused by power/ground voltage mismatch between the driver and the receiver. On the other hand, the gate AC noise sensitivity metric is important for many other noise types like interconnect coupling noise.

D. Experiments

We have applied our model to three example dynamic CMOS gates to test the accuracy of the model. The logic gates are designed using a 0.18 micron process with a supply voltage of 1.8 V. We have used two-pole approximation for the input noise waveforms. For each input of each gate, we have generated 500 random cases spanning a wide range of possible input noise waveforms (a_0, a_1, p_1, and p_2) and output load (C_L). The gate noise transfer model parameters (k, V_T, R_0, and C_0) are chosen such that the sum of the square errors is minimized. The extracted parameters for the three gates as well as average and maximum model errors in comparing with SPICE simulation results are shown in Table I. The average error in peak output noise is about 3% and the maximum errors are always less than 10%. In Fig. 2, model output noise waveforms of the *aoi*21 gate are compared with SPICE simulation results. The model curves are able to match SPICE results very well in term of both noise peak and overall noise waveform.

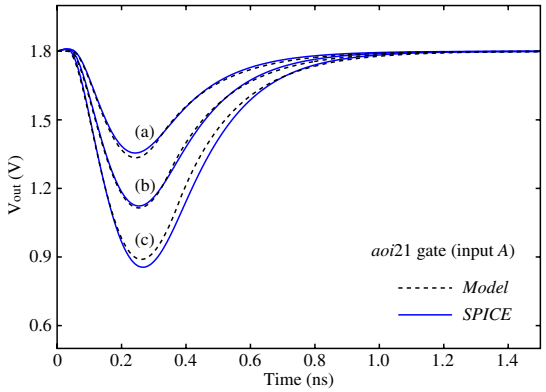

Fig. 2. Comparison of output waveforms. $C_L = 20fF$, $a_0 = 0$, $p_1 = 5.0$ GHz, $p_2 = 10.0$ GHz. (a) $a_1 = 3.0$. (b) $a_1 = 3.4$. (c) $a_1 = 3.8$.

III. CONCLUSIONS

In this paper, we have presented an efficient method to model the gate noise transfer characteristic for dynamic CMOS logic gates. Both DC and AC noise sensitivity formulas are derived that can be used as guidances in circuit and layout design phases to improve gate dynamic noise tolerance. Experiments have shown that noise waveforms obtained by the proposed model match with SPICE simulation results very well.

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