Ultra-Low Energy Reconfigurable Spintronic Threshold Logic Gate

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ABSTRACT
This paper introduces a novel design of reconfigurable Spintronic Threshold Logic Gate (STLG), which employs spintronic weight devices to perform current mode weighted summation of binary inputs, whereas, the low voltage spintronic threshold device carries out the thresholding operation in an energy efficient manner. The proposed STLG can operate at a small terminal voltage of ~50mV, resulting in ultra-low energy consumption. The device-circuit simulation results for common benchmarks show that the proposed STLG circuit can achieve 87.5% and 11.1% energy reduction compared with state-of-the-art CMOS look-up-table (LUT) and Memristive Threshold Logic Gate (MTLG) respectively. The ultra-low programming energy of spintronic weight device also leads to three orders lower reconfiguration energy of STLG compared with MTLG design.

Keywords
Magnetic domain wall strip; Reconfigurable logic; Threshold logic; Magnetic tunnel junction; Spintronic

1. INTRODUCTION
A threshold logic gate (TLG) essentially constitutes of summation of weighted inputs, followed by a threshold operation as shown in Fig. 1, where IN_i's are multiple binary inputs, W_i's are scalar weights with which the corresponding inputs are multiplied and θ is the threshold [1]. The same TLG circuit can implement different Boolean functions by reconfiguring the weights, threshold, or both. In previous research, TLG has been implemented in CMOS and other bulk semiconductor technologies, such as CMOS look-up-tables (LUT) [1][3], single electron transistors [4] and resonant tunneling diode [5]. Such hardware implements suffer from power, delay and area overhead. Recent discovery of nano-scale memristor, whose resistance can be programmed with an applied electric field, has led to proposal of energy-efficient reconfigurable memristive TLG (MTLG) [2][3][6]. Compared with CMOS LUT based TLG design, such MTLG designs can potentially provide two orders lower energy consumption and high area density [3][11]. However, due to the intrinsic high energy consumption and long programming delay of memristor (Ag-Ch[2], TiO2[3]), the memristor based TLG suffers from high power and long delay in reconfiguration operation, thereby eschewing the benefits of reconfigurable logic computing.

Recent experiments on spintronic devices have demonstrated high speed switching of nano-scale magnets with spin polarized currents [7][14]. Together with other characteristics, including non-volatility, zero leakage current and high integration density, spintronic devices have been explored to design compact, low power memory [13], Boolean logic [8][11], analog and neuromorphic computing [9][10][12][13]. In this work, we propose a spintronic weight device (SWD) based on magnetic domain wall strip and magnetic tunnel junction. The continuous conductance of SWD can be programmed using a small current (~30μA) pulse within 2 ns. We then propose an ultra-low voltage (~50mV) spintronic TLG (STLG) design that employs SWD to perform current mode weighted summation of binary inputs, whereas, the low voltage spintronic threshold device carries out the threshold operation in an energy efficient manner. Spintronic device-circuit simulations for common benchmarks show that the proposed STLG achieves ultra-low energy consumption for both computation and reconfiguration operations compared with CMOS LUT and MTLG designs.

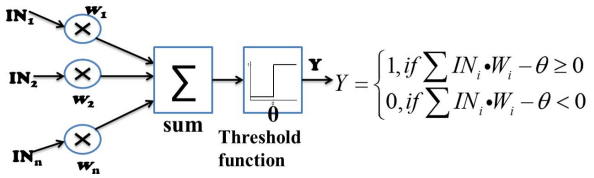

Figure 1. A schematic representation of threshold logic gate (TLG) and its mathematical expression

The rest of this paper is organized as follows. Section-2 presents the proposed spintronic weight device structure and circuit model. In section-3, the spintronic threshold device in TLG is introduced. The proposed circuit design of spintronic threshold logic gate is presented in section-4. Section-5 discusses the device-circuit co-simulation of the proposed STLG and performance comparison with CMOS LUT and MTLG. Section-6 concludes the paper.

2. SPINTRONIC WEIGHT DEVICE
A TLG can be divided into three steps, i.e. *weighing*, *summation* and *thresholding* as shown in Fig.1. In this section, we present the device structure and operation of the proposed spintronic weight device (SWD). The SWD has a programmable continuous conductance range, which can be employed to implement the first step (weighing) of a TLG.

The proposed SWD is based on a composite device structure consisting of a Domain Wall Motion (DWM) magnetic strip and a magnetic tunnel junction (MTJ) as shown in Fig. 2a. The MTJ consists of two ferromagnetic layers with an insulator (MgO) barrier sandwiched between them. The 'free' ferromagnetic layer (d4) connects laterally to two anti-parallel fixed magnetic domains - d1 and d2 [9][15][16]. The transition area between these two domains is called *domain wall* (DW). The larger thickness at the edges of the free layer is used to stabilize the DW at an

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intermediate position within the free layer [15]. Recent experiments have shown that the steady DWM can be induced using current injection along the magnetic nano-strip [14][17]. For example, in Fig. 2a, when the electrons are injected into d2, they become spin-polarized and exert a Spin-Transfer Torque (STT) on the DW. If the STT is large enough to overcome the pinning field, it leads to steady DWM (to d1 in this case). The authors in [14] demonstrate steady DWM critical current density of ~6×10^{11}A/m^2 and ~60m/s DW velocity for 20nm-wide magnetic nano-strips. A *Neel* type DW is formed due to the small strip width (20nm) [14].

The proposed SWD device can be treated as a four terminal device with lateral and vertical current paths. For the lateral path (d1 to d2, ± x direction), d1 forms the input programming port, assuming d2 is supplied with a constant voltage. The DW can be moved along the free layer depending on the lateral current pulse magnitude, direction and duration [14][17], leading to a continuous resistance/ conductance change of the MTJ in the vertical direction.

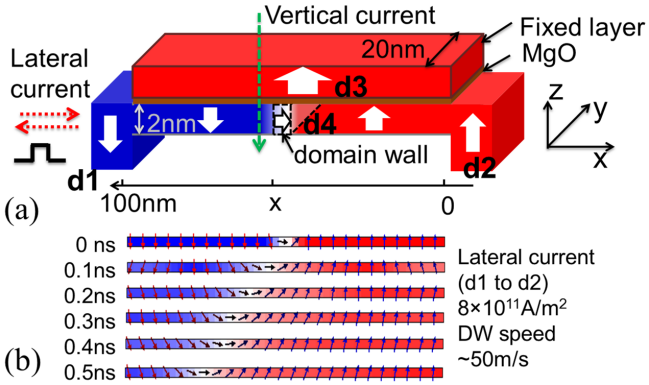

Figure 2. (a) The proposed spintronic weight device structure, (b) micro-magnetic simulation of free layer DW motion with 8×10^{11} A/m^2 lateral current injection from d1 to d2

The transient micro-magnetic simulation plot of the free layer using *mumax*[3] [18] is shown in Fig. 2b, where a 0.5ns current pulse with magnitude of 8×10^{11}A/m^2 is applied from d1 to d2. The device parameters used in the simulation are listed in table-1[9]. We benchmarked the micro-magnetic simulation with the experimental data in [14] (the same nano-strip width of 20nm is fabricated) and it shows a good match as shown in Fig. 3a.

The vertical path (from d3 to d4, ± z direction) is used for sensing the position of DW in terms of MTJ vertical conductance. MTJ conductance is a function of voltage, tunneling oxide thickness (t_{MgO}) and the angle between free layer and pinned layer magnetizations. The atomistic level simulation framework based on Non-Equilibrium Green's Function (NEGF) formalism [19] is used to evaluate the MTJ resistance. In order to simulate the proposed device with CMOS interface circuits in HSPICE, SWD is modeled as three parallel MTJs with variable conductance

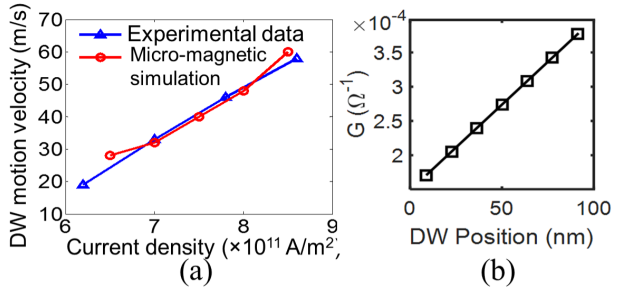

Figure 3. (a) Simulated DW motion velocity vs. lateral current density, (b) SWD conductance vs. DW position in the free layer

Table 1. SWD device parameters

Symbol	Quantity	Values
α	Damping coefficient	0.02
Ku	Uniaxial anisotropy constant	3.5×10^5 J/m3
Ms	Saturation magnetization	6.8×10^5 A/m
A_{ex}	Exchange stiffness	1.1×10^{-11} J/m
P	Polarization	0.6
t_{MgO}	MgO thickness of SWD	1.1nm

depending on DW positions.

$$G_L = \left(W\left(L - x - 0.5L_{DW}\right)\right)/RA_{AP} \quad (1)$$

$$G_R = \left(W\left(x - 0.5L_{DW}\right)\right)/RA_P \quad (2)$$

$$G_{DW} = \left(WL_{DW}\right)/RA_{DW} \quad (3)$$

where, G_L, G_{DW} and G_R are respectively the vertical conductance of left anti-parallel, domain wall and right parallel equivalent MTJ conductance; x is DW position (middle point), L is the length of free layer (100nm), L_{DW} is the domain wall length, W is the width of free layer, RA_{AP}, RA_{DW} and RA_P are respectively MTJ resistance-area product for anti-parallel, DW and parallel configurations obtained in the NEGF based MTJ model [19]. The conductance of the SWD can then be computed as:

$$G_{SWD} = G_L + G_{DW} + G_R \quad (4)$$

Fig. 3b shows the SWD conductance is linearly proportional to the DW positions in the free layer (with t_{MgO}=1.1nm). Thus, this device can be employed as weights at the inputs of a TLG by programming to a specific conductance. Based on our micro-magnetic simulation, the conductance of SWD can be programmed from minimum to maximum using a 30µA-2ns current pulse, which leads to low reconfiguration energy of the proposed TLG.

3. SPINTRONIC THRESHOLD DEVICE

In this section a spintronic threshold device (STD) is described. It will serve as the third step (thresholding) of a TLG.

The device structure of STD is shown in Fig. 4a. It constitutes of a thin and short nano-magnet domain-d3 connecting two anti-parallel fixed magnetic domains, i.e. d1 and d2. Domain-1 forms the input port and domain-2 is grounded. The magnetization of free layer (d3) can be written parallel to d2 by injecting a current (larger than critical current) along it from d1 to d2 and vice-versa [11][14]. A fixed small magnet m1 and d3 form a MTJ to read the state of d3. Unlike in SWD, the fixed layer of sense MTJ in STD is very small (20nm×20nm). The resistance states are binary, i.e. either high (AP) or low (P).

The threshold of STD, i.e. the minimum current magnitude required to switch the free layer magnetization (move DW from one end to the other end), is determined by the critical current density and DW velocity. Based on our micro-magnetic simulation and device dimension as shown in Fig. 4a, the STD current threshold is ~30µA for 1ns switching, corresponding to DW velocity of ~50m/s. Recently, application of spin orbital coupling has been explored for reducing the critical current and increasing DWM velocity [20]. The threshold current can be

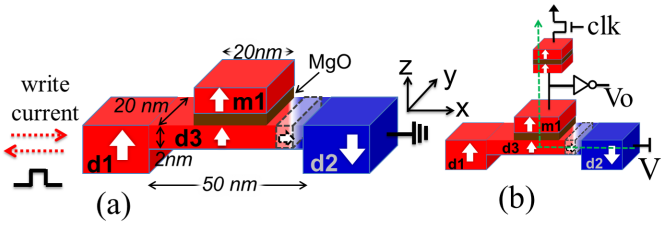

Figure 4. (a) STD device structure, (b) STD sense circuit

further reduced to be less than 10µA. The effective resistance of the MTJ formed between m1 and d3 is smaller when they have the same magnetization and vice versa. The ratio of the two resistances is defined in terms of tunneling magnetoresistance (TMR). As shown in Fig. 4b, STD forms a voltage divider with a fixed reference MTJ to sense the resistance state. Static current in the voltage divider can be minimized by increasing the MTJ oxide thickness. Note that in the detection circuit, the transient current with short duration (1ns) and low magnitude (~2µA) flows from d2 to m1, which will not disturb the state of d3. In summary, the circuit in Fig. 4b can detect the polarity of the current flow at its input node, acting as an ultra-low voltage and compact current comparator that can be employed in the following STLG design.

4. DESIGN OF SPINTRONIC THRESHOLD LOGIC GATE

Fig. 5 shows the circuit realization of a single Spintronic Threshold Logic Gate (STLG). In this section, we use two input STLG as an example to explain the design. Larger number of fan-ins can also be implemented and will be analyzed in section-5. This design mainly consists of three components, corresponding to three steps of a TLG, namely *weighing*, *summation* and *thresholding* as shown in Fig. 5. In STLG, SWD conductance can be pre-programmed to specific values (listed in Table-3) for different Boolean functions. Since the weights and threshold of a TLG can be either positive or negative, two SWDs combined as one *weight unit* are used to represent one input weight. For example, in Fig. 5, the difference of G_{1+} and G_{1-} represents the weight for input-1(i.e. $W_1=G_{1+}-G_{1-}$), which can be positive, negative or zero. Note that, in the proposed design the threshold is treated as the weight of an extra reference input whose value is always high (V_{ref} in Fig.5). Thus, the TLG function can be rewritten as $output= sign(\sum IN_i*W_i-1*W_r)$, where IN_i is the Binary input, W_i is the corresponding weight and W_r is the threshold value. Note that, in Table-2, $Ref=-W_r$. The input voltage signal to STLG is received through CMOS transistors with source terminals connected to a potential $V+\Delta V$ (for positive SWD) and $V-\Delta V$ (for negative SWD) where ΔV can be $\sim 50mV$. These input transistors act as deep triode region current sources (DTCS) [11]. The STD is connected to a DC supply-V. The static current therefore flows across a small terminal voltage of ΔV, resulting in small static power consumption. Moreover, the dynamic power dissipation is also largely reduced due to ultra-small voltage swing. Due to the small resistance of magneto metallic STD, the current flowing through out of each weigh unit is approximately $V_i\Delta V(G_{i+}-G_{i-})$, where V_i is binary value (0 or 1) indicating input state, G_{i+} and G_{i-} are the corresponding SWD conductance. Thus the current out of each weight unit can be either positive ($G_{i+}>G_{i-}$ & $V_i=1$), negative ($G_{i+}<G_{i-}$ & $V_i=1$) or zero ($G_{i+}=G_{i-}$ or $V_i=0$). Thus the positive or negative weights of each input is encoded as the conductance difference of G_{i+} and G_{i-}. The current flowing into the input of STD is expressed as $I_{STD}=\sum[V_i\Delta V(G_{i+}-G_{i-})+1*\Delta V(G_{r+}-G_{r-})]$. The direction of current flowing at the input of a STD, and hence the output of a TLG, would depend upon the input data and the corresponding weights. Table-2 and Table-3 list

Table 2. Different Boolean function weights

Function	Weight				Function	Weight			
	A	B	C	Ref		A	B	C	Ref
AB	2	2	-	-3	A+B	2	2	-	-1
ABC	1	1	1	-3	A+B+C	1	1	1	-1
AB+BC+CA	1	1	1	-2	A+BC	2	1	1	-2
AB+AC	2	1	1	-3					

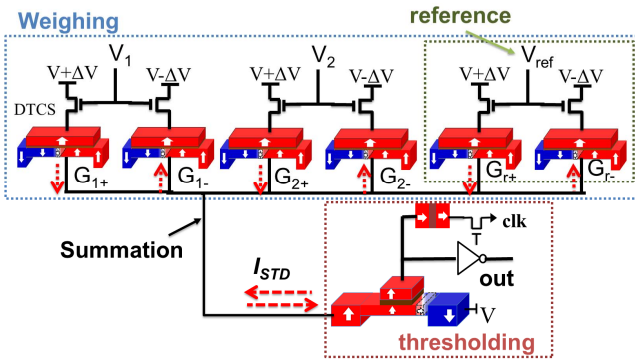

Figure 5. Proposed spintronic threshold logic gate

the detailed resistance values of weights and references for different Boolean functions. The output of the STD detection circuit associated with each TLG, in turn, drives the fan-out TLGs. Due to the non-volatility of the STD, the proposed STLG design can be easily extended to realize a pipelined architecture without inserting the CMOS latches.

5. SIMULATION AND PERFORMANCE

In this section, we discuss circuit simulation and performance of the proposed STLG. 45nm NCSU Product Development Kit (PDK) library is used in HSPICE circuit simulation [21].

In this work, 2-input and 3-input linearly separable Boolean functions [3] are employed to demonstrate the functionality and performance of the proposed design. Table-2 lists few samples of TLG Boolean functions with their weights and references (negative value of threshold). Table-3 lists the SWD resistance values for different Boolean functions. Fig. 6 shows the HSPICE transient simulation plots for STLG implementing 2-input "AND" Boolean functions. Three complementary clocks are used in the circuit simulation. The first clock is "reset" clock, which is used to reset the STD. A -32µA current is applied at the input terminal of STD, leading to shift of DW to the right end of domain-3. The initial state of STD sense MTJ is in parallel state. When "Clk1" is on ('computation' cycle in Fig.6), the input voltages are applied in the corresponding DTCS transistors and the net current flowing into the STD is determined by the weighted summation of inputs. When the net current is greater than the threshold current, DW will be moved to the left (i.e. sense MTJ in AP state), or the sense MTJ still remains in P state (initial state). For input "A" and "B" with values of (11, 10, 01, 00), the corresponding net current flowing into STD is (31, 26, 26, 21)µA. Since the threshold current of STD is ~30 µA, it can be seen in Fig. 6 that the sense MTJ resistance (R_MTJ) is (high, low, low, low). When "Clk2" is on ('sense' cycle), the STD sense circuit read the state of MTJ and sends the binary voltage output to next TLG through an inverter.

Fig. 7a presents the computation energy consumption of STLG compared with CMOS LUT and MTLG [3] for linearly separable Boolean functions. It can be seen that both STLG and MTLG are much more energy efficient than CMOS LUT. On average, STLG

Table 3. Different STLG weights and energy

Function	A+ (KΩ)	A- (KΩ)	B+ (KΩ)	B- (KΩ)	C+ (KΩ)	C- (KΩ)	Ref+ (KΩ)	Ref- (KΩ)	Energy (fJ)
AB	3.24	5.85	3.24	5.85	-	-	5.85	2.65	5.7066
A+B	3.24	5.85	3.24	5.85	-	-	5.85	4.17	6.3231
ABC	4.17	5.85	4.17	5.85	4.17	5.85	5.85	2.65	6.8544
A+B+C	4.17	5.85	4.17	5.85	4.17	5.85	5.85	4.17	6.4848
AB+BC+CA	4.17	5.85	4.17	5.85	4.17	5.85	5.85	3.24	6.6726
A+BC	3.24	5.85	4.17	5.85	4.17	5.85	5.85	3.24	6.6726
AB+AC	3.24	5.85	4.17	5.85	4.17	5.85	5.85	2.65	6.8544

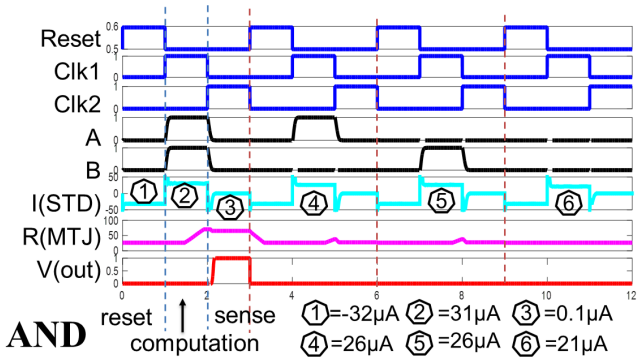

Figure 6. HSPICE simulation results of STLG implementing "AND" Boolean functions

consumes 87.5% and 11.1% less energy compared to LUT and MTLG respectively. Such large energy saving mainly due to 1): ultra-low voltage (~50mV) across STLG 2): low STD current 3): DTCS transistors working in deep triode region. As for delay of TLG design, STLG is the worst due to three step operations, namely reset, computation and sense.

Recent proposed MTLG attracts a lot of interests due to the non-volatility, programmability and high area density of memristors [2][3]. However, MTLG suffers from high reconfiguration energy consumption due to high programming voltage (0.6V in Ag-Ch memristor[2] and 1.3V in TiO_2 memristor[3]) and long programming time (few μs [2]). Our proposed SWD conductance can be programmed much more energy efficiently and faster, greatly lowering the reconfiguration energy consumption in TLG design. In this work, we define the *reconfiguration energy* as the averaged energy of programming the weight from minimum to maximum and from maximum to minimum. For CMOS LUT, it is the averaged energy of writing "0" and writing "1". For Ag-Ch memristor, authors in [2] used 0.3V~1μs and -0.6V~1μs voltage pulses to program memristance between 10KΩ to 100KΩ. While in spintronic weight device, a ±30μA~2ns current pulse can move the DW from one end to the other, thus programming the weight from minimum to maximum or maximum to minimum. Fig. 7c and 7d present the reconfiguration speed and energy consumption of LUT, memristor (Ag-Ch) and SWD. It can be seen that the CMOS LUT consumes least energy and has the fastest programming speed. SWD reconfiguration energy and delay are slightly larger than CMOS LUT, however, it is almost three orders lower in energy consumption and three orders faster in programming speed compared with memristors (Ag-Ch) [2].

6. CONCLUSION

In this paper, we propose a spintronic weight device that can be combined with spintronic threshold device to design spintronic threshold logic gate. Ultra-low energy is achieved due to low voltage (~50mV), low current computing facilitated by the spintronic devices. Such spin-CMOS hybrid hardware can achieve 87.5% and 11.1% energy reduction compared with state-of-the-art CMOS LUT and memristor based threshold logic gate designs respectively. Moreover, the spintronic weight device also leads to low power and fast speed in reconfiguration operation of the proposed design. Compared with reconfigurable MTLG design, the proposed STLG consumes three orders lower reconfiguration energy, opening a new door for future post-CMOS, ultra-low energy reconfigurable computing era.

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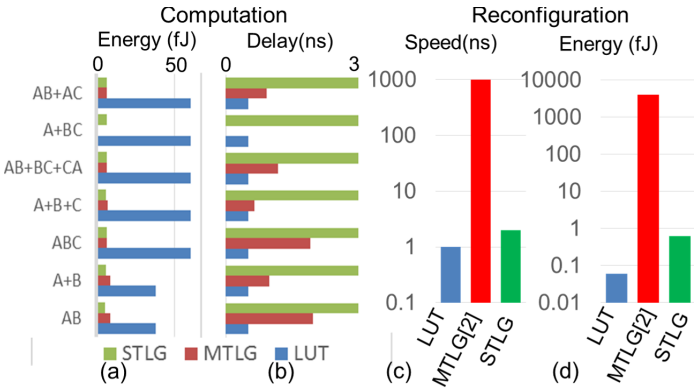

Figure 7. Comparison of (a) computation energy, (b) delay; comparison of TLG reconfiguration (c) speed and (d) energy

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