Ambipolar Independent Double Gate FET Logic

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ABSTRACT

In this work, we present a review of recent logic circuit design research using ambipolar independent double gate field effect transistors (Am-ICDGFETs). In a first approach, we examine compact logic and show that, with respect to conventional CMOS-like static logic structures and for comparable power consumption, time delay and integration density can be reduced by 25% and 45% respectively. We then turn to reconfigurability, and demonstrate a key use of ambipolarity in a 16-function dynamically reconfigurable logic cell based on a sum-of-products Boolean function implementation, which achieves remarkable gains in terms of power consumption (9x) and in terms of intrinsic time delay (5x) with respect to conventional 16nm LP CMOS-based look-up table circuits. Finally, we tackle the question of logic synthesis for design paradigms using such fine-grain reconfigurable cells, and show how binary decision diagrams can be adapted to this purpose to generate, in a flexible way, multiple input selective function sets. Using this technique, a generated circuit was also evaluated and shown to compare very favorably to its CMOS equivalent.

Categories and Subject Descriptors

B.7.1 [**Hardware**]: Integrated Circuits – *Types and Design Styles.*

General Terms

Performance, Design

Keywords

Ambipolarity, Carbon Nanotubes, Standard Cells, Reconfigurable Logic, Logic Synthesis, Binary Decision Diagrams

1. INTRODUCTION

In the context of nanoscale CMOS computing architectures, the quadruple mastery of power, performance, cost and reliability appears almost as impossible as squaring the circle. However, the emergence of four-terminal devices, with complementary intrinsic properties, responds to device-level expectations with favorable benchmark figures against Si-CMOS transistors, and shows the potential to provide novel logic blocks for digital architectures.

Initial work opened the way to fine-grain reconfigurability by exploiting the additional terminal. A cell using 6 DG-MOS transistors (FinFETs) and capable of achieving 8 functions was designed in [1], ensuring reconfigurability by modulating the transistor threshold voltages via the back gates. For DG-CNTFETs, the ambipolarity behaviour has been explored intensively in the construction of logic cells with various logic styles. In [2] a 2-input dynamically reconfigurable logic cell CNT_DRC_7T cell was developed, which is able to achieve 14 elementary logic functions, with 3 control signals. More recently in [3], Ben Jamaa et al. presented the benefits of designing field-programmable gate arrays (FPGAs) using reconfigurable DG-CNTFET logic gates instead of look-up tables (LUTs).

Area- and power-efficient reconfigurable cells based on emerging devices have also been proposed [4][5] with incomplete operator sets (i.e. where the number of achievable functions is less than 2^c, where c represents the number of possible combinations of data inputs, itself related to the number of inputs n by $c=2^n$).

In this work, we review recent work examining how ambipolarity in independently controlled double gate FETs can improve over conventional logic techniques, both for standard logic cells and, particularly importantly for cost and reliability issues, reconfigurable cells. The paper begins by describing, in section 2, device principles, a candidate CNT-based technology, and characteristic parameters for modeling and comparative simulations with a 16nm low-power CMOS technology. Then, in section 3, we introduce an approach to build compact logic cells and benchmark the circuits in terms of circuit-based and technology-based gain. In section 4, we present and benchmark a full functionality fine-grain 2-input reconfigurable cell, while in section 5 we discuss novel logic synthesis techniques capable of handling new design paradigms generated by the ambipolar logic approach.

2. DEVICE CHARACTERISTICS

In an ambipolar independently controlled double gate field effect transistor (Am-ICDGFET), the front gate G turns the device on or off, in the same way as the regular gate of a MOSFET; while the polarity-gate PG controls the device polarity setting to n- or p-type with a positive (V_{BG}-V_S=+V) or negative (V_{BG}-V_S=-V) voltage, respectively. Careful technology engineering (e.g. gate materials, layer thicknesses) is required to ensure that both gates of the Am-ICDGFET will achieve the desired functionality over the correct range of voltages. The symbol that will be used throughout this paper for this in-field programmable FET is shown in Figure 1.

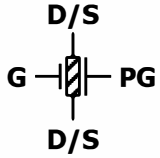

Figure 1 Am-ICDGFET symbol

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2.1 CNT-based Am-ICDGFET technology

One way of achieving such a device is through using carbon nanotubes (CNT) as transistor channels. Despite concerns related to manufacturing yield (variations in CNT diameter / chirality, misaligned / misplaced CNTs, contact resistance), various types of CNTFET devices have been produced experimentally, with realistic and CMOS-compatible process flow steps. In this work, we assume the fabrication of a DG-CNTFET based on aligned semiconducting CNTs [6], applying the self-alignment technique [7] and using one top gate and one back-gate [8], as well as potential hybrid integration with CMOS technology and consequently with metal interconnections defined by CMOS-compatible lithography steps.

Figure 2shows the structure of the CNTFET with double gates, where the back gate BG controls source and drain carrier access and is shielded from the inner channel by the front gate FG.

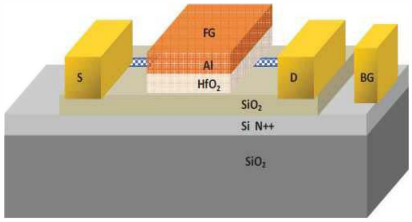


Figure 2 DG-CNTFET device. Cross-section [8]

2.2 Device compact model

Several compact models [9][10] have been developed to describe CNTFET technologies such as Schottky barrier (SB) CNTFETs or MOS-like CNTFETs with a top gate or surrounding gates. In this work, we used a physically accurate compact model of a DG-CNTFET with efficient convergence and simulation speed compatible with circuit design. The compact model is detailed in [11], where it was shown to include the most significant mechanisms such as the sub-band at the metal–nanotube interface, charge and electrostatic modeling, band-to-band tunneling effect, and quasi-ballistic transport. The model holds for various nanotube configurations (chirality / number / diameter) and for a range of values of polarity-gate and supply voltages. Furthermore, the comparison of the model with measurements from two technologies published in the literature – a DG-CNTFET from IBM (used as an Am-ICDGFET) [12] and a DG-CNTFET from Stanford University (used as a MOS-like CNTFET) [13] – showed the accuracy of the compact model in different technology configurations since the values of the extracted parameters are close to those in the considered technologies. We point out that the parameters of the model presented in [11] have been tuned to fit with the device structure suggested for this work in figure 2. More details are shown below (2.3 device parameters).

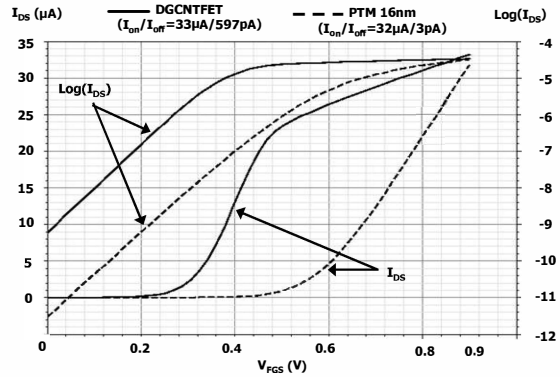
2.3 Device parameters

In much of the following work, we aim to demonstrate not only the performance gain of novel circuit structures exploiting ambipolarity with respect to conventional structures in CMOS technology (which is a combination of gains due to both technology and circuit structure), but also the intrinsic advantage of these structures, through comparison to conventional circuit structures using identical device models.

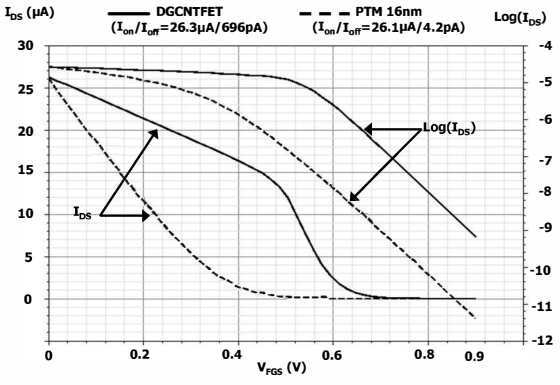
For silicon CMOS technology (for which we use the acronym SiSL), we use a 16nm low power (LP) Predictive Technology Model (PTM) [14]. Since we aim to obtain quantitative comparisons, it is further necessary to calibrate the CMOS transistor width to match the on-current performance of the DG-CNTFET, for both types of transistor (p-type and n-type). Table 1 shows the parameters used for the DG CNTFET compact model as presented in [11] and the tuned length/width of the predictive model. Figure 3(a) (resp. Figure 3(b)) shows the I_D/V_{GS} characteristic of the DG-CNTFET model and the 16nm LP PTM model for n-type (resp. p-type) configuration, where V_{GS} varies between 0V and +0.9V, while V_D=0.9V (resp. V_S=0.9V) and V_S=0V (resp. V_D=0V). It is worth noticing that for equal I_{on}, the DG-CNTFET leakage current is over two orders of magnitude higher than that of the 16nm LP PTM transistor, mainly due to the lower threshold voltage (V_{th}) by about 0.2V.

Table 1. DG-CNTFET and CMOS transistor parameters

Parameters	DG-CNTFET	16nm LP PTM
Drain access channel length	50nm	0nm
Source access channel length	50nm	0nm
Inner channel	20nm	16nm
Width	50nm	56nm (n-type) 90nm (p-type)
Number of nanotubes	12	-
Diameter of 1 nanotube	0.86nm	-
Supply voltage	0.9V	0.9V
Chirality (n,m)	(11,0)	-



(a)



(b)

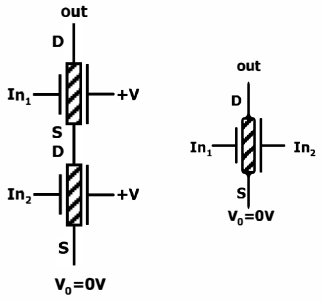
Figure 3 I_{DS}/V_{GS} characteristics. n-branch (V_{BG}-V_S = +V = +0. 9V) (a) ; p-branch (V_{BG}-V_S = -V = -0. 9V) (b)

3. COMPACT AMBIPOLAR LOGIC

Using the in-field controllability of Am-ICDGFETs, it is possible to develop highly compact (low transistor count) logic circuits. In this section, we describe the fundamental building block, demonstrate the approach for a complementary static logic XOR gate using DG-CNTFET technology and estimate circuit-based and technology-based performance gains with respect to conventional logic structures built in a 16nm silicon CMOS technology.

3.1 TTS structure

By connecting data inputs to each independent gate in an Am-ICDGFET, conventional TTS (two transistors in series) structures can be substituted by single transistors with no loss of functionality and lead to more compact logic gates. Further, since equivalent logic path resistance is proportional to the number of transistors in series (and inversely proportional to the average transistor width), this would also enable the reduction of RC time constants and consequently time delay. In fact, two transistors in series (TTS structure) either demonstrate a path resistance of $2R_{ch}$ (with no transistor resizing) or an input gate capacitance of $2C_g$ (with transistor width doubling to reduce overall path resistance), where R_{ch} and C_g represent the channel resistance and gate capacitance of a single minimum width transistor, respectively.



(a) (b)

Figure 4 TTS structure using two n-biased Am-ICDGFETs (a) Equivalent TTS structure using single Am-ICDGFET (b)

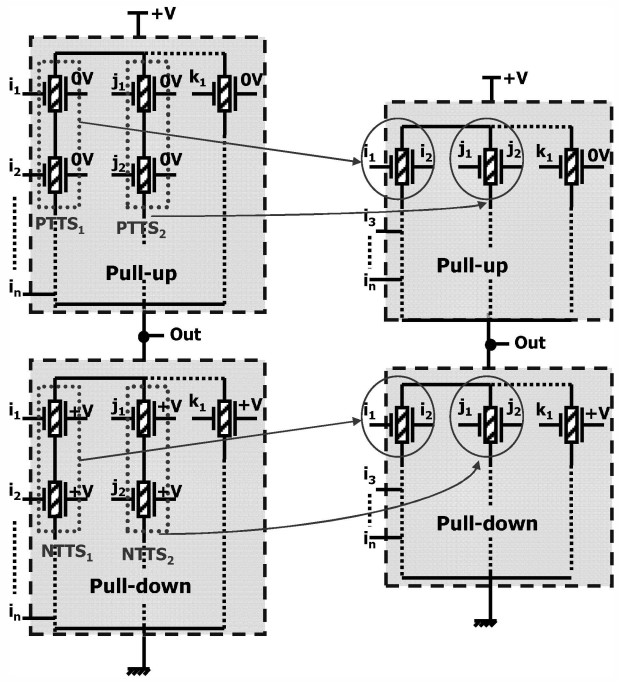
Figure 4(a) illustrates a conventional TTS structure, where both transistors are n-type since the back (polarity) gate BG is set to +V and V_0 is set to 0V (i.e. V_{BG}-V_S=+V). In this case, a path is established between V_0 and "out" only for In_1In_2="11". In the single Am-ICDGFET structure, shown in Figure 4(b), the same condition is true since for In_2="1", the back gate BG is set to +V such that the transistor is n-type and will be ON only if In_1="1" also. For other combinations In_1In_2= {"01","10","00"} the transistor will be OFF. Thus, this NTTS (n-type TTS) structure can be replaced by a single Am-ICDGFET. The same reasoning holds for PTTS (p-type TTS) with V_0 at +V and back gates BG at 0V (i.e. V_{BG}-V_S=-V) in the initial structure.

Hence, in a complementary static logic approach based on pull-up networks using p-type transistors and pull-down networks using n-type transistors, this approach can be applied in the case of many complex logic gates as shown in the next section.

3.2 Double-Gate Static Logic (DGSL)

In our approach, we replace any NTTS and PTTS structure in static logic pull-down and pull-up networks respectively with equivalent Am-ICDGFETs. A generic example illustrating the transformation between a Conventional CMOS Static-Logic (CSL) structure and the Double-Gate Static Logic (DGSL) structure using the TTS approach is shown in Figure 5, where for demonstration purposes the circuit contains both NTTS and PTTS structures. It should be noted that in the majority of standard cell circuits, a TTS structure in one network usually implies a parallel transistor structure in the other.

If we consider *n* to be the number of inputs of the function, *m* the number of NTTS structures and *p* the number of PTTS structures that can replace two AND-related inputs in the function path, the required number of transistors will be *2n-(m+p)*.



(a) (b)

Figure 5 CSL structure (a), DGSL structure (b)

3.3 2-Input XOR gate

The approach can be applied to any complementary static logic gate containing TTS structures. In simple monotonic gates, such as the NAND (resp. NOR) gate, where the pull-down (resp. pull-up) network contains one NTTS (resp. PTTS) and the pull-up (resp. pull-down) network is formed from 2 transistors in parallel, the pull-down (resp. pull-up) network can be substituted with a single Am-ICDGFET and the transistor count is lowered by one. However, in the case of more complex gates such as XOR/XNOR gates and multiplexers, the gain can be more significant and the approach can be applied to all branches of the gate.

The conventional CMOS-type 2 input XOR structure (CSL) is shown in Figure 6(a). By applying the approach to this gate, Figure 6(b) shows a compact XOR gate where all TTS structures were substituted with a single Am-ICDGFET, leading to a reduced transistor count with a simpler structure of 4 transistors instead of 8 (not counting the data input inverters required for A and B).

Figure 6(c) shows simulation results, where we suppose the following conditions: (i) data frequency of 4Gbps; (ii) equal rise and fall times (20ps) at both front and back gate inputs; (iii) capacitive load of 150aF; (iv) supply voltage of 0.9V; (v) single-rail clock and data inputs (i.e. +V=0.9V, V0=0V). Cyclic simulations using Spectre™ were carried out to establish mean

power consumption and worst-case time delay over all data combinations. The parameters shown in Table 1 were used for all transistors in the logic gates. No resizing was carried out to balance branch resistances since this technique can be applied to all gates by using parallel transistors and has no impact from a comparative point of view.

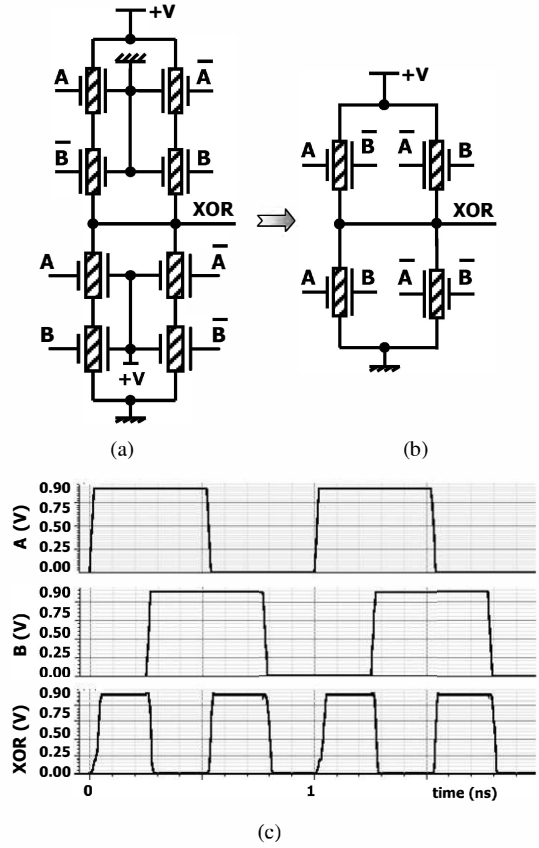


Figure 6 2-input XOR gate: CSL structure (a) DGSL structure (b) DGSL simulated waveform (c)

3.4 Performance evaluation and discussion

As mentioned in section 2.3, a comparative study was carried out to establish the performance gain achieved by the novel circuit structure, as distinguishable from the performance gain achieved by the technology alone. Hence three types of simulation were carried out in this investigation program: conventional static logic structures built with silicon CMOS technology (SiSL), conventional static logic structures built with DG-CNTFET technology (CSL), and the novel double-gate static logic circuits designed in this work and built with DG-CNTFET technology (DGSL). Hence, technology-based performance gain can be quantified as the difference between CSL – SiSL, while circuit-based performance gain can be quantified as the difference between DGSL – CSL. The overall performance gain is DGSL – SiSL.

To clearly highlight the benefits of the approach, we simulated logic gates where the occurrence of TTS structure is high. Four different monotonic gates were simulated (XOR, XNOR, 2:1MUX, 4:1MUX) and results are shown in Figure 7. In fact, the impact of our approach on these different logic gates is almost identical. Various performance metrics were evaluated: power consumption "P", time delay "TD", Power-Delay-Product "PDP", transistor count for each cell "# TRAN", and active area "AREA" (i.e. sum of all channel areas W*L).

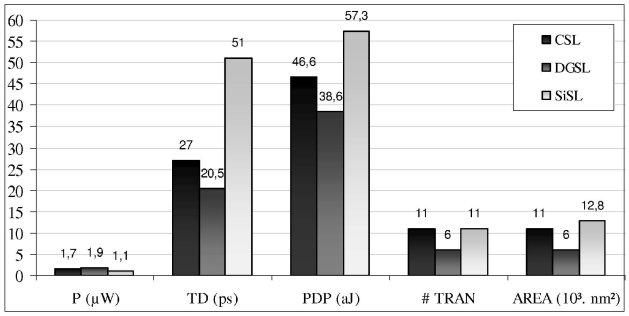


Figure 7 Comparison of average values of static logic gates

The technology-alone (CSL – SiSL) comparison shows that power is increased with the DG-CNTFET technology by over 50%, mainly due to the high leakage current as mentioned in section 2.3. Also, although fewer transistors are used, the average power consumption in the DGSL approach increases slightly (10%) compared to the CSL approach. This increase in power consumption is due to the shorter path from V_{dd} to ground that the new structures create. Since there are fewer transistors in series, the resistance per branch from (V_{dd}/Gnd) to output decreases to the channel resistance of a single transistor (R_{ch}) and results in a consequently higher short-circuit current during signal transition time. In the conventional structure, two transistors in series offer a path resistance of $2R_{ch}$. However, this also has a positive impact on worst-case time delay, which is improved by 25% due to the reduced time constant associated with path resistance and load capacitance. The technology-based gain is 47%. The overall PDP of gates built with DG-CNTFET technology is also improved with respect to silicon technology. The technology-based gain is 19%, while the circuit-based gain is 17%.

A further benefit provided by the approach is the strong transistor count reduction of around 45%. While conventional static logic generally requires *2n* transistors (where *n* represents the fan-in) as mentioned in section 3.2, DGSL cells only require *2n-(m+p)* transistors (where *m* represents the number of NTTS structures and *p* represents the number of PTTS structures in the conventional gates).

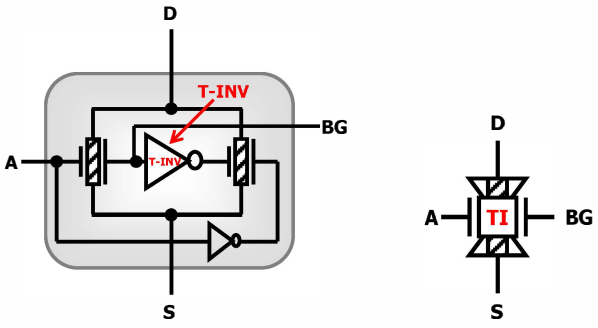
4. RECONFIGURABLE LOGIC GATES

The existence of a polarity gate, as a vector to reconfigure the transistor type to n- or p-type, opens up many possibilities for reconfigurable logic. In this section, we describe a 2-input reconfigurable dynamic logic cell designed using Am-ICDGFET devices able to achieve the whole set of 16 functions. In addition, we describe a necessary Am-ICDGFET transmission gate structure to eliminate logic level degradation within the structure, and then compare the performance levels to conventional CMOS look-up table logic.

4.1 Building blocks

The reconfigurable cell, based on dynamic logic, essentially requires a network of transmission gates to propagate logic levels with no degradation and for a wide range of data and control voltage combinations. To obtain full swing in all configurations, we use a transmission gate formed by two CNTFETs in parallel controlled by complementary signals, both for data on the front gate and for control on the back (polarity) gate. While the data is a

binary signal (such that complementarity requires a simple inverter), the control is a ternary signal and requires a ternary inverter (T-INV). The structure of the transmission gate, capable of switching between all three states (n-type, p-type and OFF) is shown in Figure 8(a) and is abbreviated as "TI" in the associated symbol shown in Figure 8(b).



(a) (b)

Figure 8 Am-ICDGFET transmission gate: structure (a), symbol (b)

T-INV controls the back-gate of the parallel Am-ICDGFET and operates according to {+V→0V, +V/2→+V/2, 0V→+V}. The structure of the T-INV is shown in Figure 9; it is composed of two transistors and two resistors of 100kΩ each. This value is the result of tradeoff within a range of values giving acceptable ternary noise margins; with increasing resistance comes higher delay and area, and lower power consumption and dependency on Am-ICDGFET channel resistance.

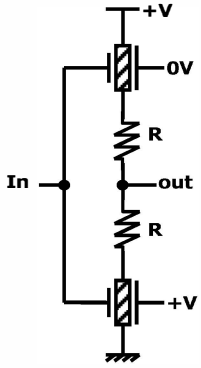


Figure 9 T-INV structure

4.2 2-input 16-function logic gate

Every Boolean function can be written in canonical form as a sum of products (SOP), where each product is a "minterm". For a two-variable function f(A,B), the possible minterms are: A∧(¬B), (¬A)∧B, (¬A)∧(¬B), A∧B. Full functionality for a two-variable function implies the availability of 16 (2^c, where $c=2^n$ and n is the number of inputs) operations. This can be achieved by combining minterms and cascading with a configurable inverter/follower output stage, as shown in the proposed cell (SOP-DRLC) using 4 transistors and 5 ambipolar transmission gates (Figure 10). Transmission gates TI_1 and TI_2 of the function path are placed in series to form a first minterm (wired AND), while TI_3 and TI_4 form a second minterm. Both structures are connected in parallel (wired OR) to enable the potential use of the sum of both minterms.

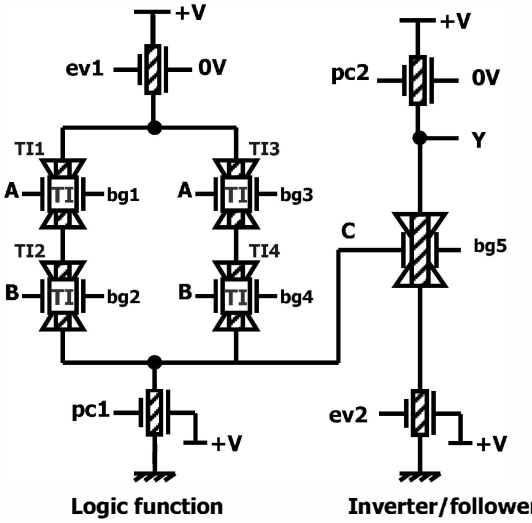


Figure 10 SOP based dynamically reconfigurable dynamic logic cell SOP-DRLC

The implementation of this cell requires single polarity inputs (i.e. 0V for logic "0" and +V for logic "1"), to avoid additional inverters and dual rail interconnects. In the case of complemented inputs, Am-ICDGFETs can be configured to p-type using the corresponding PG voltage (-V). In this cell, there are ten inputs and one output:

- two boolean data inputs A and B (where the logic levels are represented by the supply voltage values 0V and +V).
- five control inputs $bg_{\{1\text{-}5\}}$ to configure the circuit
- a four-phase clock signal set consisting of 2 precharge inputs pc1, pc2 and 2 evaluation inputs ev1, ev2. The signals are non-overlapping as in classical CMOS dynamic logic gates
- circuit output "Y"

These circuit signals are illustrated in Figure 11, showing a cyclic simulation of the SOP-DRLC circuit in the NAND configuration.

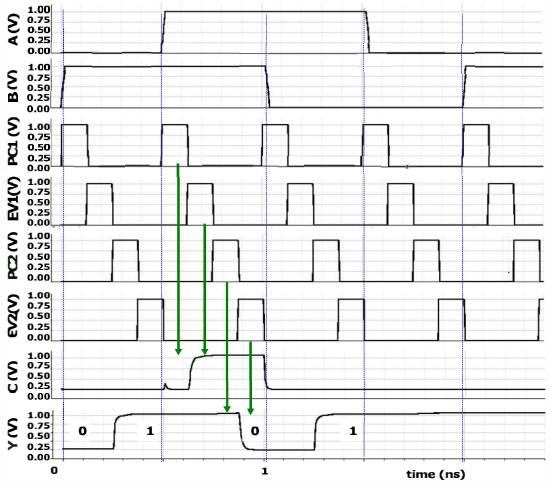


Figure 11 Simulation results for SOP-DRLC in NAND configuration

The available basic binary operations and the associated configuration PG voltage combinations are shown in Table 2.

Table 2. SOP-DRLC configuration table

bg1=bg2	bg3	bg4	bg5	Y
V/2	0V	0V	0V	¬(A∨B)
V/2	0V	0V	+V	(A∨B)
V/2	+V	0V	+V	(¬A)∨B
V/2	0V	+V	+V	A∨(¬B)
V/2	0V	+V	0V	(¬A)∧B
V/2	+V	0V	0V	A∧(¬B)
V/2	+V	+V	0V	A∧B
V/2	+V	+V	+V	¬(A∧B)
+V	0V	+V	+V	¬B
+V	0V	+V	0V	B
+V	+V	0V	0V	A
+V	+V	0V	+V	¬A
0V	+V	+V	0V	¬(A⊕B)
0V	+V	+V	+V	A⊕B
V/2	V/2	V/2	0V	⊥
V/2	V/2	V/2	+V	T

4.3 Performance evaluation and discussion

A comparative study was carried out between the SOP_DRLC cell shown in Figure 10 and a CMOS 2-LUT structure such as that typically used in FPGAs, based on transmission-gate multiplexers and implemented in 16nm LP PTM CMOS technology.

Cyclic simulations using Spectre™ were carried out to establish mean power consumption and worst-case time delay over all data combinations and function configurations. Figure 12 shows the overall simulation results for power consumption "P", time delay "TD", power-delay product "PDP", and transistor count for each cell "# TRAN". We suppose the following conditions: (i) data frequency of 2Gbps; (ii) equal rise and fall times (20ps) at both front and back gate inputs; (iii) capacitive load of 75aF; (iv) supply voltage of 0.9V; (v) single-rail clock and data inputs (i.e. +V=0.9V, V_0=0V). The parameters shown in Table 1 were used for all transistors in the logic gates.

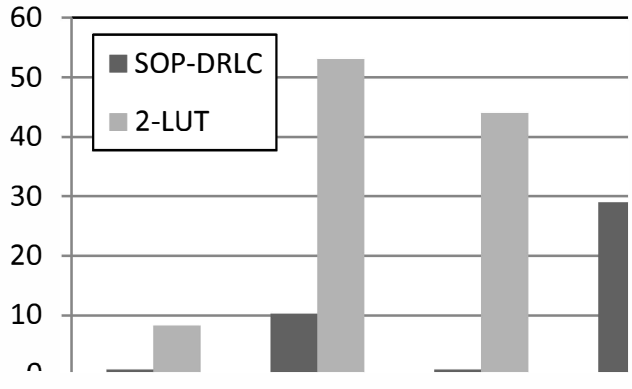


Figure 12 Comparison between DG-CNTFET based SOP-DRLC and 16nm LP CMOS-based 2-input LUT

Compared to conventional CMOS-based 2-input LUTs, we observe that DG-CNTFET based SOP-DLRC achieve a remarkable gain (9x) in term of power consumption. Concerning time delay, although dynamic logic is characterized by clock-limited latency, it is clear that the intrinsic gain is around 5x, such that overall PDP reduction is around 45x.

5. DESIGN TOOLS

For Am-ICDGFETs, no systematic design methodology exists to generate reconfigurable cells from function definition. Such a methodology can be used to facilitate and optimize logic cell generation, for any number of inputs and also for any particular subset of functions. This can lead to interesting optimization strategies based on the identification of most-used operations in classes of applications. In this section, we describe a method through its constituent steps and rules that should be applied, from definition of the output function to circuit implementation at the transistor level.

5.1 Am-BDD synthesis technique

We show here that the BDD (binary decision diagram) logic synthesis technique can be adapted to the Am-ICDGFET device. The main impact is that unlike conventional BDDs, one node can have more than two edges depending on the functions that can be reached at the output; a single edge can have different values; and multiple functions can be mapped onto the same BDD sharing the same output. The steps of the proposed method are the following:

Step 1
Define the set of functions to be realized at the output of the reconfigurable cell
Step 2
Map BDDs of all functions to the same BDD (to identify shared nodes and edges) /* This common BDD will be abbreviated Am-BDD (for Ambipolar-BDD). One important point here is the necessity to use the same variable ordering when mapping the BDD of each function. */
Step 3
Label every edge connecting two different nodes in Am-BDD
Step 4
Define rules to be respected before implementing the Am-BDD into a pass-transistor network. The edges mapped in the graph will be represented as transistors at the circuit level according to the following rules:

1. *If an edge is used by all functions in the Am-BDD then*
   a. *If the edge value is the same for all functions, the transistor representing this edge does not need to be reconfigurable at the circuit level.*
   b. *If there is a difference between the edge values, the transistor representing this edge is reconfigurable at the circuit level and will be in either n- or p-state.*
2. *If an edge is not used by all functions in the Am-BDD, then the transistor representing this edge is reconfigurable at the circuit level and must include the off-state.*

Step 5
Implement pass-transistor circuit. /* A '0' edge means that the corresponding transistor is configured as P-type (PG=0V), while a '1' edge means that the corresponding transistor is configured as N-type (PG=+V). If an edge is not used by a function, its corresponding transistor will be switched off (PG=V/2). */

5.2 Full-function set 2-input reconfigurable cell (16F-AmBDD)

In this section, we aim to generate the same reconfigurable function as that described in section 4. The general structure of the Am-BDD for the 16 different functions is shown in Figure 13, where for the sake of clarity, we have only represented the various

nodes and edges; the corresponding values of the configuration signals for each edge are shown in Table 3.

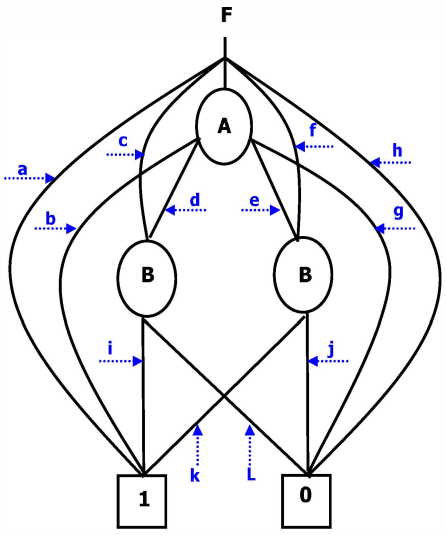


Figure 13 Am-BDD of 2-input 16-function reconfigurable cell

Table 3. Am-BDD 2-input 16-function configuration table

a	b	c	d	e	f	g	h	i	j	k	l	F
V/2	V/2	V/2	0V	V/2	V/2	+V	V/2	0V	V/2	V/2	+V	¬(A∨B)
V/2	+V	V/2	V/2	0V	V/2	V/2	V/2	V/2	0V	+V	V/2	(A∨B)
V/2	0V	V/2	V/2	+V	V/2	V/2	V/2	V/2	0V	+V	V/2	(¬A)∨B
V/2	V/2	V/2	+V	V/2	V/2	0V	V/2	0V	V/2	V/2	+V	A∧(¬B)
V/2	+V	V/2	0V	V/2	V/2	V/2	V/2	0V	V/2	V/2	+V	A∨(¬B)
V/2	V/2	V/2	V/2	0V	V/2	+V	V/2	V/2	0V	+V	V/2	(¬A)∧B
0V	V/2	V/2	V/2	V/2	V/2	V/2	V/2	V/2	V/2	V/2	V/2	T
V/2	V/2	V/2	V/2	V/2	V/2	V/2	+V	V/2	V/2	V/2	V/2	⊥
V/2	V/2	V/2	V/2	+V	V/2	0V	V/2	V/2	0V	+V	V/2	A∧B
V/2	0V	V/2	+V	V/2	V/2	V/2	V/2	0V	V/2	V/2	+V	¬(A∧B)
V/2	+V	V/2	V/2	V/2	V/2	0V	V/2	V/2	V/2	V/2	V/2	A
V/2	0V	V/2	V/2	V/2	V/2	+V	V/2	V/2	V/2	V/2	V/2	¬A
V/2	V/2	+V	V/2	V/2	V/2	V/2	V/2	0V	V/2	V/2	+V	¬B
V/2	V/2	V/2	V/2	V/2	+V	V/2	V/2	V/2	0V	+V	V/2	B
V/2	V/2	V/2	0V	+V	V/2	V/2	V/2	0V	0V	+V	+V	¬(A⊕B)
V/2	V/2	V/2	+V	0V	V/2	V/2	V/2	0V	0V	+V	+V	A⊕B

In the Am-BDD we chose a variable ordering (A, B). In view of the fact that the technique requires the same variable ordering for all functions when mapping the Am-BDD, functions which do not include the variable A in their expression (i.e. 1, ¬B, B, 0) require a direct path to the output without using node A (edges a, c, f, h).

This example shows that the method can be adapted to some issues such as variable ordering (incurring however a penalty of more edges). Furthermore, it shows that the technique is sufficiently flexible to be applied to any number of output functions. Figure 14 represents the final circuit implementation of the 2-input Reconfigurable Static Logic 12-Transistor cell (RSL-12T). This maps quite naturally to a layout of reduced-complexity using DG-CNTFETs with aligned CNTs.

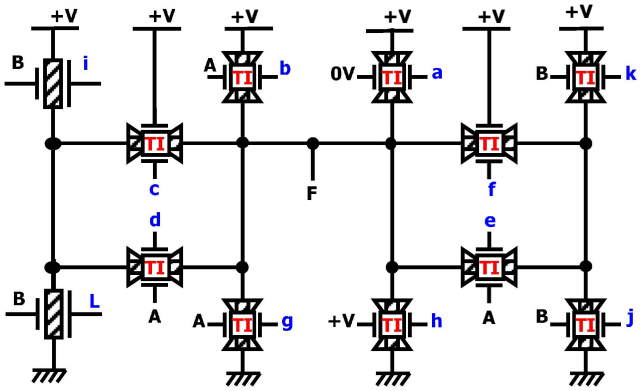


Figure 14 Reconfigurable Static Logic 12-Transistor cell (RSL-12T)

5.3 Performance evaluation and discussion

Various performance metrics such as power consumption, transistor count and worst-case delay of the proposed Reconfigurable Static Logic 12-Transistor cell (RSL-12T) were evaluated to highlight its characteristics, and to compare them to those of a CMOS-2LUT based on silicon technology using a 16nm predictive model.

Similarly as to in previous sections, we ran simulations with a frequency of 1GHz with equal rise and fall times (20ps) and capacitive load of 150aF, and with no difference in rise and fall times between front and back gate inputs. The supply voltage was 0.9V and data inputs were single rail (i.e. +V=0.9V, V0=0V). Cyclic simulations were carried out to establish mean power consumption and worst-case time delay over all data combinations.

Figure 15 shows the results of simulations in terms of average power "P", average time delay "av.td" and worst-case time delay "worst.td" for each cell. Figure 16 is a qualitative comparison between these two cells in terms of transistor count, number of achievable functions and number of configuration signals. Table III shows the values for every function.

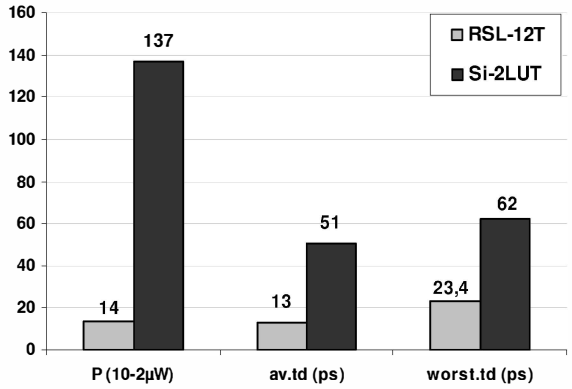


Figure 15 Average power consumption and delay comparison

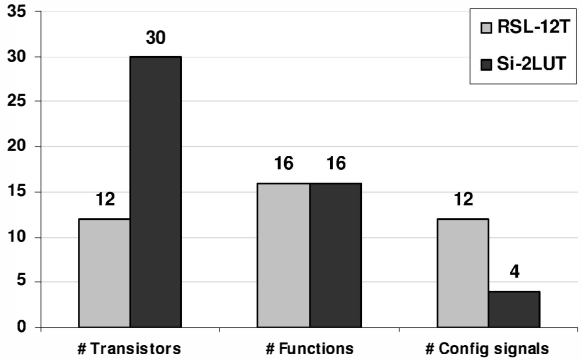


Figure 16 Resource and functionality comparison

The ambipolar property of DG-CNTFETs, coupled with the Am-BDD synthesis technique, enabled a high-speed and energy-efficient 16-function reconfigurable logic cell RSL-12T to be developed. It demonstrates a significant decrease (9x) in terms of power consumption when compared to 2-LUT based on silicon technology using a 16nm predictive model and built with a transmission gate logic style. Concerning the time delays, an improvement of 3x is achieved for both metrics; the average time delay as well as the worst case time delay.

Of course, the main disadvantage of this approach is the high number of configuration signals, especially when no correlation can be identified between them. This number of control signals grows exponentially with the number of inputs when we aim to build a structure implementing all functions. On one hand, the high number of control signals increases the risk of instability and the inability to realize some functions in the case of the presence of defects on one control signal. On the other hand, the very fact that no correlation exists between signals can also offer a certain advantage since all signals are independent from faulty lines, such that several functions are still obtainable in the presence of faults. In any event, the Am-BDD approach is still valid as an abstract canonical means of building larger reconfigurable Am-ICDGFET structures.

6. CONCLUSION

Recent logic circuit design research using Am-ICDGFETs has broadened from initial work on reconfigurable logic to compact logic and logic synthesis. In this paper, we examined compact logic and showed that by replacing TTS structures by single Am-ICDGFETs, both time delay and integration density can be reduced by 25% and 45%. We then go through the design of a 16-function dynamically reconfigurable logic cell based on a sum-of-products Boolean function implementation, and quantify gains in terms of power consumption (9x) and in terms of intrinsic time delay (5x) with respect to a conventional 16nm LP CMOS-based look-up table circuit. Such an approach begs the question of design tools and logic synthesis, and we looked at how binary decision diagrams can be adapted to this purpose to generate, in a flexible way, multiple input selective function sets. As such, tools are now in place to envisage the exploration of low-power designs, complex architectures and hardware demonstrators.

7. ACKNOWLEDGMENTS

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