Transfer Characteristics and High Frequency Modeling of Logic Gates Using Carbon Nanotube Field Effect Transistors (CNT-FETs)

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ABSTRACT

In the present work, current model equations from an analytical model for carbon nanotube field effect transistors are utilized to calculate the transfer characteristics of different logic gates such as inverters, NAND gates, and NOR gates. A small signal model has been implemented and the necessary parameters have been calculated to describe the high frequency response for these logic gates. Results show that how different diameters and wrapping angles of carbon nanotubes, determined by the chiral vector (n,m), can change the transfer characteristics, small signal parameters, and high frequency response for devices based on carbon nanotubes.

Categories & Subject Descriptors

B.7.1 Types and Design Styles, Advanced technologies; VLSI (very large scale integration)

General Terms

Design

Keywords

Carbon nanotubes, transfer characteristics, cut-off frequency, small signal model, CNT-logic.

1. INTRODUCTION

Since carbon nanotubes were firstly discovered in 1991 [1], the research and study of these cylindrical materials has been outstanding [2,3]. Carbon nanotubes are 1D graphene sheets rolled into a tubular form [4,5] with electronic properties being predicted by their diameter and wrapping angle [6-8]. Many applications have been proposed over the past decade including nanometer-sized semiconductor devices [9-11]. The first carbon nanotube field effect transistor was fabricated in 1998 [4,12]. These first CNT-FETs showed a Schottky barrier phenomena, resembling Schottky diode characteristics at the electrode contacts [13-15], a fact that had been a real disadvantage since MOSFETs do not show these Schottky barriers [16,17]. However, latter CNT-FETs fabricated in 2004 [18,19] did not show any of this barrier characteristic, which was achieved by changing the electrode material at the source and drain ends. These successful accomplishments have brought carbon nanotube based technology closer to replacing current CMOS technology especially at the end of Moore's law in sight [20-22]. Models for carbon nanotube field effect transistors (CNT-FETs) have already been implemented, including the current transport models by Raychowdhury, John, and Guo [23-25] and the high frequency small signal models by Burke and Castro [26-30]. Logic gates using CNT-FETs have also been fabricated [31-33] and their transfer characteristics have been presented [32-35]. In the current work, our previously calculated models [36] for the current transport and small signal models for the high frequency response have been utilized to present the transfer characteristics of different logic gates and analyze their high frequency response.

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2. CNT-FET DEVICE

2.1 N-Type and P-Type

Although the computer simulations performed in this work were done using intrinsic carbon nanotubes, CNT-FETs work under the same conditions as CMOS [20] and therefore, can be classified as n-type and p-type transistors [19]. Figure 1 shows the basic cross sectional view of a CNT-FET.

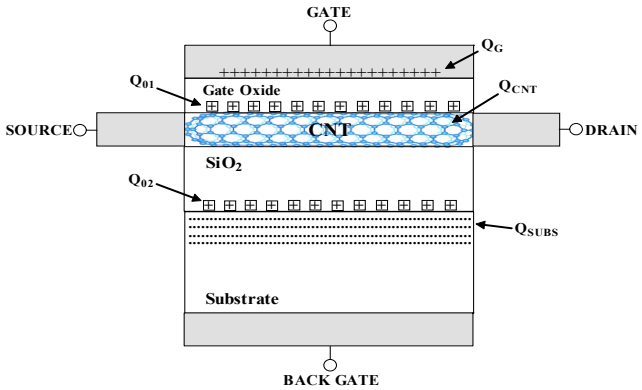

Figure 1. Intrinsic cross sectional view of a CNT-FET.

Even though the equations described in this section are for n-type transistors, the same equations can be applied for p-type transistors by changing the respective parameters.

The current model equation for CNT-FETs is described as:

$$I_{ds} = \beta\left[f\left(\psi_{cnt}(L), V_{gs}\right) - f\left(\psi_{cnt}(0), V_{gs}\right)\right] \quad (1)$$

where $f\left(\psi_{cnt}(x), V_{gs}\right) = \left(V_{gs} + V_{sb} - V_{fb} + \frac{KT}{q}\right)\psi_{cnt}(x) - \frac{1}{2}\psi_{cnt}^2(x)$ and $\beta = \frac{\mu C_{ox}}{L^2}$.

L is the gate length, μ is the mobility, K is Boltzmann's constant, T is temperature, V_{fb} is the flat band voltage given by

$$V_{fb} = \phi_{ms} - \frac{Q'_{01}}{C'_{ox1}} - \left(Q'_{02} + Q'_{subs}\right)\left(\frac{1}{C'_{ox1}} + \frac{1}{C'_{ox2}}\right), \quad (2)$$

where φ_{ms} is the sum of the contact potential between the gate and the substrate, and C_{ox} is the gate oxide capacitance given by [37,38]

$$C_{ox} = \frac{2\pi\varepsilon_{ox} L}{\ln\left(\frac{T_{ox} + r + \sqrt{T_{ox}^2 + 2T_{ox} r}}{r}\right)}, \quad (3)$$

where T_{ox} is the thickness oxide, r is the carbon nanotube radius and e_{ox} is the permittivity constant.

Equation (1) can be used given that the transistor has turned on, i.e. the carbon nanotube has become significantly conductive, this condition is defined numerically as the threshold voltage as,

$$V_{gb} \geq V_{sb} + V_{fb} + \frac{E_c}{q} - \frac{KT}{q} - \frac{(I)e^{-1}}{Slope}, \quad (4)$$

where ***I*** is an integral specific of each carbon nanotube defined by

$$I = \frac{1}{\sqrt{KT}}\left[\sqrt{\frac{E_c}{2}} + \int_0^{\frac{\eta E_c}{KT}} \frac{KTx + E_c}{\sqrt{x\left(KTx + 2E_c\right)}} e^{-x} dx\right], \quad (5)$$

where E_c is the energy conduction band minimum, this integral is computed using numerical integration.

Once the voltage in Eq. (4), known as the threshold voltage, has been applied at the gate, $\psi_{cnt}(0)$ is the channel potential at the source end, given by

$$\psi_{cnt}(0) = \frac{V_{gb} - \Delta I e^{-1} - V_{fb} + \Delta Slope\left(V_{sb} + \frac{E_c}{q} - \frac{KT}{q}\right)}{1 + \Delta Slope} \quad (6)$$

and $\psi_{cnt}(L)$ is the channel potential at the drain end, found using two regions of operation depending on the drain to source voltage, V_{ds}. These two regions are: a linear region, for $V_{ds} \leq V_{gs} - V_{fb} - \frac{E_c}{q} + \frac{KT}{q} + \frac{(I)e^{-1}}{Slope}$, and a saturation region, otherwise. The equations are defined as follows:

- Linear Region

$$\psi_{cnt}(L) = \frac{V_{gb} - \Delta I e^{-1} - V_{fb} + \Delta Slope\left(V_{ds} + V_{sb} + \frac{E_c}{q} - \frac{KT}{q}\right)}{1 + \Delta Slope} \quad (7)$$

- Saturation Region

$$\psi_{cnt}(L) = V_{gb} - V_{fb} \quad (8)$$

where $Slope = \frac{\sqrt{\frac{2E_c}{KT} + 1} - Ie^{-1}}{\frac{2KT}{q}}$.

3. TRANSFER CHARACTERISTICS

Using Eqs. (1) – (8), two different carbon nanotubes have been used to simulate the transfer characteristics of a NAND gate, a NOR gate (Figure 2) and an inverter using MATLAB software capabilities. Figures 3 and 4 show the transfer characteristics for these logic gates.

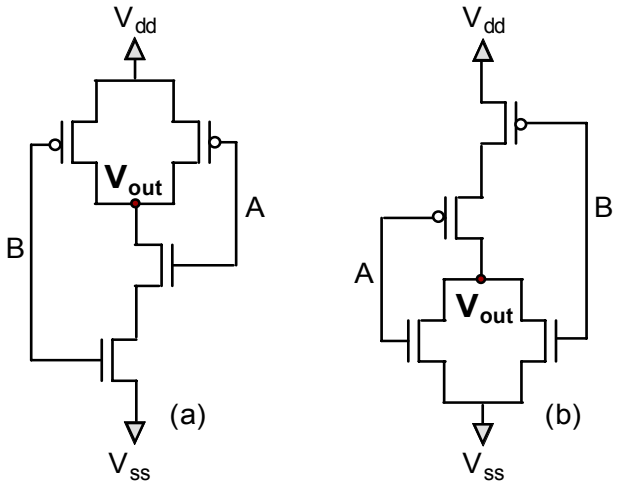

Figure 2. (a) NAND gate configuration and (b) NOR gate configuration.

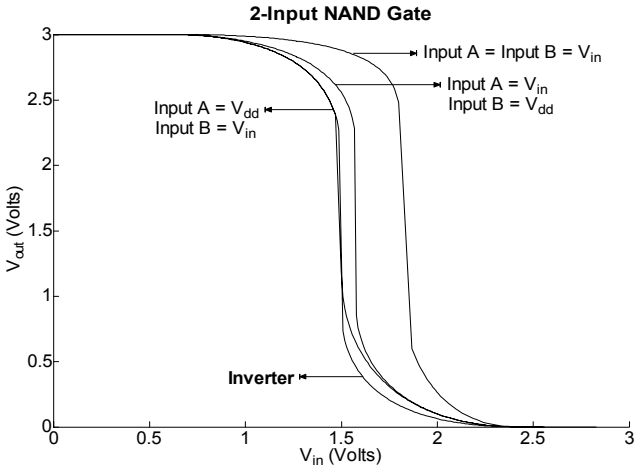

Figure 3. Transfer characteristics of a NAND gate using (5,3) CNTs.

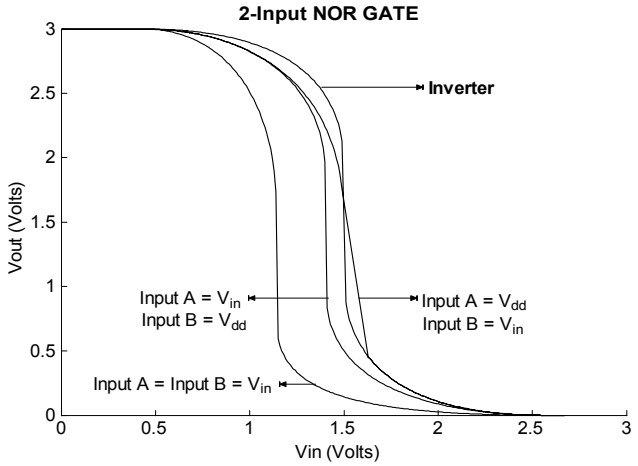

Figure 4. Transfer characteristics of a NOR gate using (7,3) CNTs.

4. SMALL SIGNAL MODEL

4.1 Resistance Model

The total resistance of a conductive carbon nanotube is given by [26,39] and can be split in two parts, the contact and the channel resistances are described as follows.

$$R = \frac{h}{4e^2}\frac{\lambda + L}{\lambda} = \frac{h}{4e^2} + \frac{h}{4e^2}\frac{L}{\lambda} = R_c + R_{ch}, \quad (9)$$

where h is Planck's constant, e is the charge of an electron, and λ is the mean free path for electrons inside the carbon nanotube [40].

The contact resistance can be further divided in two equal parts corresponding to the drain and source resistances as, $R_s = R_d = \frac{R_c}{2} = \frac{h}{8e^2}$, and the channel resistance, R_{ch}, corresponds to the drain to source resistance R_{ds}.

4.2 Capacitance Model

There are three type of capacitances in a CNT-FET [26,27], the parasitic capacitances ($C_{par,gs}$ and $C_{par,gd}$), the oxide capacitances (C_{ox1} and C_{ox2}), and the quantum capacitance (C_Q). The parasitic and oxide capacitances are both due to geometry and fabrication processes, and the quantum capacitance is due to the transport phenomena in the carbon nanotube.

The parasitic capacitance is given by [41,42]

$$C_{par} = C_{par,gs} = C_{par,gd} = \frac{\varepsilon_o \varepsilon_{ox} W}{\pi/2} \ln\left(1 + T_{poly}/T_{ox}\right), \quad (10)$$

where W is the width of the gate, T_{poly} is the thickness of the gate material.

The oxide capacitance can be found using Eq. (3) and the quantum capacitance is found as [27,43]

$$C_Q = \left(e^2 2L\right)/\left(h v_F\right), \quad (11)$$

where V_F is the Fermi velocity of electrons in nanotubes.

The gate to source capacitance (excluding the parasitic) is a serial combination of the oxide capacitance and quantum capacitance [27] as follows:

$$C_{gs} = \left(\left(4C_Q\right)^{-1} + \left(C_{ox1}\right)^{-1}\right)^{-1}, \quad (12)$$

Because of the particular band structure of carbon nanotubes, a carbon nanotube has four possible conductive channels [5,8]. These four channels are modeled by four quantum capacitances in a parallel combination, hence the number four next to the C_Q in Eq. (12). Figure 5 shows the small signal model of a CNT-FET [28-30].

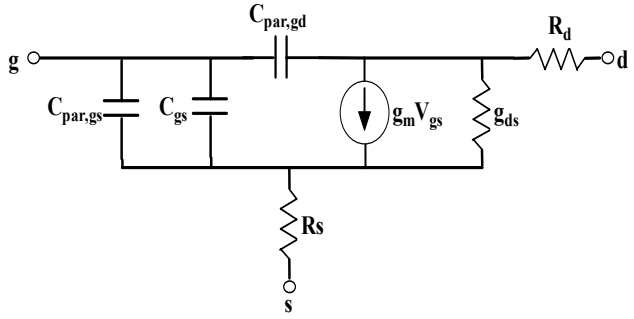

Figure 5. Small signal model of a CNT-FET.

Table 1 shows the values necessary for the small signal model of Figure 5. These parameters have been calculated using Eqs. (1) – (12), for $Q_{01}=0$, $Q_{02}=0$, $\varphi_{ms}=0$, $L=50\ \mu m$, $T_{ox1}=40\ nm$, and $T_{ox2}=400\ nm$.

Table 1. Small signal parameters for different CNTs.

(n,m)	g_m (μS)	R_{ds} (K)	C_{gs} (aF)
(3,1)	110.712	132.304	0.905
(3,2)	130.307	155.073	0.920
(4,2)	142.419	163.271	0.935
(4,3)	152.060	173.949	0.946
(5,1)	147.573	170.990	0.939
(5,3)	160.487	178.877	0.958
(6,1)	157.014	173.776	0.952
(7,3)	173.377	190.281	0.978
(9,2)	180.755	194.566	0.990
(11,3)	191.188	199.610	1.011

5. CUT OFF FREQUENCY

The cut-off frequency of a CNT-FET can be analytically examined from Figure 5 as [26,44]:

$$f_T = \frac{1}{2\pi}\frac{g_m}{\left[C_{gs}\left(1 + R_c g_{ds}\right) + C_{par}\left(2 + 2R_c g_{ds} + R_c g_m\right)\right]}. \quad (13)$$

In order to calculate the cut-off frequency for a CNT-FET, the transistor is taken to be in saturation, a value of V_{gs} is chosen and g_m, R_{ds}, and V_{ds} are calculated accordingly. Figure 6 shows the plot of the cut-off frequency using Eq. (13).

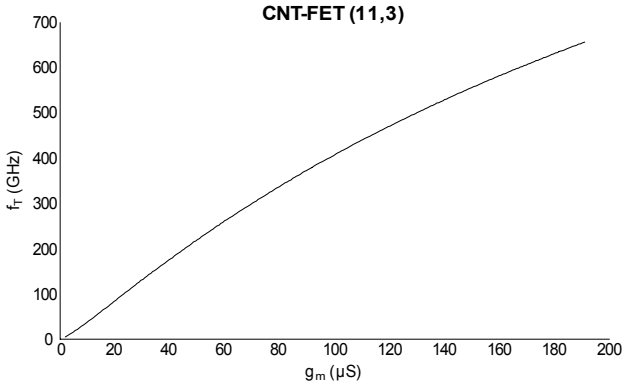

Figure 6. Plot of the Cut-off frequency, f_T vs the transconductance, g_m.

Table 2 shows the cut-off frequencies for different devices based on CNTs using SPICE with the parameters in Table 1.

Table 2. Cut-off frequencies for different CNTs.

(n,m)	CNT-FET f_T (GHz)	Inverter f_T (GHz)	NAND f_T (GHz)	NOR f_T (GHz)
(3,1)	538.760	476.502	347.023	347.478
(3,2)	614.519	536.402	388.764	389.448
(4,2)	656.305	570.369	413.611	412.297
(4,3)	688.743	595.940	431.052	430.781
(5,1)	673.804	583.014	422.241	423.290
(5,3)	716.472	614.519	444.613	446.164
(6,1)	704.012	606.487	440.046	440.332
(7,3)	755.188	644.892	465.759	466.166
(9,2)	778.732	662.087	477.939	478.596
(11,3)	806.539	682.728	492.975	493.517

6. CONCLUSION

Transfer characteristics of different logic gates and their high frequency response have been calculated using existing analytical models for the current transport in CNT-FETs. Cut-off frequencies were also presented showing values in the upper GHz range. The results presented in this work provide designers with a better understanding of carbon nanotubes and their potential in a wide range of applications on integrated circuits.

7. ACKNOWLEDGMENT

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