Design and Analysis of Compact Ultra Energy-Efficient Logic Gates Using Laterally-Actuated Double-Electrode NEMS

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ABSTRACT

Nano-Electro-Mechanical Switches (NEMS) are among the most promising emerging devices due to their near-zero subthreshold-leakage currents. This paper reports device fabrication and modeling, as well as novel logic gate design using "laterally-actuated double-electrode NEMS" structures. The new device structure has several advantages over existing NEMS architectures such as being immune to impact bouncing and release vibrations (unlike a vertically-actuated NEMS) and offer higher flexibility to implement compact logic gates (unlike a single-electrode NEMS). A comprehensive analytical framework is developed to model different properties of these devices by solving the Euler-Bernoulli's beam equation. The proposed model is validated using measurement data for the fabricated devices. It is shown that by ignoring the non-uniformity of the electrostatic force distribution, the existing models "underestimate" the actual value of $V_{pull\text{-}in}$ and $V_{pull\text{-}out}$. Furthermore, novel energy efficient NEMS-based circuit topologies are introduced to implement compact inverter, NAND, NOR and XOR gates. For instance, the proposed XOR gate can be implemented by using only two NEMS devices compared to that of a static CMOS-based XOR gate that requires at least 10 transistors.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles – *Advanced technologies.*

General Terms
Design, Performance and Reliability.

Keywords
Energy-Efficient Electronics, Laterally-Actuated NEMS, Logic Design, Nano-Electro-Mechanical Switches, Process Variation, Steep-Subthreshold Switch.

1. INTRODUCTION

While aggressive scaling of CMOS devices offers performance improvements as per Moore's law [1], it has already been proven that the subthreshold swing (that determines OFF current) of these transistors has a fundamental lower limit of 60 mV/decade [2]. Hence, research groups have attempted to develop novel non-classical semiconductor, devices which are capable of offering lower subthreshold swings (or steeper subthreshold slopes). For instance, it has been shown through experiments that NEMS devices can exhibit an incredibly low subthreshold swing of 2 mV/decade [3]. As a result, NEMS have generated a great amount of interest especially for integration in the future energy-efficient IC design applications [4]-[6].

There are several techniques to implement NEMS devices such as cantilever (beam) and fixed-fixed based structures [7]-[11]. For instance, several groups have reported promising simulations [11]-[14] and experimental results [15]-[17] on vertically-actuated cantilever switches. However, these vertical switches, with a single actuation electrode, suffer from impact bouncing and a long settling time due to release vibrations [12]. The fabrication and modeling of laterally-actuated double-electrode NEMS are reported here to overcome these challenges and such devices are employed for the design of compact logic gates. It is shown that such structures not only improve the energy efficiency of logic circuits, but that they also offer the possibility of implementing highly compact logic gates.

Since the operation of NEMS involves interactions between the mechanical and electrical elements, the accurate modeling of such systems requires solving the mechanical and electrical equations simultaneously. Moreover, it is important to consider the impact of the non-uniform distribution of the electrostatic forces along the beam. While there are several existing methods that perform electro-mechanical calculations [18]-[26], some previous works consider the non-uniformity of the electrostatic force distributions only through simulations. Although such approaches are reasonable, an analytical modeling approach is preferred since it provides much better insights into the physical nature of the problem. Therefore, this paper, offers a fully-analytical solution for Euler-Bernoulli's beam equation that takes into account such non-uniformities. It should be noted that although the focus of the paper is on "laterally-actuated" NEMS, the proposed models can be applied to both lateral and vertical structures. This paper also proposes novel NEMS-based circuit topologies to implement compact ultra energy efficient inverter, NAND, NOR and XOR gates.

In summary, this paper has three key contributions: (1) The device fabrication and characterization of novel "laterally-actuated double-electrode NEMS" are reported; (2) a comprehensive analytical modeling framework is developed to determine different properties of these devices such as the intrinsic delay, $V_{pull\text{-}in}$ and $V_{pull\text{-}out}$; and (3) design of compact and energy-efficient logic gate components using such NEMS devices are demonstrated for the first time.

This paper is organized as follows. Section 2 provides an overview of the device structure, operation and fabrication flow. Section 3 includes the analytical modeling approach and in Section 4, novel logic gate design strategies and circuit simulation results are reported. Finally, Section 5 concludes this paper.

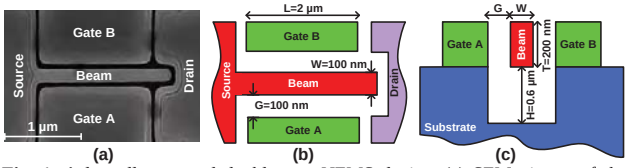

Fig. 1. A laterally-actuated double-gate NEMS device: (a) SEM picture of the fabricated device, (b) schematic of the top-view and (c) the cross-sectional view schematic. Typical values of the different dimensions are also shown here.

2. DEVICE STRUCTURE AND FABRICATION PROCESS

2.1 Device Structure and Operation Principle

The schematic of a lateral NEMS device along with an SEM picture of the fabricated transistor are shown in Fig. 1. The top-view schematic of the device (Fig. 1 (b)) corresponds to the SEM picture shown in Fig. 1 (a). Similarly, the sketch shown in Fig. 1 (c) provides a cross-sectional view of the transistor. This device has two gate terminals or electrodes (A & B in Fig. 1 (a)), which can be controlled independently. The basic operation of the device is illustrated in Fig. 2 where, by applying a bias voltage between one of the gates (for example, Gate A) and the source (Gate B is biased at the same voltage as the source), opposite charges appear on the beam and the corresponding gate terminal, generating an electrostatic force. If the gate voltage is smaller than a threshold value ($V_{pull\text{-}in}$), as shown in Fig. 2 (a), the beam bends slightly, but does not touch the drain terminal. However, if the bias voltage is larger than $V_{pull\text{-}in}$, the beam deflates sufficiently to touch the drain and hence, creates a conduction path from the source to drain as shown in Fig. 2 (b). A sketch of a typical I_{DS}-V_{GS} characteristic of such a device is presented in Fig. 2 (c) where I_{DS} denotes the source-drain current and V_{GS} refers to the gate-source voltage difference. It can be observed that the device exhibits hysteresis.

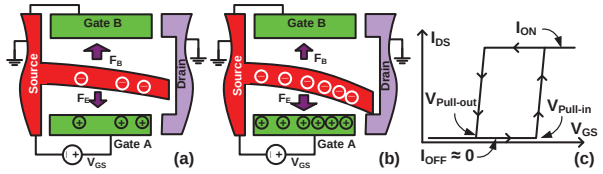

Fig. 2. The basic operation of the laterally-actuated NEMS device: (a) when $V_{GS} < V_{pull\text{-}in}$, (b) when $V_{GS} > V_{pull\text{-}in}$, and (c) I_{DS}-V_{GS} characteristics of the device.

2.2 Fabrication Process Steps

The lateral NEMS devices are fabricated using a standard CMOS flow where 193 nm lithography and dry patterning are employed. The process starts with a silicon dioxide substrate that has a silicon layer on top and a

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buffer sacrificial layer in between (Fig. 3 (a)). After structural patterning followed by dry etch (Fig. 3 (b)), the metallic layer is selectively patterned to form the lateral contact areas (Fig. 3 (c)). Then, a special release process is employed to eliminate stiction (Fig. 3 (d)).

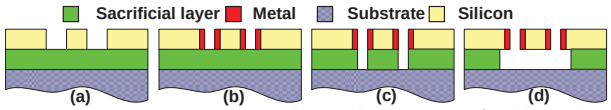


Fig. 3. Fabrication process steps: (a) the initial substrate/sacrificial layer/silicon stack, (b) sidewall patterning, (c) trench process and (d) release etch.

3. ANALYTICAL MODELING FRAMEWORK

3.1 Preliminaries

While numerous papers have attempted to calculate $V_{pull\text{-}in}$ and $V_{pull\text{-}out}$ of NEMS, most previous works fail to analytically model the impact of the non-uniform distribution of the electrostatic forces along the beam. The analytical modeling approach is preferred since it can be used for efficient and comprehensive design optimization and scaling analysis. The importance of taking such phenomena into account is demonstrated in Fig. 4 (a) where the electric field generated by a NEMS device is simulated using a commercial field solver. As it can be observed, the strength of the electric field is significantly different along the length of the beam.

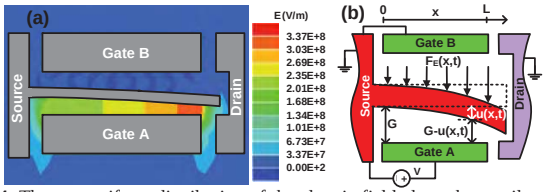


Fig. 4. The non-uniform distribution of the electric field along the cantilever: (a) simulation results from a field simulator (to best view this figure, refer to the electronic version) and (b) the basic problem settings for considering the non-uniformity of the electric field.

The deflation of a cantilever beam at any moment of time along it's length (u(x,t)) is related to the distribution of the electrostatic force ($F_E(x,t)$) by the Euler-Bernoulli's beam equation [27] as shown in Fig. 4 (b). In this equation, ρ is the mass density and A denotes the cross-sectional area of the beam; E and I represent the Young's modulus and momentum of inertia of the beam, respectively.

$$\rho A\frac{\partial^2 u(x,t)}{\partial t^2}+\frac{\partial^2}{\partial x^2}\left(EI\frac{\partial^2 u(x,t)}{\partial x^2}\right)=F_E(x,t) \qquad (1)$$

From Fig. 4 (b) it can be observed that the distance between the beam and the Gate A at location x and time t is G – u(x,t). Using the parallel plate model to compute the coupling capacitance between the beam and the substrate, the electrostatic force ($F_E(x,t)$) can be calculated as (2) where W denotes the width of the beam/gate; V is the gate bias; β is a coefficient, which accounts for the fringing effects and ε_0 is the permittivity of vacuum.

$$F_E(x,t)=\frac{1}{2}\beta\frac{\varepsilon_0 V^2 W}{(G-u(x,t))^2}=\frac{\lambda}{(G-u(x,t))^2} \quad where \quad \left(\lambda=\frac{\beta\varepsilon_0 V^2 W}{2}\right) \qquad (2)$$

Equation (1) shows that $F_E(x,t)$ is a function of u(x,t). On the other hand, u(x,t) itself is a function of $F_E(x,t)$ as described by (2). This interdependency is taken into account in this work by simultaneously solving (1) and (2). The framework provided here can be used to calculate the bending profile of the beam (u(x,t)), which can be subsequently employed to determine the important properties of the NEMS device.

In the above equations, $F_E(x,t)$ and u(x,t) are assumed to be functions of both time (t) and the location along the beam (x), which make (1) a partial differential equation. However, considering a quasi-static switching process, one can disregard the time dependency of variables as shown by (3(a)). Alternatively, the x dependency can be dropped to model the system only in the time domain as indicated by (3(b)).

$$(a)\quad EI\frac{\partial^4 u(x)}{\partial x^4}=\frac{\lambda}{(G-u(x))^2} \qquad (b)\quad \rho A\frac{\partial^2 u(t)}{\partial t^2}=\frac{\lambda}{(G-u(t))^2} \qquad (3)$$

Since 3(a) is a differential equation of the fourth degree, it requires four boundary conditions, which are summarized in (4). The first two boundary conditions (4(a)-(b)) are imposed at the clamped end of the beam (x = 0) while the other two (4(c)-(d)) are required at the free end (x = L) (as shown in Fig. 4 (b)). The boundary conditions at x = 0 state that both the deflection and slope are zero at the fixed end. The boundary conditions at x = L indicate that at the free end of the beam, both the shear force and bending moment are zero. Note that above boundary conditions are valid when the device is not ON (beam is not connected to the drain terminal (see Fig. 2 (a)). Therefore, boundary conditions shown in (4) can only be used for calculating $V_{pull\text{-}in}$. Once the device is ON, both ends of the beam must be considered as fixed ends as the beam touches the drain terminal. Therefore, while the boundary condition at x = 0 (5(a)-(b)) remain identical to (4(a)-(b)), the boundary conditions at x = L must be modified as (5(c)-(d)) where ζ is a small non-negative value to prevent the denominator of the right hand side of 3(a) and 3(b) from becoming zero. The physical interpretation of ζ is that at x = L, although the air gap is very small, it never vanishes completely. The boundary conditions shown in (5) will be used for calculating $V_{pull\text{-}out}$.

$$(a)u(x=0)=0 \quad (b)\frac{\partial u(x=0)}{\partial x}=0 \quad (c)\frac{\partial^2 u(x=L)}{\partial x^2}=0 \quad (d)\frac{\partial^3 u(x=L)}{\partial x^3}=0 \qquad (4)$$

$$(a)u(x=0)=0 \quad (b)\frac{\partial u(x=0)}{\partial x}=0 \quad (c)u(x=L)=G-\zeta \quad (d)\frac{\partial u(x=L)}{\partial x}=0 \qquad (5)$$

3.2 Solving Euler-Bernoulli's Equation in the x-Domain

Equation (3(a)) is a non-linear fourth-order differential equation, which implies that there is no systematic way to solve it analytically. However, it is possible to find a closed-form answer, if the right-hand side of the differential equation is linearized. Once it is linearized, one can guess the general form of the solution and obtain the coefficients by considering the boundary conditions. Note that the general solution to (3(a)) is the superposition of the particular solution ($u_P(x)$) and the complementary solution ($u_C(x)$), or in other words, $u(x) = u_C(x) + u_P(x)$. The complementary solution ($u_C(x)$) can be obtained by setting the right-hand side of (3(a)) to zero, which suggest that the $u_C(x)$ must be a polynomial of the third degree. By applying the Taylor series expansion and keeping the first three terms, the right hand side of 3(a) can be estimated with a polynomial similar to "$\alpha x^2 + \beta x + \gamma$" where α, β and γ are to be determined. If the right hand side of 3(a) is a second order polynomial, the particular solution ($u_P(x)$) for (3(a)) should be a polynomial of the sixth degree. Therefore, combining two polynomials ($u_C(x) + u_P(x)$), one can suggest that the general solution for (3(a)) is a sixth order polynomial as shown by (6) where $k_0 \sim k_6$ need be determined.

$$u(x)=k_0+k_1x+k_2x^2+k_3x^3+k_4x^4+k_5x^5+k_6x^6 \qquad (6)$$

Assuming the general form of u(x) as shown in (6) and considering the boundary conditions at x = 0 (4(a)-(b)), one can linearize 3(a) by applying the Taylor expansion around x = 0. By keeping only the first three terms, one gets:

$$\frac{\lambda}{(G-u(x))^2}\approx\lambda\left[\frac{1}{G^2}+\frac{6\times k_1+2\times k_2 G}{G^4}x^2\right] \qquad (7)$$

On the other hand, the left-hand side of (3(a)), considering (6), can be easily re-written as (8):

$$EI\frac{\partial^4 u(x)}{\partial x^4}=360k_6x^2+120k_5x+24k_4=\lambda\left[\frac{1}{G^2}+\frac{6\times k_1+2\times k_2 G}{G^4}x^2\right] \qquad (8)$$

By equating the corresponding coefficients in (8), one gets:

$$(a)24k_4=\frac{\lambda}{G^2},\quad (b)120k_5=0,\quad (c)360k_6=\lambda\left(\frac{6\times k_1+2\times k_2 G}{G^4}\right) \qquad (9)$$

Furthermore, applying the boundary conditions (4(a)-(b)) and (4(c)-(d)), one gets (10) and (11), respectively.

$$(a)k_0=0,\quad (b)k_1=0 \qquad (10)$$

$$(a)120k_6L^3+24k_4L+6k_3=0 \quad (b)360k_6L^2+24k_4=0 \qquad (11)$$

Equations (9)-(11) provide seven equations for the seven unknown variables ($k_0 \sim k_6$), which can be analytically solved (although the final equations are not included here due to limited space). Using (9)-(11), the actual curvature of the beam in response to a particular gate bias can be modeled as shown in Fig. 5. The different physical dimensions of the devices are indicated in Fig. 5 (a) and various bending profiles of the beam (on the vertical axis) along its length (on the horizontal axis) are plotted in Fig. 5 (b). Given these profiles, it is possible to evaluate the total electrostatic and elastic forces that are applied to the beam. Once the forces are determined, the $V_{pull\text{-}in}$ and $V_{pull\text{-}out}$ can be easily calculated.

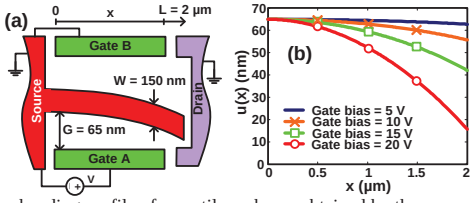


Fig. 5. The bending profile of a cantilever beam obtained by the proposed model: (a) physical dimensions of the device (the fringing effect factor (β) is estimated to be *1.2*) and (b) the curvature of the beam under different bias conditions.

Equations (9)-(11) are obtained assuming the boundary conditions in (4), which are valid only when the device is OFF and hence, they can only be used to calculate $V_{pull\text{-}in}$. To calculate $V_{pull\text{-}out}$, the bending profile must be evaluated when the device is ON. To do so, repeating a similar procedure and applying the boundary conditions (5(a)-(b)) and (5(c)-(d)), one gets (10) and (12), respectively. Therefore, (8), (9), (10) and (12) provide the necessary formulas to calculate the curvature of the beam when the device is ON.

$$(a)k_6L^6+k_4L^4+k_3L^3+k_2L^2=\zeta \quad (b)6k_6L^5+4k_4L^3+3k_3L^2+2k_2L=0 \qquad (12)$$

3.2.1 *Pull-in Voltage Calculation*

As shown in Fig. 2, $V_{pull\text{-}in}$ is the voltage at which the electrostatic force (F_E) exceeds the elastic force (F_B), thereby pulling the cantilever beam all the way down. However, since the device characteristic involves hysteresis, in order to compute $V_{pull\text{-}in}$ accurately, one must start off from zero gate bias and increase it gradually until the pull-in condition occurs ($F_E > F_B$). The algorithm for computing $V_{pull\text{-}in}$ using the proposed framework is shown in Fig. 6 (a). A simulation result obtained by applying this algorithm is also reported in Fig. 6 (b) where the horizontal and vertical axes are the gate bias and force, respectively. It can be observed that F_B is initially higher, but F_E becomes eventually larger due to increased bias. Note that the $V_{pull\text{-}in}$ for this particular device should be ≈ 20 V.

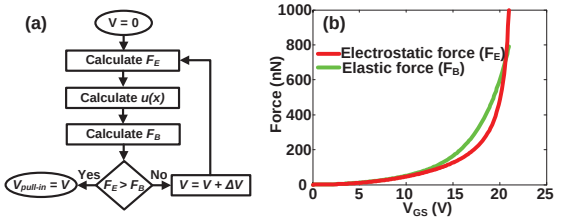


Fig. 6. $V_{pull\text{-}in}$ Calculation: (a) the algorithm and (b) simulation results for the device dimensions shown in Fig. 5 (a).

Using the proposed method, one can evaluate the impact of process variation on the $V_{pull\text{-}in}$ distribution. For instance, Fig. 7 (a) reports the sensitivity of $V_{pull\text{-}in}$ to Young's modulus (E), air gap (G) and width of the beam (W). In this figure, the vertical axis shows the percentage of $V_{pull\text{-}in}$ fluctuations caused by 1% variations in each of those parameters. Here, the air gap size is the dominant source of $V_{pull\text{-}in}$ fluctuations followed by the device width. Moreover, Fig. 7 (b) illustrates the $V_{pull\text{-}in}$ distribution due to 5% variation in all aforementioned parameters. The standard deviation of the $V_{pull\text{-}in}$ distribution is ≈ 11 % of its mean value. Note that the sensitivity of $V_{pull\text{-}in}$ to these parameters is about the same for various beam lengths (L).

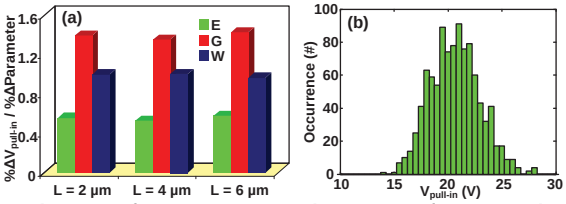


Fig. 7. The impact of process variation: (a) the sensitivity of $V_{pull\text{-}in}$ to each of the important design parameters and (b) the distribution of $V_{pull\text{-}in}$ due to 5% variation of *E*, *G* and *W* parameters (device dimensions are shown in Fig. 5 (a)).

3.2.2 *Pull-out Voltage Calculation*

A similar approach can be taken to evaluate the $V_{pull\text{-}out}$ of NEMS devices. Pull-out occurs when the electrostatic force (F_E) is no longer stronger than the elastic force (F_B) due to a reduced gate voltage (Fig. 2 (a)). As shown in Fig. 8 (a), to evaluate the $V_{pull\text{-}out}$, one must start off from any gate voltage higher than the $V_{pull\text{-}in}$ and reduce it gradually until the pull out condition occurs ($F_E < F_B$). Fig. 8 (b) depicts the F_E and F_B curves, which are generated using such a $V_{pull\text{-}out}$ calculation algorithm where the horizontal and vertical axes are gate bias and force, respectively. Since the curvature of the beam is unchanged prior to pull-out, the elastic force (F_B) remains constant. However, by reducing the gate voltage, the electrostatic force (F_E) decreases until it becomes lower than F_B and hence, the pull-out phenomena initiates. From Fig. 8 (b), one can conclude that $V_{pull\text{-}out}$ for this device is ≈ 8V.

The impact of fluctuations in Young's modulus (E), air gap (G) and width of the beam (W) on the $V_{pull\text{-}out}$ are investigated as shown in Fig. 9 (a) where the vertical axis represents the sensitivity of $V_{pull\text{-}out}$ to the above parameters. It can be observed that unlike $V_{pull\text{-}in}$, the variation in the air gap size and the device width can equally impact the $V_{pull\text{-}out}$ of these devices. Moreover, Fig. 9 (b) illustrates the $V_{pull\text{-}out}$ distribution due to 5% variations in those device parameters. The standard deviation of the $V_{pull\text{-}out}$ distribution is ≈ 3.5 % of its mean value suggesting that $V_{pull\text{-}in}$ exhibits higher sensitivity to process variation under an identical scenario.

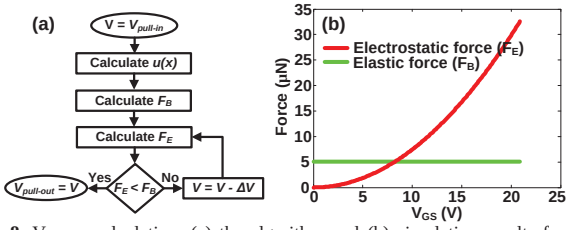


Fig. 8. $V_{pull\text{-}out}$ calculation: (a) the algorithm and (b) simulation results for the device dimensions shown in Fig. 5 (a).

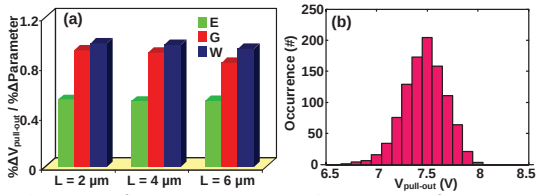
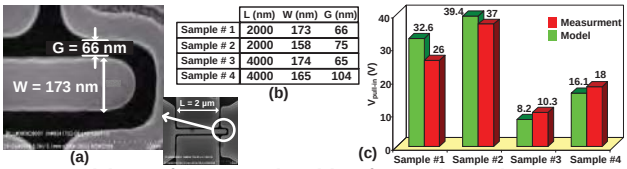


Fig. 9. The impact of process variations: (a) the sensitivity of $V_{pull\text{-}out}$ to each of the important design parameters and (b) the distribution of $V_{pull\text{-}out}$ due to 5% variations in *E*, *G* and *W* parameters. Device dimensions are shown in Fig. 5 (a).

3.2.3 *Model Validation & Comparison with Existing Models*

The calculated $V_{pull\text{-}in}$ values are validated against measurement data obtained from fabricated devices as shown in Fig. 10. The different geometrical dimensions of the fabricated devices (Fig. 10 (a)) are measured and reported in Fig. 10 (b). Using this data, the $V_{pull\text{-}in}$ values are calculated and compared to the actual measured results as shown in Fig. 10 (c). It can be observed that the calculated values are in good agreement with the measured values. The small amount of discrepancies is typically due to the inherent limitations and errors that creep in the physical measurements of device parameters.



	L (nm)	W (nm)	G (nm)
Sample # 1	2000	173	66
Sample # 2	2000	158	75
Sample # 3	4000	174	65
Sample # 4	4000	165	104

Fig. 10. Validation of the proposed modeling framework: (a) The SEM picture along with the physical dimensions of Sample #1 (b) The geometrical dimensions of the four samples and (c) comparison between the measured and calculated $V_{pull\text{-}in}$ values.

The $V_{pull\text{-}in}$ calculations performed by the proposed model and the most commonly used existing model [22] are compared in Fig. 11 (a) for NEMS devices with various beam lengths. It is shown that the conventional model "underestimates" the actual value of the $V_{pull\text{-}in}$ and $V_{pull\text{-}out}$. Note that neglecting the impact of non-uniform electrostatic force profile results in even larger errors in shorter devices. The reason is that the shorter devices have higher curvatures and hence, the distribution of force in such devices is highly non-uniform.

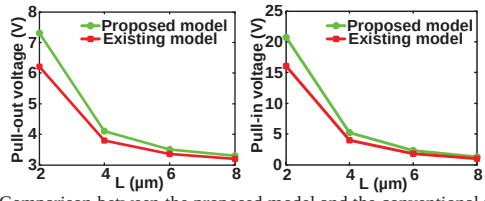


Fig. 11. Comparison between the proposed model and the conventional model for calculating (a) $V_{pull\text{-}in}$ and (b)$V_{pull\text{-}out}$. Device dimensions are shown in Fig. 5 (a).

3.3 Solving Euler-Bernoulli's Equation in the Time Domain

One of the key characteristics of a NEMS device is its intrinsic delay that is defined as the time delay between applying the gate bias and the moment the device turns ON (during which, the cantilever moves from its original position and touches the drain). Such a time delay can be determined by solving (3(b)), which is a non-linear second order differential equation. Fortunately, by employing an auxiliary variable y(t), as defined by (13), one can analytically solve this differential equation as follows:

$$y(t) = \frac{\partial u(t)}{\partial t} \rightarrow \frac{\partial^2 u(t)}{\partial t^2} = \frac{\partial y(t)}{\partial u(t)} \cdot \frac{\partial u(t)}{\partial t} \rightarrow \frac{\partial^2 u(t)}{\partial t^2} = \frac{\partial y(t)}{\partial u(t)} \cdot y(t) \qquad (13)$$

By substituting (13) into (3(b)), one gets:

$$\rho A \frac{\partial^2 u(t)}{\partial t^2} = \frac{\lambda}{(G-u(t))^2} \rightarrow \frac{\partial y(t)}{\partial u(t)} . y(t) = \frac{\lambda/\rho A}{(G-u(t))^2} \rightarrow \int y(t) dy = \int \frac{(\lambda/\rho A) du}{(G-u(t))^2} \qquad (14)$$

Equation (14) is a first order differential equation that can be easily solved to obtain a formula for y(t). Subsequently, the equation by which the auxiliary variable is defined, can be solved to provide a formula for u(t) as shown by (15).

$$\frac{1}{\sqrt{-2C_1}} \left[\sqrt{(G-u(t))\left(-\frac{\lambda/\rho A}{C_1} - G + u(t)\right)} - \frac{\lambda}{C_1} \tan^{-1} \left(\frac{\sqrt{(G-u(t))\left(-\frac{\lambda/\rho A}{C_1} - G + u(t)\right)}}{\frac{\lambda/\rho A}{C_1} + G - u(t)} \right) \right] = t + C_2 \qquad (15)$$

In (15), C1 and C2 are two constants of integration that must be determined using the boundary conditions of the problem as shown by (16)-(17). The first boundary condition, (16), indicates that the beam displacement

at t = 0 is zero (i.e., the beam is not deflected). The second boundary condition, (17), indicate that the speed of the beam at t = 0 is zero.

$$u(t=0)=0 \rightarrow C_2=0 \tag{16}$$

$$y(t)=\frac{\partial u(t=0)}{\partial t}=0 \rightarrow \frac{2(\lambda/\rho A)}{G}+2C_1=0 \rightarrow C_1=-\frac{\lambda}{\rho AG} \tag{17}$$

Equations (15)-(17) provide the analytical formulas that are required for evaluating the intrinsic delay of NEMS devices. Note that in (15), t is equal to the intrinsic delay, if u(t) is the deflection of the beam at the moment when pull-in occurs.

4. NOVEL LOGIC GATE DESIGNS

Exclusive properties of the laterally-actuated double-gate NEMS offer opportunities for designing ultra compact logic gates. That is because the existence of two independent gate terminals provides higher flexibility to control the operation of the device through two data signals. In this subsection, novel device-level architectures for implementing inverter (the simplest logic gate), NAND, NOR (two universal logic gates) and XOR (the most common building block of the arithmetic units) are proposed.

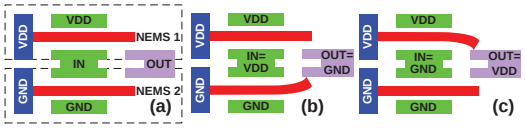


Fig. 12. The proposed inverter gate based on laterally-actuated double-gate NEMS transistors: (a) the design, (b) The device sketch when the input is "high" and (c) the device sketch when the input is "low".

The inverter gate can be implemented using two NEMS devices as shown in Fig. 12 (a) where the input (labeled as 'IN') is formed by connecting one gate from each transistor. The drain terminals of two devices are tied together to create the output (labeled as 'OUT'). The source terminal of 'NEMS1' and 'NEMS2' are connected to supply voltage (labeled as 'VDD') and ground (labeled as 'GND'), respectively. Furthermore, the second gate terminal of 'NEMS1' and 'NEMS2' are tied to VDD and GND, correspondingly. The basic operation of the inverter is illustrated in Fig. 12 (b) (when the input is 'high') and Fig. 12 (c) (when the input is 'low'). If the input is 'high' (tied to VDD), NEMS1 is OFF since the beam and both gates are at the same voltage level (there is no electrostatic force to bend the beam). However, the beam of NEMS2 is tied to GND and the input is connected to VDD, which creates sufficient electrostatic attraction to deflect the beam and turn the device ON, thus connecting OUT to GND. The reverse of the above scenario occurs when the input is 'low' (tied to GND); NEMS2 is OFF and the output is connected to VDD through NEMS1.

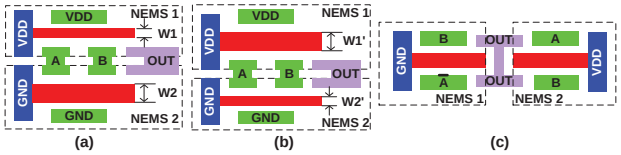


Fig. 13. Logic gate designs using laterally-actuated double-gate NEMS devices: (a) NAND, (b) NOR and (c) XOR gate designs.

The implementation of two-input NAND, NOR and XOR logic gates are illustrated in Fig. 13 and the ON/OFF states of NEMS devices in each logic gate are summarized in Table 1 for all the possible input patterns. Note that unlike the previous devices, the gate terminal of NEMS transistors employed in these designs are divided into two segments in order to provide more flexibility. The NAND gate is realized using two such NEMS transistors as shown in Fig. 13 (a). Note that the cantilever beam of NEMS2 is deliberately designed to be wider than that of NEMS1 (W2 > W1). As a result of such implementation, more force is required to bend the cantilever of NEMS2 compared to that of NEMS1 because wider beams are stiffer. In this design, W2 is chosen such that connecting only one of the inputs (A or B) to GND does not generate enough electrostatic force to turn the device ON. However, once both A and B are 'high', the beam can be sufficiently deflected to touch the drain terminal and connect OUT to GND.

Table 1. The states of NEMS devices (ON or OFF) and the output value of logic gates (NAND, NOR and XOR) for different combinations of inputs.

	NAND			NOR			XOR		
	NEMS1	NEMS2	OUT	NEMS1	NEMS2	OUT	NEMS1	NEMS2	OUT
A='0'&B='0'	ON	OFF	'1'	ON	OFF	'1'	ON	OFF	'0'
A='0'&B='1'	ON	OFF	'1'	OFF	ON	'0'	OFF	ON	'1'
A='1'&B='0'	ON	OFF	'1'	OFF	ON	'0'	OFF	ON	'1'
A='1'&B='1'	OFF	ON	'0'	OFF	ON	'0'	ON	OFF	'0'

Therefore, the basic operation of the NAND gate can be explained as follows (see Table 1). If both inputs are low, the NEMS1 turns ON (NEMS2 is OFF) connecting the output to VDD. If only one of the inputs (either A or B) is 'low', NEMS1 again turns ON whereas NEMS2 remains OFF since one 'high' input is not able to deflect the beam sufficiently to turn the device ON. Finally, when both inputs are high, NEMS1 is OFF and inputs A and B are jointly able to generate enough electrostatic force to turn NEMS2 ON. A similar approach is adapted to implement a NOR gate as shown in Fig. 13 (b). Here, the only difference is that, unlike the NAND gate, the cantilever of NEMS1 is made wider than NEMS2 (W2'<W1').

The architecture of the XOR gate is shown in Fig. 13 (c) where only two NEMS transistors are required. Note that for static CMOS implementation of XOR gates at least 10 transistors are necessary. This indicates that laterally-actuated double-gate NEMS devices are an excellent candidate for the implementation of highly compact arithmetic units, which extensively employ XOR gates as their main building blocks. In the proposed XOR architecture, NEMS2 remains OFF when A and B have the same logic value; however, NEMS1 turns ON and connects the output to GND (see Table 1). NEMS2 is OFF because when A=B='high', there is no electrostatic attraction between NEMS2's beam and two gates (A and B). On the other hand, when A=B='low', both inputs generate electrostatic force, but in opposite directions and hence, NEMS2 remains OFF despite the existence of those forces. Note that when A and B have different logic values, NEMS1 is ON and NEM2 turns OFF and hence, OUT is connected to VDD.

5. CONCLUSIONS

This paper, reports the fabrication and modeling of laterally-actuated double-electrode NEMS structures and design of novel logic gates using such devices. A comprehensive analytical framework is developed to solve the Euler-Bernoulli's beam equation in order to model the different electrical properties of such devices. The model is validated using the measurement data of the fabricated devices. It is shown that by ignoring the non-uniformity of the electrostatic force distribution, the existing models "underestimate" the actual values of $V_{pull\text{-}in}$ and $V_{pull\text{-}out}$. Furthermore, novel NEMS-based inverter, NAND, NOR and XOR gates are proposed. It is shown that an XOR gates can be implemented using only two NEMS devices and hence, it is possible to develop ultra compact NEMS-based arithmetic units. The proposed NEMS device and logic gates can potentially lead to unprecedented levels of energy-efficiency in digital IC design.

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