Ambipolar Double-gate FETs for the Design of Compact Logic Structures

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ABSTRACT

We present in this paper a circuit design approach to achieve compact logic circuits with ambipolar double-gate devices, using the in-field controllability of such devices. The approach is demonstrated for complementary static logic design style. We apply this approach in a case study focused on Double Gate Carbon Nanotube FET (DG-CNTFET) technology and show that, with respect to conventional CMOS-like static logic structures and for comparable power consumption, time delay and integration density can both be improved by a factor of 1.5x and 2x, respectively. Compared with a predictive model for 16nm CMOS technology, the gates built according to the design approach described in this work and based on DG-CNTFET offer a gain of 30% concerning Power-Delay-Product (PDP).

Categories and Subject Descriptors

B.6.1 [**Logic Design**]: Design style –*Combinational logic, logic arrays*. B.7.1. [**Integrated Circuits**]: Types and Design styles – *advanced technologies, gate arrays.*

General Terms

Performance, Design.

Keywords

Four-terminal devices, ambipolar double-gate devices, static logic, CNTFETs, emerging technologies.

1. INTRODUCTION

The "Beyond CMOS" concept has motivated much research on emerging research devices and materials, as described in the ITRS [1]. Novel materials and devices have been explored showing an ability to complement or even replace the CMOS transistor or its channel in systems on chip before silicon-based technology will reach its limits. These possible emerging technologies range from transistors made from silicon nanowires to devices made from nanoscale molecules.

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Some of the most promising devices are carbon-based nanodevices such as the carbon-nanotube (CNT) field-effect transistor (FET) (CNTFET) or the graphene-nanoribbon FET. Furthermore, such a device can be built in the context of double gate devices which can be classified in terms of their gate geometry regardless of the underlying device process; Typically the front and back gates of DG devices are connected together resulting in a 3-Terminal device to improve the performance of conventional single gate bulk CMOS devices [2] [3] [4].

DG devices with independent gates are 4-Terminal devices and show the potential to provide novel logic blocks and innovative techniques for digital design thanks to their specific intrinsic properties. Many works [6] [7] have shown how such a device opens the way for fine-grain reconfigurability since DG devices can be used to realize in-field programmable ambipolar devices, i.e. devices whose p- or n-type behaviour can be programmed in-field using the fourth terminal. Also, a variety of circuits in logic and memory can benefit from independent gate operation of DG devices, such as those presented in [8] for low power and high performance.

Moreover, multiple gate structures have also shown the potential to develop new logic gates with a significant decrease in transistor count, with for example FinFETs [7] or with Double Gate CNTFET in [9], where it was demonstrated that the use of ambipolar double-gate FETs can reduce the transistor count in clocked standard cells by the use of the additional terminal of the DG-CNTFET. Independent gate control can also be used to merge parallel transistors in non-critical paths [8]. This results in a reduction of the effective switching capacitance and hence power dissipation.

In this work, we present an approach which uses double-gate ambipolar transistors in complementary static-logic style to reduce transistor count by merging transistors-in-series into a single transistor in multiple input logic circuits (such as complex gates and multiplexers), and evaluate its impact on power consumption and time delay, using a compact model, in the case of DG-CNTFETs with maximal flexibility at the layout level.

We begin by describing the technological hypotheses and modelling in section 2. We present the concept of the approach in section 3 and its application to the complementary-static logic structure with several examples, and then performance evaluation of the novel circuits obtained from this approach in the case of DG-CNTFETs is presented and compared to a 16nm CMOS technology predictive model in section 4. Section 5 is the conclusion.

2. TECHNOLOGICAL HYPOTHESES AND MODELLING

2.1 DG CNTFET fabrication

At present, various types of CNTFET devices have been produced experimentally, but there is no standard CNTFET process. In many works using CNTFET devices [10] [11], realistic and CMOS-compatible process flow steps have been suggested to manufacture such a device. A prior work, presented the structure of a DG CNTFET based on aligned semiconducting CNTs [12], applying the self-alignment technique [13] and using two top gates [14], as well as potential hybrid integration with CMOS technology and consequently with metal interconnections defined by CMOS-compatible lithography steps. In this work, the same hypotheses are kept, except that the structure used here does not have two top-gates, but a top-gate and a back-gate in order to be more faithful to the compact model used later for simulations. Figure 1(a), reported from a recent work [11] using the same compact model, shows the structure of the CNTFET with double gates. The front gate FG turns the device on or off, in the same way as the regular gate of a MOSFET; while the back-gate BG controls the device polarity setting to N- or P-type with a positive (V_{BG}-V_S= +V) or negative (V_{BG}-V_S= -V) voltage, respectively. The symbol for this in-field programmable CNTFET is shown in Fig 1(b).

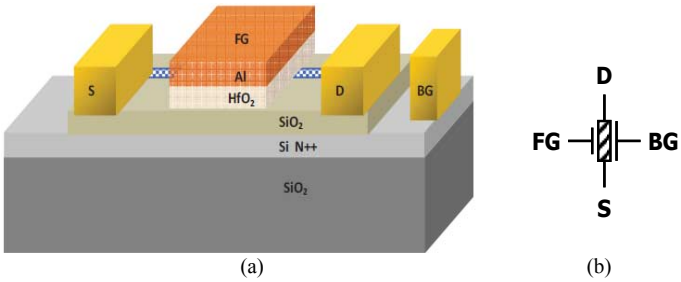


Figure 1. DG-CNTFET device (a), symbol (b)

2.2 DG-CNTFET compact model

Many compact models [15] [16] have been developed to describe CNTFET technologies such as Schottky barrier (SB) CNTFETs or MOS-like CNTFETs with a top gate or surrounding gates. However, none of these are able to model a DG CNTFET properly. In prior works [6] [9] simulations were carried out with the model presented in [17] which is limited to thermionic transport without taking into account the coupling between the FG and BG and does not include SB (sub-band) modeling or BTBT (band-to-band tunneling). Recently, a more accurate model has been presented in [10]. To the best of our knowledge; it represents the first physically accurate model of a DG CNTFET with efficient convergence and simulation speed compatible with circuit design. The compact model is detailed in [10], where it was shown to include the most significant mechanisms such as the SB at the metal–nanotube interface, charge and electrostatic modeling, BTBT effect, and quasi-ballistic transport. Furthermore, the comparison of the model with measurements from two technologies published in literature; a DG CNTFET from IBM [18] and a DG CNTFET from Stanford University (used as a MOS-like CNTFET) [19], showed the accuracy of the compact model on different technology configurations since the values of the extracted parameters are close to those in the available technologies. We mention that although the structure of DGCNTFET suggested in this work is not exactly the same with the case modeled in [10], we suppose that the physical behaviour of the device is the same and we used the model in [10] for all simulations in this work.

3. NOVEL FAMILY OF DG-CNTFET LOGIC CELLS

In the case of the DG-CNTFET, completely new prospects for reconfigurability are possible due to its ambipolar (N- and P-type) behavior. In previous works, ambipolarity was exploited to build dynamically reconfigurable logic cells [9]. In the same perspective, a complete design methodology (using Ambipolar Binary Decision Diagrams Am-BDD) to generate reconfigurable cells based on ambipolar devices was defined in [6]. However in this work, rather than using the back-gate reconfigurability and associated states (N-type, P-type, off-state) for reconfigurability purposes, we used the back-gate signal as a free variable in order to design compact logic gates.

3.1 General concept

Equivalent logic path resistance is proportional to the number of transistors in series, and inversely proportional to the average transistor width. Hence, two n-type transistors in series (NTTS structure) or p-type transistors in series (PTTS structure) must either demonstrate a path resistance of $2R_{ch}$ with no transistor resizing or an input gate capacitance of $2C_g$ with transistor width doubling to reduce overall path resistance (where R_{ch} and C_g represent the channel resistance and gate capacitance of a single minimum width transistor, respectively). Hence two transistors in series (TTS structures) are critical for path resistance and gate capacitance optimization, with consequent impact on delay, power and area. The switching between the n- and p-states in ambipolar DG CNTFETs allows TTS structures to be substituted by a single DGFET with no loss of functionality as shown in figures 2 and 3 for the NTTS and PTTS structures respectively.

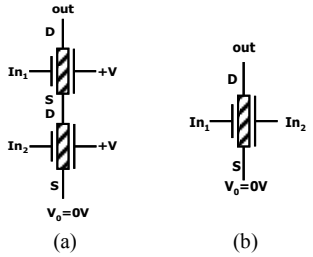


Figure 2. Direct transposition of CMOS-NTTS structure with ambipolar DGFETs (a), Single ambipolar DGFET equivalent TTS structure (b)

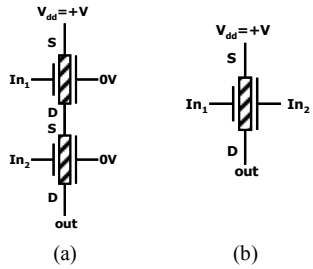


Figure 3. Direct transposition of CMOS-PTTS structure with ambipolar DGFETs (a), Single ambipolar DGFET equivalent TTS structure (b)

In the initial NTTS structure in figure 2(a), both transistors are N-type since the back gate BG is set to +V and V_0 is set to 0V (i.e. V_{BG}-V_S=+V). In this case, a path is established between "V_0" and "out" only for In_1In_2="11". In the single ambipolar DGFET structure, shown in figure 2(b), the same condition is true since for In_2="1", the back gate BG is set to +V such that the transistor is N-type and will be ON only if In_1="1" also. For other combinations In_1In_2= {"01","10","00"} the transistor will be OFF. Thus, the NTTS structure can be replaced by a single ambipolar DGFET.

By analogy, the PTTS structure in figure 3(a) obtains the same benefit since both transistors are P-type when the back gate BG is set to 0V and V_{dd} is set to +V (i.e. V_{BG}-V_S=-V). Again, In this case, a path is established between "V_{dd}" and "out" only for In_1In_2="00". In the single ambipolar DGFET structure, shown in figure 3(b), the same condition is true since for In_2="0", the back gate BG is set to 0V such that the transistor is P-type and will be ON if In_1="0". For other combinations In_1In_2= {"01","10","11"} the transistor will be OFF.

Hence, in a complementary static logic approach based on a pull-up network formed from p-type transistors and a pull-down network formed from n-type transistors, this approach can be applied in the case of many complex logic gates as shown in the next section.

3.2 Double-Gate static logic (DGSL) cells

3.2.1 Generic function

In our approach, we replace any NTTS and PTTS structures in static logic pull-down and pull-up networks respectively with equivalent ambipolar DGFETs. A generic example illustrating the transformation between a Conventional CMOS Static-Logic (CSL) structure and the Double-Gate Static Logic (DGSL) structure using the TTS approach is shown in figure 4. In the figure, both circuits implement the output function.

Out= $\neg[(i_1 \wedge i_2 \wedge i_3 \wedge ... i_n) \vee (j_1 \wedge j_2) \vee (k_1)]$.

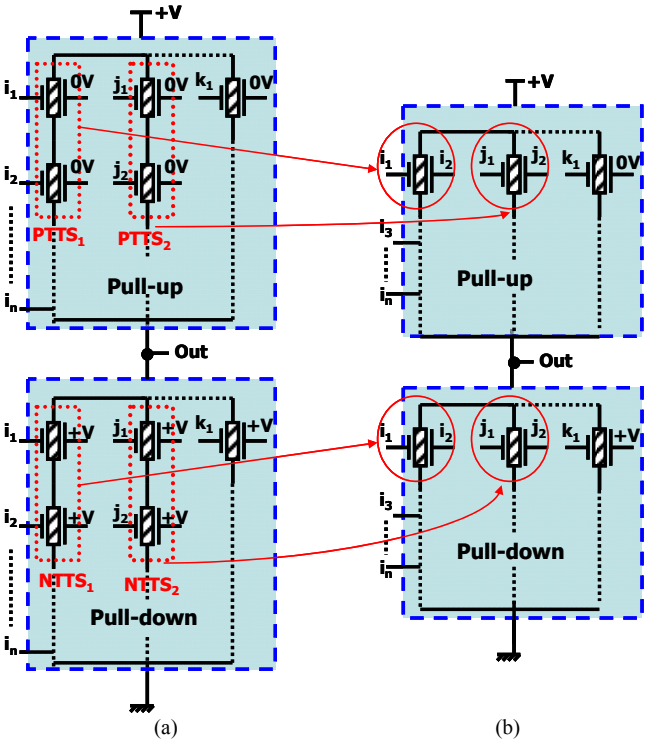


Figure 4. CSL structure (a), DGSL structure (b)

If we consider that n is the number of inputs of the function, m is the number of NTTS structures and p is the number of PTTS structures that can replace two AND-related inputs in the function path, the required number of transistors will be 2n-(m+p).

3.2.2 Examples: 2-input XOR gate and multiplexers

The approach can be applied to any complementary static logic gate containing TTS structures. In for example simple monotonic gates, such as the NAND (resp. NOR) gate, where the pull-down (resp. pull-up) network contains one NTTS (resp. PTTS) and the pull-up (resp. pull-down) network is formed from 2 transistors in parallel, only the pull-down network is substituted with a single ambipolar DGFET and we obtain a gain of a single transistor. However, in the case of more complex gates such as XOR/XNOR gates and multiplexers, the gain can be more significant and the approach can be applied to all branches of the gate.

The conventional CMOS-type 2 input XOR structure (CSL) is shown in figure 5(a). By applying the approach to this gate, figure 5(b) shows a compact XOR gate where all TTS structures were substituted with a single ambipolar DGFET, leading to a reduced transistor count with a simpler structure of 4 transistors instead of 8. Figure 5(c) shows simulation results under the conditions detailed in section IV.

We note that in figure 5(a), we choose to connect the back gates of the pull-up transistors to the ground and the back gates of the pull-down transistors to V_{dd}. But this choice is not consistent, we could connect the back gates to any different voltage with respect to the condition that the polarity of the device is set to N- or P-type with a positive (V_{BG}-V_S= +V) or negative (V_{BG}-V_S= -V) voltage, respectively.

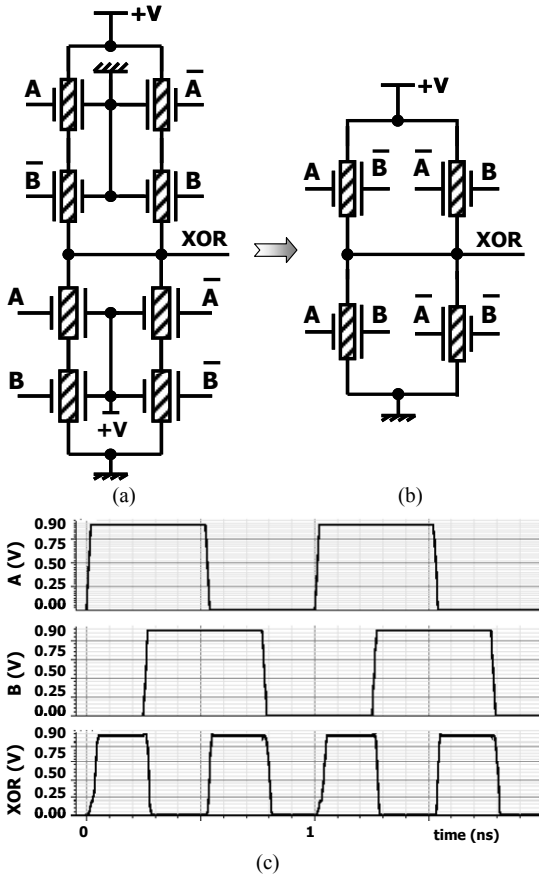
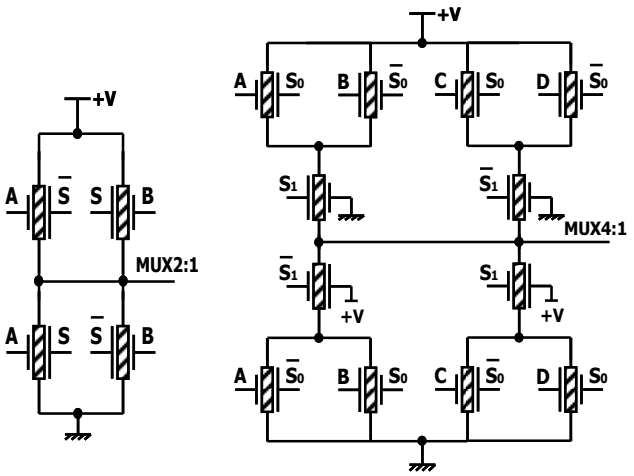


Figure 5. 2-input XOR gate: CSL structure(a) DGSL structure (b) DGSL simulated waveform (c)

To further illustrate the principle of the DGSL cells, some examples of elementary circuits are shown in figure 6. The structure of the static logic 2:1 MUX is very similar to the XOR gate so the same gain in terms of transistor count is observed. In the case of static logic 4:1 MUX, we are using 8 transistors fewer than in the conventional structure, i.e. a reduction of 40% is observed rather than 50% as in 2:1 MUX or the XOR gate .



(a) (b)

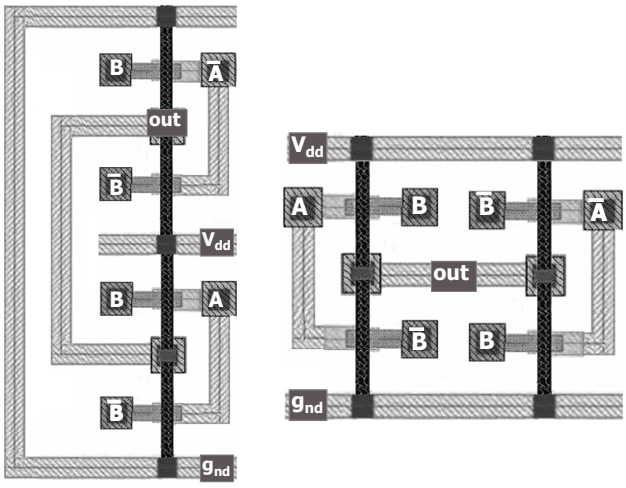
Figure 6. DGSL 2:1MUX gate (a), DGSL 4:1MUX (b)

3.2.3 Layout of DGSL structure

Figure 7(a) shows one layout of the XOR gate. This layout exploits the approach of building a complementary logic circuit along the length of a single nanotube. Here all transistors are built with the same nanotube.

In figure 7(b) we propose a second layout of the XOR gate using two nanotubes to show the possibility of direct transposition of the schematic view on a layout level.

As with any standard cell approach, the layout must be normalized to a set *y*-dimension, in order to place cells in rows. The inverted function (i.e. the XNOR function in this case) can be achieved by simply flipping the layout.



(a) (b)

Figure 7. Layout of DGSL XOR gate: single nanotube (a) double nanotubes(b)

4. PERFORMANCE EVALUATION

While the principal goal of using the TTS association approach is to reduce transistor count in logic cells, the impact of such a reduction is expected to be extended to various performance metrics of the logic cell such as power consumption and delay.

In this section, we compare the new logic gates with their equivalent gates based on conventional CMOS-type logic. Using the same ambipolar DGFET device we extend the comparison to conventional CMOS logic built with silicon technology (SiSL) based on the Predictive Technology Model (PTM) 16nm low power (LP) transistor models [20].

4.1 Device models

While this approach is valid for any ambipolar DGFET, we evaluate performance metrics using a DG-CNTFET device model, as described in section II [10].

To obtain an objective and quantitative performance and power consumption comparison between the cells using this model with conventional cells using the CMOS PTM 16nm LP model, we fit the width of the CMOS transistors in such a way as to obtain the same I_{on} current. Table I shows the parameters used for the DG CNTFET compact model as presented in [10] and the tuned length/width of the predictive model.

In [10], the model is described in detail, with various nanotube configurations (chirality/number/diameter) for a range of values of back-gate and supply voltages. In our case, we chose configurations to enable a reasonable comparison with the PTM 16nm model in term of channel length, width, voltage and consequent I_{on}.

TABLE I Parameters of transistors used

Parameters	DG CNTFET	PTM 16nm LP
Drain access channel length	50nm	-
Source access channel length	50nm	-
Inner channel	20nm	16nm
Width	50nm	56nm(n-type)/80nm(p-type)
Chirality (n,m)	(11, 0)	-
Nb of nanotubes	12	-
Diameter of 1 nanotube	0.861176 nm	-
Supply voltage	0.9 V	0.9 V

Figures 8 and 9 show the I_{DS}/V_{GS} characteristics of the DG CNTFET model and PTM 16nm model, respectively for n-type and p-type configurations, where V_{GS} varies between 0 and 0.9 V, V_D=0.9V and V_S=0V.

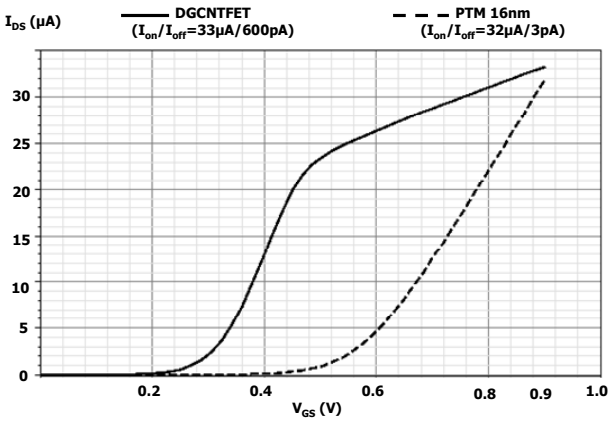


Figure 8. I_{DS}/V_{GS} characteristics of the n-branch

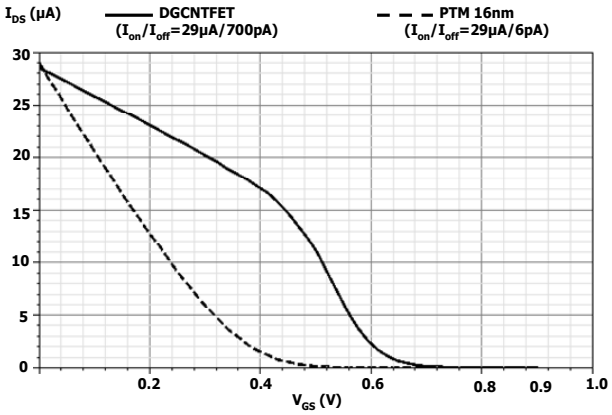


Figure 9. I_{DS}/V_{GS} characteristics of the p-branch

4.2 Program of investigation

Our comparative study was carried out between conventional static logic structures; figure 4(a), built with DG-CNTFET technology (CSL), Silicon static logic technology (SiSL) and equivalent DGSL circuits designed in this work, figure 4(b).

We suppose that there is no difference in rise and fall times between front and back gate inputs. We ran simulations with a frequency of 1GHz and equal rise and fall times (20ps) with a capacitive load of 150aF. The supply voltage was 0.9V and clock and data inputs were single rail (i.e. +V=0.9V, V_0=0V). Cyclic simulations were carried out to establish mean power consumption and worst-case time delay over all data combinations.

We ran SPECTRE simulations and used the parameters shown in table I for all transistors in the logic gates (i.e. W/L ratio of 2.5 for the DG-CNTFET, 3.5 for n-type CMOS transistors and 5.5 for p-type CMOS transistors). No resizing was carried out to balance branch resistances since this technique can be applied to all gates by using parallel transistors and has no impact from a comparative point of view.

Four different monotonic gates were simulated (XOR, XNOR, 2:1MUX, 4:1MUX) and results are shown in table II. Various performance metrics were evaluated: power consumption "P", time delay "TD", transistor count for each cell "# TRAN", the active area "AREA" (i.e. sum of all channel areas W*L) and Power-Delay-Product "PDP".

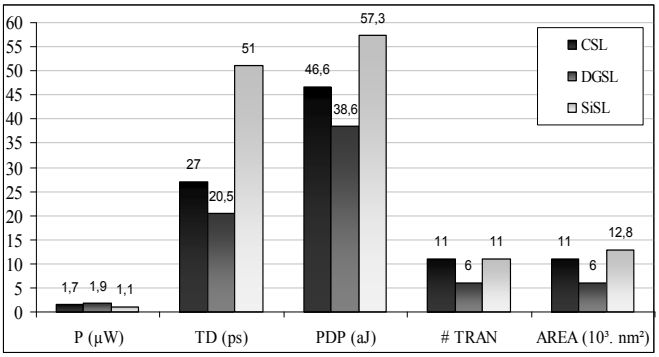


Figure 10. Comparison of average values of static logic gates

4.3 Discussion

Comparison figures show that the impact of the TTS association approach on different logic gates, proposed in this work, is almost identical.

Although fewer transistors are used, the average power consumption in this approach increases slightly (10%) compared to the conventional approach. This increase in power consumption is due to the shorter path from V_{dd} to ground that the new structures create. Since there are fewer transistors in series, the resistance per branch from (V_{dd}/G_{nd}) to output decreases to the channel resistance of a single transistor (R_{ch}) and results in a consequently higher short-circuit current during signal transition time. In the conventional structure, two transistors in series offer a path resistance of $2R_{ch}$. However this increase in current per transistor is not expected to be a reliability issue, since I_{on} in CNTFETs can attain a value 20–30X higher than that of state-of-the-art Si MOSFETs [21].

Compared with a conventional static logic structure (CSL), the new logic gates (DGSL) show an improvement in worst-case time delay of nearly 1.5X. This decrease in time delay is due to the use of fewer transistors in series, reducing the equivalent channel resistance and associated time constant with load capacitance accordingly.

One principle benefits provided by the approach is the important gain in terms of the number of transistors. While conventional static logic generally requires *2n* transistors (*n* representing fan-in), the new cells only require *2n-(m+p)* transistors (where *m* represents the number of NTTS structures and *p* represents the number of PTTS structures in the conventional gates). Table II shows clearly that for some gates only half of transistors are needed compared to conventional logic.

In this study, we also compare the power consumption and time delay of the DG-CNTFET logic gates to that of conventional Si-CMOS logic gates based on a low power (LP) 16nm predictive model. Simulations showed that CTN technology offer an improvement of 2X concerning the time delay but with an increase of power consumption of almost 2X over 16 nm silicon technology.

TABLE II COMPARISON OF CSL vs DGSL gates

	P (µW)			td(ps)			# tran			PDP (aJ)			Area (10^3. nm^2)		
	CSL	DGSL	SiSL	CSL	DGSL	SiSL	CSL	DGSL	SiSL	CSL	DGSL	SiSL	CSL	DGSL	SiSL
2XOR	2,3	2,5	1,3	21,0	16,0	40,0	8	4	8	48,3	40,0	52,0	8	4	9,3
2XNOR	2,3	2,5	1,4	21,0	16,0	36,7	8	4	8	48,3	40,0	51,4	8	4	9,3
MUX2:1	0,6	0,6	0,6	26,0	20,0	36,0	8	4	8	15,9	12,5	21,6	8	4	9,3
MUX4:1	1,7	1,9	1,2	40,0	30,0	91,0	20	12	20	68,0	57,0	109,2	20	12	23,4
Average	1,7	1,9	1,1	27,0	20,5	50,9	11	6	11	46,6	38,6	57,3	11	6	12,8

In fact, figures (8) and (9) illustrating the I_{DS}/V_{GS} characteristics of both model devices used for our simulations with an equal I_{on}, explain clearly the better speed and the worse power consumption of the DG CNTFET compared to the PTM 16nm. This is mainly due to the lower threshold voltage (V_{th}) of DGCNTFET compared to the PTM 16nm.

Performance is linked to I_{ds} which, in turn, is proportional to V_{th} $\{I_{ds} \propto (V_{DD} - V_{th})^{1\sim2}\}$. Power consumption (P) depends on static leakage current $I_{leakage}$, also dependent on V_{th} $\{I_{leakage} \propto e^{-C \times Vth}\}$ and P depends as well on Short-circuit current $\{ I_{SC} \propto (\beta.\tau_{in}/12.V_{DD}).(V_{DD}- 2.V_{th})^3.f \}$. However, the PDP of gates built with DG CNT technology remains better than Si technology. By applying the approach presented in this work, we achieve an improvement of ~30% as compared to Si gates using the PTM 16nm CMOS model.

Finally, it is worth mentioning that while this work is expressed through DG CNTFETs, the main specific FET device characteristic required is that of controllable (double-gate) ambipolarity. It is expected that the circuit techniques described in this paper are also valid using other devices with this property, such as double-gate transistors based on silicon nanowires [5] or potentially in the future on graphene.

5. CONCLUSION

We have described and evaluated an approach specifically exploiting the ambipolar property of DGFETs to reduce efficiently the transistor count for logic cells in complementary static logic, leading to a greater integration density (2x) by replacing all two n-type transistors in series in the pull-down network and all two p-type transistors in series in the pull-up network with a single DGFET for equivalent functionality. When deployed onto DG-CNTFET technology and for comparable average power consumption figures, the reduction in the on-channel resistance of the function path results in a reduced delay (up to 1.5X). Compared to silicon technology based on a 16 nm predictive model, DG-CNTFET technology shows better performance but worse power consumption with a 30% of improvement concerning PDP.

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