1. Description

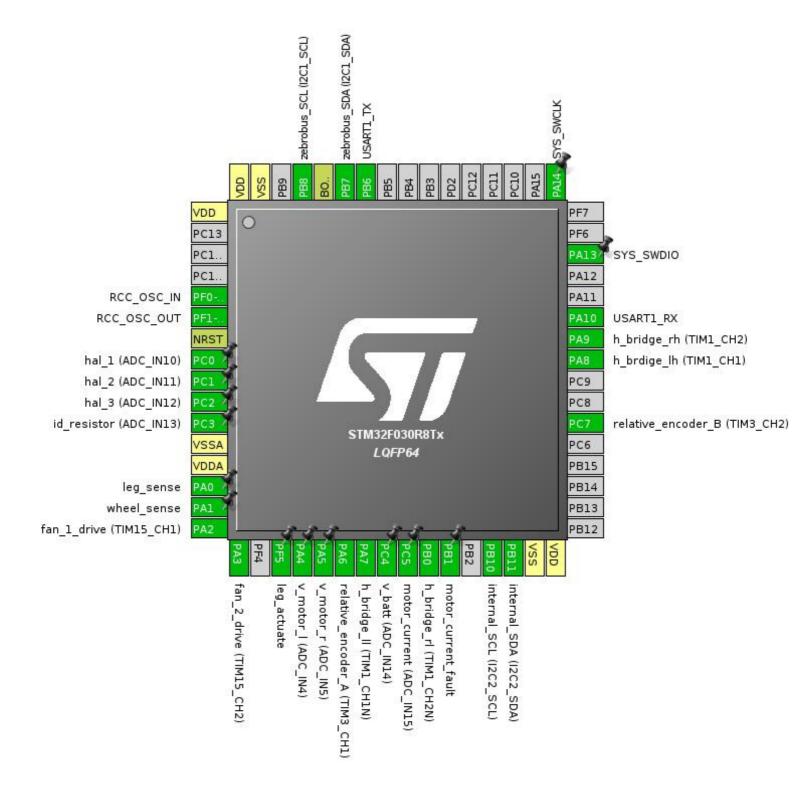
1.1. Project

Project Name	poot
Board Name	poot
Generated with:	STM32CubeMX 4.14.0
Date	05/20/2016

1.2. MCU

MCU Series	STM32F0
MCU Line	STM32F0x0 Value Line
MCU name	STM32F030R8Tx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



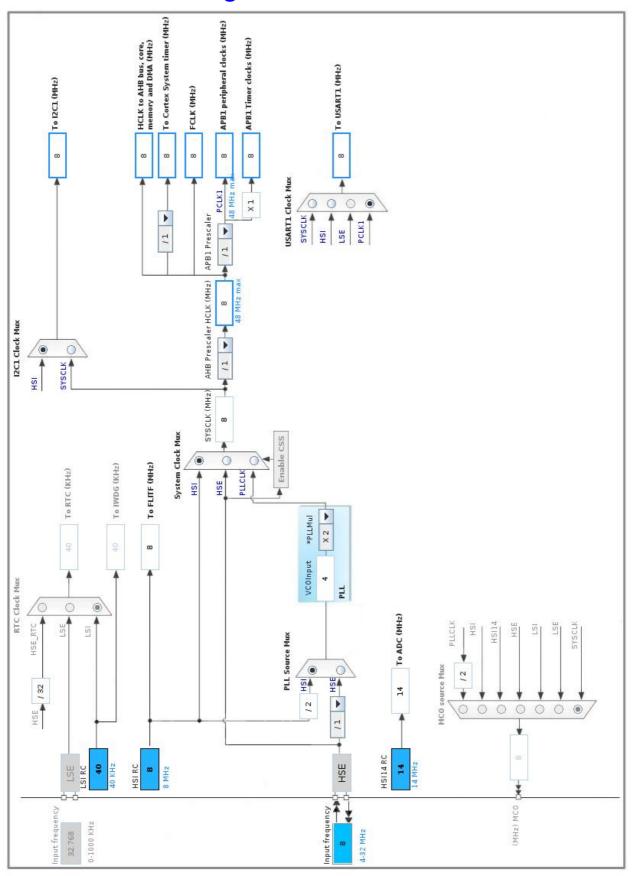
3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP64	(function after		Function(s)	
	reset)			
1	VDD	Power		
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	1/0	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC_IN10	hal_1 (ADC_IN10)
9	PC1	I/O	ADC_IN11	hal_2 (ADC_IN11)
10	PC2	I/O	ADC_IN12	hal_3 (ADC_IN12)
11	PC3	I/O	ADC_IN13	id_resistor (ADC_IN13)
12	VSSA	Power		,
13	VDDA	Power		
14	PA0 *	I/O	GPIO_Output	leg_sense
15	PA1 *	I/O	GPIO_Output	wheel_sense
16	PA2	I/O	TIM15_CH1	fan_1_drive (TIM15_CH1)
17	PA3	I/O	TIM15_CH2	fan_2_drive (TIM15_CH2)
19	PF5 *	I/O	GPIO_Input	leg_actuate
20	PA4	I/O	ADC_IN4	v_motor_l (ADC_lN4)
21	PA5	I/O	ADC_IN5	v_motor_r (ADC_IN5)
22	PA6	I/O	TIM3_CH1	relative_encoder_A (TIM3_CH1)
23	PA7	I/O	TIM1_CH1N	h_bridge_II (TIM1_CH1N)
24	PC4	I/O	ADC_IN14	v_batt (ADC_IN14)
25	PC5	I/O	ADC_IN15	motor_current (ADC_IN15)
26	PB0	I/O	TIM1_CH2N	h_bridge_rl (TIM1_CH2N)
27	PB1 *	I/O	GPIO_Input	motor_current_fault
29	PB10	I/O	I2C2_SCL	internal_SCL (I2C2_SCL)
30	PB11	I/O	I2C2_SDA	internal_SDA (I2C2_SDA)
31	VSS	Power		
32	VDD	Power		
38	PC7	I/O	TIM3_CH2	relative_encoder_B (TIM3_CH2)
41	PA8	I/O	TIM1_CH1	h_brdige_lh (TIM1_CH1)
42	PA9	I/O	TIM1_CH2	h_bridge_rh (TIM1_CH2)
43	PA10	I/O	USART1_RX	
46	PA13	I/O	SYS_SWDIO	
49	PA14	I/O	SYS_SWCLK	
58	PB6	I/O	USART1_TX	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
59	PB7	I/O	I2C1_SDA	zebrobus_SDA (I2C1_SDA)
60	воото	Boot		
61	PB8	I/O	I2C1_SCL	zebrobus_SCL (I2C1_SCL)
63	VSS	Power		
64	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC

mode: IN4 mode: IN5 mode: IN10 mode: IN11 mode: IN12 mode: IN13 mode: IN14 mode: IN15

5.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler Asynchronous clock mode
Resolution ADC 12-bit resolution
Data Alignment Right alignment

Scan Conversion Mode Forward

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled
Low Power Auto Power Off Disabled

ADC_Regular_ConversionMode:

Sampling Time 1.5 Cycles
External Trigger Conversion Edge None

WatchDog:

Enable Analog WatchDog Mode false

5.2. I2C1

12C: 12C

5.2.1. Parameter Settings:

Timing configuration:

I2C Speed Mode Standard Mode

I2C Speed Frequency (KHz)100Rise Time (ns)0Fall Time (ns)0Coefficient of Digital Filter0

Analog Filter Enabled
Timing 0x2000090E

Slave Features:

Clock No Stretch Mode Disabled
General Call Address Detection Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0

5.3. I2C2

mode: I2C

5.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode Standard Mode

I2C Speed Frequency (KHz)100Rise Time (ns)0Fall Time (ns)0Coefficient of Digital Filter0

Analog Filter Enabled
Timing 0x2000090E

Slave Features:

Clock No Stretch Mode Disabled
General Call Address Detection Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0

5.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Disabled
Prefetch Buffer Enabled
Data Cache Disabled

Flash Latency(WS) 0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSI14 Calibration Value 16

5.5. SYS

mode: Serial-WireDebug Timebase Source: SysTick

5.6. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1 CH1N Channel2: PWM Generation CH2 CH2N

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 0

Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0

Trigger Output (TRGO) Parameters:

Master/Slave Mode Disable (no sync between this TIM (Master) and its Slaves

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable

BRK Polarity High

Break And Dead Time management - Output Configuration:

Automatic Output State Disable

Off State Selection for Run Mode (OSSR) Disable

Off State Selection for Idle Mode (OSSI) Disable

Lock Configuration Off

Dead Time 0

PWM Generation Channel 1 and 1N:

Mode PWM mode 1

Pulse (16 bits value) 0

Fast Mode Disable
CH Polarity High
CHN Polarity High
CH Idle State Reset
CHN Idle State Reset

PWM Generation Channel 2 and 2N:

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High
CHN Polarity High

CH Idle State Reset
CHN Idle State Reset

5.7. TIM3

Clock Source: Internal Clock

Channel1: Input Capture direct mode Channel2: Input Capture direct mode

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 0

Internal Clock Division (CKD) No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode Disable (no sync between this TIM (Master) and its Slaves

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection Rising Edge
IC Selection Direct
Prescaler Division Ratio No division
Input Filter (4 bits value) 0

Input Capture Channel 2:

Polarity Selection Rising Edge
IC Selection Direct
Prescaler Division Ratio No division

Input Filter (4 bits value) 0

5.8. TIM15

mode: Clock Source

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 0

Internal Clock Division (CKD)

No Division

Repetition Counter (RCR - 8 bits value) 0

Trigger Output (TRGO) Parameters:

Master/Slave Mode Disable (no sync between this TIM (Master) and its Slaves

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable BRK Polarity High

Break And Dead Time management - Output Configuration:

Automatic Output State Disable

Off State Selection for Run Mode (OSSR) Disable

Off State Selection for Idle Mode (OSSI) Disable

Lock Configuration Off

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Fast Mode Disable

CH Polarity High
CH Idle State Reset

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High
CH Idle State Reset

5.9. **USART1**

Mode: Asynchronous

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate 38400

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Data Inversion Disable Disable TX and RX Pins Swapping Overrun Enable DMA on RX Error Enable MSB First Disable

* User modified value

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC	PC0	ADC_IN10	Analog mode	No pull-up and no pull-down	n/a	hal_1 (ADC_IN10)
	PC1	ADC_IN11	Analog mode	No pull-up and no pull-down	n/a	hal_2 (ADC_IN11)
	PC2	ADC_IN12	Analog mode	No pull-up and no pull-down	n/a	hal_3 (ADC_IN12)
	PC3	ADC_IN13	Analog mode	No pull-up and no pull-down	n/a	id_resistor (ADC_IN13)
	PA4	ADC_IN4	Analog mode	No pull-up and no pull-down	n/a	v_motor_l (ADC_IN4)
	PA5	ADC_IN5	Analog mode	No pull-up and no pull-down	n/a	v_motor_r (ADC_IN5)
	PC4	ADC_IN14	Analog mode	No pull-up and no pull-down	n/a	v_batt (ADC_IN14)
	PC5	ADC_IN15	Analog mode	No pull-up and no pull-down	n/a	motor_current (ADC_IN15)
I2C1	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	High *	zebrobus_SDA (I2C1_SDA)
	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	High *	zebrobus_SCL (I2C1_SCL)
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	High *	internal_SCL (I2C2_SCL)
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	High *	internal_SDA (I2C2_SDA)
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	
	PA14	SYS_SWCLK	n/a	n/a	n/a	
TIM1	PA7	TIM1_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	h_bridge_II (TIM1_CH1N)
	PB0	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	h_bridge_rl (TIM1_CH2N)
	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	h_brdige_lh (TIM1_CH1)
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	h_bridge_rh (TIM1_CH2)
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	relative_encoder_A (TIM3_CH1)
	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	relative_encoder_B (TIM3_CH2)
TIM15	PA2	TIM15_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	fan_1_drive (TIM15_CH1)
	PA3	TIM15_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	fan_2_drive (TIM15_CH2)
USART1	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	High *	
	PB6	USART1_TX	Alternate Function Push Pull	Pull-up	High *	
GPIO	PA0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	leg_sense
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	wheel_sense

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF5 PB1	GPIO_Input GPIO_Input	Input mode	No pull-up and no pull-down No pull-up and no pull-down	n/a n/a	leg_actuate motor_current_fault

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
System tick timer	true	0	0
Flash global interrupt		unused	
RCC global interrupt		unused	
ADC global interrupt	unused		
TIM1 break, update, trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt		unused	
TIM15 global interrupt	unused		
I2C1 global interrupt	unused		
I2C2 global interrupt	unused		
USART1 global interrupt	unused		

^{*} User modified value

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F0
Line	STM32F0x0 Value Line
MCU	STM32F030R8Tx
Datasheet	024849_Rev2

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	poot
Project Folder	/tmp/poot
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F0 V1.5.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	