NG-LARGE

NX1H140TSP

Preliminary Datasheet

Ver 1.0

Nov 2018

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1 Summary

Radiation Tolerance

- Radiation hardening by design in configuration memories and registers.
- SEL immune up to LET > 60MeV.cm^2/mg.
- Device Configuration SER < 1.70 10^{-4}/day (GEO)
- Total ionizing dose > 100Krads.
- Embedded EDAC for user memory mitigation.
- Embedded configuration memory scrubbing.
- Fast automatic memory configuration repair.
- Embedded bitstream integrity check (CMIC).

Main Features

- 65 nm STm C65-SPACE process technology.
- ARM Cortex R5 Processor as hard macro
- 4-Input Look-up tables.
- Lut expender to support up to 16 bits boolean functions.
- High performance carry chains.
- Advanced interconnect network to support random logic and coarse grain block functions.
- DSP Blocks for complex arithmetic operations.
- User memories with variable width and depth.
- Configuration modes: JTAG, Parallel 8 bits, Parallel 16 bits, Master Serial SPI, Space Wire.
- Integrated Space Wire interface available for user applications.
- Dedicated lowskew distribution network for clock, reset and load enable signals.
- On-chip thermal monitoring capability.

Input / Output Features

- Multiple I/O powering support from 1.5V to 3.3V
- Cold sparing support.
- Programmable output drive to support multiple industry standards.
- Embedded logic to support DDR2 and DDR3.
- 800 Mbps I/O support.
- LVDS compatible mode.
- All pins support 2000V of ESD-HBM.
- Embedded logic to support Space Wire Data Strobe encoding.
- Programmable delay lines on all pins.
- Programmable resistive termination.

2 Features

The NG-LARGE NX1H140TSP device is a Radiation Hardened By Design SRAM-based FPGA manufactured on STM C65 Space process with following resources.

2.1 Resources

Device	NG-LARGE
Capacity	
Equivalent System Gates	15 000 000
ASIC Gates	1 900 000
Modules	
Register	129 024
LUT-4	137 088
Carry	32 256
Embedded RAM	-
Core RAM Blocks (48K-bit)	192
Core RAM Bits (K = 1024)	9 216 K
Core Register File Blocks (64 x 16-bit)	672
Core Register File Bits	924 K
Embedded DSP	384
Clocks	32
Embedded Serial Link	
Hex 6 Gbps,SERDES Tx/rx	4
SpaceWire 400Mbps	1
I/Os	
I/O complex Banks	10
I/O simple Banks	14
User I/Os	700
FF-1152	674
LG / CG-1152	674
I/O PHYSICAL INTERFACES	-
DDR/DDR2	20
SpaceWire	20

2.2 Electrical Specifications

Symbol	Parameter	Value	Units
V_{core}	Nominal core voltage	1.2	V
VDDIO	Nominal I/O voltage	1.5 or 1.8 or 2.5 or 3.3	V
VDD2V5A	Nominal auxiliary analog voltage	2.5	V

2.3 Operating Conditions

Parameter	Value	Units
Temperature Range	-55 to +125	°C
Power Supply Tolerance	±10	$\%V_{cc}$

2.4 Radiation Performance

All resources are protected against radiation.

- Configuration Memory Cells are built with dedicated RH layout to guarantee a very low probability of soft-errors,
- User Register and DFF are also built with RH layout,
- Register files and Embedded Dual-Port RAM are protected with ECC.
- Clock tree has double redundancy
- Remaining critical logic blocks are triplicated.

Hereafter Orbital upset rates calculated with CREME96 (Solar min, 100mils shielding, 2µm sensitive volume thickness),

Total Ionizing Dose	100Krads Tested up to 300Krads
Heavy ions Latch Up susceptibility @ 125°C, 1.32V	LET > 60MeV.cm^2/mg
Configuration Memory SEU @ 25°C, 1.08V	GEO SER < 2.1 10^{-4}/day/device LEO SER < TBD
Embedded RAM + EDAC SEU/SET @ 25°C, 1.08V	GEO SER < 2,16 10^{-11}/day/bit LEO SER < 2,20 10^{-12}/day/bit
DFF SEU/SET @ 25°C, 1.08V	GEO SER < 1.80 10^{-9}/day LEO SER < 1.22 10^{-14}/day
Bitstream Management SEFI @ 25°C, 1.08V	GEO SER < TBD LEO SER < TBD

On top of that, even the SER's versus various orbits are very low, the bitstream is verified with an integrated scrubber controller named CMIC.

2.5 Configuration

The NG-LARGE are configured by loading the bitstream into internal configuration memory using one of these following modes:

- JTAG,
- Slave Parallel 8 bits,
- Slave Parallel 16 bits
- Slave SpaceWire, compliant ECSS-E-ST-50-12C link,
- Master SPI

The NG-LARGE NX1H140TSP bitstream size depends on the application size (configuration) and the number of user Core RAM and Core Register Files to be initialized.

2.6 Configuration Memory Integrity Check (CMIC)

The CMIC is an embedded engine performing automatic verification and repair of the configuration memory.

A CMIC reference memory is initialized during the bit stream download process with reference data computed by the NXmap software.

Once the initialization is done, the CMIC engine can be periodically activated to perform the following sequence:

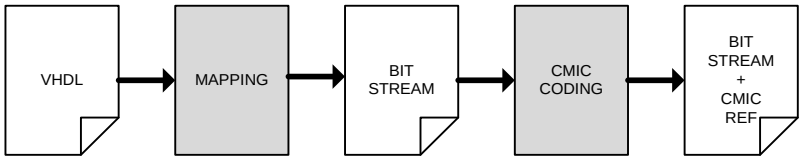
1. Read configuration data
2. Calculate signature
3. Compare the signature with CMIC reference
4. If a mismatch is detected:
    a. Calculate faulty address (BAD @) and faulty bit location
    b. Read DATA[BAD @]
    c. Repair flipped bit
    d. Write DATA[BAD @]

The CMIC period can be set by the user. The minimum period is 3.2 ms.

The CMIC reference memory is protected by ECC.

The CMIC does not need to access the external NVRAM when performing checks and repairs at run time. When a faulty bit is detected, the repair process is launched automatically and a notification signal is generated. This signal can be used by external means to manage this situation at system level.

CMIC Reference Generation



When the bit stream is downloaded from an external NVRAM, the bit stream data is sent to the configuration memory and the CMIC reference data is stored in special RAM protected with ECC.

3 Functional Description

3.1 Device Architecture

The NG-LARGE FPGA NX1H140TSP is based on NanoXplore patented interconnect architecture offering the highest logic density as well as high efficiency mapping. Application mapping is supported by NanoXplore tools based on proprietary algorithms tailored to the interconnect topology.

The device is composed of a central fabric embedding the programmable logic, RAM and DSP blocks, and peripheral I/O buffers. The fabric is covered with a grid of high level functional blocks interleaved with interconnect structures providing routing resources to realize the connections within the fabric and to the peripheral I/O buffers. The programmable logic resources are arranged in a hierarchical structure called a TILE with a specific local interconnect network. The I/O buffers are arranged into multiple banks. Each bank has its own I/O buffer supply voltage.

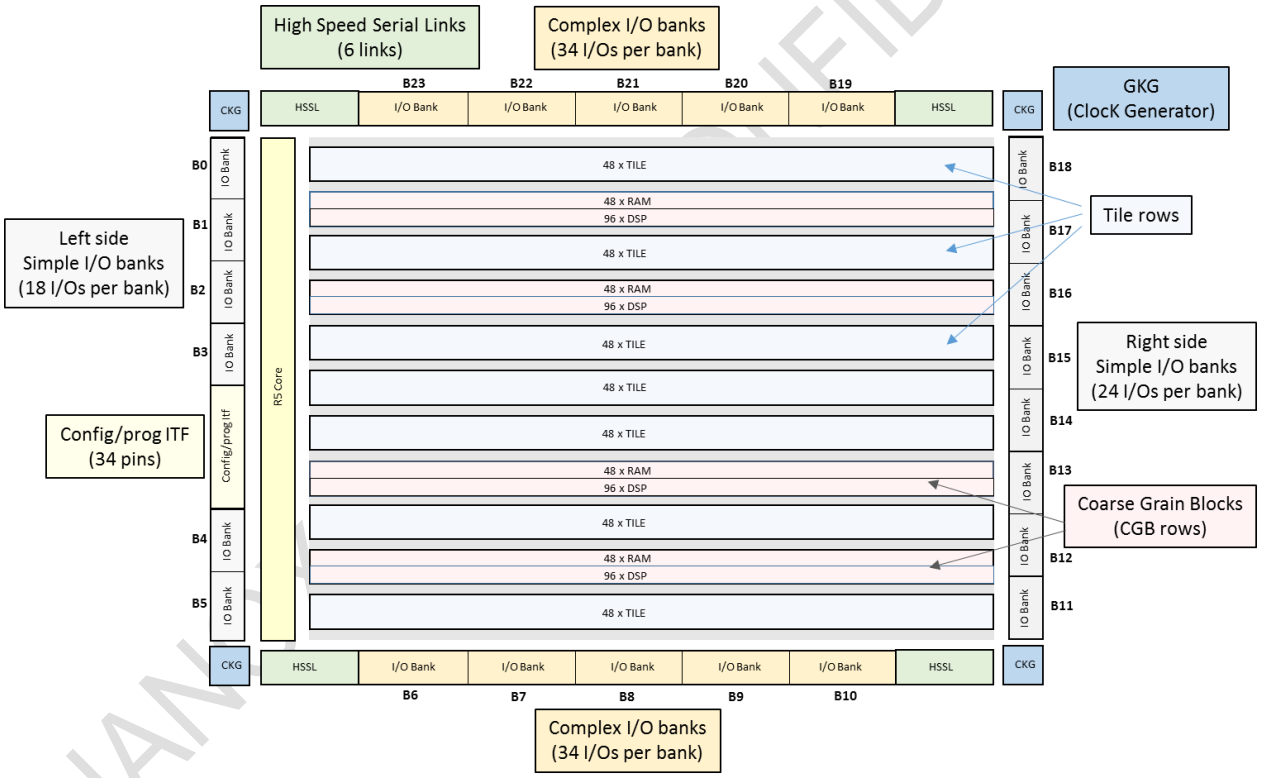


Figure 1: Device Floor Plan

NG-LARGE die features :

- **I/O Ring**
  - 6 “Left Simple” I/O Banks (18 I/Os per bank) B0 to B5
  - 8 “Right Simple” I/O Banks (24 I/Os per bank) B11 to B18

  - 10 “Complex” I/O Banks (34 I/Os per bank) B6 to B10 (bottom) and B19 to B23 (top)

- 4 HSSL blocks (High Speed Serial Link)
  - Each HSSL block includes 6 Multi Gigabit Transceivers

- 1 “Service” configuration bank Prog/interface (left side)

- **4 PLL** clock generators CKG0, CKG1, CKG2 and CKG3 (on each corner)

- **Array of 7 rows of 48 tiles (336 tiles total)**
  - 4-input LUTs : 384 x 7 x 48 = 129 024
  - Flip-flops : 129 024
  - Carry Logic bits : 32 256
  - X-LUT : 4 032
  - Register_File : 672

- **Array of 4 rows of 48 Coarse Grain Blocks (192 CGB)**
  - 48 Kbit True Dual Port RAM blocks per CGB : 192 RAM blocks
  - DSP blocks (2 per CGB) : 384 DSP blocks

- **ARM CORTEX R5 core**

3.2 Device Features

The NG-LARGE NX1H140TSP core logic offers general logic resources based on logic resources usage, and specialized direct resources used to efficiently chain DSP blocks in a same CGB row.

3.2.1 TILE

Each tile includes Functional Elements (FE) and additional complementary logic such as arithmetic logic, X-LUT and Register_File.

Common FE features :

Four inputs and one output truth table • implements any 1 to 4-input Boolean function
Optional register on output • 1 bit edge sensitive flip-flop (DFF) • Programmable synchronous / asynchronous reset • Programmable positive / negative clock edge • Programmable Load enable
DFF Initialization by bit stream

The random logic is implemented with 4-input look up tables (LUT). The LUT output signal can be optionally stored in a register. The terminals I1, I2, I3, I4, and OUT are connected to the TILE interconnect network. The inputs RST, LE and CLK are connected to the TILE low skew network.

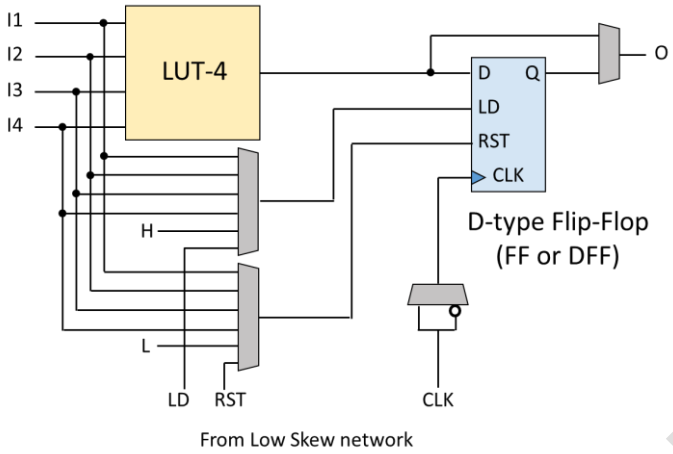


Figure 2: LUT and DFF (FE)

Tile logic resources :

384 LUT	4 stripes of 4 rows each x 24 columns
384 DFF	
96 Carry Logic	2 rows of 4-bit x 12 columns (stripes 1 & 2)
24 X-LUT	One row of 24 x X-LUT (stripe 3)
2 Register File 64 x 16-bit each + 2 CDC (Clock Domain Changer)	One row of two Register_File (stripe 4)

Tile FEs and additional logic distribution : Each tile includes an array of 24 columns of 16 FEs (total 384 FEs) + additional logic, organized in 4 stripes of 24 columns of 4 FEs.

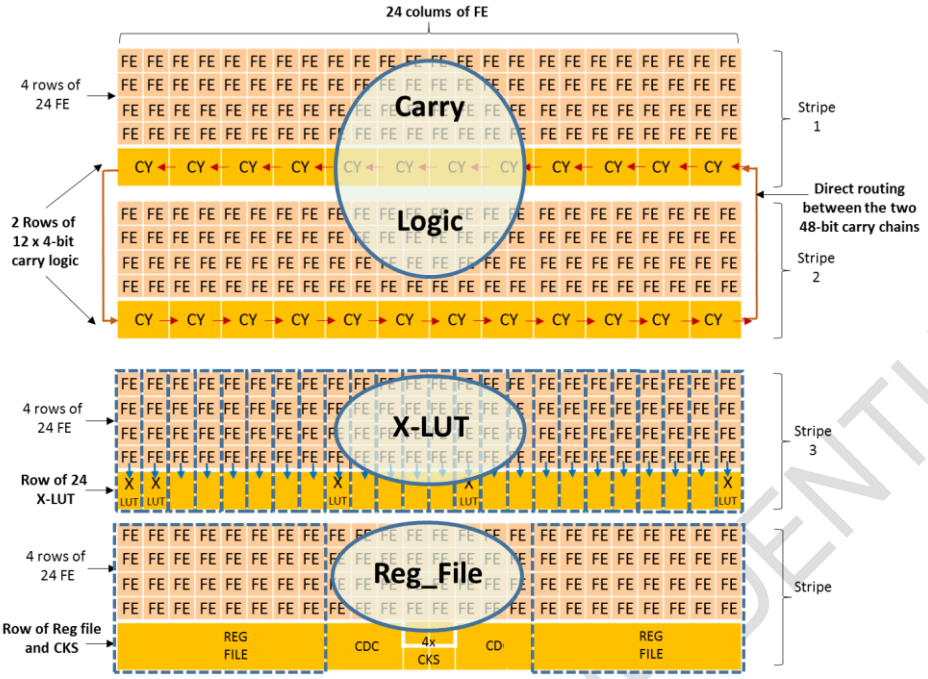


Figure 3: Tile distribution

3.2.1.1 Carry Logic

Arithmetic operators requiring a carry propagation can be implemented with a hard wired carry logic. In order to accelerate the carry propagation through wide operators, a 4-bits carry look ahead circuit is added in the carry propagation path. Versatile arithmetic operators can be implemented by combining the carry logic with LUT and DFF.

Carry Logic features :

Combines one LUT with carry propagation logic
Fast 4 bits carry look ahead acceleration
Up to 96-bit chain (can be split at any 4-bit boundary)

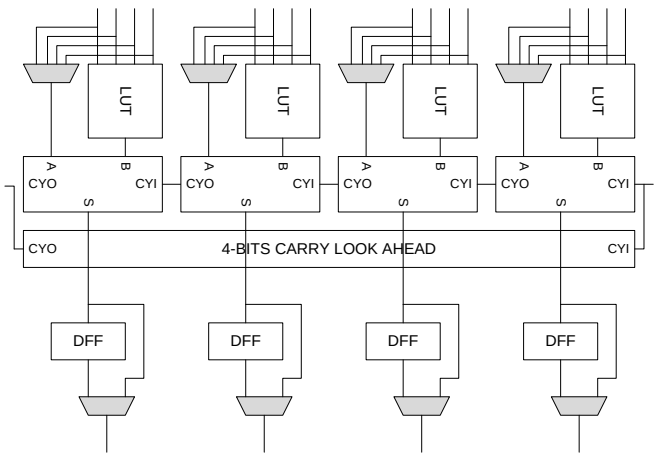


Figure 4: Carry Chain Diagram

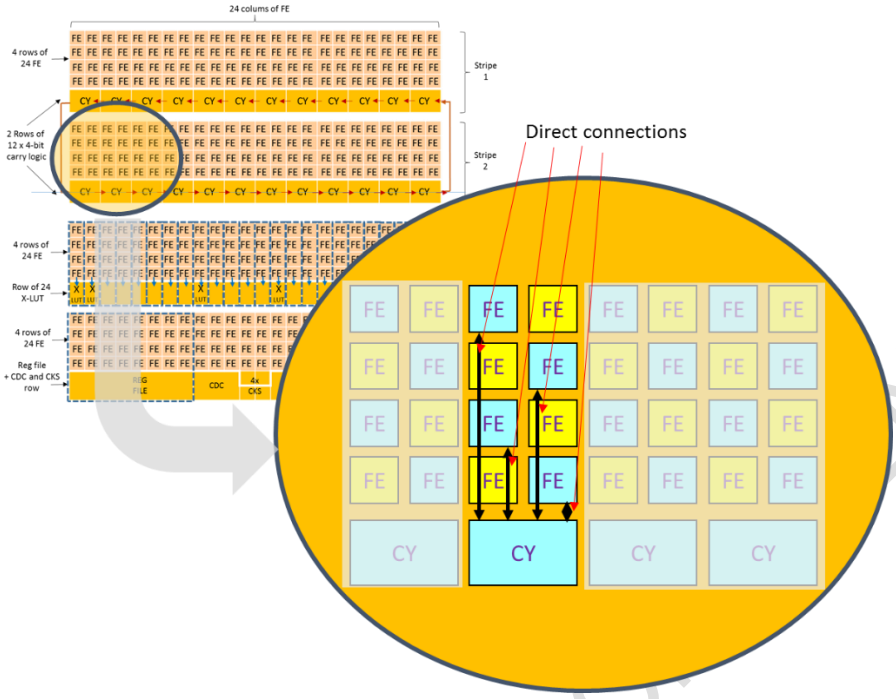


Figure 5: FE and carry logic

3.2.1.2 X-LUT (extension LUT in stripe 3)

To support wide boolean equations, a group of four LUT can provide four inputs directly to a fifth X-LUT without routing through the interconnect network. One TILE contains 384 LUT and 24 X-LUT.

X-LUT features :

Four inputs and one output truth table • Implements any 1 to 4-inputs Boolean function
X-LUT Configuration • Allow to implement up to 16-input Boolean function
Optional register on output • 1 bit edge sensitive flip-flop (DFF) • Programmable synchronous / asynchronous reset • Programmable positive / negative clock edge • Programmable Load enable
DFF optionally initialized by bit stream

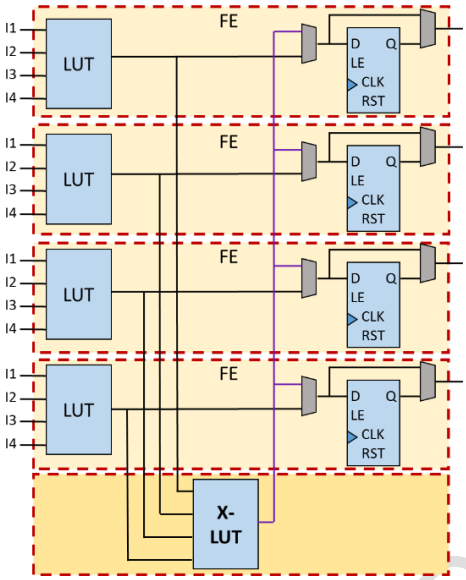


Figure 6: FE with X-LUT

The stripe 4 of each tile includes two Simple Dual Port 64 x 16-bit elements as well as two CDCs (Clock Domain Changer). The CDC can be used for FIFO implementation with the Register_file to swap respectively the read and write pointers to the write and read clocks.

Small memory blocks can be implemented with a 64 x 16-bit register file array. It is inserted between the LUT and DFF. The DFF can be bypassed or used as an optional output pipe line register. The clock inputs are connected to the TILE low skew network.

A hardware SECDED EDAC function generates the ECC bits on the input port and performs error correction and detection on the output port. The EDAC bits are stored in extra memory bits which are not accessible to the user application.

Register File and CDC features

Register_file : Synchronous Simple Dual Port SRAM
64 x 16-bit words
One synchronous read only port
One synchronous write only port
Optional pipe-line output register
Programmable positive / negative clock edge
Initialization by bitstream
Embedded SECDED EDAC
CDC : dual 6-bit Clock Domain Changer for FIFO pointers

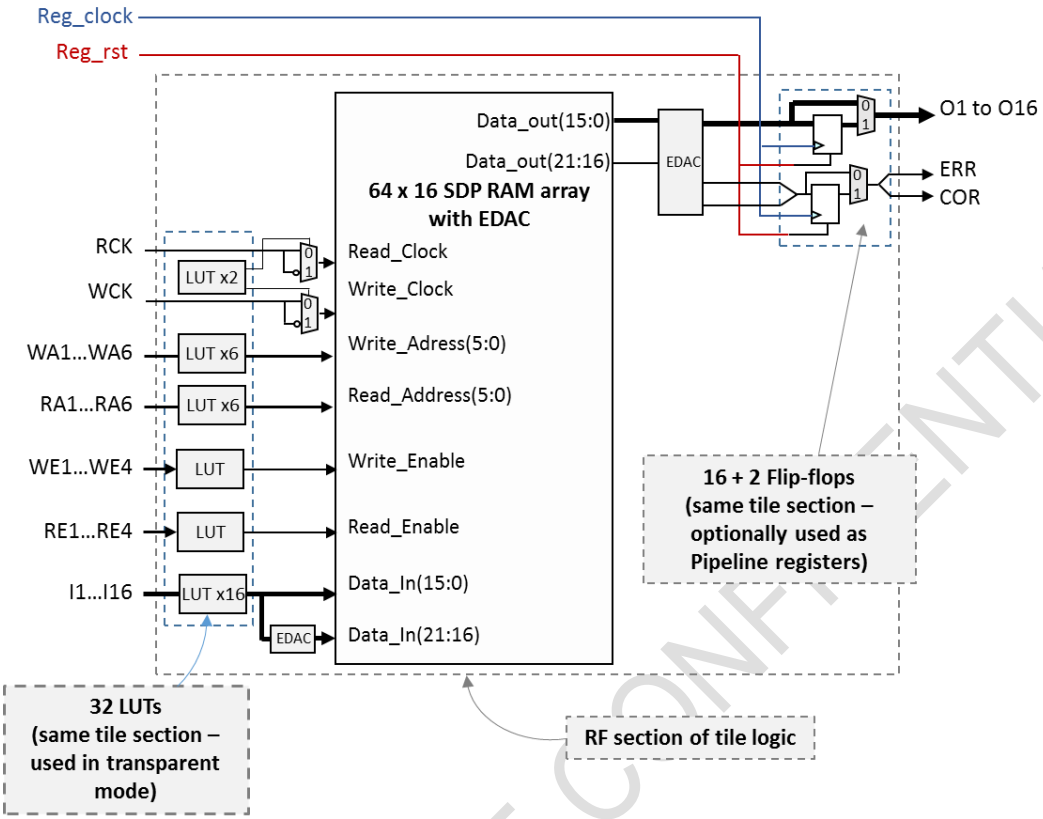


Figure 7: Register_file simplified block diagram

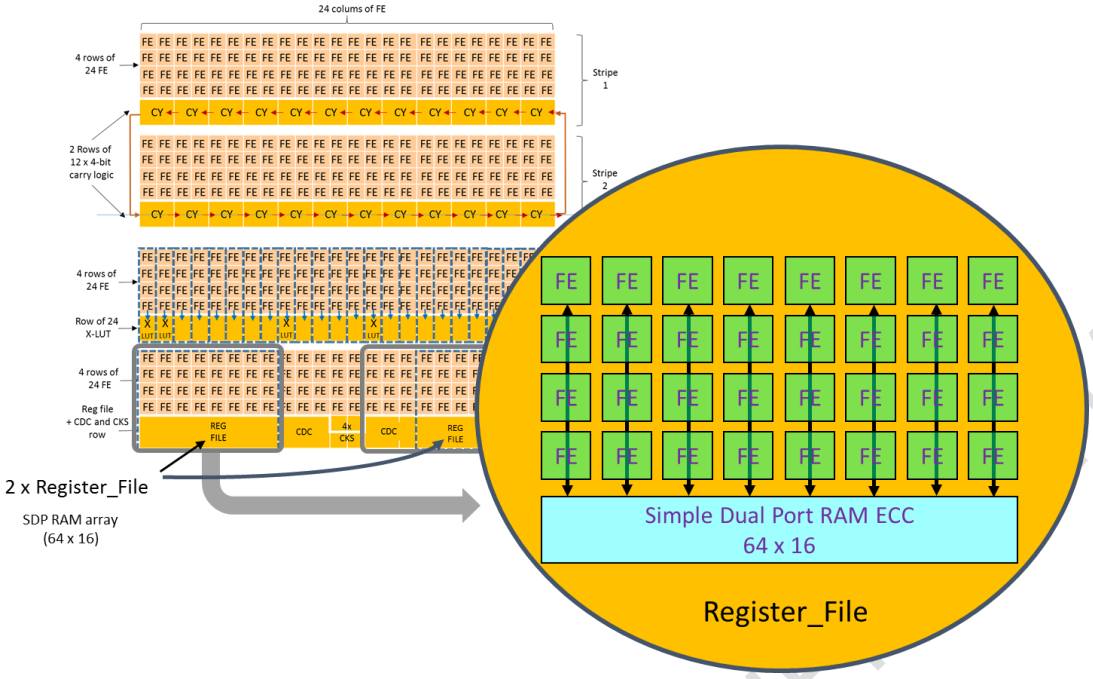


Figure 8: FEs with Register_file

3.2.2 Memory

The memory block is a true dual-port synchronous 48K-bits SRAM. The memory is configurable and supports various modes of operation. Each port can perform a read or write operation. The data can be protected by a hardware SECDED EDAC. This EDAC function can be bypassed. The ECC signature is computed during the write cycle and checked during the read cycle.

An optional feature is the Read Repair mode. When this mode is enabled and a correctable error is detected during the read cycle, then the memory array is updated with the corrected data/ECC value.

In addition NG-LARGE provides an embedded scrubbing able to automatically repair the block RAM contents even while no read is performed.

With EDAC: • 2048 x 1-bit • 2048 x 2-bits • 2048 x 6-bits • 2048 x 9-bits • 2048 x 18-bits
Without EDAC: • 49152 x 1-bit • 24576 x 2-bits • 12288 x 4-bits • 6144 x 8-bits • 1024 x 12-bits

• 2048 × 24-bits
Programmable positive / negative clock edge
Optional pipe-line output register
Initialization by bit stream
Embedded EDAC
Automatic repair mode

Table 1: RAM block features

Read Cycle:

When the memory is enabled in a memory read cycle (CSx = 1 and WEx = 0), the address is stored on the rising memory clock (CLKMEMx) edge, and data appears at the output bus after the access time. The chronogram is shown on the next figure. The optional output pipeline registers are available in all memory configurations. These registers are clocked by CLKREGx signals, which may be different from the main memory clock signals CLKMEMx. The memory pipeline register may be forced to zero by asserting the synchronous RSTx signal. Both memory clocks and register clocks may have individually configured polarity. The presence of output pipeline registers is determined independently for each port.

Write Cycle:

When the memory is enabled in a memory write cycle (ENBx = 1 and WEx = 1), the address is stored and data is written to the memory on the rising edge of the memory clock (CLKMEMx). During a write access DOUT maintains the output previously generated by a read operation.

Note: Simultaneous write by both ports of a same memory location or simultaneous read/write are not allowed.

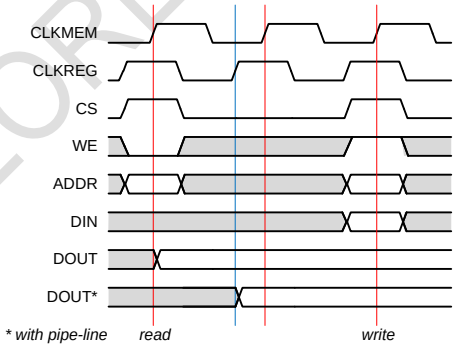


Figure 9: RAM block timing diagram

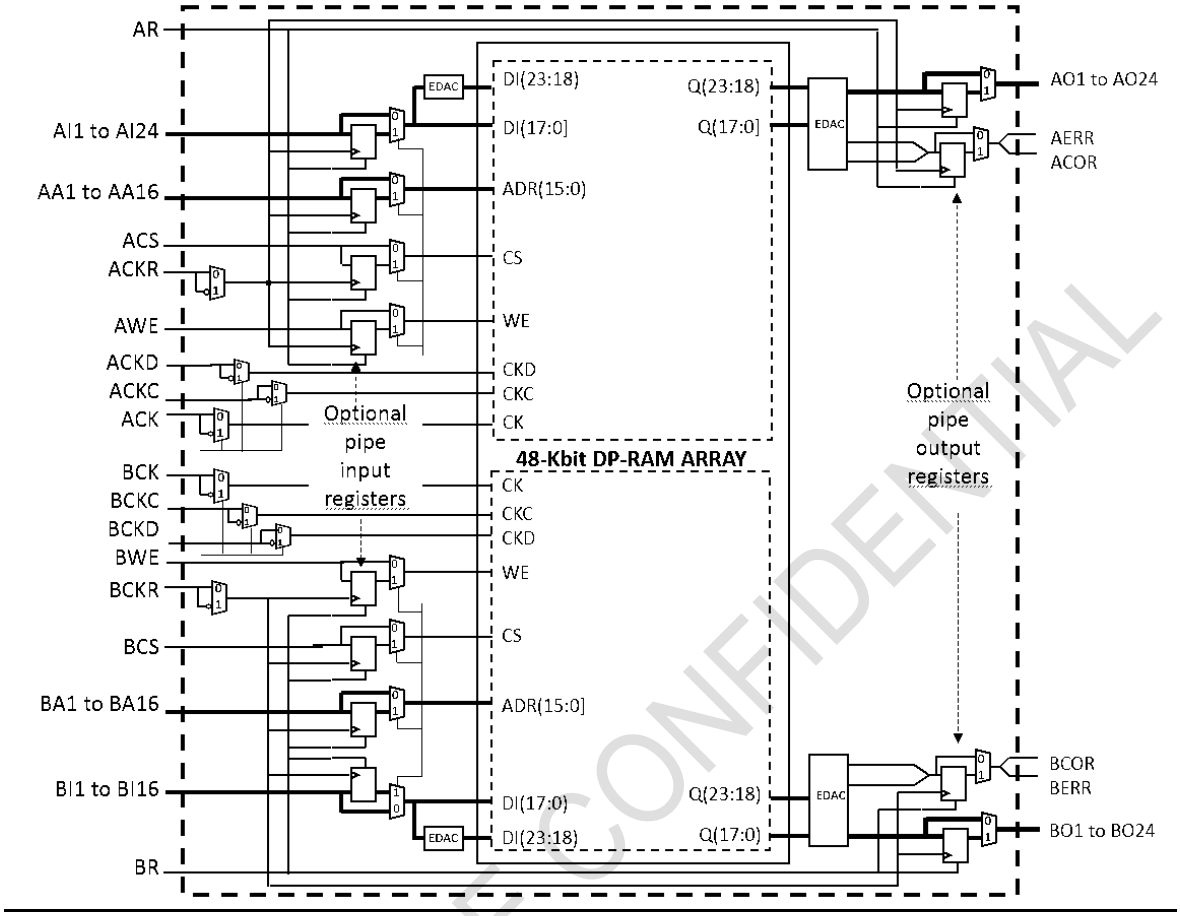


Figure 10: RAM block simplified diagram

3.2.3 DSP

The DSP can implement arithmetic computations such as multiply, multiply-add or subtract, multiply-accumulate, and arithmetic wire shift for higher precision calculation. The ability to cascade multiple DSP allows for users to achieve high performance algorithms such as FIR with a minimum of fabric resource usage.

A single DSP has a 19×24 multiplier, a 56-bit arithmetic unit (ALU), an 18-bit pre adder (ADD) and several pipeline registers (PR). Two adjacent DSP can be combined to support 24 x 24 multiplications. The DSP can be configured to operate in unsigned or signed mode. When in signed mode, all operands format is two's complement format.

19x24 signed / unsigned multiplier
56-bit arithmetic and logic unit
18-bit pre adder (19-bit result)
Programmable Pipeline stages

Possibility to cascade up to 96 DSP blocks
Support for Higher order 24x30 multiply
Signed (two's complement) or unsigned mode
Among Single DSP operations: • 18 x 24-bit Multiplication: Z[35:0] = A[23:0] x B[17:0] • 18 x 24-bit Multiplication and Addition: Z[55:0] = A[23:0] x B[17:0] + CZI[55:0] • 18 x 24-bit Multiplication and 56-bit Accumulation: Z[55:0] = (A[23:0] x B[17:0]) + CZO • 18-bit Pre-adder, Multiplication and 56-bit adder Multiplication and Addition with Pre-adder: Z[55:0] = A[23:0] * (B[17:0] + D[17:0]) + CZI[55:0] •
Among Multi DSP operations at full speed (~300 MHz) • 24 x 34-bit Multiplication (2 DSP blocks) Z[53:0] = A[23:0] * B[29:0] • 18 x 18-bit complex multiplier (4 DSP blocks) • Parallel N-tap FIR filter – non symmetric : N x DSP block • Parallel N-tap FIR filter – symmetric : N/2 DSP blocks

Table 2: DSP block features

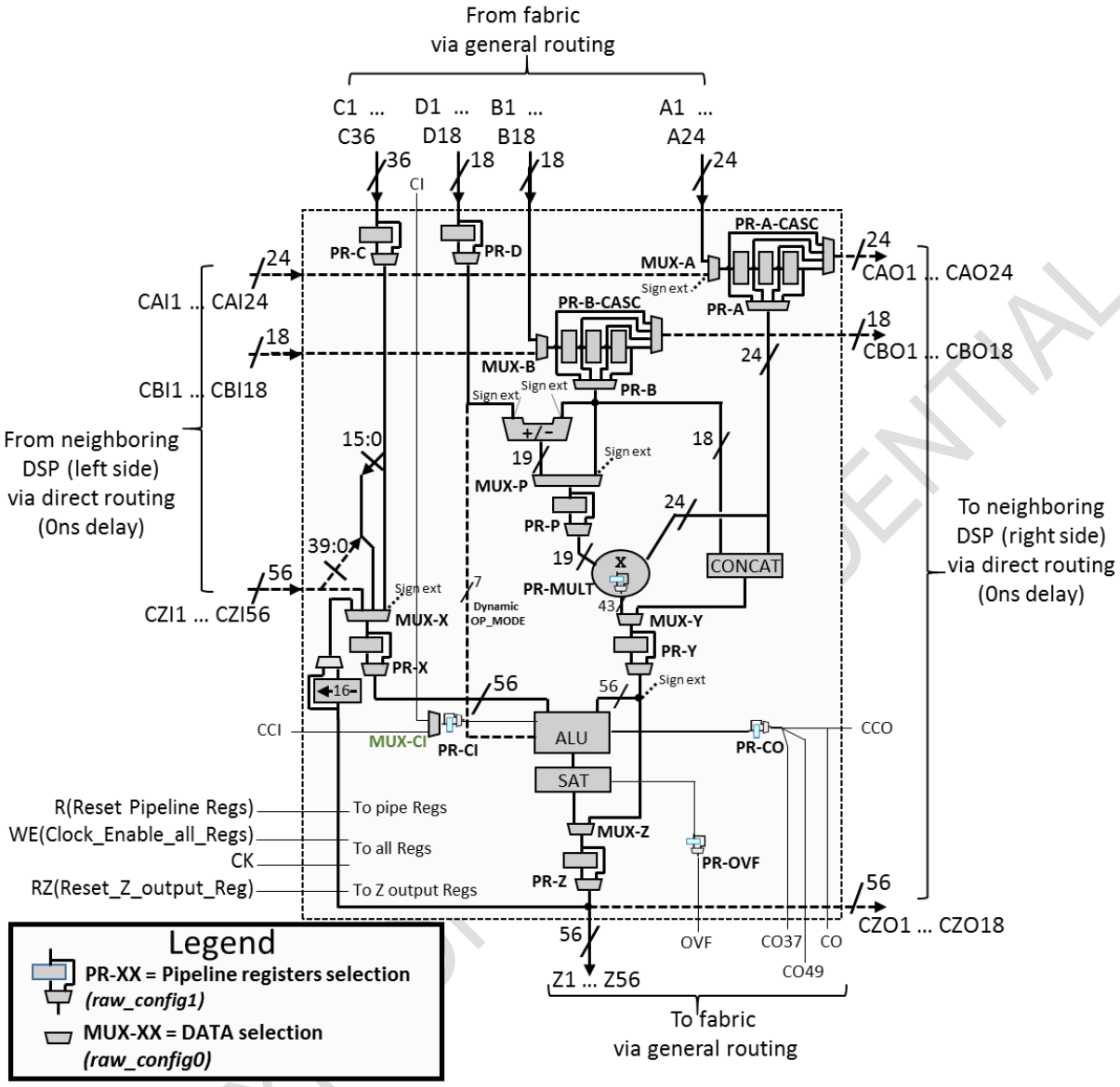


Figure 11: DSP block simplified diagram

3.2.4 I/O Buffers

The I/O buffer (IOB) provides input, output, and bidirectional interfaces. Each IOB can be configured to meet various voltage, current, and impedance configurations and supports cold sparing. The input and output path logic can be configured to provide various data and clocking interfaces with the fabric. Two adjacent IOB can be paired to form a differential buffer. A programmable resistor network provides on-chip termination connected to an external voltage VTO, or a differential resistive termination between two paired IOBs.

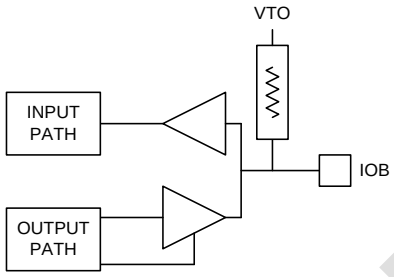


Figure 12: Single Ended IOB

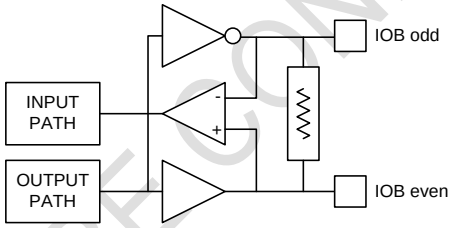


Figure 13: Differential IOB Pair

NX1H140TSP user I/Os are assembled in pairs P/N. Each pair may be used as either a true differential signal or two unipolar signals.

NX1H140TSP devices I/O banks support I/O standards as listed in Table 3.

Standard	Type	Supply	Drive	Turbo	Speed MHz or Mb/s	Special considerations	Notes
LVCMOS 3.3V	SE	3.3 V	2–16 mA	No	100MHz		
LVCMOS 2.5V	SE	2.5 V	2–16 mA	Yes/No	300MHz		
LVCMOS 1.8V	SE	1.8 V	2–16 mA	Yes/No	300Mb/s		
LVCMOS 1.5V	SE	1.5 V	2–16 mA	Yes/No	300MHz		
SSTL 2.5V – I/II	SE	2.5 V	8 mA / 16 mA	Yes/No	600Mb/s	Controlled Source Impedance	DDR
SSTL 1.8V – I/II	SE	1.8V	8.6 / 13.4 mA	Yes/No	800Mb/s	Controlled Source Impedance	DDR
HSTL 1.8V – I/II	SE	1.8 V	8 / 16 mA	Yes	800Mb/s	Controlled Source Impedance	DDR

Standard	Type	Supply	Drive	Turbo	Speed MHz or Mb/s	Special considerations	Notes
HSTL 1.8V – I/II	SE	1.8 V	8 / 16 mA	No	400Mb/s	Controlled Source Impedance	DDR
HSTL 1.5V – I/II	SE	1.5 V	8 / 16mA	Yes	800Mb/s	Controlled Source Impedance	DDR
HSTL 1.5V – I/II	SE	1.5 V	8 / 16mA	No	400Mb/s	Controlled Source Impedance	DDR
LVDS 2.5V	DIF	2.5 V	3.5mA		800Mb/s		DDR

Table 3: IO Buffer Standard List

Each buffer has programmable delay lines on their input and output paths and can be combined with a register, shift registers and a CDC function to provide various types of data interface and clocking modes with the FABRIC. The following schematics illustrate the output, input and termination interfaces. The programmable delay line is used to align incoming or outgoing data with the external clocking environment and can be bypassed.

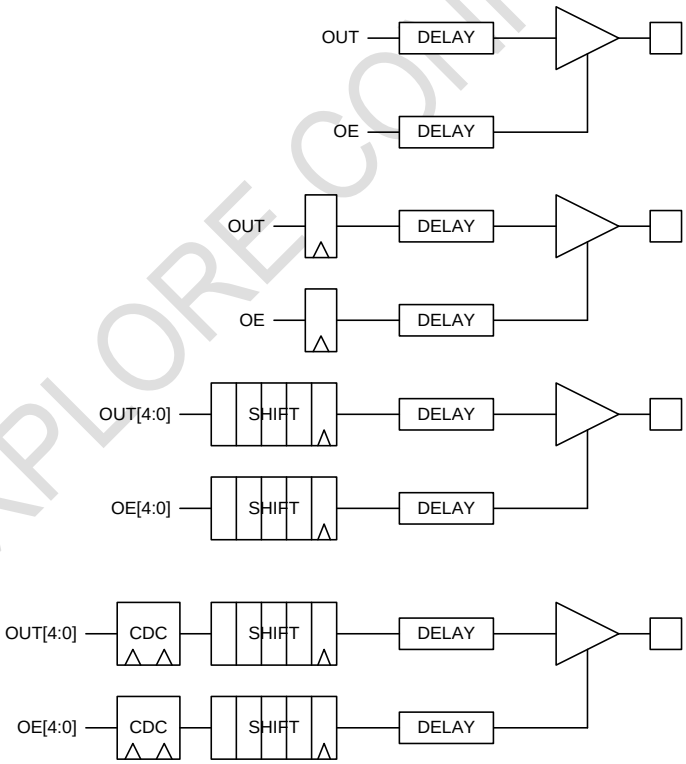


Figure 14: Output Path

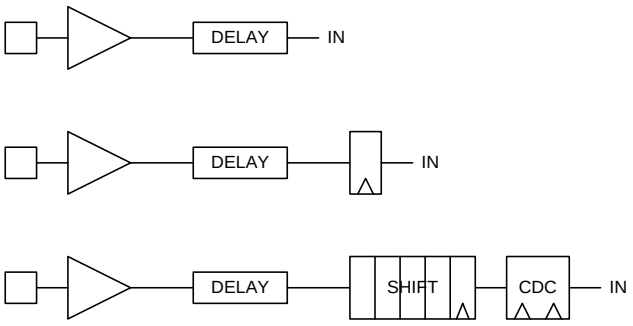


Figure 15: Input Path

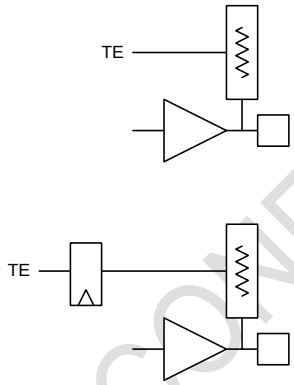


Figure 16: Termination Path

Programmable strength
Supports multiple voltage levels (1.5V – 3.3V)
Single ended operation
Differential operation
Programmable slew rate
Programmable pre-emphasis
Programmable resistive termination
External termination voltage
Programmable input level
Programmable input delay line
Programmable output delay line
Termination-enable control
Input register
Output register
Output-enable register
Termination-enable register

Table 4: IO Buffer Features

3.2.4.1 On-chip resistive termination

The programmable on-chip resistive termination network is controlled through 4-bits control signal. This 4-bit value is assigned to the IOs within a NXpython script file for each IO requiring

internal input impedance adaptation. Those parameters can be also assigned in the HDL source code by instantiating the I/O primitives.

It can be used for both single-ended and differential input/output signals. **Erreur ! Source du renvoi introuvable.** presents minimum and maximum resistance values at given VDDIO voltage when on-chip termination is activated.

In single-ended mode, the VTO pads of the IO banks using internal impedance adaptation must be connected to an external VTO voltage. VTO must be nominally set at VDDIO/2 and can be adjusted according to the range listed Table 5.

In differential termination mode, or if termination resistors are not used, VTO pads may be left unconnected.

Notes: Rtmin and Rtmax values cover ±10% variations on VDDIO, VTO and VDD2V5 supply voltages, process corners, -40 to 125C° temperature variations. Non-silicided poly resistance variations defined by foundry design rules are not taken into consideration.

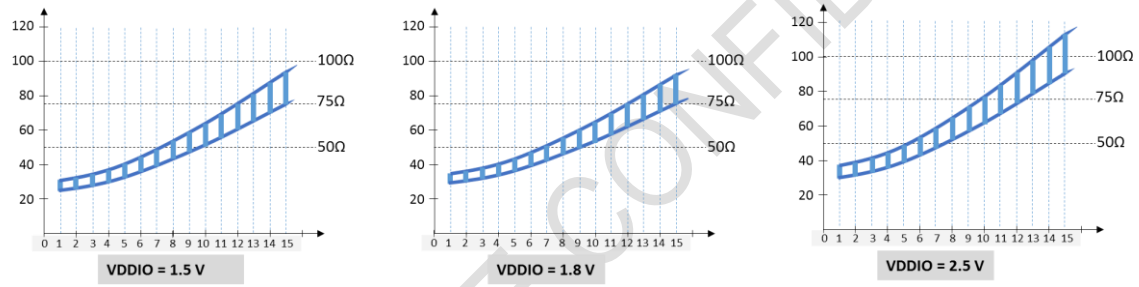


Figure 17: Impedance adaptation resistor values

VDDIO	VTO nom
1.5 V	0.75 V +/-5%
1.8 V	0.9 V +/-5%
2.5 V	1.25 V +/-5%

Table 5: VTO range vs VDDIO

For VDDIO 1.5 V and 1.8 V, on-chip termination can be activated for all pads in a given bank. In case of VDDIO 2.5 V, on-chip termination can be activated on maximum 11 due to the limitation on power supply rails.

3.2.4.2 Delay line

The delay lines are PVT compensated. Through calibration, maximum reachable delay is approximately between 7.3ns and 20 ns, where delay step of the 64-bits delay line varies approximately between 110ps and 310ps.
However, NXmap sets the delay steps to 159 ps.

The delay lines are PVT compensated and provide a programmable delay range from 0.34 ns to 10.34ns with 63 steps of 159ps. The delay line can be bypassed.

3.2.4.3 Weak Termination

By default, each I/O pad has a 10 KΩ to 40 KΩ pull-up. In addition each user's I/Os can optionally have an additional 2KΩ to 6KΩ pullup. No pull-down or keeper is available on NG-MEDIUM I/Os.

3.2.4.4 Pre-Emphasis and Slew-rate control

Edge boost (pre-emphasis) mode can accelerate rising and falling edges up to 25% while stepped activation (slew control) mode can slow down by up to 40 % (Test case: half drive strength, 100MHz output, 6pf of load). It has to be noted that these numbers depend strongly on the chosen drive strength and the driven load. In NXmap software, the user can set the output buffer to : "slow", "medium" or "fast".

3.2.5 IO Banks

An I/O Bank is composed of several IOB and supply pins forming a homogeneous structure sharing:

- A same IO power supply VDDIO
- A same resistive termination supply VTO

The following is a summary of the I/O features in the complex and simple banks

I/O Features	Complex banks	Simple banks
Number of I/O Pads	30	30/22
Resistive termination	Yes	No
Differential	Yes	No
Delay line	Yes	Yes
Single DFF	Yes	Yes
CDC	Yes	No
Shift register	Yes	No
DDR	Yes	No
SpaceWire	Yes	No

Table 6: Simple and complex banks I/O features

Simple I/O Banks present differential pairs allowing I/O supplies of 1.5V, 1.8V, 2.5V or 3.3V;

Complex I/O Banks present 17 differential pairs, allow the same I/O supplies of 1.5V, 1.8V, 2.5V or 3.3V, and offer additional features:

- DDR2 interface capability
- Controlled impedance termination capabilities
- SpaceWire interface capability

3.2.5.1 DDR Support

11 IOB can be combined to form a physical DDR (Figure 18) with 9 DQ (8 data, 1 data mask) and 2 DQS (differential strobe). The DDR INTERFACE will do data and clock alignment, and data serialization.

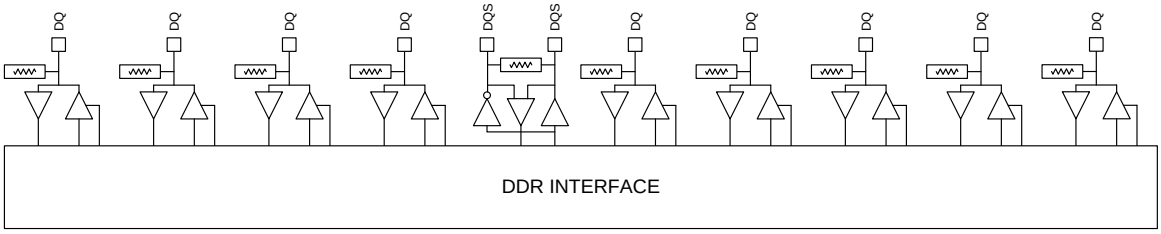


Figure 18: DDR Physical Interface

3.2.5.2 Space-Wire Support

4 IOB and dedicated Tx and Rx modules can be combined to implement a physical media access layer of a Space Wire interface (Figure 19).

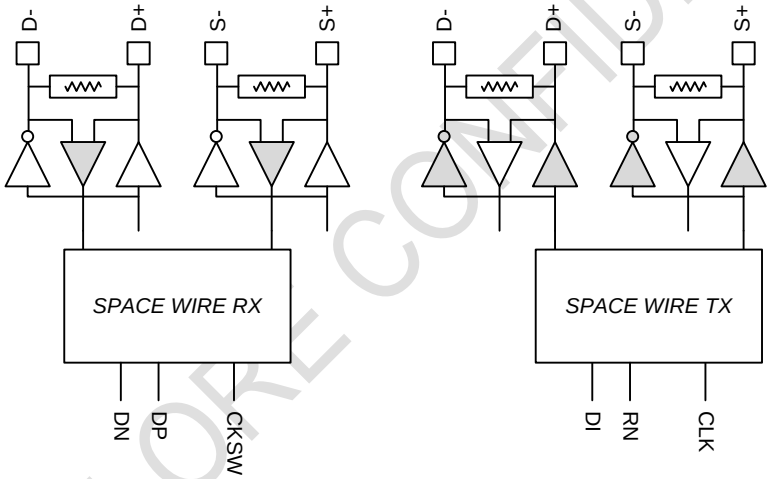


Figure 19: Space Wire Physical Interface

The SpaceWire Tx module receives the transmit clock (CLK), a reset input (RN) and the serial data input (DI) and generates the Data Strobe LVDS outputs. The Rx module receives the Data Strobe LVDS inputs and generates the data clock (CKSW) the positive edge data (DP) and the negative edge data (DN). The Tx and Rx chronograms are illustrated in the next figures.

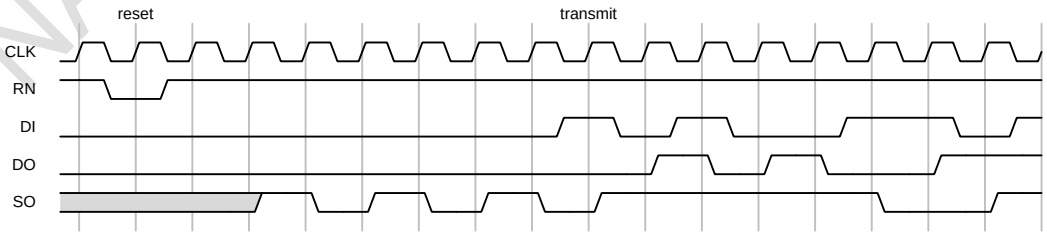


Figure 20: Space Wire Tx Chronogram

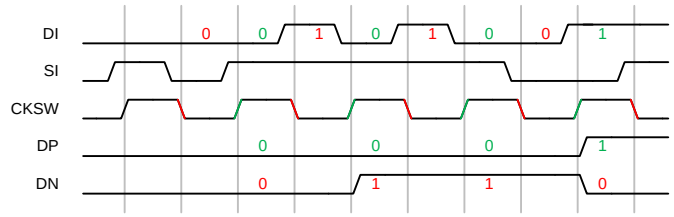


Figure 21: SpaceWire Rx Chronogram

3.2.6 High Speed Serial Links (HSSL)

The HSSL block provides multi-protocol high-speed serial link capability with multi-rate support. The next figure illustrates the block diagram of the HSSL block, which is composed of 6 RX/TX lanes, a PLL, and a calibration circuit. Each transceiver lane includes the PMA and PCS hard macros. The SERDES block has configurable features such as data width (up to 80 bits in parallel), equalization and protocol dependent properties.

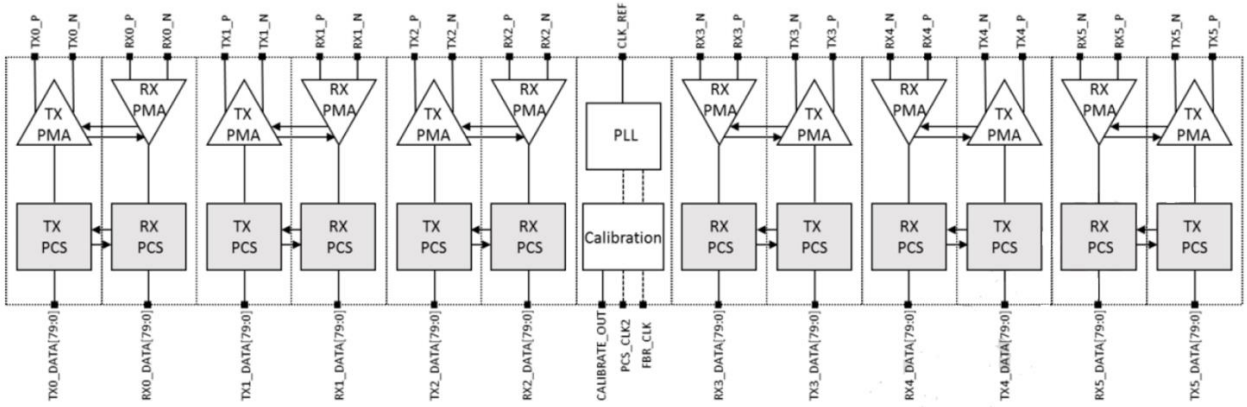


Figure 22: 6-channel HSSL block diagram

The HSSL supports the following protocols:

Protocol	Type	Encoding
ESistream	3.125(1)-6.25 Gbps	14b/16b
Serial RapidIO	3.125(1)-6.25 Gbps	8b/10b
JESD204B	3.125(1)-6.25 Gbps	8b/10b
SpaceFibre	3.125(1)-6.25 Gbps	8b/10b
Other protocols can be supported		

(1) Lower bitrate are possible when oversampling modes are activated

Table 7: HSSL supported protocols

HSSL features summary:

0.781 – 6.25 Gbps data rate
Half rate TX/RX
20/32/40/64/80-bit parallel interface (2, 4 or 8-word itf)
Per link multi-are Clock and Data Recovery (CDR)
Programmable CTLE equalization
Programmable 50 Ohms on-chip termination
Serial/Parallel TX-RX loopback test
SST-based output drivers
3-tap programmable pre-emphasis (1 pre, 1 main, 1 post)
Programmable driver output voltage level
Multi-protocol compatible
Bypassable PCS features
Oversampling modes: ½ and ¼ rate
Differential operation
Polarity selection
Receiver Elastic Buffer
Per lane power-down capability

Table 8: HSSL features summary

The next figure shows the simplified internal block diagram of a transmitter and receiver channel, PLL and calibration.

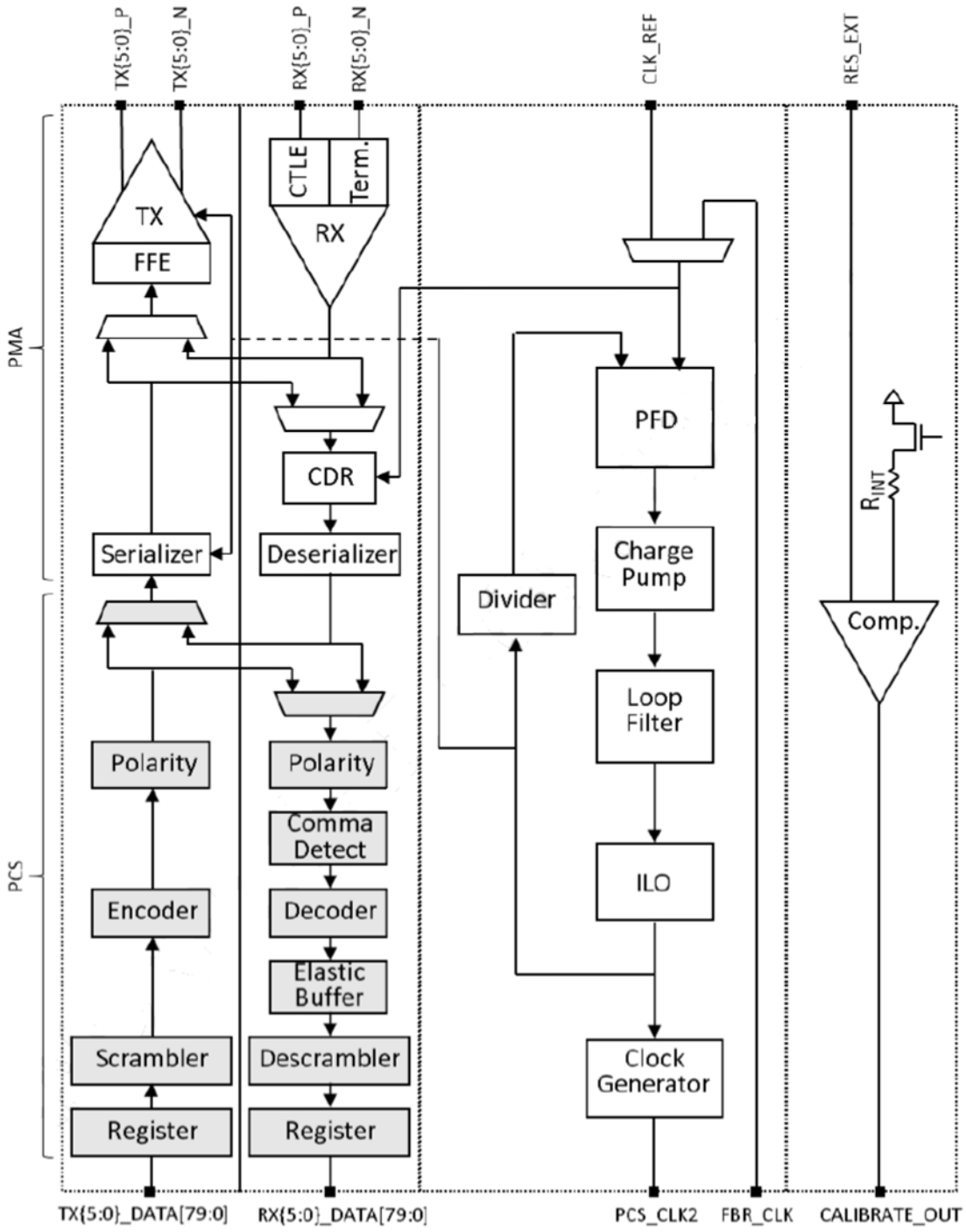


Figure 23: HSSL channel internal simplified diagram

3.2.6.1 HSSL PLL

The PLL provides a stable internal bit clock up to 6.25 GHz which is synthesized from a lower frequency input reference clock. This bit clock is used to generate each transmission bit clock. The designed PLL is a charge pump based PLL.

A +/-100ppm plesiosynchronous operation is guaranteed by design in each data lane individually and independently (TX data lane and RX data lane).

3.2.6.2 HSSL RX

At the beginning of the reception, the signal is matched to 50 Ω, filtered with CTLE, amplified and sampled. Then the frequency and phase of the signal is adjusted with the Clock Data Recovery (CDR) for a synchronous sampling of data. At the end of this process, the data is deserialized. The parallel data passes through the PCS blocks. The data sign is reconstructed due to the possible inversion depending on the external implementation. After that, the parallel data is adjusted to the word boundaries with the recognition of the comma symbol. The data, then, passes through the decoder. An elastic buffer is included to compensate the frequency difference of the TX and RX. The data is finally descrambled before being transferred to the FPGA fabric.

3.2.6.3 HSSL TX

The data is received by the PCS block where it passes through the scrambler before being encoded. The data sign is, then, imposed by the polarity block. After that, the parallel data is processed with the PMA blocks which consists of serializer, FFE filter, and driver. Serializer is the block which generates the serial output from up to 32-bit parallel input. FFE filter applies the pre-emphasis to compensate the ISI introduced by the channel. Driver is the block where the strength of each tap is assigned, the line impedance is set depending on PVT variations, and output signal level is adjusted.

3.2.6.4 HSSL Calibration

Due to PVT variations, the output resistance of the TX and the input resistance of the RX might deviate from the nominal values which disturbs the continuity of the channel impedance. Therefore, a calibration circuit is added to determine precisely the internal resistance values w.r.t to an external resistance.

3.2.7 Clocks Distribution

The clocking resources can manage various clocking schemes within the FABRIC or between the IOB and the FABRIC. Therefore the clock distributions spans multiple non homogeneous resources. To achieve the required performance and minimize the skew, the clock distribution

is split into several zones. Each zone has its own clock distribution coupled to adjacent IO banks to achieve complex clocking schemes between the periphery and the synchronous elements within the FABRIC.

3.2.7.1 Clock Tree Architecture

The NG_LARGE core logic is split in four zones. Each zone can use up to 12 global clocks.

Zone 1 : Top-left area of the tile and CGB array. 4 upper rows of 24 tiles + 2 upper rows of CGB

Zone 2 : Top-right area of the tile and CGB array. 4 upper rows of 24 tiles + 2 upper rows of CGB

Zone 3 : Bottom-right area of the tile and CGB array. 2 upper rows of 24 tiles + 2 remaining rows of CGB

Zone 4 : Bottom-left area of the tile and CGB array. 3 upper rows of 24 tiles + 2 remaining rows of CGB

The next f**Erreur ! Source du renvoi introuvable.**illustrates the clock distribution architecture. There are three types of clock nets:

- Core clock CCK
- Core & I/O Ring clock MCK
- I/O Ring clock RCK

Each CKG receives source clocks from 4 bank inputs (PAD) or 2 fabric signals (AUX_CLK).

The fabric provides 8 inputs to the CCK switch in order to propagate some internal generated signals to the clock distribution.

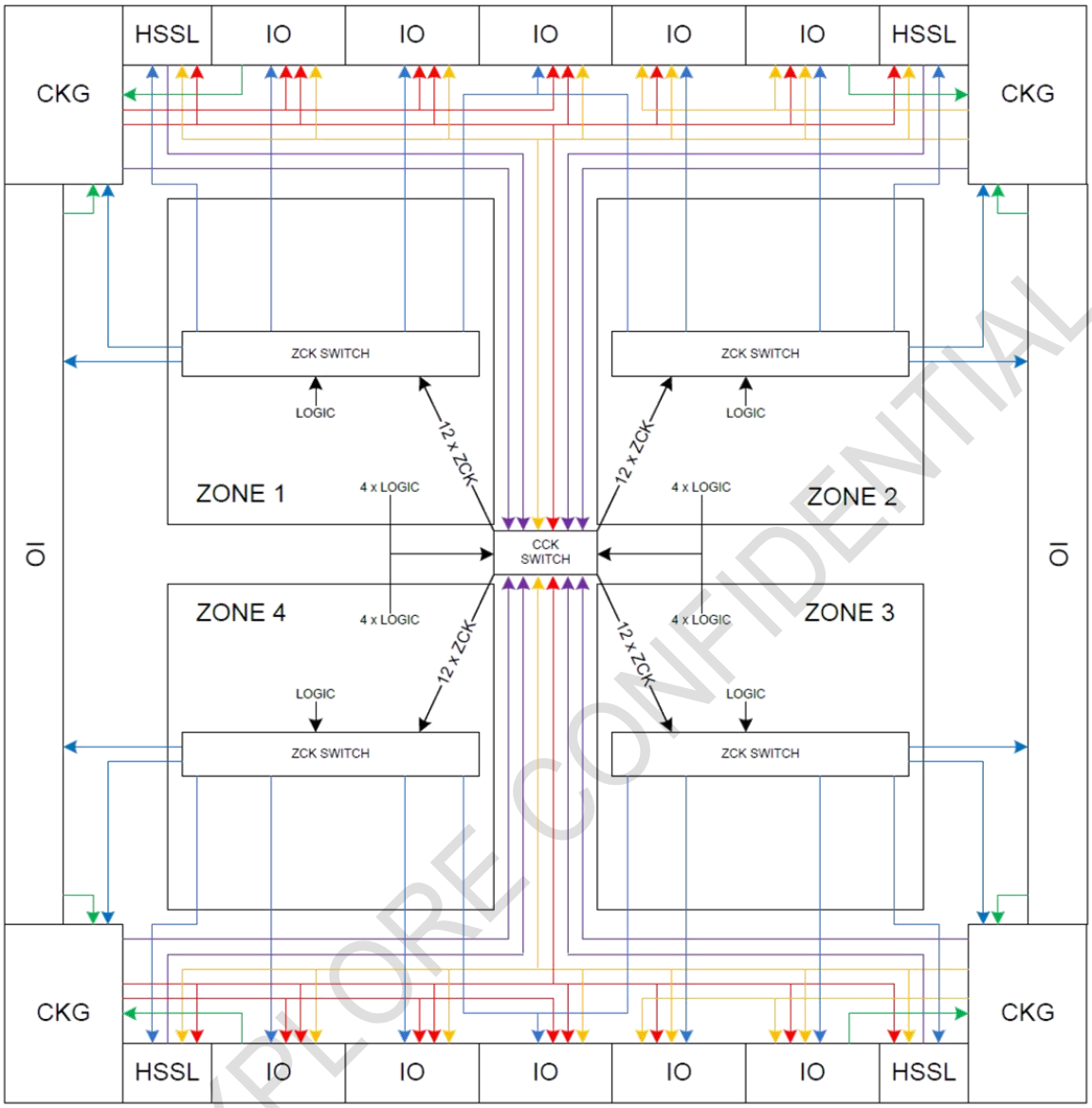


Figure 24: Clock distribution diagram

Clock distribution summary

4 x Clock Generators (CKG)
Each CKG provides 4 x CCK (core), 3 x MCK (mixed core & ring), 3 x RCK (ring)
Each CKG receives 2 x FABRIC inputs and 4x BANK inputs
4 x Clock Zones
12 x ZCK per Clock Zone

3.2.7.2 Clock Management

Each Clock Generator is composed of the main blocks:

- One PLL
- Ten frequency dividers / Waveform generators (WFG)

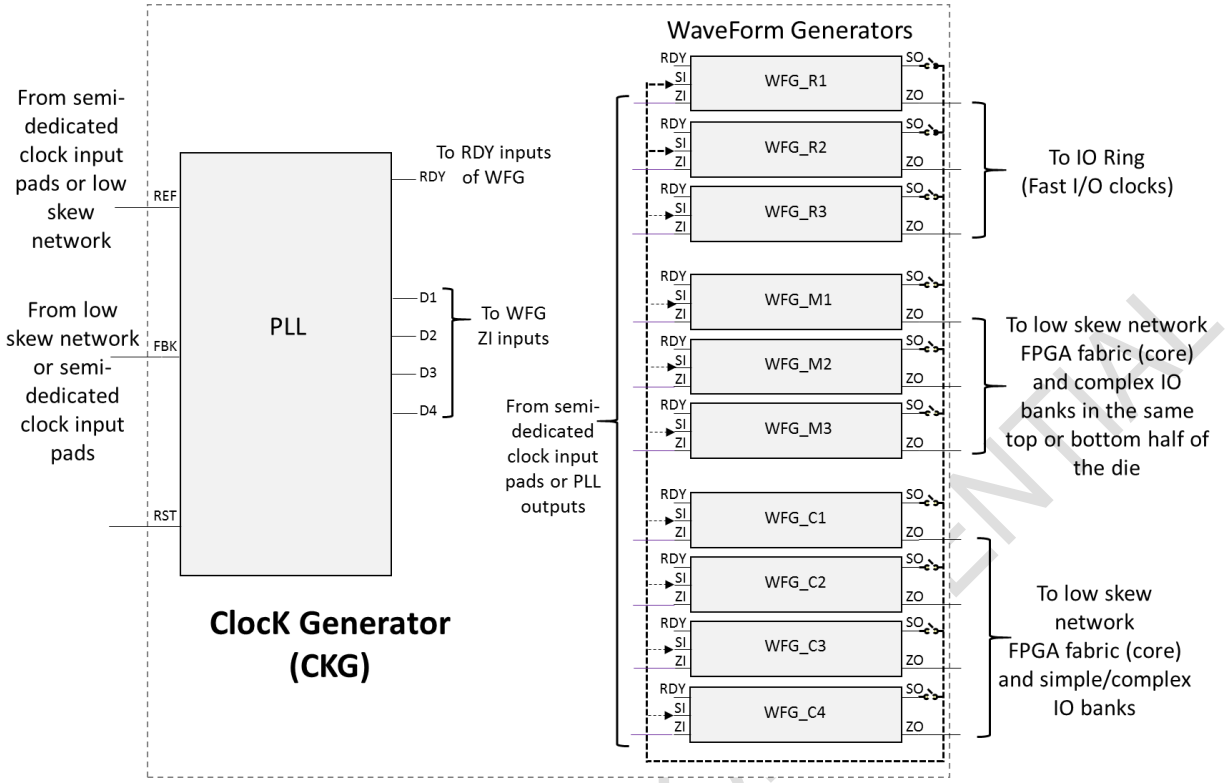


Figure 25: Clock Generator (CKG) simplified diagram

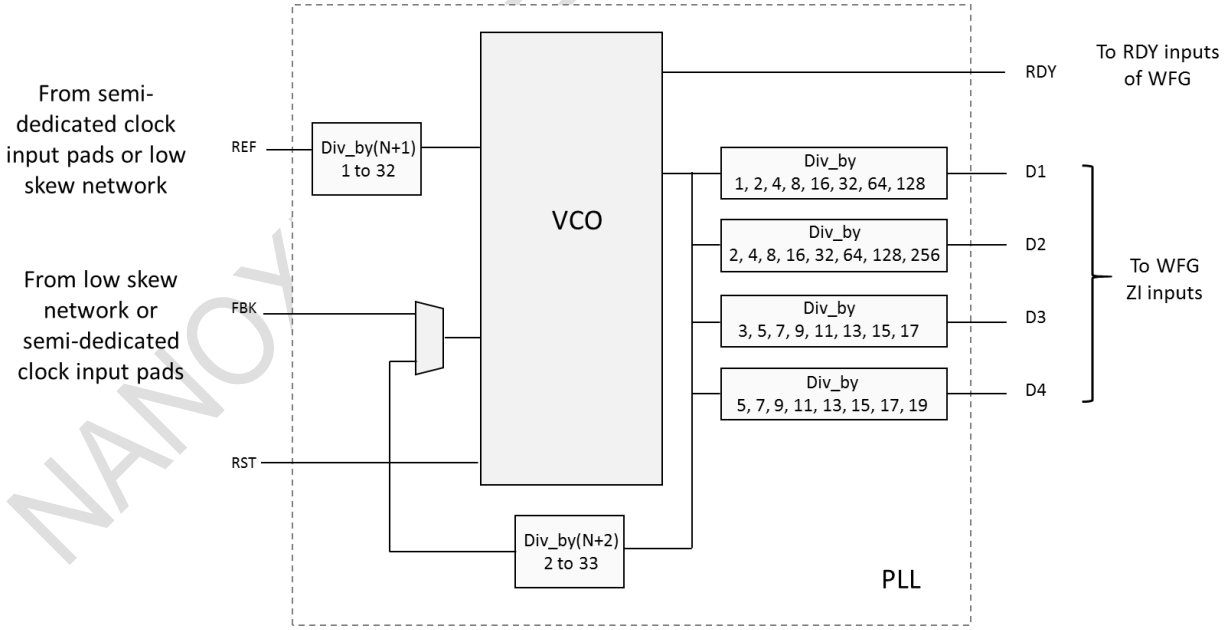


Figure 26: PLL diagram

Pin Name	Direction	Description
REF	Input	Incoming clock to the PLL.
FBK	Input	Feedback clock to the PLL
RST	Input	Re-initializes the PLL
D1, D2, D3, D4	Output	Divided clock outputs
RDY	Output	Goes high when PLL is locket

Table 9: PLL Pin Description

Input frequency: 20 MHz – 200 MHz
VCO frequency: 200 MHz – 1200 MHz
Output frequency: • D1, D2, D3 and D4 outputs : 1 MHz to 800 MHz
Maximum power: 26 Mw
Maximum static phase error (clockin – extfbclk): +/- 200ps
Lock time: 100µs
Single period jitter: +/- 60ps @ clk* = 200MHz, REF = 20MHz
Cycle to cycle jitter: +/- 90ps @ clk* = 200MHz, REF = 20MHz
Long term jitter: +/- 330ps @ clk* = 200MHz, REF = 20MHz

Table 10: PLL Characteristics

3.3 Power supplies

NX1H140TSP devices require the following power supplies:

- VDD1V2	Core logic supply	1.2V ± 10%
- VDD2V5A	Auxiliary analog supply, static	2.5V ± 10%

Configuration bank supplies:

- VDDIO_SERVICE	Configuration bank supply	3.3V ± 10%
- VDD_LVDS	Configuration LVDS supply	2.5V ± 10%

Simple I/O banks supplies:

- VDDIO_n	I/O banks supplies	1.5, 1.8, 2.5 or 3.3V

Complex I/O banks supplies:

- VDDIO_n	I/O banks supplies	1.5, 1.8, 2.5 or 3.3V
- VDDS_n	I/O termination switches supply	2.5 or 3.3V (*)
- VTO_n	Termination supplies	½ of VDDIO_n supply

HSSL supplies:

- HSSL_TX_VDDA	HSSL driver supply	1.2V
- HSSL_2V5A	HSSL analog supply	2.5V
- HSSL_D_VDD	HSSL digital supply	1.2V

(*) VDDS_n switch voltage should be 3.3V if VDDIO_n=3.3V, else 2.5V. VDDS_n is subject to pollution from the terminated I/Os and should be separated from sensible power supplies.

VDD1V2 Core supply current is fully dependent on the downloaded application and working frequency
VDDIO_n I/O supply current is fully dependent on the downloaded application, used I/O standard and working frequency
VDD2V5A analog supply current is static
VDD_SERVICE current is dependent on programming interface mode and activity.

Symbol	Parameter	Min	Typ	Max	Unit
IDD1V2	Quiescent* Core supply current	TBD	400	TBD	mA
IDD2V5A	Quiescent* VDD2V5A supply current	-	100	-	mA
IDD_SER	Quiescent* VDD_SERVICE supply current	TBD	20	TBD	mA
IDD1V2HSSL	Quiescent* HSSL supply current	TBD	200	TBD	mA
IDD2V5HSSL	Quiescent VDD2V5A HSSL supply current	-	10	-	mA

*Quiescent current is measured when the chip is turned on in safe-config mode without any design.

4 Device configuration

4.1 Purpose of NX1H140TSP configuration

NG-LARGE chips are SRAM-based FPGAs. To achieve user-defined functionality their configuration bitstream must be downloaded first.

NG- LARGE chips are always accessible through JTAG, and also support several configuration modes, as a function of the state of MODE[2:0] pins sampled at power-up. RST_N is a dedicated input pin that allows to reset the configuration engine, and launches the configuration process after RST_N is released. (It can't be used to reset the FPGA user's logic).

4.2 Configuration modes:

The NG-LARGE configuration modes are :

- JTAG (always available independently of the MODE(2:0) setting
- Spacewire
- Slave parallel 8-bit
- Slave Parallel 16-bit
- Master Serial SPI
- Master Serial SPI with VCC control

4.3 Configuration Timing Characteristics

Configuration clock inputs

Symbol	Parameter	Min	Typ	Max	Unit
TCKF	JTAG clock frequency		8		MHz
CLKF	Slave Parallel clock frequency	2 x TCKF		100	MHz
SpWF	Slave SpaceWire data rate			400	Mbit/S

Configuration clock outputs

Symbol	Parameter	Min	Typ	Max	Unit
Fbase	Clock dividers base frequency	45	50	55	MHz
SPIF	Master SPI clock frequency		Fbase/N*		MHz

Notes *:

- Division factor is 2 ≤ N ≤ 17. Default factor is 17 and may be dynamically changed during bitstream download with values provided by the bitstream generation software

5 I/O Characteristics

5.1 General Description

I/O Absolute maximum ratings (VDDIO)	-0.33 to 3.66 V
Operating temperature	-40 to 125 °C

Table 11: DC Characteristics

Each pad of each I/O bank can be configured as input-only, output-only or input-output.

5.2 I/O Standards DC/AC Specifications

	VDDIO (V)			Vref ([1]) (V) (Internally generated)			VTO (V)			
Standard	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**Standard Support**
LVCMOS 3V3	3.15	3.3	3.45	-	1.49	-	-	-	-	JESD8C.01
LVCMOS 2V5	2.375	2.5	2.625	-	1.25	-	-	-	-	JESD8-5
LVCMOS 1V8	1.71	1.8	1.89	-	0.9	-	-	-	-	JESD8-7
LVCMOS 1V5	1.425	1.5	1.575	-	0.75	-	-	-	-	JESD8-11
SSTL 2V5 class I/II	2.3	2.5	2.7	1.13	1.25	1.38	Vref-0.04	Vref	Vref+0.04	JESD8-9
SSTL 1V8 class I/II	1.7	1.8	1.9	0.838	0.9	0.9	Vref-0.04	Vref	Vref+0.04	JESD8-15
HSTL 1V8 class I/II	1.7	1.8	1.9	0.838	0.9	0.9	-	Vref	-	JESD8-6
HSTL 1V5 class I/II	1.4	1.5	1.6	0.68	0.75	0.9	-	Vref	-	JESD8-6
LVDS 2V5	2.25	2.5	2.75	-	-	-	-	-	-	ANSI/TIA/EIA-644

[1] *Vref represents an internally generated reference voltage, which is generally equal to the half of VDDIO voltage and used as reference for timing test.*

Table 12: I/O Standard DC characteristics

	AC				DC						
Standard	**VIH(V)**	**VIL(V)**	**VOH(V)**	**VOL(V)**	**VIH (V)**	**VIL (V)**	**VOH (V)**	**VOL (V)**	**IOH (mA)**	**IOL (mA)**	Standard Support
LVCMOS 3V3	-	-	-		2	0.8	2.4	0.4	-2, -4,-8,16	2, 4, 8, 16	JESD8C.01
LVCMOS 2V5	-	-	-	-	1.7	0.7	1.7	0.7			JESD8-5
LVCMOS 1V8	-	-	-	-	0.65*VDDIO	0.35*VDDIO	VDDIO-0.45	0.45			JESD8-7
LVCMOS 1V5	-	-	-	-	0.65*VDDIO	0.35*VDDIO	0.75*VDDIO	0.25*VDDIO			JESD8-11
SSTL 2V5 class I	Vref+0.31	Vref-0.31	VTO+0.6	VTO-0.6	Vref+0.15	Vref-0.15	Vt+0.6	Vt-0.6	-8.1	8.1	JESD8-9
SSTL 2V5 class II	Vref+0.31	Vref-0.31	VTO+0.8	VTO-0.8	Vref+0.15	Vref-0.15	Vt+0.8	Vt-0.8	-16.2	16.2	JESD8-9
SSTL 1V8 class I	Vref+0.25	Vref-0.25	VTO+0.6	VTO-0.6	Vref+0.125	Vref-0.125	Vt+0.6	Vt-0.6	-8.6	8.6	JESD8-15
SSTL 1V8 class II	Vref+0.25	Vref-0.25	VTO+0.6	VTO-0.6	Vref+0.125	Vref-0.125	Vt+0.6	Vt-0.6	13.4	13.4	JESD8-15
HSTL 1V8 class I	Vref+0.2	Vref-0.2	VDDIO-0.6	0.6	Vref+0.1	Vref-0.1	VDDIO-0.5	0.5	-8	8	JESD8-6
HSTL 1V8 class II	Vref+0.2	Vref-0.2	VDDIO-0.6	0.6	Vref+0.1	Vref-0.1	VDDIO-0.5	0.5	-16	16	JESD8-6
HSTL 1V5 class I	Vref+0.2	Vref-0.2	VDDIO-0.5	0.5	Vref+0.1	Vref-0.1	VDDIO-0.4	0.4	-8.0	8.0	JESD8-6
HSTL 1V5 class II	Vref+0.2	Vref-0.2	VDDIO-0.5	0.5	Vref+0.1	Vref-0.1	VDDIO-0.4	0.4	-16	16.0	JESD8-6

Table 13: I/O Single-Ended Standards AC/DC Input Output Specifications

	VICM (V) Input common mode			VID (V) Input differential		
Standard	**Min**	**Typ**	**Max**	**Min**	**Max**	Standard Support
LVDS 2V5[1]	F < 200 MHz : 0.6 F > 200 MHz : 0.5	1.25	F < 100 MHz : 1.75 100 MHz < F < 200 MHz : 1.65 F > 200 MHz : 1.4	0.1	-	ANSI/TIA/EIA-644

	VOD (V) [2] Output Differential			V OCM (V) Output common mode			
Standard	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	Standard Support
LVDS 2V5[(1)]	0.63	0.95	1.3	1.02	1.2	1.42	ANSI/TIA/EIA-644

(1) NG-MEDIUM IO PADS programmed as LVDS2V5 are “LVDS-compatible”, therefore AC/DC specifications are different that standard support ANSI/TIA/EIA-644 specifications.

(2) For R termination 100 Ω under DC conditions.

Table 14: I/O Differential Standards AC/DC Input Output Specifications

5.3 I/O Input/Output Switching Characteristics

5.3.1 Generic I/O Buffer Testbench

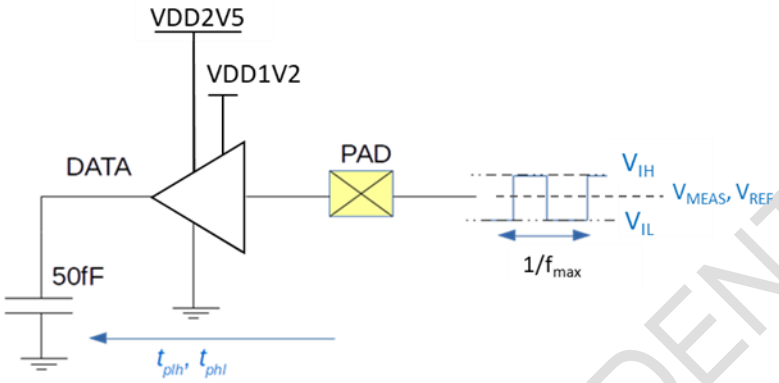


Figure 27: input buffer testing

I/O Standard	V_{IL} [V]	V_{IH} [V]	V_{MEAS} [V] (1)	V_{REF} [V] (2)
LVCMOS 3.3V	0	3.3	1.5	-
LVCMOS 2.5V	0	2.5	1.25	-
LVCMOS 1.8V	0	1.8	0.9	-
LVCMOS 1.5V	0	1.5	0.75	-
SSTL 2.5V Class I/II	V_{REF}-0.75	V_{REF}+0.75	V_{REF}	1.25
SSTL 1.8V Class I/II	V_{REF}-0.5	V_{REF}+0.5	V_{REF}	0.9
HSTL 1.8V Class I/II	V_{REF}-0.5	V_{REF}+0.5	V_{REF}	0.9
HSTL 1.5V Class I/II	V_{REF}-0.5	V_{REF}+0.5	V_{REF}	0.75
LVDS 2.5	V_{REF}-0.125	V_{REF}+0.125	0 (3)	1.25

Notes:
(1) Input voltage level from which the measurements starts.
(2) This is the input voltage reference used for input signal generation.
(3) The value is given in differential input voltage.

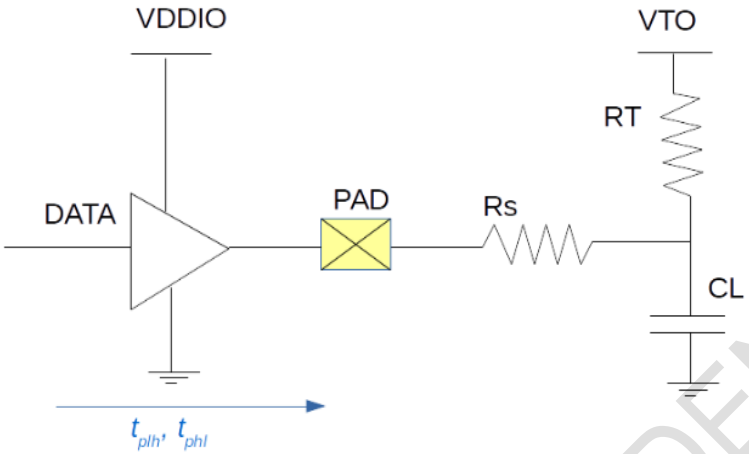


Figure 28: output buffer testing

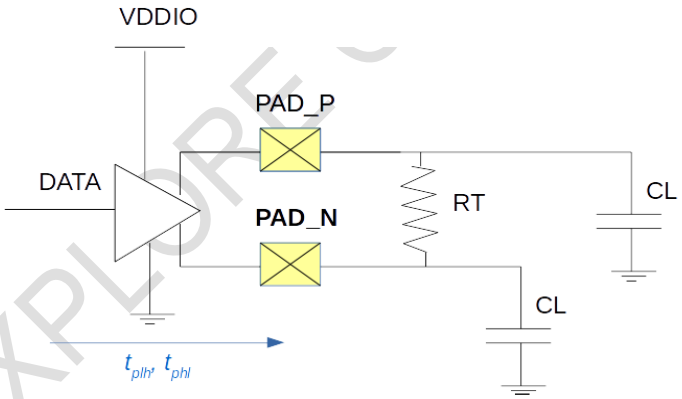


Figure 29: Differential output buffer testing

5.3.2 IO Input Buffer Switching Characteristics

Standard	tplh (1) (ns)	tphl (1) (ns)	trise (2) (ps)	tfall (2) (ps)	turbo	fmax (MHz)
LVCMOS 3V3	0.843	0.833	98	62	Yes	300
LVCMOS 3V3	1.84	1.74	98	62	No	200
LVCMOS 2V5	0.812	0.840	98	62	Yes	300
LVCMOS 2V5	1.59	1.83	98	62	No	200
LVCMOS 1V8	0.795	0.856	98	62	Yes	300
LVCMOS 1V8	1.52	2.24	98	62	No	200
LVCMOS 1V5	0.805	0.887	98	62	Yes	300
LVCMOS 1V5	1.79	2.56	98	62	No	200
SSTL 2V5	0.813	0.844	98	62	Yes	300
SSTL 2V5	1.72	2.3	98	62	No	200
SSTL 1V8	0.815	0.884	98	62	Yes	400
SSTL 1V8	2.32	2.6	98	62	No	200
HSTL 1V8	0.815	0.884	98	62	Yes	400
HSTL 1V8	2.33	2.59	98	62	No	200
HSTL 1V5	0.818	0.909	98	62	Yes	400
HSTL 1V5	2.35	2.69	98	62	No	200
LVDS 2V5	0.874	0.957	98	62	Yes	400
LVDS 2V5	3.00	2.64	98	62	No	200

Table 15: I/O Input Buffer Switching Characteristics

Simulation conditions: Worst-case operating conditions as VDDnominal=1V2*0.9 V and -40C junction temperature. A worst-case packaging parasitic model is used.

5.3.3 Output Buffer Switching Characteristics

Standard	tplh [1] (ns)	tphl [1] (ns)	rising ramp (V/ns)	falling ramp (V/ns)	F_{max} for Cload (MHz)
LVCMOS 3V3 2mA	3.81	4.98	0.42	0.39	50
LVCMOS 3V3 4mA	2.6	3.04	0.81	0.77	100

LVCMOS 3V3 8mA	2.07	2.06	1.27	1.61	200
LVCMOS 3V3 16mA	1.75	1.76	3.22	3.39	300
LVCMOS 2V5 2mA	4.65	5.22	0.27	0.24	50
LVCMOS 2V5 4mA	3.02	3.14	0.52	0.48	100
LVCMOS 2V5 8mA	2.10	2.56	1.06	0.75	200
LVCMOS 2V5 16mA	1.80	1.85	2.32	1.74	300
LVCMOS 1V8 2mA	3.62	4.09	0.29	0.25	50
LVCMOS 1V8 4mA	2.92	3.07	0.43	0.38	100
LVCMOS 1V8 8mA	2.09	2.11	0.88	0.77	200
LVCMOS 1V8 16mA	1.82	1.72	1.94	1.88	300
LVCMOS 1V5 2mA	4.16	3.75	0.21	0.24	50
LVCMOS 1V5 4mA	2.87	2.78	0.40	0.41	100
LVCMOS 1V5 8mA	2.10	2.03	0.85	0.76	200
LVCMOS 1V5 16mA	1.82	1.77	1.81	1.59	300
SSTL2V5 class I	1.64	1.64	1.55	1.52	300
SSTL2V5 class II	1.49	1.51	2.76	2.39	300
SSTL1V8 class I	1.60	1.60	1.82	1.66	400
SSTL1V8 class II	1.53	1.52	1.81	1.63	400
HSTL1V8 class I	1.58	1.57	1.18	1.17	400
HSTL1V8 class II	1.47	1.51	1.14	1.07	400
HSTL1V5 class I	1.61	1.61	1.19	1.15	400
HSTL1V5 class II	1.51	1.54	0.91	0.89	400
LVDS 2V5 [2]	1.61	1.61	1.43	1.41	400

Table 16: Output Buffer Switching Characteristics

Notes:
Simulation conditions: Worse-case operating conditions as VDDIOnom*0.9 and 125C junction temperature. A worse-case packaging parasitic model is used. Output buffer input signal transition time is set as one tenth of the signal pulse width which varies with F_{max} and the duty cycle is 0.5. No parasitic nor transmission line effect due to board traces are considered in this characterization. Spice benches consider only RLC parasitic due to packaging and a resistive/capacitive load connected directly to PAD pin, for which values can be found in (reference to table 22 I/O standard termination specifications).

5.3.4 IO Standard Termination Specifications

Standard	Rs (Ω)	RT (Ω)	CL (pF)	VT (V)
LVCMOS 3V3	-	-	5	0
LVCMOS 2V5	-	-	5	0
LVCMOS 1V8	-	-	5	0
LVCMOS 1V5	-	-	5	0
SSTL 2V5 class I	25	50	5	1.25
SSTL 2V5 class II	25	25	5	1.25
SSTL 1V8 class I	20	50	5	0.9
SSTL 1V8 class II	20	25	5	0.9
HSTL 1V8 class I	-	50	5	0.9

HSTL 1V8 class II	-	25	5	0.9
HSTL 1V5 class I	-	50	5	0.75
HSTL 1V5 class II	-	25	5	0.75
LVDS 2V5	-	100	5	-

Table 17: I/O Standard Termination Specifications

6 Packaging

The NG-LARGE FPGA (NX1H140TSP) is delivered on the following packages :

- LG1752 : Land Grid Array 1752 pins, 1.0mm pitch
- CG1752 : Ceramic column Grid Array 1752 pins
- FF1752 : Fine pitch Flip-chip organic ball grid array, 1752 balls
- FF1152 : Fine pitch Flip-chip organic ball grid array, 1152 balls
- DIECOM : Die form (tested at ambient temperature)

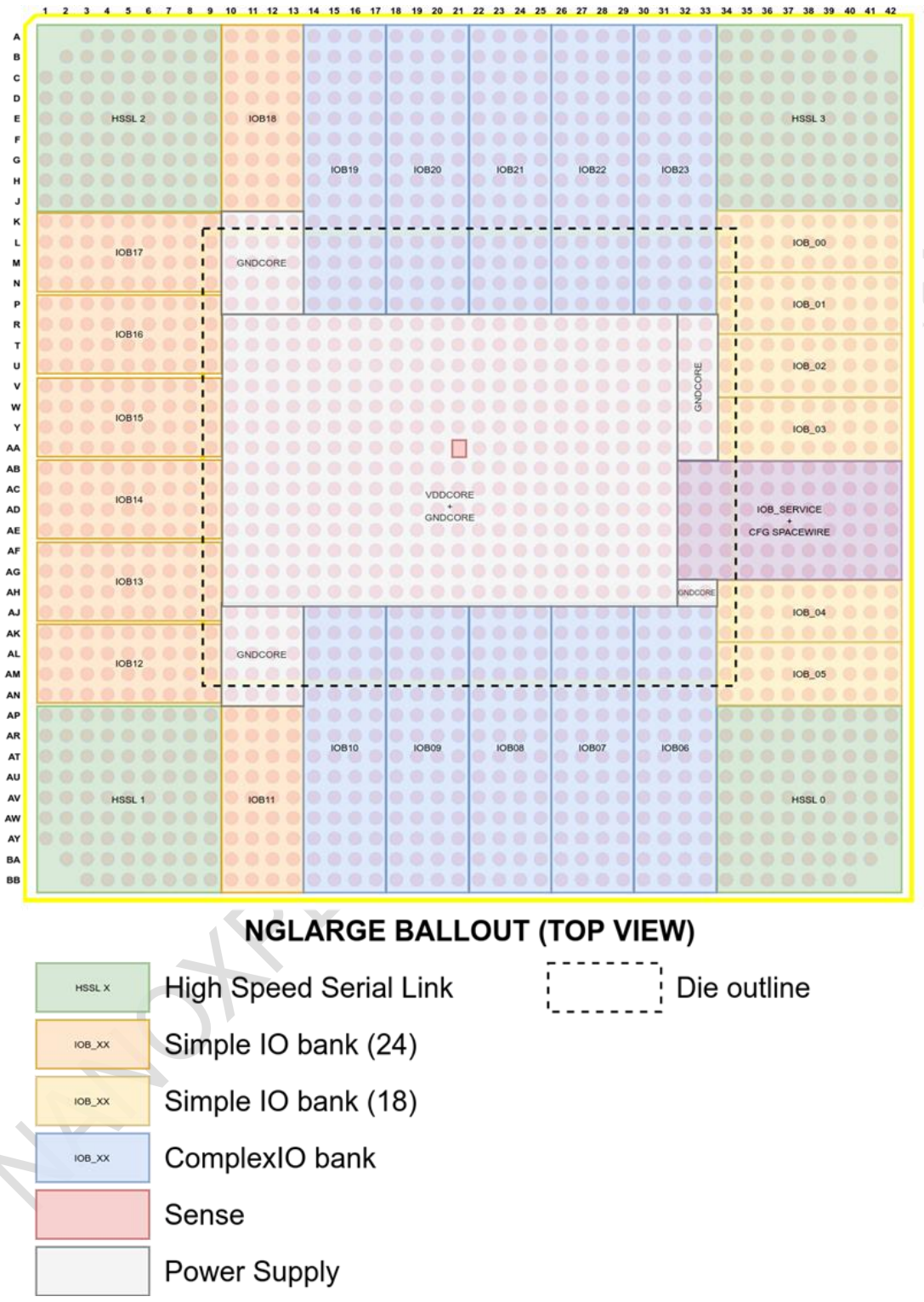
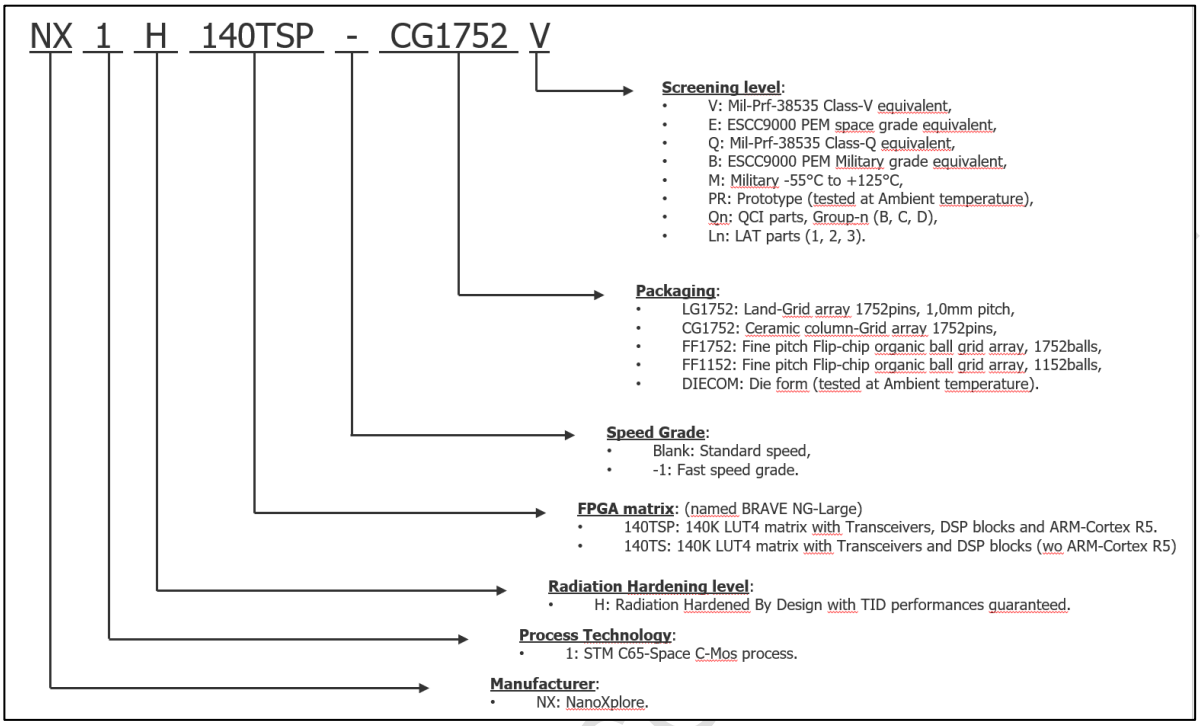


Figure 30: NG-LARGE pins distribution

Global I/O pin floorplan for FF1752 package

The pins assignment to be defined

7 Ordering Information



8 Glossary

Acronym	Description
ALU	Arithmetic Logic Unit
CG	Clock Generator
CGA	Column Grid Array
CMIC	Configuration Memory Integrity Check
CMOS	Complementary Metal Oxide Semiconductor
DDR	Double Data Rate
DFF	D-Flip Flop
DPRAM	Dual-Port Read Access Memory
DSP	Digital Signal Processor
ECC	Error Correction Circuit
EDAC	Error Detection And Correction
FPGA	Field Programmable Gate Array
HSSL	High Speed Serial Link
HSTL	High-Speed Transceiver Logic
IOB	Input Output Block
LGA	Land Grid Array
LUT	Look-Up Table
LVCMOS	Low Voltage CMOS
LVDS	Low Voltage Differential Signal
CQFP	Multilayer Quad Flat Package
PCI	Peripheral Component Interconnect
PLL	Phase-Locked Loop
RH	Radiation Hardened

RHBD	Radiation Hardened By Design
SECDED	Single Error Correction, Double Error Detection
SEFI	Single-Event Functional Interrupt
SEL	Single-Event Latch-up
SER	Soft-Error Rate
SET	Single-Event Transient
SEU	Single-Event Upset
SpW Tx & Rx	SpaceWire Transceiver & Receiver
SSTL	Stub Series Terminated Logic

9 Revision history

The following table shows the revision history of the NX1H140TSP datasheet

Date	Version	Revision
2018-11-30	1.0	Initial NG-LARGE datasheet