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1. SYSTEM DESCRIPTION

1.1 General

IFE shall access the clients with their native UART, STACAN, GPIO and LED connections.

1.2 Device and package

- Device family: PolarFire
- Part Number : MPF300TL-FCG484I
- Family : PolarFire
- Die : MPF300TL
- Package : FCG484
- Speed : STD
- Core Voltage : 1.0

Figure 1. IFE Block Diagram

1.3 FPGA Main Functionality

- Converts 2 SPW interface to 40 uarts interfaces and 1 SPW for external use.
  Data rate – Up to 24Mbps. Default: 10Mbps.
- Control the UART tranmitter (RS485/RS422 protocol).
  Data rate – Up to 921600 bps. Default: 115200bps.
- CANBUS interface
- Controls the GPIOs and LEDs discrets.
- Endianess: BIG Endean – MSB first.
- JTAG Interface for FPGA programming and debugging
- SPW debugger - TBD

No.	Interface	Name	Type	Description
1	SPW communication		SpW (LVDS)	2 x SPW interface 1 x SPW for external use

2	UARTs communication		(LVCOMS)	40 BI directional uarts extentions Support RS422 / RS485.
3	UART EN [0..39]		(LVCOMS)	GPIO
4	POR		Power on reset	External HW reset
5	JTAG (Programming and debug)			FPGA debug interface shall support AIT debugging (JTAG-RS422 – TBD)
6	GPIO		Discrets	
7	CAN-BUS			
8	LED x3		Discrets	

Table 1. Internal interfaces

1.3.1 MAJOR BLOCKS

1.3.1.1 SPW INTERFACES

The modules contain the following functionality:

1. Control type: this type controls the FPGA registers and get status from the FPGA.
2. Data type: Streaming Data from/to UART blocks.

1.3.1.2 UART Modules

The uart blocks has the following features:

1. Data from/to SPW blocks.
2. Controls the TX_EN.
3. Configurable - baud rate, parity and stop bit configuration.

1.3.1.3 CAN-BUS Module

This module tranfers data to/from SPW to CAN-BUS.

1.3.1.4 GPIO/LED block

Controls the GPIO's discrets.

2. COMMUNICATION PROTOCOL

2.1 Space Wire Protocol

2.1.1 Space Wire Frame

CARD ID 1b	FPGA 7b (0x00)	R/W 1b	ADD 15b	Length 2Byte	Data 1Byte to 256Byte	CS 2Byte	EOP

CPU To/From External Device

CARD ID 1b	Device 7b	N/A 1b	N/A 15b	Length 2Byte	Data 1Byte to 1024Byte	CS 2Byte	EOP

CPU Broadcast/Multicast To UART Devices

CARD ID 1b	Device 7b (0x3C)	W b01	N/A 15b	Length 2Byte	Data 1Byte to 1024Byte	CS 2Byte	EOP

nACK – interrupt msg.

CARD ID 1b	Device 7b	ERR STATUS 1Byte	EOP

Table 2 - SPW Frame Configuration

Device table:

FPGA	0x00	
UART1	0x01	
UART2	0x02	
…		
UART40	0X28	
SPW #3	0x29	
SPW #4	0x2A	
CAN-BUS	0x2B	
Broadcast	0x3C	

2.1.2 SPW Communication Mechanisms

FPGA shall receive SPW packets simultaneously from all 3 SPW channels.

FPGA shall transmit SPW packets to the last received SPW packet channel.

2.1.3 CAN-BUS – TBD

2.2 UART frame:

START bit	8 DATA bits								PARITY	STOP bit
	D0	D1	D2	D3	D4	D5	D6	D7		

Table 3 - UART Frame

3. REGISTERS

The registers shall be implemented in BitGen tool.

3.1 Control Registers

3.1.1 UART Reset Register:

The reset shall be for the whole UART module, including FIFOs.

Register #1:

Description	Bit	Options	Default	Remarks
Reset UART #8:1	7:0	0x1 for reset	0x0	

Table 4 - UART reset register #1

Register #2:

Description	Bit	Options	Default	Remarks
Reset UART #16:9	7:0	0x1 for reset	0x0	

Table 5 - UART reset register #2

Register #3:

Description	Bit	Options	Default	Remarks
Reset UART #24:17	7:0	0x1 for reset	0x0	

Table 6 - UART reset register #3

Register #4:

Description	Bit	Options	Default	Remarks
Reset UART #32:18	7:0	0x1 for reset	0x0	

Table 7 - UART reset register #4

Register #5:

Description	Bit	Options	Default	Remarks
Reset UART #40:33	7:0	0x1 for reset	0x0	

Table 8 - UART reset register #5

3.1.2 UART Configuration Register x 40:

The configuration registers shall be in consecutives addresse, in order to support writing/reading to/from all configuration registers in one write/read command.

For each UART 3 configuration register shall be implemented:

Register #6:

Description	Bit	Options	Default	Remarks
Reseved	7	0x1 for reset	'0'	
Time Out	6:0	Up to 128 bits	X"32"	50 bits

Table 9 - UART reset register #1

Register #7:

Description	Bit	Options	Default	Remarks
Baud_Rate(bps)	7:4	From 9600 to 921600	"0110"	115200bps
Start_bit	3	NA	'0'	Always one start bit
Stop_bit	2	'0' – 1 stop bit '1' – 2 stop sits	'0'	
Parity	1:0	"00" - None "01" - Odd "10" - Even "11" - NA	"01"	Odd

Table 10 - UART Configuration register #2

Register #8:

Description	Bit	Options	Default	Remarks
Reserved	7:4	Reserved	0x0	
Data length (bits)	3	NA	'0'	8bits - LSB first
Type	2	'0' - RS422 '1' - RS485	'0'	RS422
TX_Enable	1	'0' - Auto '1' - Always On	'0'	Auto - See note below Enabled while transmitting
UART_Rx_Enable	0	'0' - Enabled '1' - Disabled	'0'	Enabled - See note below

Table 11 - UART Configuration register #3

Configuration Register description:

a. Time Out: (7 bits)

   1) for transmitting data - after sending packet FPGA waits for timeout x UART bits before transmitting another packet.

   2) For receiving data - verifing FPGA received packet when the UART RXD signal value is '1' for timeout x UART bits.

b. Baud rate: (4 bits)

   921600 = 0x9; 460800 = 0x8; 230400 = 0x7; 115200 = 0x6 (**Default**); 57600 = 0x5; 38400 = 0x4; 28800 = 0x3; 19200 = 0x2; 14400 = 0x1; 9600 = 0x0;

c. Stop bit: 1/2 bits (1 bit)

   1 bit = 0x0 (**Default**); 2 bits = 0x1

d. Parity: Even/Odd/None (2 bits)

   None = 0x0; Odd = 0x1 (**Default**); Even = 0x2

e. Data length: 8 bits - unconfigurable

f. Type: RS485/RS422 (1 bit)

   RS422 = 0x0 (**Default**); RS485 = 0x1

g. TX Enable: (1 bit)

   Auto = 0x0 (**Default**); Always On: 0x1

h. UART Rx Enable: Enable/disable (1 bit)

   Enable = 0x0 (**Default**); Disabled = 0x1

   ~~Upon POR the all RS422 receivers (RX) shall be input enabled.~~

   Note: When disabled, the receive and transmit channels content are ignored.

i. Transmit Enable (TX Enable):

   In Auto mode: When transmitter data available, all RS422 transmitters' outputs (TX) shall be automatically enabled.
   Where no data is transmitted, TX enable shall be automatically disabled.

   A provision for of always ON, enable shall be implemented.

   For RS485 interfaces:

   For RS485, the FPGA will automatically switch the transceiver into receive mode. The TX shall be enabled when transmiting packet.

3.2 SPW#3 Configuartion

Register #125:

Description	Bit	Options	Default	Remarks
Reserved	7:2	Reserved	0x0	
Data_Rate	1:0	"00" – 9.6Mbps "01" – 12Mbps "10" – 16Mbps "11" – 24Mbps	"00"	(Mbps)

Table 12 - SPW#3 Configuration

3.3 GPIOs and LEDs Control Register

Register #126:

Description	Bit	Options	Default	Remarks
reserved	7:6		"00"	
GP_OUT_0	5	'0' – LOW, '1' - HIGH	'0'	
GP_OUT_1	4	'0' – LOW, '1' - HIGH	'0'	
GP_OUT_2	3	'0' – LOW, '1' - HIGH	'0'	
LED0	2	'0' – Blinking @1Hz '1' - ON	'0'	For debug
LED1	1	ON – '1', OFF – '0'	'0'	For debug
LED2	0	ON – '1', OFF – '0'	'0'	For debug

Table 13 – GPIO and LEDs #3 Configuration

3.3.1 CAN-BUS Register

Register #127:

Description	Bit	Options	Default	Remarks
Reserved	7	Reserved	'0'	
CAN-Bus_Node_Number	6:1	Up to 63 clients	'0'	
TX_Enable	0	'0' - Disabled '1' - Enabled	'0'	

Table 14 - CAN-BUS Configuration

3.4 Status Registers

3.4.1 UART Status Register x 40:

The status registers shall be in consecutives addresses.

The FPGA shall support reading all status registers in one read command.

For each UART 3 status registers shall be implemented:

Register #130:

Description	Bit	Default	Remarks
Resereved	7:2	Resereved	X"0"
Receiver FIFO #Bytes (9:8)	1:0	"00"	MSB ?

Table 15 - UART Status register #1

Register #131:

Description	Bit	Default	Remarks
Receiver FIFO #Bytes (7:0)	7:0	0x0	LSB ?

Table 16 - UART Status register #2

Register #132:

Description	Bit	Default	Remarks
Resereved	7:2	Resereved	X"0"
Transmitter FIFO #Bytes (9:8)	1:0	"00"	MSB ?

Table 17 - UART Status #3

Register #133:

Description	Bit	Default	Remarks
Transmitter FIFO #Bytes (7:0)	7:0	0x0	LSB ?

Table 18 - UART Status #4

Register #134:

Description	Bit	Default	Remarks
RX FIFO Full	7	0x0	RX FIFO is full
RX FIFO Empty	6	0x0	RX FIFO is empty
TX FIFO Full	5	0x0	TX FIFO is full
TX FIFO Empty	4	0x0	TX FIFO is empty
Parity Error	3	0x0	Valid for last transmit
FRAME_ERROR	2	0x0	Indicates that the stop bit(s) is zero (valid STOP bit is to be '1').
OVERRUN_ERROR	1	0x0	Indicates that a new data was received by the UART , while previous data was not read, meaning RX_RD_EN was not asserted between two consecutive RX_VALID assertions
RBRK_ERROR	0	0x0	Receiver Brake indication (during idle condition, there is continues zero on RX_SERIAL bit)

Table 19 - UART Status #5

3.4.2 GPIOs Status Register

Register #200:

Description	Bit	Options	Default	Remarks
GP_IN_0	7	'0' – LOW, '1' - HIGH	'1'	
GP_IN_1	6	'0' – LOW, '1' - HIGH	'1'	
GP_IN_2	5	'0' – LOW, '1' - HIGH	'1'	
reserved	4:0	reserved	"00"	

Table 20 - UART Status #5

3.4.3 SPW Channels Error

Register #2201:

Description	Bit	Options	Default	Remarks
Received_uart_cs_error	7	'0' – OK, '1' - error	'0'	
reserved	6:0	reserved	0x0	