IFE

Programmers Guide

Classification: Unclassified

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1. Global Enums

The following table lists the global enums.

Enum Name	Enum Value	Enum Color
ERROR_OK	Width: 1	
OK	**0 | 0x0**	
ERROR	**1 | 0x1**	
ON_OFF	Width: 1	
OFF_bit	**0 | 0x0**	
ON_bit	**1 | 0x1**	
ON_BLINKING	Width: 1	
BLINKING	**0 | 0x0**	
LED_ON	**1 | 0x1**	
FULL_EMPTY	Width: 1	
EMPTY	**0 | 0x0**	
FULL	**1 | 0x1**	
EMPTY_FULL	Width: 1	
FULL	**0 | 0x0**	
EMPTY	**1 | 0x1**	
RESET_OPER	Width: 1	
OPER	**0 | 0x0**	
RESET	**1 | 0x1**	
TWO_ONE	Width: 1	
ONE	**0 | 0x0**	
TWO	**1 | 0x1**	
HIGH_LOW	Width: 1	

LOW	**0 | 0x0**	
HIGH	**1 | 0x1**	
TX_ENABLE	Width: 1	
Auto	**0 | 0x0**	
Always_On	**1 | 0x1**	
PARITY	Width: 2	
None	**0 | 0x0**	
Odd	**1 | 0x1**	
Even	**2 | 0x2**	
NA	**3 | 0x3**	
SPW_RATE	Width: 2	
Mbps_9_6	**0 | 0x0**	
Mbps_12	**1 | 0x1**	
Mbps_16	**2 | 0x2**	
Mbps_24	**3 | 0x3**	
BAUD_RATE	Width: 4	
RATE_9600	**0 | 0x0**	
RATE_14400	**1 | 0x1**	
RATE_19200	**2 | 0x2**	
RATE_28800	**3 | 0x3**	
RATE_38400	**4 | 0x4**	
RATE_57600	**5 | 0x5**	
RATE_115200	**6 | 0x6**	
RATE_230400	**7 | 0x7**	
RATE_460800	**8 | 0x8**	

RATE_921600	9 | 0x9	
DISABLE_ENABLE	Width: 1	
ENABLE	**0 | 0x0**	
DISABLE	**1 | 0x1**	
ENABLE_DISABLE	Width: 1	
DISABLE	**0 | 0x0**	
ENABLE	**1 | 0x1**	

2. Component IFE_top

1. Memory Map

Item	Type	Offset	Size	Array Size	Total Size
FPGA_Ver	[Register]	0x00	1	1	1
FPGA_Year	[Register]	0x01	1	1	1
FPGA_Month	[Register]	0x02	1	1	1
FPGA_Day	[Register]	0x03	1	1	1
Reset_UART_40_33	[Register]	0x04	1	1	1
Reset_UART_32_25	[Register]	0x05	1	1	1
Reset_UART_24_17	[Register]	0x06	1	1	1
Reset_UART_16_9	[Register]	0x07	1	1	1
Reset_UART_8_1	[Register]	0x08	1	1	1
Broadcast_UART_40_33	[Register]	0x81	1	1	1

Broadcast_UART_32_25	[Register]	0x82	1	1	1
Broadcast_UART_24_17	[Register]	0x83	1	1	1
Broadcast_UART_16_9	[Register]	0x84	1	1	1
Broadcast_UART_8_1	[Register]	0x85	1	1	1
Broadcast_SPW_3_4	[Register]	0x86	1	1	1
UART40_Config_1	[Register]	0x09	1	1	1
UART40_Config_2	[Register]	0x0A	1	1	1
UART40_Config_3	[Register]	0x0B	1	1	1
UART39_Config_1	[Register]	0x0C	1	1	1
UART39_Config_2	[Register]	0x0D	1	1	1
UART39_Config_3	[Register]	0x0E	1	1	1
UART38_Config_1	[Register]	0x0F	1	1	1
UART38_Config_2	[Register]	0x10	1	1	1
UART38_Config_3	[Register]	0x11	1	1	1
UART37_Config_1	[Register]	0x12	1	1	1
UART37_Config_2	[Register]	0x13	1	1	1
UART37_Config_3	[Register]	0x14	1	1	1
UART36_Config_1	[Register]	0x16	1	1	1
UART36_Config_2	[Register]	0x15	1	1	1
UART36_Config_3	[Register]	0x17	1	1	1
UART35_Config_1	[Register]	0x18	1	1	1
UART35_Config_2	[Register]	0x19	1	1	1
UART35_Config_3	[Register]	0x1A	1	1	1
UART34_Config_1	[Register]	0x1B	1	1	1
UART34_Config_2	[Register]	0x1C	1	1	1

UART34_Config_3	[Register]	0x1D	1	1	1
UART33_Config_1	[Register]	0x1E	1	1	1
UART33_Config_2	[Register]	0x1F	1	1	1
UART33_Config_3	[Register]	0x20	1	1	1
UART32_Config_1	[Register]	0x21	1	1	1
UART32_Config_2	[Register]	0x22	1	1	1
UART32_Config_3	[Register]	0x23	1	1	1
UART31_Config_1	[Register]	0x24	1	1	1
UART31_Config_2	[Register]	0x25	1	1	1
UART31_Config_3	[Register]	0x26	1	1	1
UART30_Config_1	[Register]	0x27	1	1	1
UART30_Config_2	[Register]	0x28	1	1	1
UART30_Config_3	[Register]	0x29	1	1	1
UART29_Config_1	[Register]	0x2A	1	1	1
UART29_Config_2	[Register]	0x2B	1	1	1
UART29_Config_3	[Register]	0x2C	1	1	1
UART28_Config_1	[Register]	0x2D	1	1	1
UART28_Config_2	[Register]	0x2E	1	1	1
UART28_Config_3	[Register]	0x2F	1	1	1
UART27_Config_1	[Register]	0x30	1	1	1
UART27_Config_2	[Register]	0x31	1	1	1
UART27_Config_3	[Register]	0x32	1	1	1
UART26_Config_1	[Register]	0x33	1	1	1
UART26_Config_2	[Register]	0x34	1	1	1
UART26_Config_3	[Register]	0x35	1	1	1

UART25_Config_1	[Register]	0x36	1	1	1
UART25_Config_2	[Register]	0x37	1	1	1
UART25_Config_3	[Register]	0x38	1	1	1
UART24_Config_1	[Register]	0x39	1	1	1
UART24_Config_2	[Register]	0x3A	1	1	1
UART24_Config_3	[Register]	0x3B	1	1	1
UART23_Config_1	[Register]	0x3C	1	1	1
UART23_Config_2	[Register]	0x3D	1	1	1
UART23_Config_3	[Register]	0x3E	1	1	1
UART22_Config_1	[Register]	0x3F	1	1	1
UART22_Config_2	[Register]	0x40	1	1	1
UART22_Config_3	[Register]	0x41	1	1	1
UART21_Config_1	[Register]	0x42	1	1	1
UART21_Config_2	[Register]	0x43	1	1	1
UART21_Config_3	[Register]	0x44	1	1	1
UART20_Config_1	[Register]	0x45	1	1	1
UART20_Config_2	[Register]	0x46	1	1	1
UART20_Config_3	[Register]	0x47	1	1	1
UART19_Config_1	[Register]	0x48	1	1	1
UART19_Config_2	[Register]	0x49	1	1	1
UART19_Config_3	[Register]	0x4A	1	1	1
UART18_Config_1	[Register]	0x4B	1	1	1
UART18_Config_2	[Register]	0x4C	1	1	1
UART18_Config_3	[Register]	0x4D	1	1	1
UART17_Config_1	[Register]	0x4E	1	1	1

UART17_Config_2	[Register]	0x4F	1	1	1
UART17_Config_3	[Register]	0x50	1	1	1
UART16_Config_1	[Register]	0x51	1	1	1
UART16_Config_2	[Register]	0x52	1	1	1
UART16_Config_3	[Register]	0x53	1	1	1
UART15_Config_1	[Register]	0x54	1	1	1
UART15_Config_2	[Register]	0x55	1	1	1
UART15_Config_3	[Register]	0x56	1	1	1
UART14_Config_1	[Register]	0x57	1	1	1
UART14_Config_2	[Register]	0x58	1	1	1
UART14_Config_3	[Register]	0x59	1	1	1
UART13_Config_1	[Register]	0x5A	1	1	1
UART13_Config_2	[Register]	0x5B	1	1	1
UART13_Config_3	[Register]	0x5C	1	1	1
UART12_Config_1	[Register]	0x5D	1	1	1
UART12_Config_2	[Register]	0x5E	1	1	1
UART12_Config_3	[Register]	0x5F	1	1	1
UART11_Config_1	[Register]	0x60	1	1	1
UART11_Config_2	[Register]	0x61	1	1	1
UART11_Config_3	[Register]	0x62	1	1	1
UART10_Config_1	[Register]	0x63	1	1	1
UART10_Config_2	[Register]	0x64	1	1	1
UART10_Config_3	[Register]	0x65	1	1	1
UART9_Config_1	[Register]	0x66	1	1	1
UART9_Config_2	[Register]	0x67	1	1	1

UART9_Config_3	[Register]	0x68	1	1	1
UART8_Config_1	[Register]	0x69	1	1	1
UART8_Config_2	[Register]	0x6A	1	1	1
UART8_Config_3	[Register]	0x6B	1	1	1
UART7_Config_1	[Register]	0x6C	1	1	1
UART7_Config_2	[Register]	0x6D	1	1	1
UART7_Config_3	[Register]	0x6E	1	1	1
UART6_Config_1	[Register]	0x6F	1	1	1
UART6_Config_2	[Register]	0x70	1	1	1
UART6_Config_3	[Register]	0x71	1	1	1
UART5_Config_1	[Register]	0x72	1	1	1
UART5_Config_2	[Register]	0x73	1	1	1
UART5_Config_3	[Register]	0x74	1	1	1
UART4_Config_1	[Register]	0x75	1	1	1
UART4_Config_2	[Register]	0x76	1	1	1
UART4_Config_3	[Register]	0x77	1	1	1
UART3_Config_1	[Register]	0x78	1	1	1
UART3_Config_2	[Register]	0x79	1	1	1
UART3_Config_3	[Register]	0x7A	1	1	1
UART2_Config_1	[Register]	0x7B	1	1	1
UART2_Config_2	[Register]	0x7C	1	1	1
UART2_Config_3	[Register]	0x7D	1	1	1
UART1_Config_1	[Register]	0x7E	1	1	1
UART1_Config_2	[Register]	0x7F	1	1	1
UART1_Config_3	[Register]	0x80	1	1	1

SPW3_Config	[Register]	0x87	1	1	1
SPW4_Config	[Register]	0x88	1	1	1
GPIOs_Leds_Control	[Register]	0x89	1	1	1
NACK_DISABLE	[Register]	0x8A	1	1	1
GPIO_Status	[Register]	0x8B	1	1	1
CTRL_SPWs_Errors	[Register]	0x8C	1	1	1
Ex_SPWs_Errors	[Register]	0x8D	1	1	1
UART40_Status	[Register]	0x8E	1	1	1
UART39_Status	[Register]	0x8F	1	1	1
UART38_Status	[Register]	0x90	1	1	1
UART37_Status	[Register]	0x91	1	1	1
UART36_Status	[Register]	0x92	1	1	1
UART35_Status	[Register]	0x93	1	1	1
UART34_Status	[Register]	0x94	1	1	1
UART33_Status	[Register]	0x95	1	1	1
UART32_Status	[Register]	0x96	1	1	1
UART31_Status	[Register]	0x97	1	1	1
UART30_Status	[Register]	0x98	1	1	1
UART29_Status	[Register]	0x99	1	1	1
UART28_Status	[Register]	0x9A	1	1	1
UART27_Status	[Register]	0x9B	1	1	1
UART26_Status	[Register]	0x9C	1	1	1
UART25_Status	[Register]	0x9D	1	1	1
UART24_Status	[Register]	0x9E	1	1	1
UART23_Status	[Register]	0x9F	1	1	1

UART22_Status	[Register]	0xA0	1	1	1
UART21_Status	[Register]	0xA1	1	1	1
UART20_Status	[Register]	0xA2	1	1	1
UART19_Status	[Register]	0xA3	1	1	1
UART18_Status	[Register]	0xA4	1	1	1
UART17_Status	[Register]	0xA5	1	1	1
UART16_Status	[Register]	0xA6	1	1	1
UART15_Status	[Register]	0xA7	1	1	1
UART14_Status	[Register]	0xA8	1	1	1
UART13_Status	[Register]	0xA9	1	1	1
UART12_Status	[Register]	0xAA	1	1	1
UART11_Status	[Register]	0xAB	1	1	1
UART10_Status	[Register]	0xAC	1	1	1
UART9_Status	[Register]	0xAD	1	1	1
UART8_Status	[Register]	0xAE	1	1	1
UART7_Status	[Register]	0xAF	1	1	1
UART6_Status	[Register]	0xB0	1	1	1
UART5_Status	[Register]	0xB1	1	1	1
UART4_Status	[Register]	0xB2	1	1	1
UART3_Status	[Register]	0xB3	1	1	1
UART2_Status	[Register]	0xB4	1	1	1
UART1_Status	[Register]	0xB5	1	1	1

2. Bundle Map

3. Register Descriptions

1. FPGA_Ver

Register: FPGA_Ver		**Register Information**			
Description					
Offset		0x0000	Type	RW	
ArraySize		1			
		Bitfield Details			
Bits	Name	Description	Param	Value	
7:0	data_reg		Type	Unsigned	
			Reset	0x00	
			Access	RW	

2. FPGA_Year

Register: FPGA_Year	**Register Information**
Description	

Offset		0x0001	Type	RW
ArraySize		1		
		Bitfield Details		
Bits	Name	Description	Param	Value
7:0	data_reg		Type	Unsigned
			Reset	0x00
			Access	RW

3. FPGA_Month

Register: FPGA_Month		**Register Information**		
Description				
Offset		0x0002	Type	RW
ArraySize		1		
		Bitfield Details		
Bits	Name	Description	Param	Value
7:0	data_reg		Type	Unsigned
			Reset	0x00
			Access	RW

4. FPGA_Day

Register: FPGA_Day		Register Information			
Description					
Offset		0x0003	Type	RW	
ArraySize		1			
		Bitfield Details			
Bits	Name	Description	Param	Value	
7:0	data_reg		Type	Unsigned	
			Reset	0x00	
			Access	RW	

5. Reset_UART_40_33

Register: Reset_UART_40_33		Register Information			
Description					
Offset		0x0004	Type	RW	
ArraySize		1			
		Bitfield Details			
Bits	Name	Description	Param	Value	
0:0	rst_uart_33	Global Enum: RESET_OPER	Type	Unsigned	
			Reset	0x0	
			Access	RW	
1:1	rst_uart_34	Global Enum: RESET_OPER	Type	Unsigned	
			Reset	0x0	

			Access	RW
2:2	rst_uart_35	Global Enum: RESET_OPER	Type	Unsigned
			Reset	0x0
			Access	RW
3:3	rst_uart_36	Global Enum: RESET_OPER	Type	Unsigned
			Reset	0x0
			Access	RW
4:4	rst_uart_37	Global Enum: RESET_OPER	Type	Unsigned
			Reset	0x0
			Access	RW
5:5	rst_uart_38	Global Enum: RESET_OPER	Type	Unsigned
			Reset	0x0
			Access	RW
6:6	rst_uart_39	Global Enum: RESET_OPER	Type	Unsigned
			Reset	0x0
			Access	RW
7:7	rst_uart_40	Global Enum: RESET_OPER	Type	Unsigned
			Reset	0x0
			Access	RW

6. UART40_Config_1

Register: UART40_Config_1	Register Information

Description					
Offset		0x0009	Type	RW	
ArraySize		1			
		Bitfield Details			
Bits	Name	Description	Param	Value	
6:0	TimeOut	For transmitting data – Salience time between sending 2 packets, represented by no. of UART's bits For receiving data - Verifing received packet when the UART's RXD signal value is '1' for timeout x UART bits	Type	Unsigned	
			Reset	0x32	
			Access	RW	
7:7	Reserved1		Type	Unsigned	
			Reset	0x0	
			Access	RW	

7. UART40_Config_2

Register: UART40_Config_2		**Register Information**			
Description					
Offset		0x000A	Type	RW	
ArraySize		1			
		Bitfield Details			
Bits	Name	Description	Param	Value	
1:0	Parity	00 - None 01 - Odd 10 - Even 11 - NA Global Enum: PARITY	Type	Unsigned	
			Reset	0x0	
			Access	RW	

2:2	Stop_bit	0' – 1 stop bit '1' – 2 stop sits Global Enum: TWO_ONE	Type	Unsigned
			Reset	0x0
			Access	RW
3:3	Start_bit	NA	Type	Unsigned
			Reset	0x0
			Access	NA
7:4	Baud_Rate	921600 = 0x9; 460800 = 0x8; 230400 = 0x7; 115200 = 0x6 (Default); 57600 = 0x5; 38400 = 0x4; 28800 = 0x3; 19200 = 0x2; 14400 = 0x1; 9600 = 0x0; Global Enum: BAUD_RATE	Type	Unsigned
			Reset	0x6
			Access	RW

8. UART40_Config_3

Register: UART40_Config_3		**Register Information**		
Description				
Offset		0x000B	Type	RW
ArraySize		1		
		Bitfield Details		
Bits	Name	Description	Param	Value
0:0	UART_Enable	0' - Enabled '1' - Disabled When disabled, the receive and transmit channels content are ignored. Global Enum: ENABLE_DISABLE	Type	Unsigned
			Reset	0x0
			Access	RW
1:1	TX_Enable	0' - Auto '1' - Always On In Auto mode_ When transmitter data available, all Uarts transmitters' outputs (TX) shall	Type	Unsigned
			Reset	0x0

		be automatically enabled. Where no data is transmitted, TX enable shall be automatically disabled. all UARts acts as RS485. IN Always ON mode_ Enable shall be implemented thus, all UARts acts as RS422. Global Enum: TX_ENABLE	Access	RW
2:2	DataLength	8bits	Type	Unsigned
			Reset	0x0
			Access	NA
7:3	Reserved1		Type	Unsigned
			Reset	0x00
			Access	RW

9. Broadcast_UART_40_33

Register: Broadcast_UART_40_33		**Register Information**		
Description				
Offset		0x0081	Type	RW
ArraySize		1		
		Bitfield Details		
Bits	Name	Description	Param	Value
0:0	bc_uart_33	Global Enum: ENABLE_DISABLE	Type	Unsigned
			Reset	0x0
			Access	RW
1:1	bc_uart_34		Type	Unsigned

		Global Enum: ENABLE_DISABLE	Reset	0x0
			Access	RW
2:2	bc_uart_35	Global Enum: ENABLE_DISABLE	Type	Unsigned
			Reset	0x0
			Access	RW
3:3	bc_uart_36	Global Enum: ENABLE_DISABLE	Type	Unsigned
			Reset	0x0
			Access	RW
4:4	bc_uart_37	Global Enum: ENABLE_DISABLE	Type	Unsigned
			Reset	0x0
			Access	RW
5:5	bc_uart_38	Global Enum: ENABLE_DISABLE	Type	Unsigned
			Reset	0x0
			Access	RW
6:6	bc_uart_39	Global Enum: ENABLE_DISABLE	Type	Unsigned
			Reset	0x0
			Access	RW
7:7	bc_uart_40	Global Enum: ENABLE_DISABLE	Type	Unsigned
			Reset	0x0
			Access	RW

10. Broadcast_SPW_3_4

Register: Broadcast_SPW_3_4		Register Information			
Description					
Offset		0x0086	Type	RW	
ArraySize		1			
		Bitfield Details			
Bits	Name	Description	Param	Value	
0:0	bc_spw_3	Global Enum: ENABLE_DISABLE	Type	Unsigned	
			Reset	0x0	
			Access	RW	
1:1	bc_spw_4	Global Enum: ENABLE_DISABLE	Type	Unsigned	
			Reset	0x0	
			Access	RW	
7:2	Reserved		Type	Unsigned	
			Reset	0x00	
			Access	RW	

11. SPW3_Config

Register: SPW3_Config	Register Information		
Description			
Offset	0x0087	Type	RW
ArraySize	1		
	Bitfield Details		

Bits	Name	Description	Param	Value
1:0	SPW3_Data_Rate	When in External mode 00 – 9.6Mbps 01 – 12Mbps 10 – 16Mbps 11 – 24Mbps Global Enum: SPW_RATE	Type	Unsigned
			Reset	0x0
			Access	RW
7:2	Reserved1		Type	Unsigned
			Reset	0x00
			Access	RW

12. GPIOs_Leds_Control

Register: GPIOs_Leds_Control		**Register Information**		
Description				
Offset		0x0089	Type	RW
ArraySize		1		
		Bitfield Details		
Bits	Name	Description	Param	Value
0:0	GP_OUT_0	0' – LOW, '1' - HIGH Global Enum: HIGH_LOW	Type	Unsigned
			Reset	0x0
			Access	RW
1:1	GP_OUT_1	0' – LOW, '1' - HIGH Global Enum: HIGH_LOW	Type	Unsigned
			Reset	0x0
			Access	RW
2:2	GP_OUT_2		Type	Unsigned

		0' – LOW, '1' - HIGH Global Enum: HIGH_LOW	Reset	0x0
			Access	RW
3:3	LED_0	0' – Blinking @1Hz '1' - ON Global Enum: HIGH_LOW	Type	Unsigned
			Reset	0x0
			Access	RW
4:4	LED_1	ON – '1', OFF – '0 Global Enum: HIGH_LOW	Type	Unsigned
			Reset	0x0
			Access	RW
5:5	LED_2	ON – '1', OFF – '0 Global Enum: HIGH_LOW	Type	Unsigned
			Reset	0x0
			Access	RW
7:6	Reserved1		Type	Unsigned
			Reset	0x0
			Access	RW

13. NACK_DISABLE

Register: NACK_DISABLE		**Register Information**		
Description				
Offset		0x008A	Type	RW
ArraySize		1		
		Bitfield Details		
Bits	Name	Description	Param	Value

0:0	NACK_DISABLE	Global Enum: ENABLE_DISABLE	Type	Unsigned
			Reset	0x0
			Access	RO
7:1	Reserved		Type	Unsigned
			Reset	0x00
			Access	NA

14. GPIO_Status

Register: GPIO_Status		**Register Information**		
Description				
Offset		0x008B	Type	RO
ArraySize		1		
		Bitfield Details		
Bits	Name	Description	Param	Value
0:0	GP_IN_0	Global Enum: HIGH_LOW	Type	Unsigned
			Reset	0x0
			Access	RO
1:1	GP_IN_1	Global Enum: HIGH_LOW	Type	Unsigned
			Reset	0x0
			Access	RO
2:2	GP_IN_2	Global Enum: HIGH_LOW	Type	Unsigned
			Reset	0x0

			Access	RO
7:3	Reserved1		Type	Unsigned
			Reset	0x00
			Access	NA

15. CTRL_SPWs_Errors

Register: CTRL_SPWs_Errors		**Register Information**		
Description				
Offset		0x008C	Type	RO
ArraySize		1		
		Bitfield Details		
Bits	Name	Description	Param	Value
0:0	SPW_main_header_error	Global Enum: ERROR_OK	Type	Unsigned
			Reset	0x0
			Access	RO
1:1	SPW_main_cs_error	Global Enum: ERROR_OK	Type	Unsigned
			Reset	0x0
			Access	RO
2:2	SPW_main_channle_error	Global Enum: ERROR_OK	Type	Unsigned
			Reset	0x0
			Access	RO
3:3	SPW_redu_channle_error		Type	Unsigned

		Global Enum: ERROR_OK	Reset	0x0
			Access	RO
4:4	SPW_redu_header_error	Global Enum: ERROR_OK	Type	Unsigned
			Reset	0x0
			Access	RO
5:5	SPW_redu_cs_error	When in Redandency mode Global Enum: ERROR_OK	Type	Unsigned
			Reset	0x0
			Access	RO
7:6	Reserved		Type	Unsigned
			Reset	0x0
			Access	NA

16. Ex_SPWs_Errors

Register: Ex_SPWs_Errors		**Register Information**		
Description				
Offset		0x008D	Type	RO
ArraySize		1		
		Bitfield Details		
Bits	Name	Description	Param	Value
0:0	SPW_ex3_EEP	Global Enum: ERROR_OK	Type	Unsigned
			Reset	0x0
			Access	RO

1:1	SPW_ex4_EEP	Global Enum: ERROR_OK	Type	Unsigned
			Reset	0x0
			Access	RO
7:2	Reserved		Type	Unsigned
			Reset	0x00
			Access	NA

17. UART40_Status

Register: UART40_Status		**Register Information**			
Description		CLR - Latched register, Clear on read mechanism			
Offset		0x008E	Type	RO	
ArraySize		1			
		Bitfield Details			
Bits	Name	Description	Param	Value	
0:0	RX_FIFO_Empty	Global Enum: EMPTY_FULL	Type	Unsigned	
			Reset	0x0	
			Access	RO	
1:1	RX_FIFO_Full	Global Enum: FULL_EMPTY	Type	Unsigned	
			Reset	0x0	
			Access	RO	
2:2	TX_FIFO_Empty	Global Enum: EMPTY_FULL	Type	Unsigned	
			Reset	0x0	

			Access	RO
3:3	TX_FIFO_Full	Global Enum: FULL_EMPTY	Type	Unsigned
			Reset	0x0
			Access	RO
4:4	Parity_Error	Valid for last transmit Global Enum: ERROR_OK	Type	Unsigned
			Reset	0x0
			Access	RO
5:5	OVERRUN_Error	Indicates that a new data was received by the UART, while previous data was not read, meaning RX_RD_EN was not asserted between two consecutive RX_VALID assertions Global Enum: ERROR_OK	Type	Unsigned
			Reset	0x0
			Access	RO
6:6	FRAME_Error	Indicates that the stop bit(s) is zero (valid STOP bit is to be '1') Global Enum: ERROR_OK	Type	Unsigned
			Reset	0x0
			Access	RO
7:7	RBRK_Error	Receiver Brake indication (during idle condition, there is continues zero on RX_SERIAL bit) Global Enum: ERROR_OK	Type	Unsigned
			Reset	0x0
			Access	RO