

NOTE:

One LpGBT: 28 data pairs @ 320Mbps
10.24Gbps&FEC5 EDIN[6:0][3:0]. 8 CHs ADC
--> CSM use 20 of 28 links per chip
One GBT-SCA: 31 ADC INPUT CHs, 31 used by FE Monitoring
32th for embedded temp sensor
--> FE use 20*6=120 of 124(31*4)

To LpGBT Chip 0

CN0

LpGBT0: MEZZ 0-9
LpGBT1: MEZZ 10-19

LpGBT0 Group 6 Elink 3&2

MEZZ 0

LpGBT0 Group 6 Elink 1&0

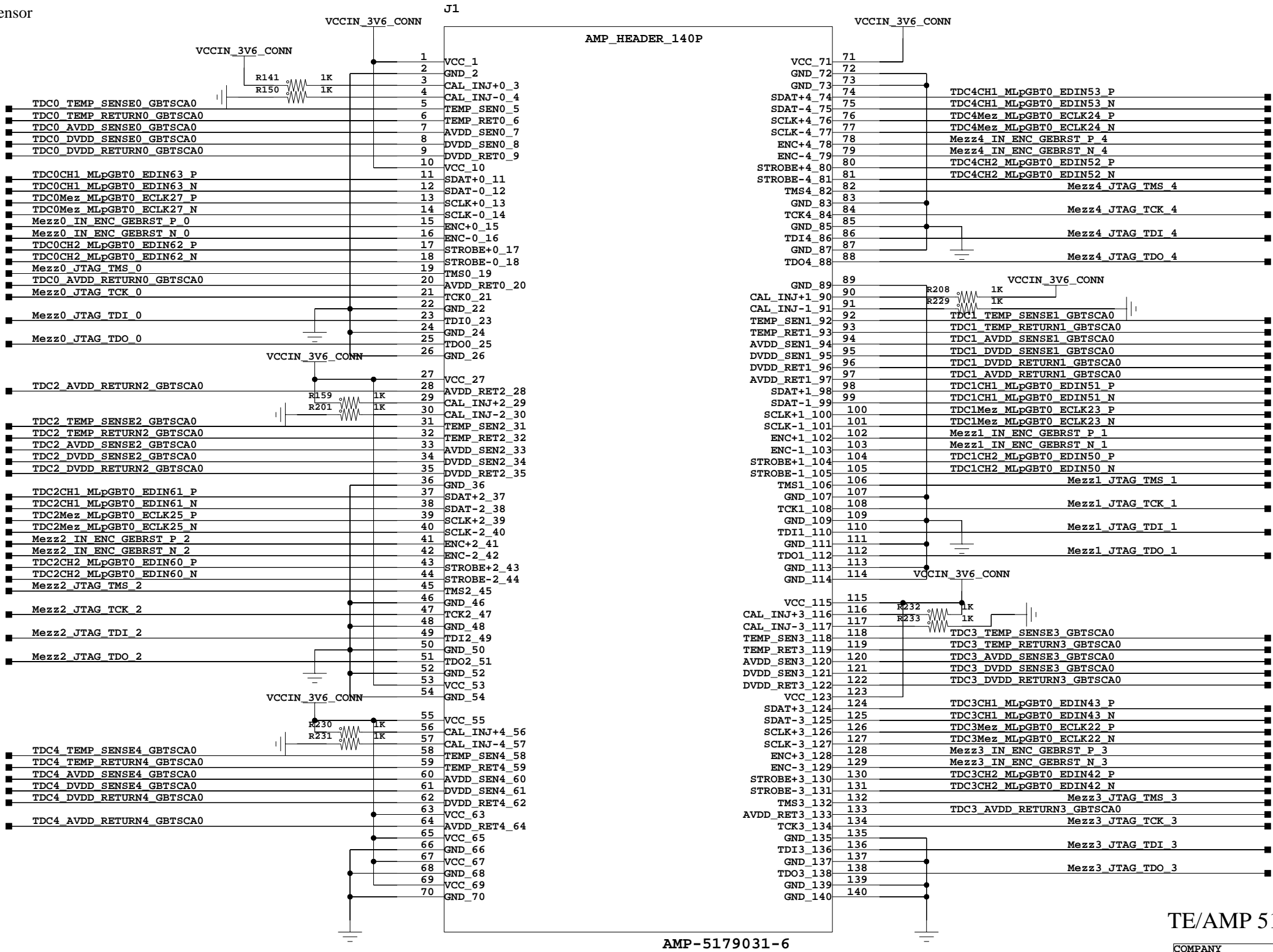
MEZZ 2

LpGBT0 Group 5 Elink 3&2

MEZZ 4

Summary:

CN0 140pin AMP connector handle 5 TDC Mezzs: TDC0-TDC4
TDC Mezz 0-4 Data handled by master LpGBT0



LpGBT0 Group 5 Elink 3&2

MEZZ 4 Cont'


LpGBT0 Group 5 Elink 1&0

MEZZ 1

LpGBT0 Group 4 Elink 3&2

MEZZ 3

TE/AMP 5179031-6 140PIN CONN.

COMPANY					
University of Michigan					
TITLE					
LpGBT_CSM Pre-production					
SIZE	B	REV	SHEET	1	OF N
DRAWN	XUEYE HU		DATE	22/05/2023:16:41	

To LpGBT Chip 0

LpGBT0: MEZZ 0-9

LpGBT1: MEZZ 10-19

CN1

LpGBT0 Group 0 Elink 0&1

MEZZ 6

LpGBT0 Group 0 Elink 2&3

MEZZ 8

LpGBT0 Group 2 Elink 0&1

MEZZ 9

LpGBT0 Group 1 Elink 0&1

MEZZ 5

LpGBT0 Group 1 Elink 2&3

MEZZ 7

LpGBT0 Group 2 Elink 0&1

MEZZ 9 Cont'


Summary:

CN1 140pin AMP connector handle 5 TDC Mezzs: TDC5-TDC9

TDC Mezz 5-9 Data handled by master LpGBT0

TE/AMP 5179031-6 140PIN CONN.

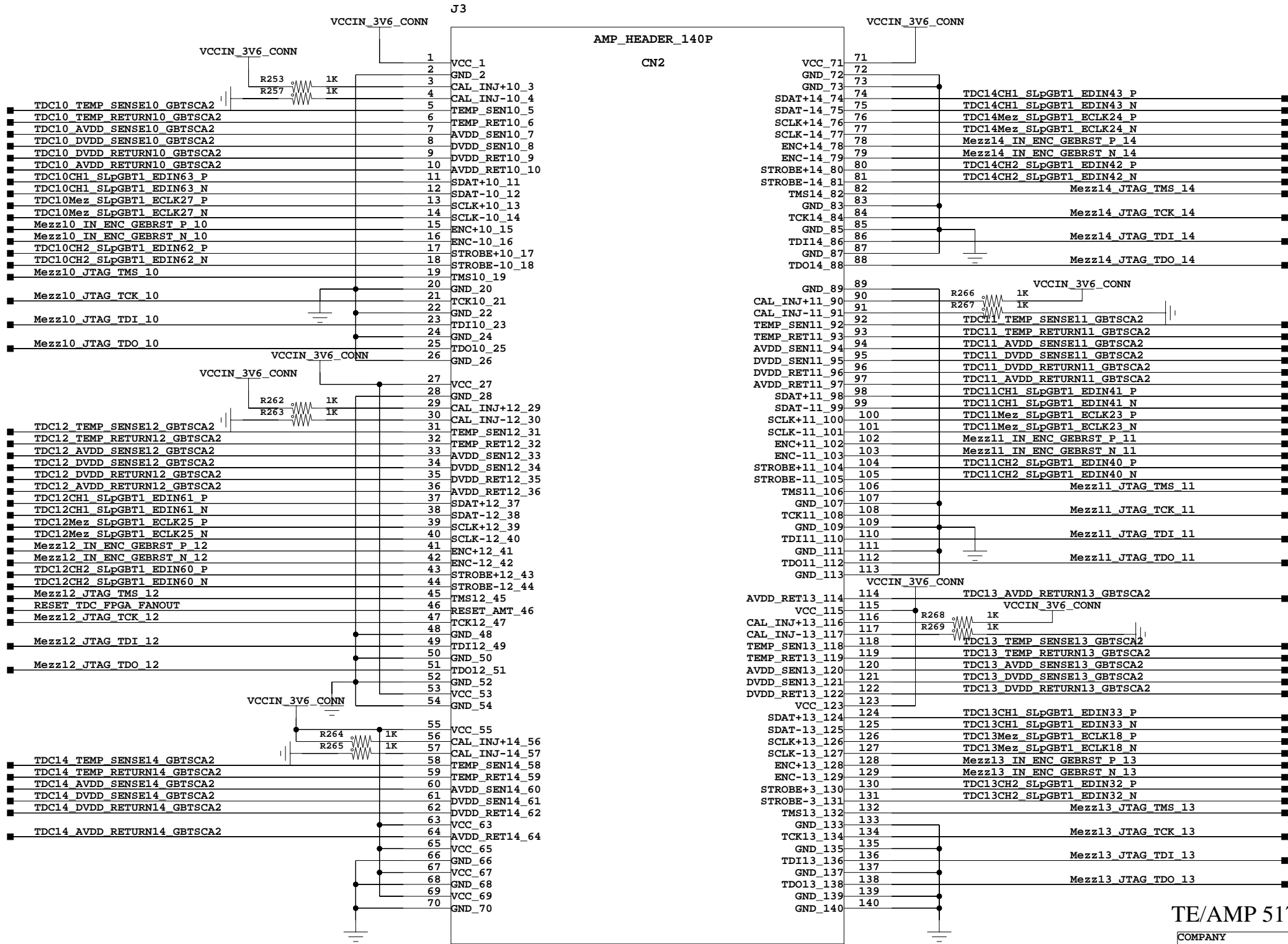
AMP-5179031-6

COMPANY					
University of Michigan					
TITLE					
LpGBT_CSM Pre-production					
SIZE	B	REV	SHEET	2	OF N
DRAWN	XUEYE HU		DATE	22/05/2023:16:42	

To LpGBT Chip 1

LpGBT0: MEZZ 0-9
LpGBT1: MEZZ 10-19

CN2



LpGBT1 Group 6 Elink 3&2

MEZZ 10

LpGBT1 Group 6 Elink 1&0

MEZZ 12

* Source RESET For All Mezz. -->
Was named as RESET_AMT_A7_SERVING

LpGBT1 Group 4 Elink 3&2

MEZZ 14

LpGBT1 Group 4 Elink 3&2

MEZZ 14 Cont'

LpGBT1 Group 4 Elink 1&0

MEZZ 11

LpGBT1 Group 3 Elink 3&2


MEZZ 13

Summary:

CN2 140pin AMP connector handle 5 TDC Mezzs: TDC10-TDC14

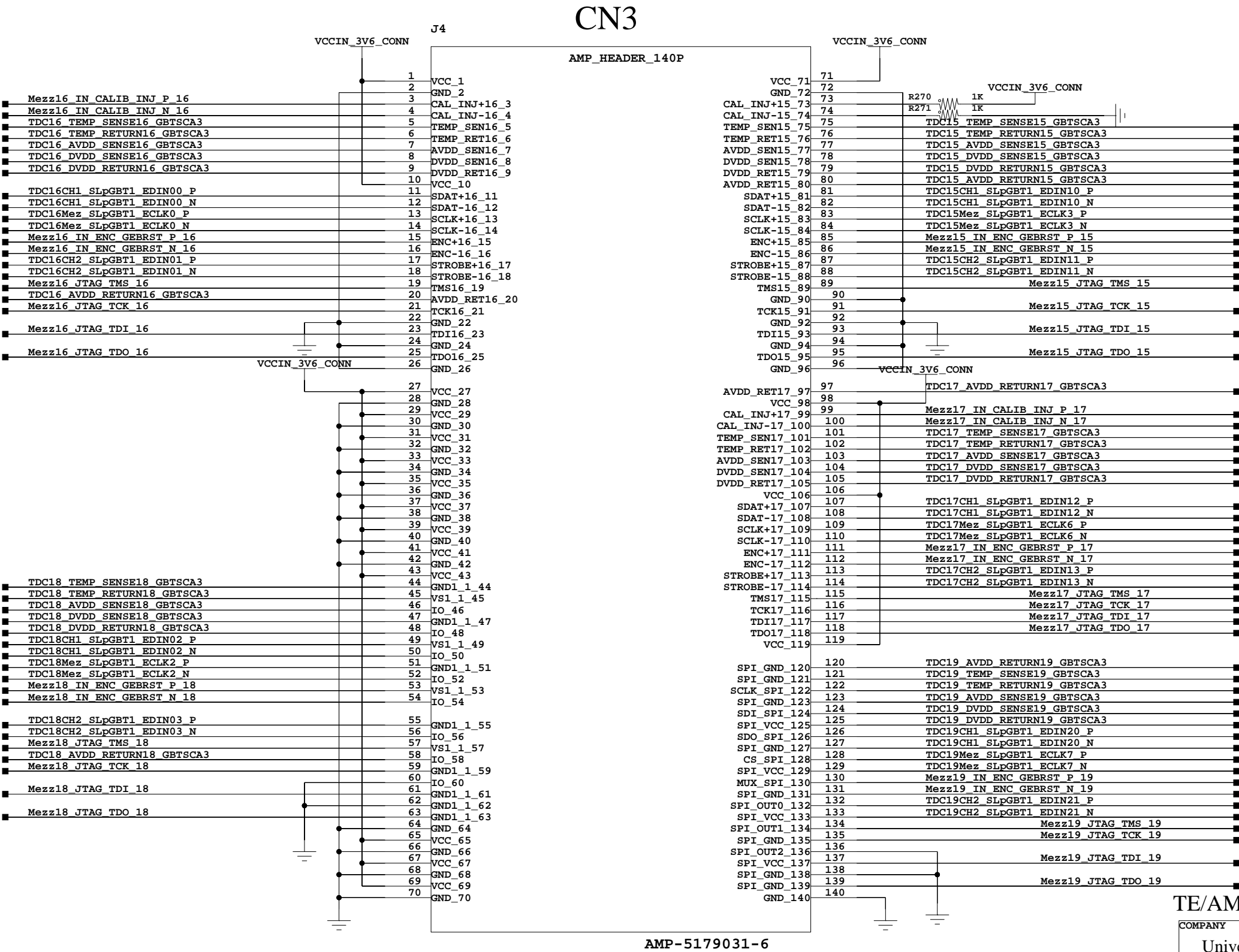
TDC Mezz 10-14 Data handled by slave LpGBT1

TE/AMP 5179031-6 140PIN CONN.

COMPANY					
University of Michigan					
TITLE					
LpGBT_CSM Pre-production					
SIZE	B	REV	SHEET	3	OF N
DRAWN	XUEYE HU		DATE	22/05/2023:16:42	

To LpGBT Chip 1

LpGBT0: MEZZ 0-9
LpGBT1: MEZZ 10-19



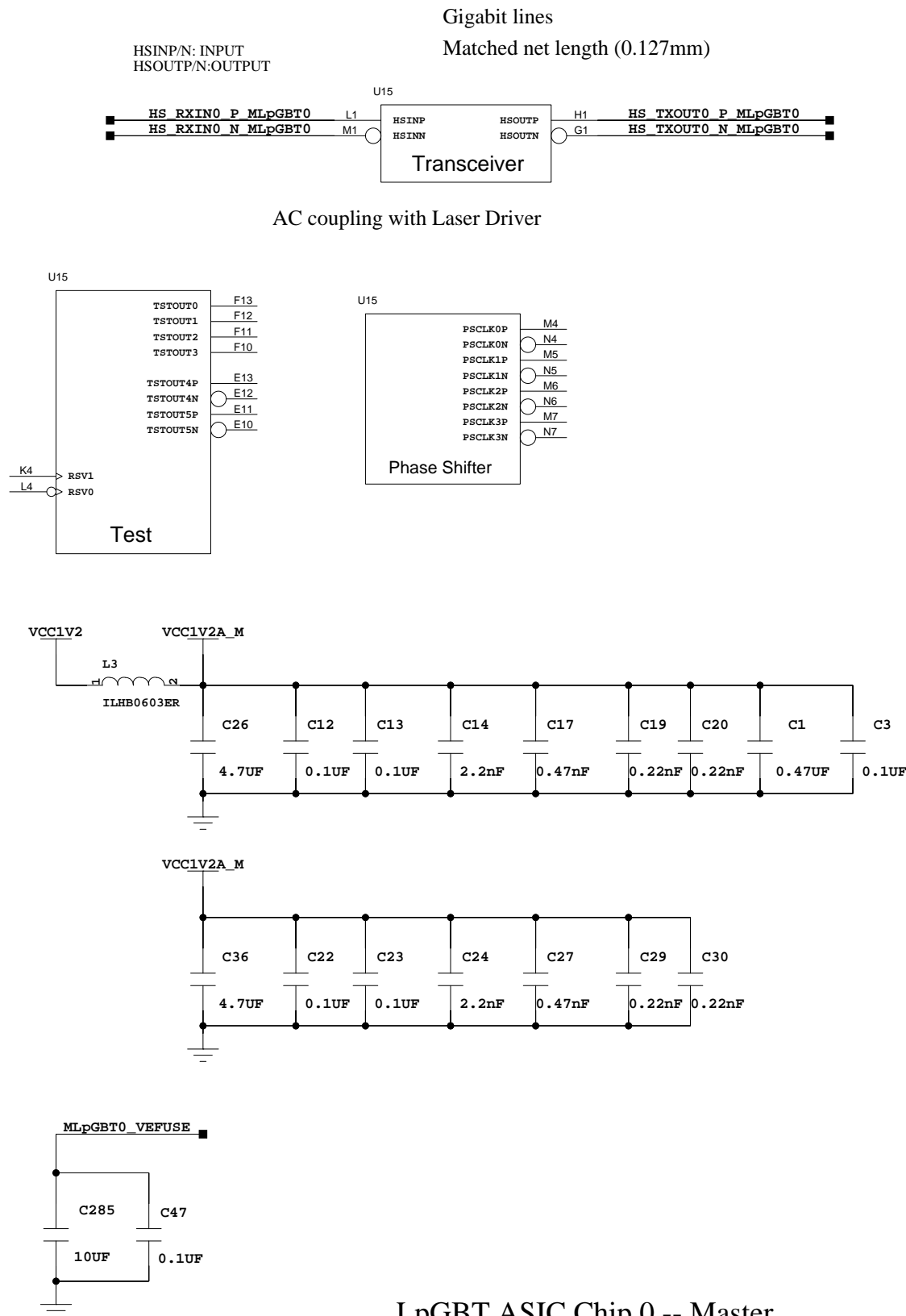
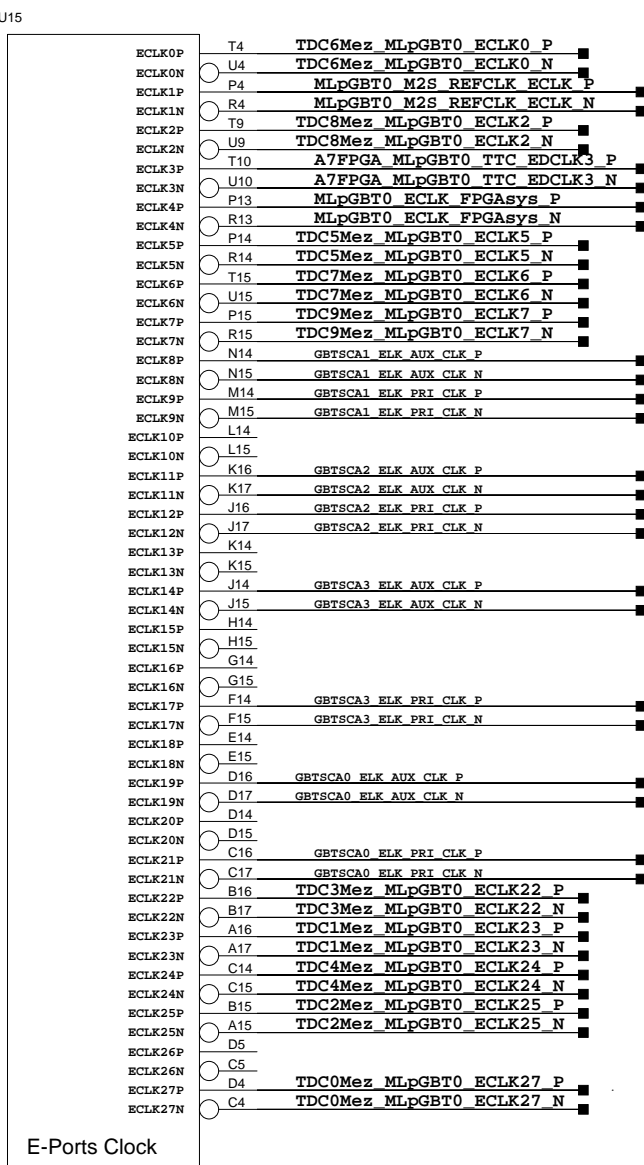
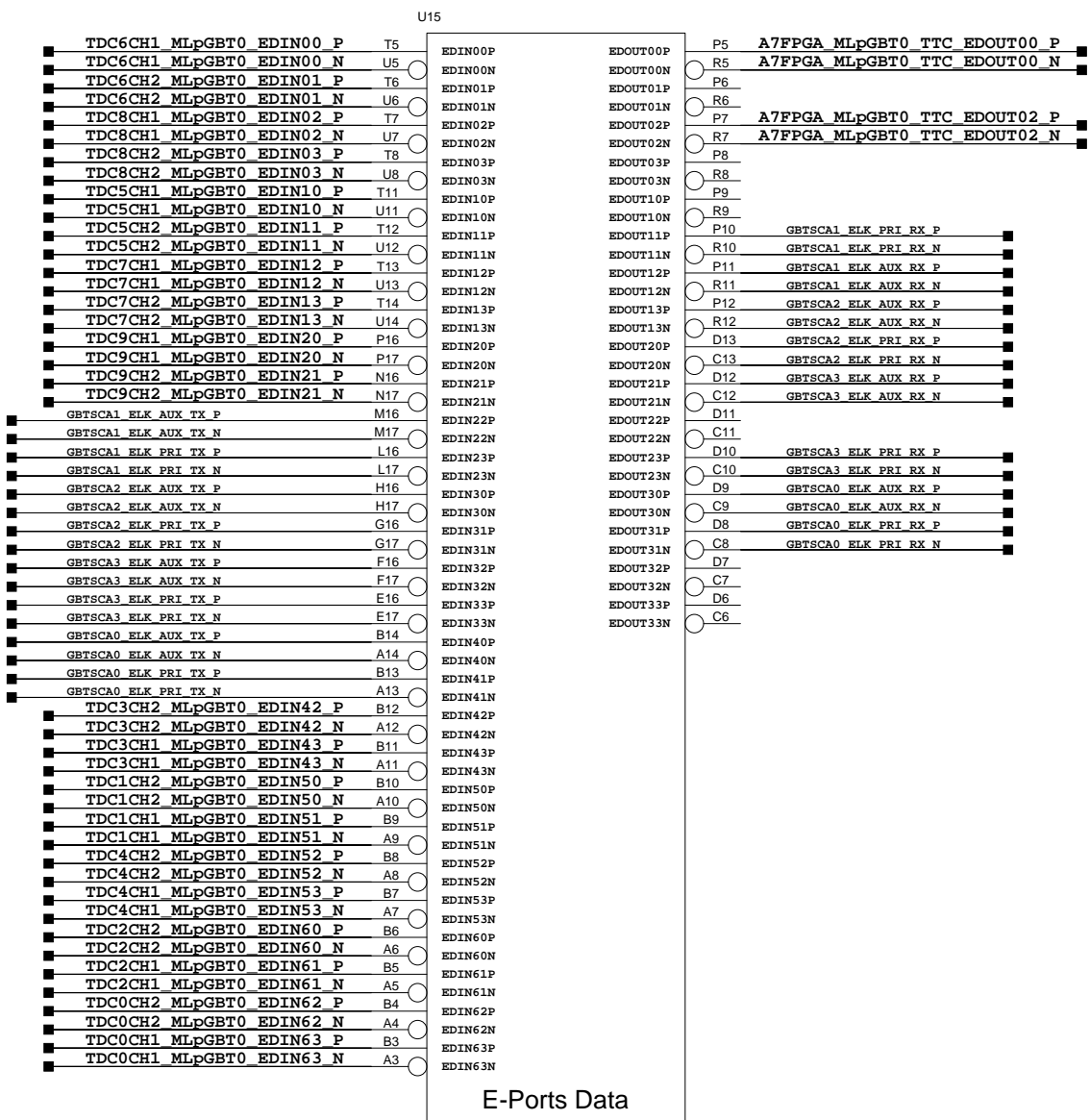
Summary:

CN3 140pin AMP connector handle 5 TDC Mezzs: TDC15-TDC19
TDC Mezz 15-19 Data handled by slave LpGBT1


TE/AMP 5179031-6 140PIN CONN.

COMPANY			<div><div></div><div>M</div></div>		
University of Michigan					
TITLE					
LpGBT_CSM Pre-production					
SIZE	B	REV	SHEET	4	OF N
DRAWN	XUEYE HU		DATE	22/05/2023:16:43	

Master LpGBT0 Transceiver mode



LpGBT ASIC Chip 0 -- Master

COMPANY					
University of Michigan					
TITLE					
LpGBT_CSM Pre-production					
SIZE	B	REV	SHEET	5	OF N
DRAWN	XUEYE HU		DATE	26/06/2022:23:31	

4

3

2

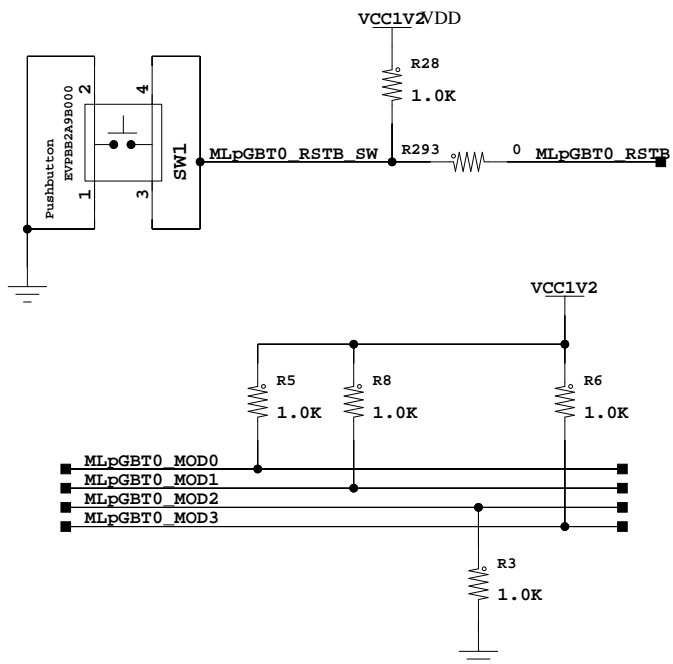
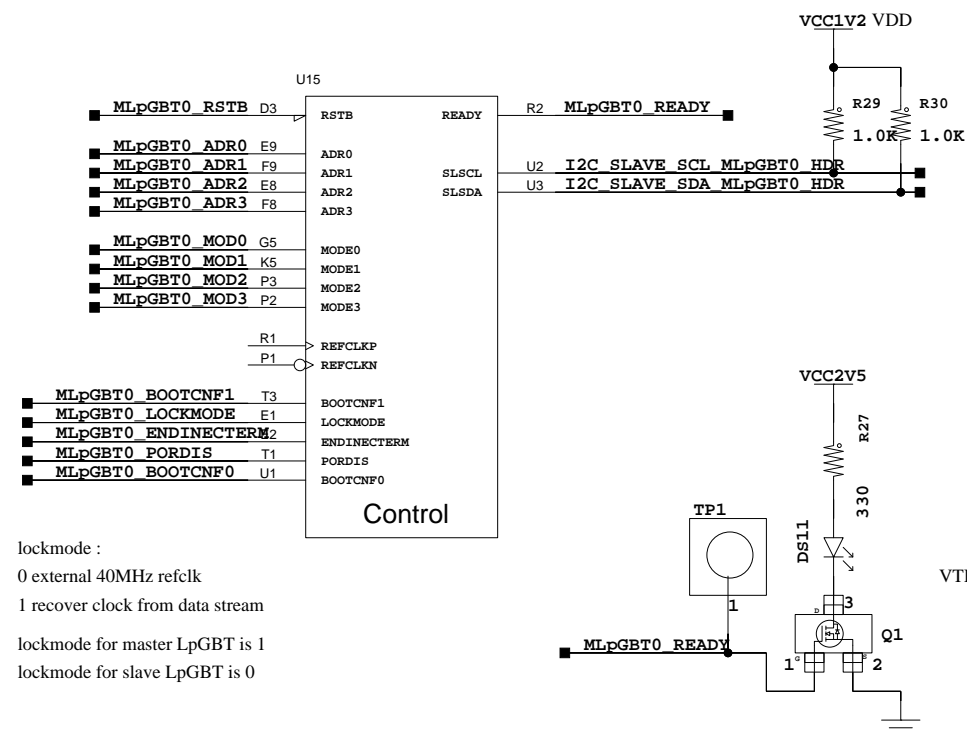
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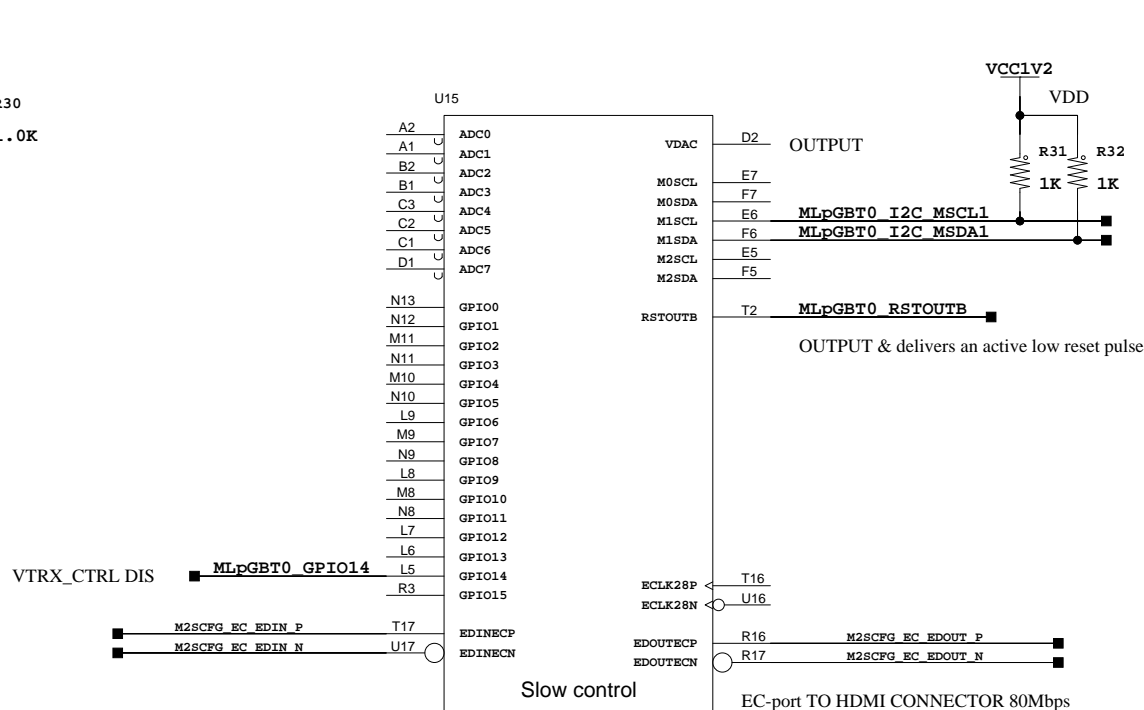
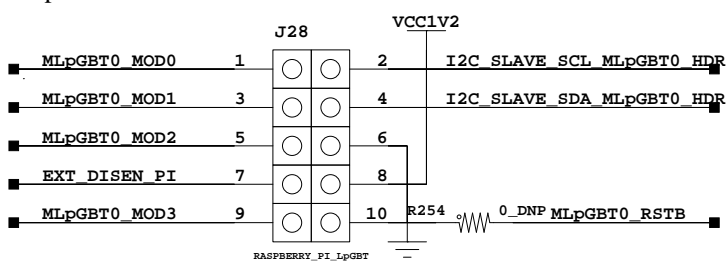
2

1

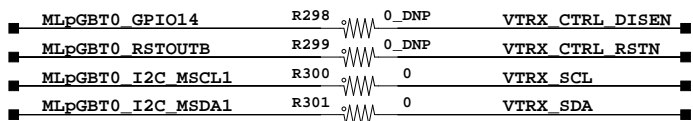


MODE [3:0] 1011: 10Gbps FEC5 Transceiver

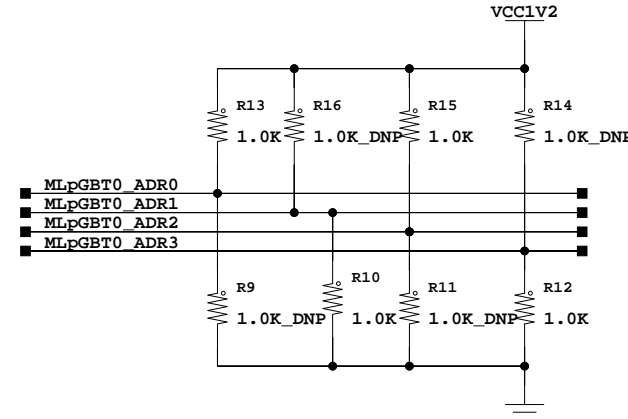
MLpGBT CONFIG FROM RASPBERRY PI



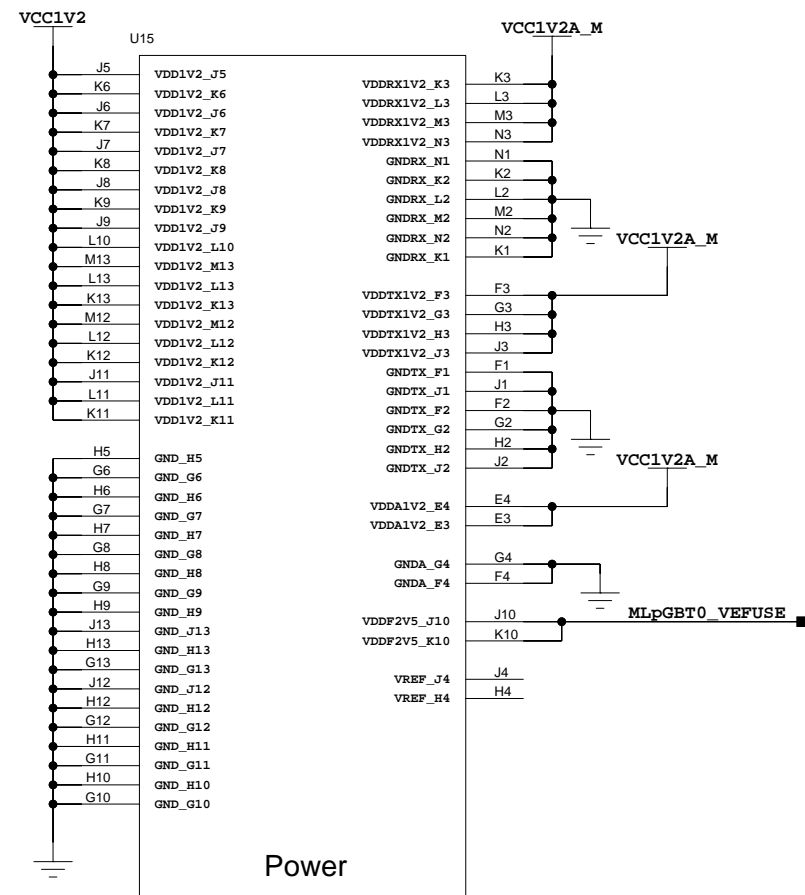
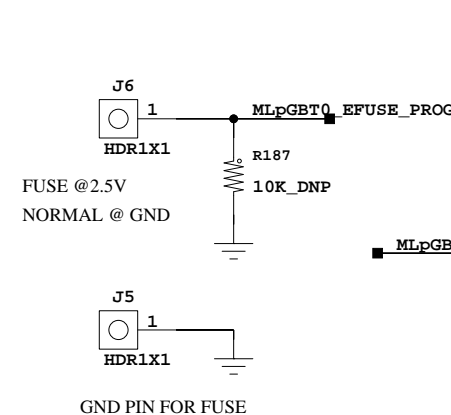
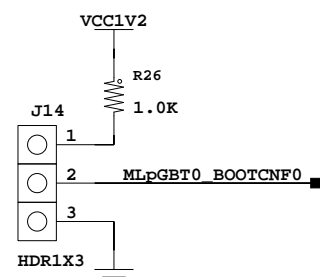
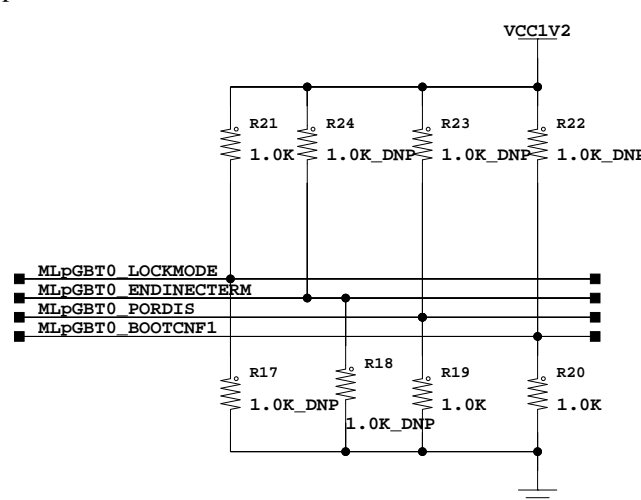
MLpGBT CONTROL VTRX




MLpGBT I2C/IC/EC address: 7'h75



MLpGBT CONTROL

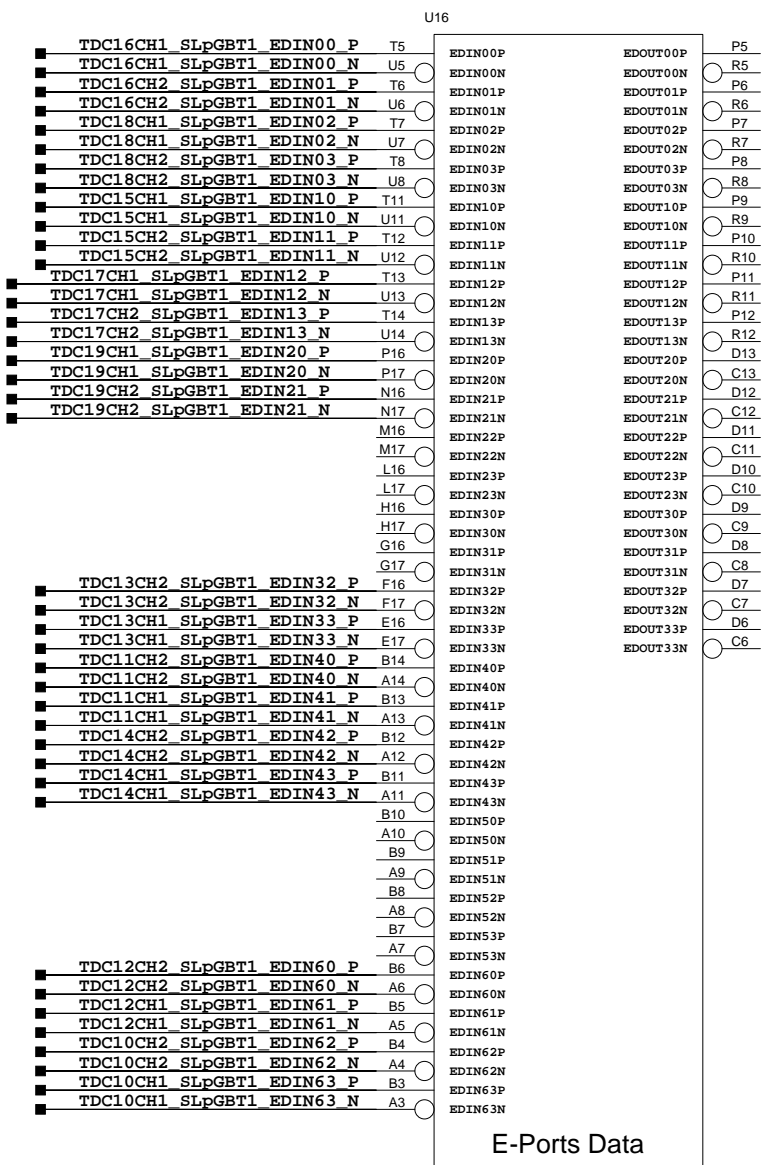


LpGBT ASIC Chip 0 -- Master

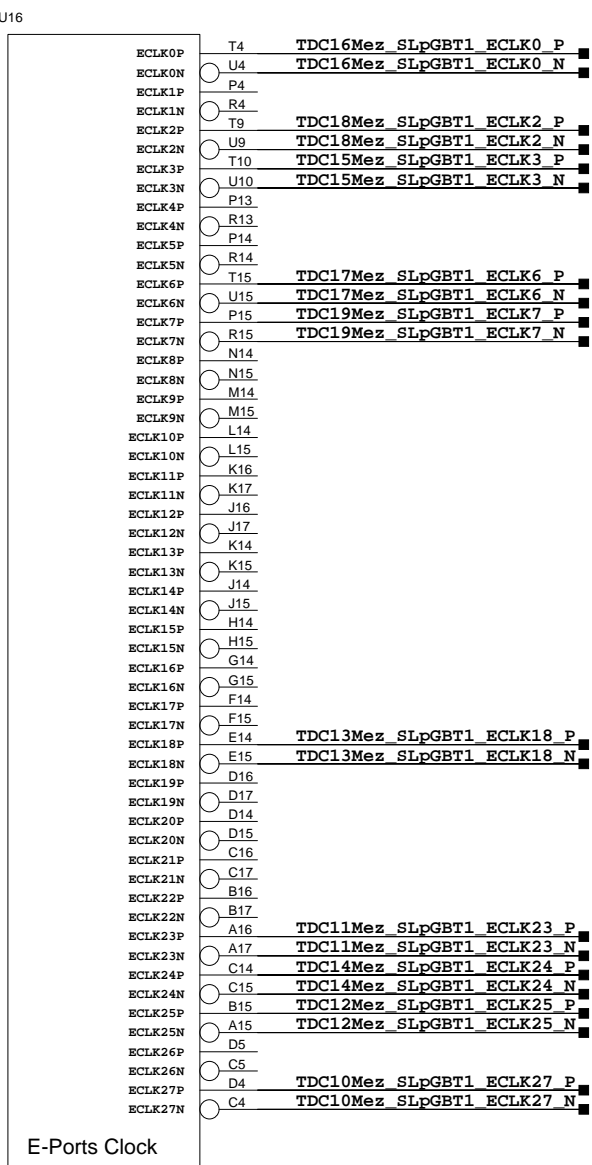
COMPANY					
University of Michigan					
TITLE					
LpGBT_CSM Prototype v2					
SIZE	B	REV	SHEET	6	OF N
DRAWN	XUEYE HU		DATE	22/05/2023:16:43	

Slave LpGBT1

Simplex TX mode



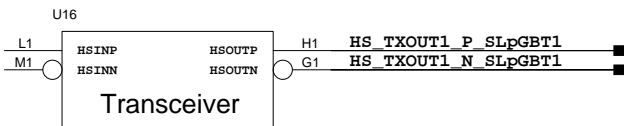
EDOUT UNAVAILABLE



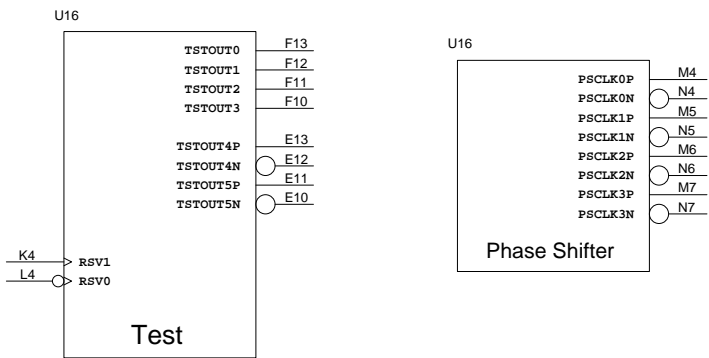
HSINP/N: INPUT
HSOUTP/N: OUTPUT

Gigabit lines

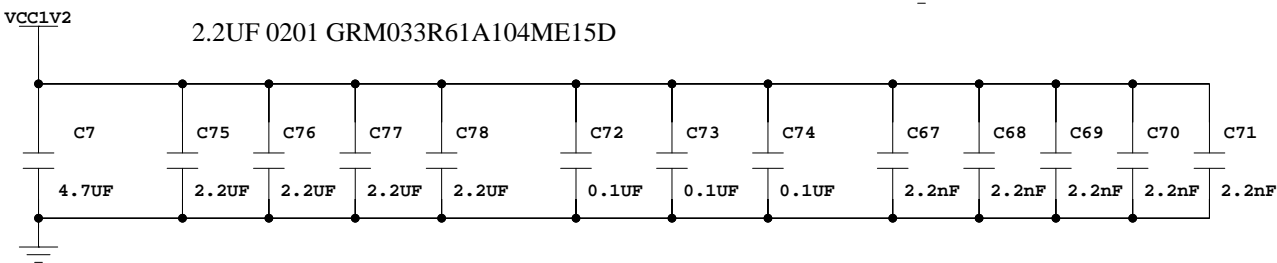
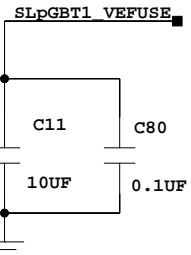
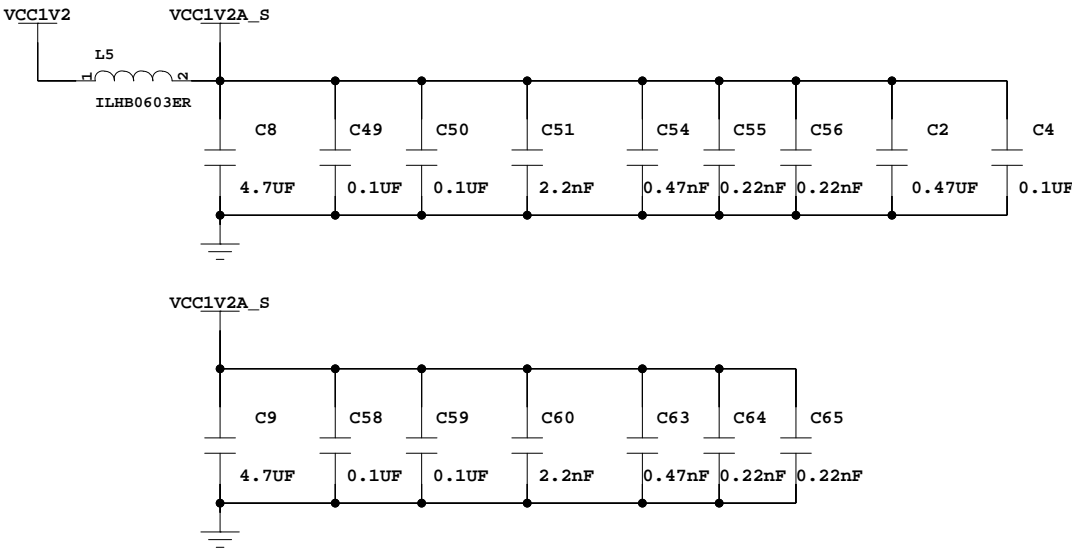
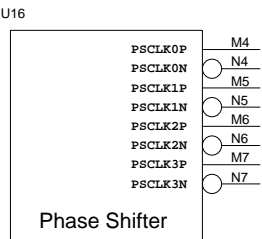
Matched net length (0.127mm)




AC coupling with Laser Driver



CH0 & 3 under-performing



LpGBT ASIC Chip 1 -- Slave

COMPANY					
University of Michigan					
TITLE					
LpGBT_CSM Prototype v2					
SIZE	B	REV	SHEET	7	OF N
DRAWN	XUEYE HU		DATE	24/03/2022:09:38	

4

3

2

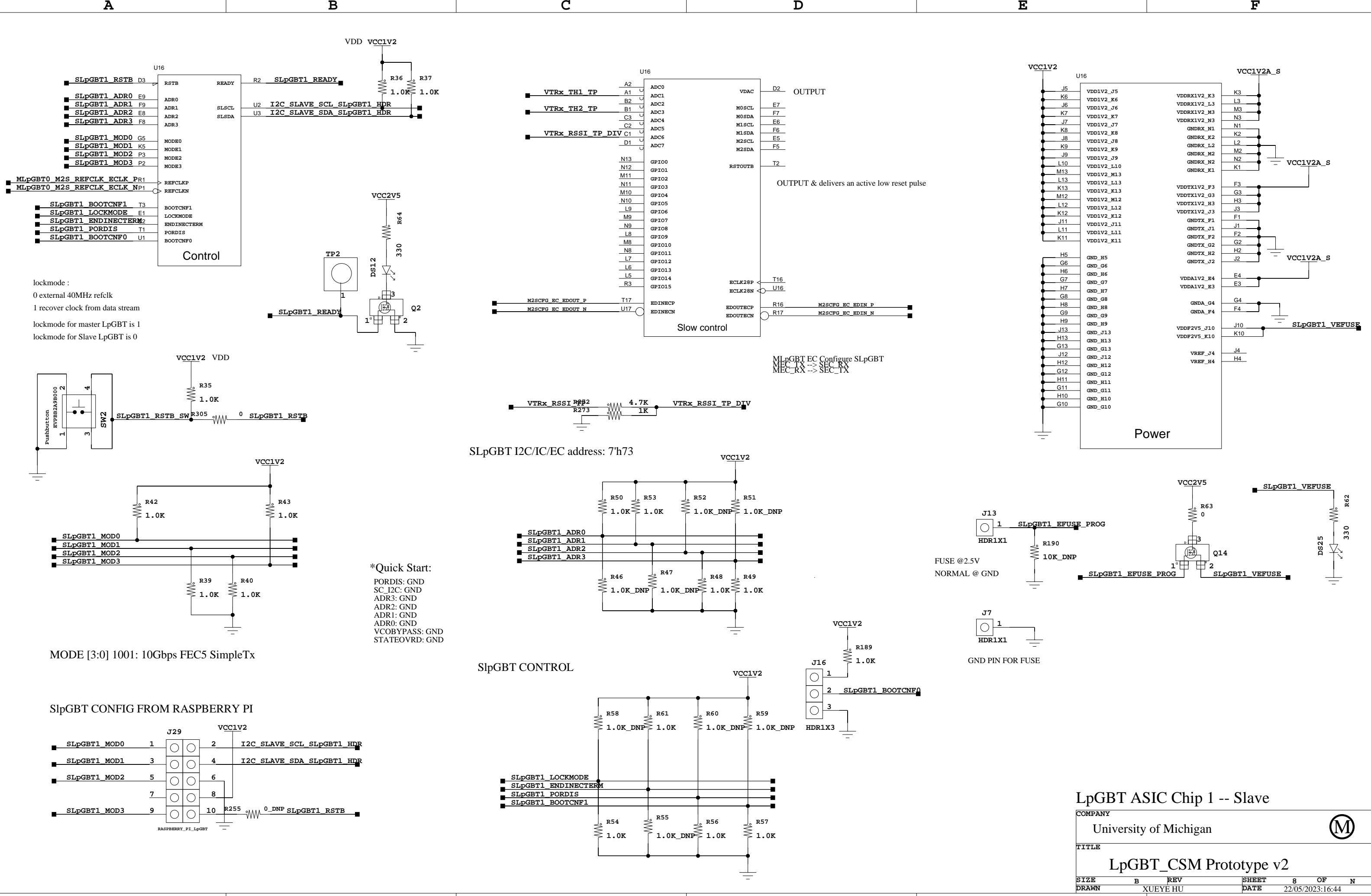
1

4

3

2

1



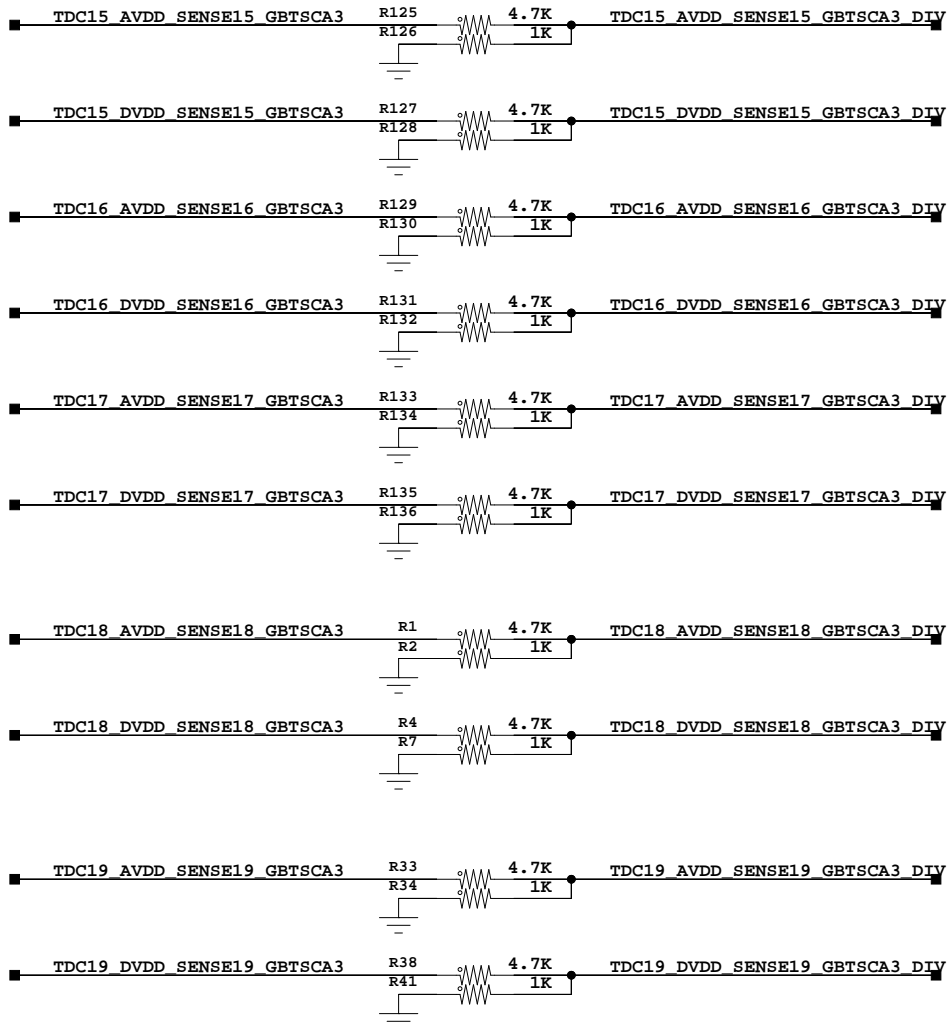
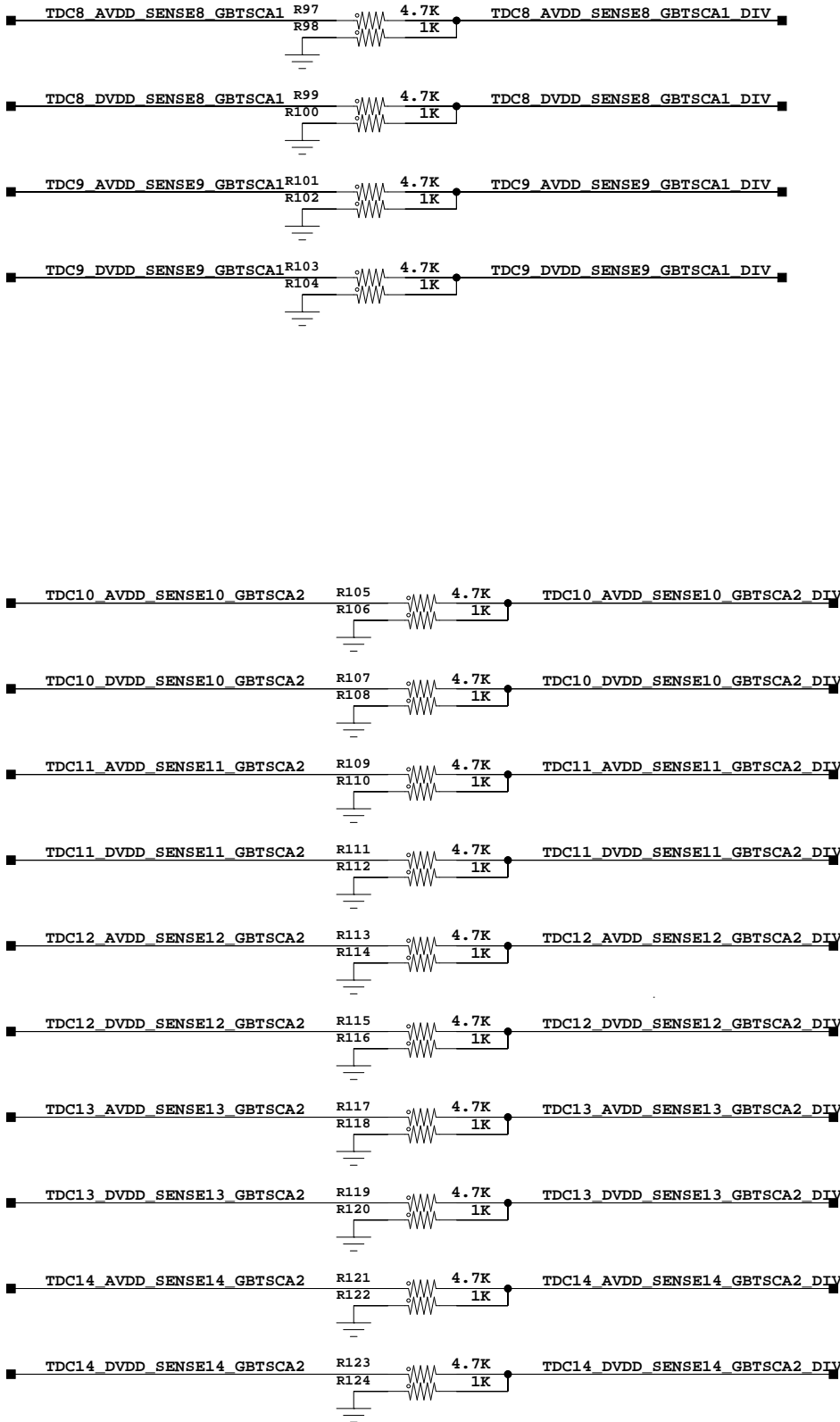
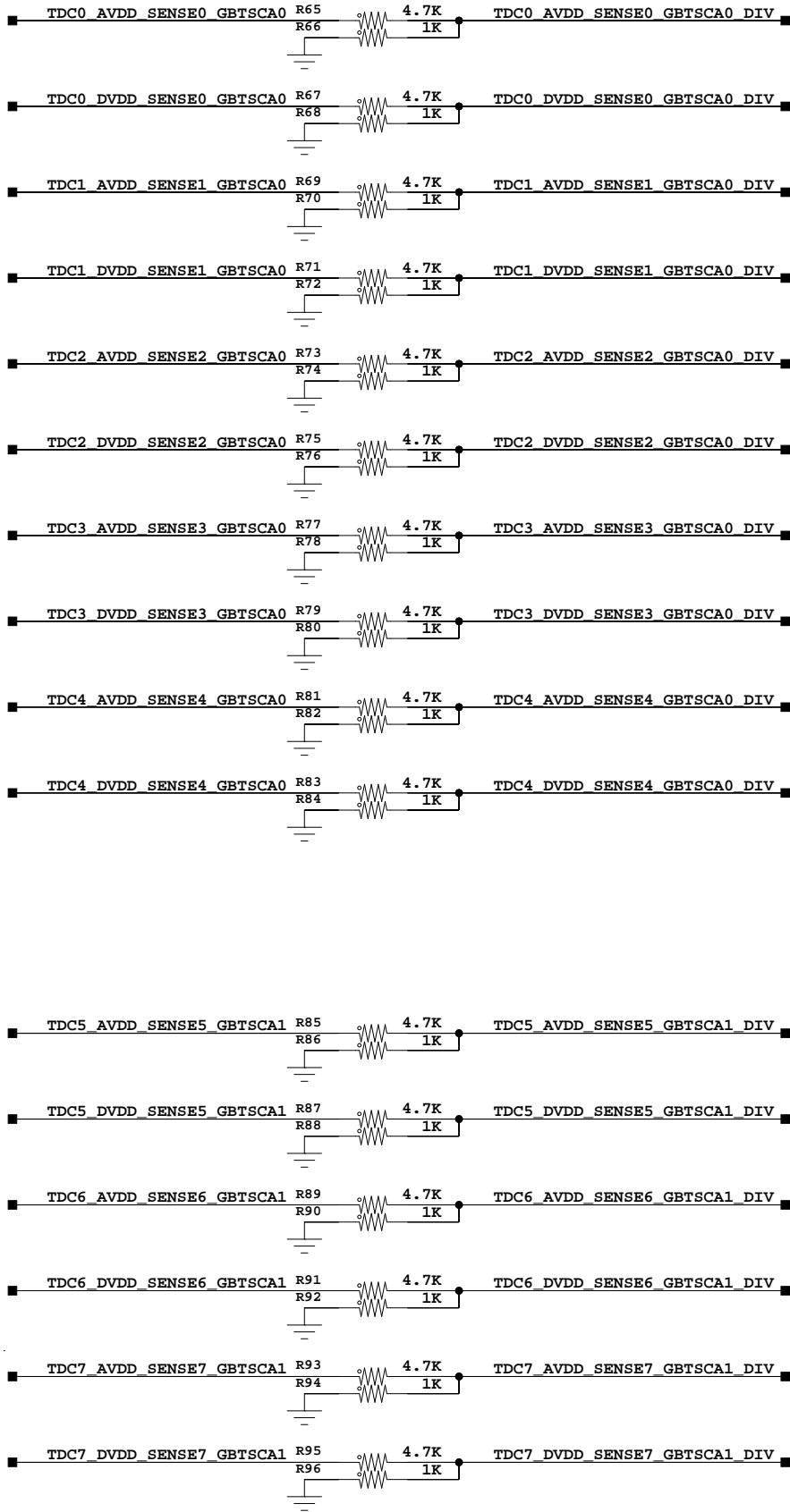
LpGBT ASIC Chip 1 -- Slave

COMPANY		University of Michigan		M	
TITLE		LpGBT_CSM Prototype v2			
SIZE	B	REV	8	OF	N
DRAWN	XUEYE HU		DATE	22/05/2023:16:44	

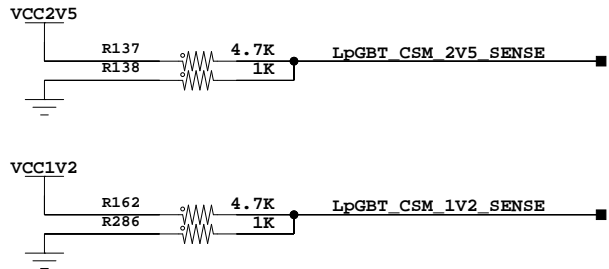
RESISTOR DIVIDER NETWORK

GBTSCA 0V-1V


NEW TDC 1.2V -- <1V
AMT 3.3V -- <1V



LpGBT-CSM Voltage monitoring



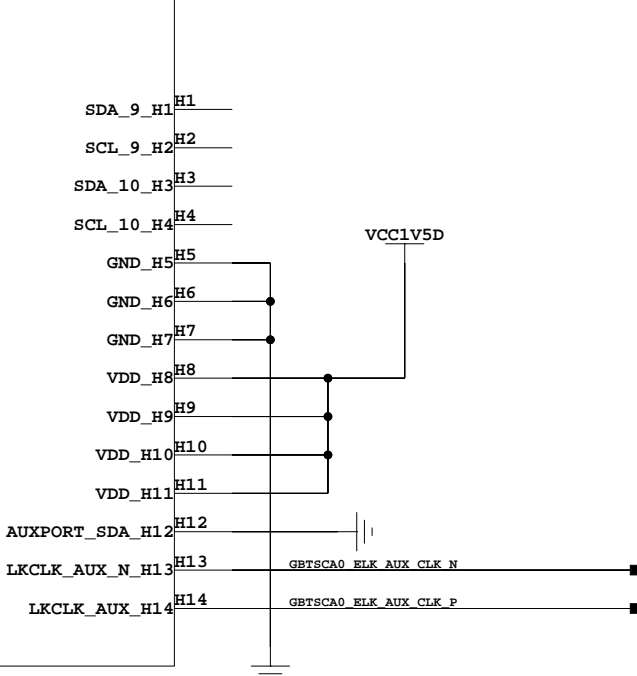
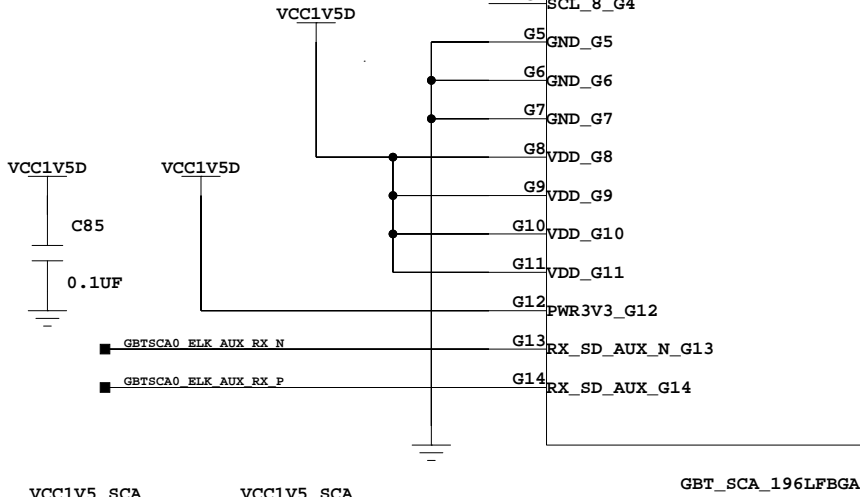
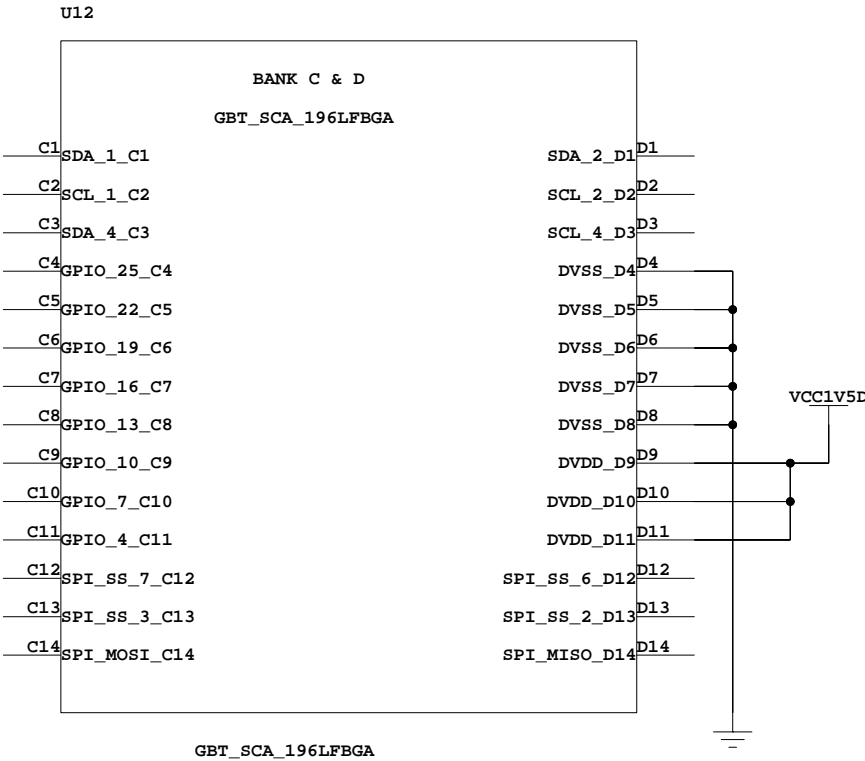
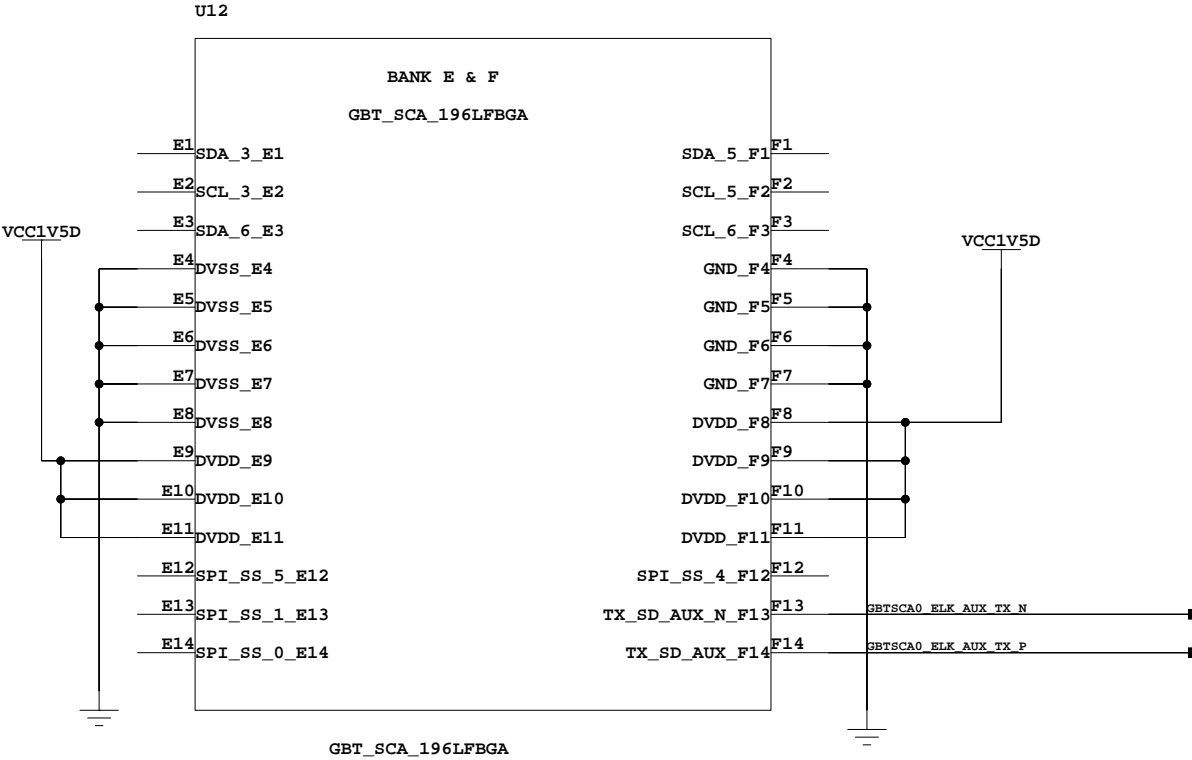
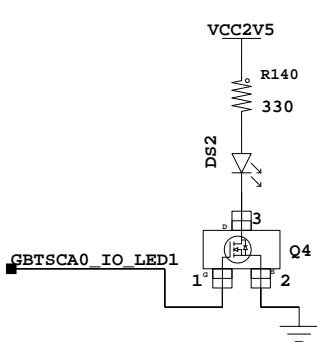
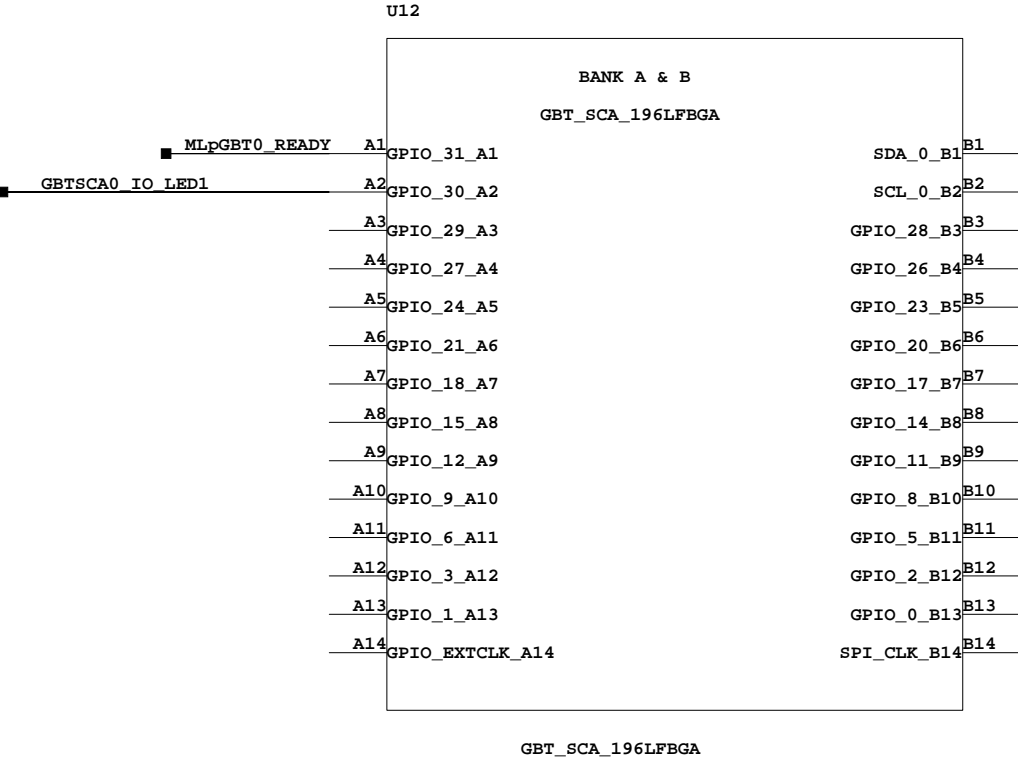
RESISTOR DIVIDER NETWORK
Mezzanine & GBTSCA

COMPANY							
University of Michigan							
TITLE							
LpGBT_CSM Prototype v2							
SIZE	B	REV	SHEET		9	OF	N
DRAWN	XUEYE HU		DATE		27/08/2022:00:04		

Note: AGND=GND; DVSS=GND; DVDD=1V5D;AVDD=1V5_SCA;VDD=1V5D

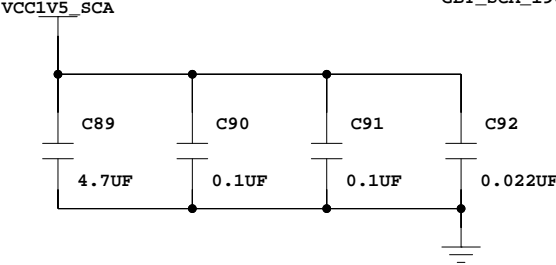
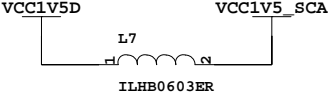
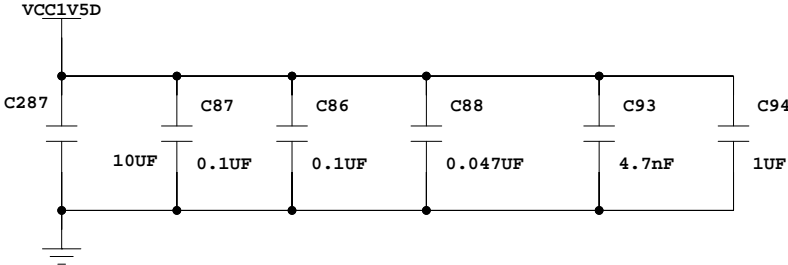
GBT-SCA IO PAD: 0-DVDD

GBT-SCA BANK A-H



GBT-SCA Decoupling

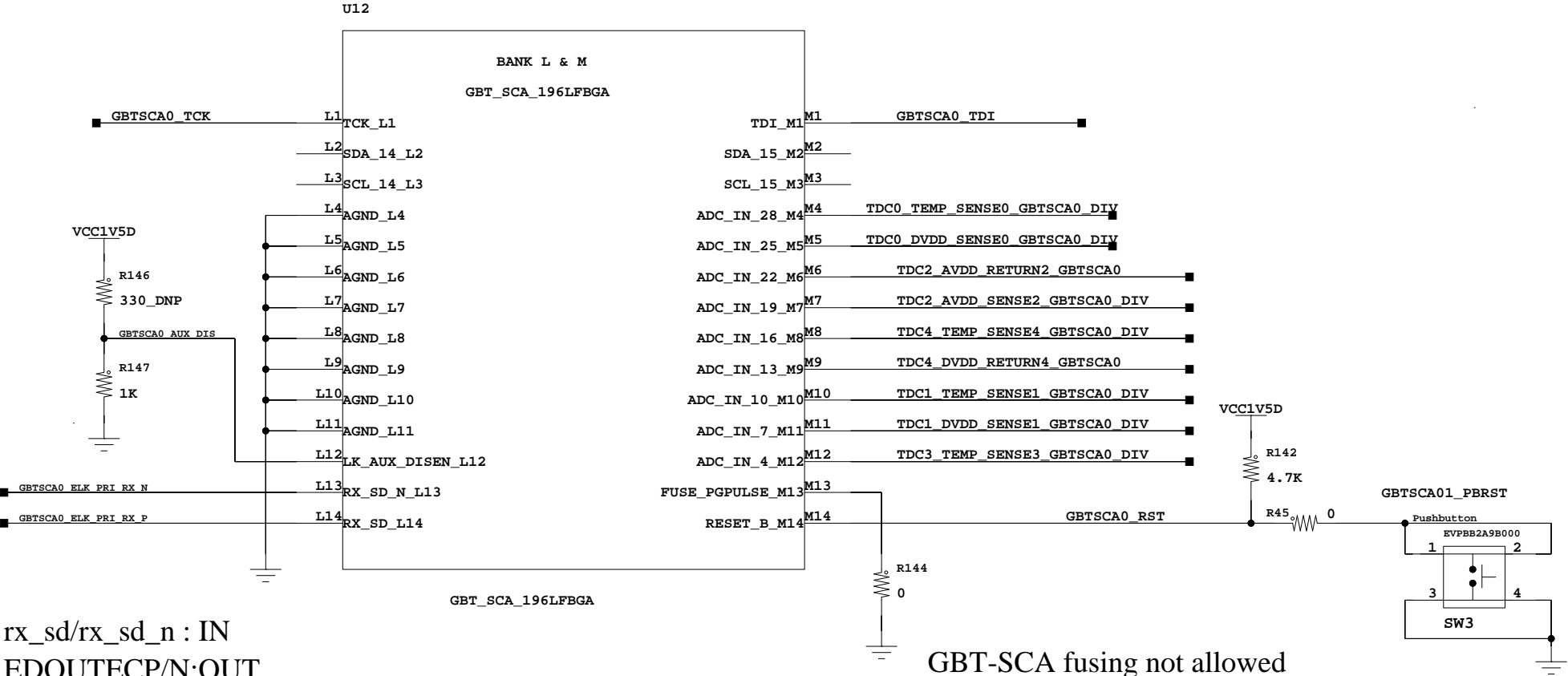
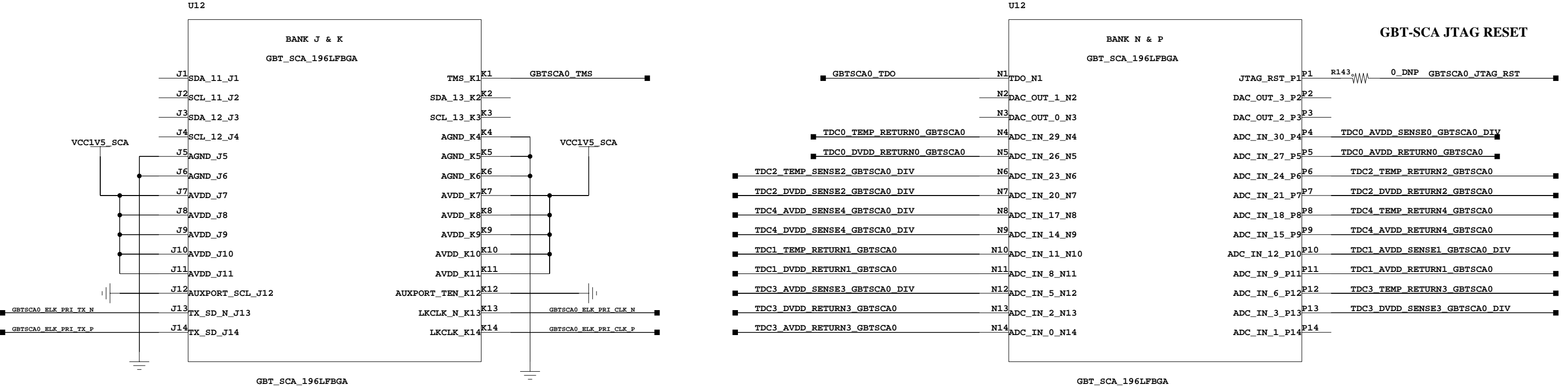
VDD & DVDD Decoupling




GBT-SCA 0

COMPANY							
University of Michigan							
TITLE							
LpGBT_CSM Prototype v2							
SIZE	B	REV		SHEET	10	OF	N
DRAWN	XUEYE HU			DATE	27/06/2022:00:40		

GBT-SCA BANK J-P



GBT-SCA 0

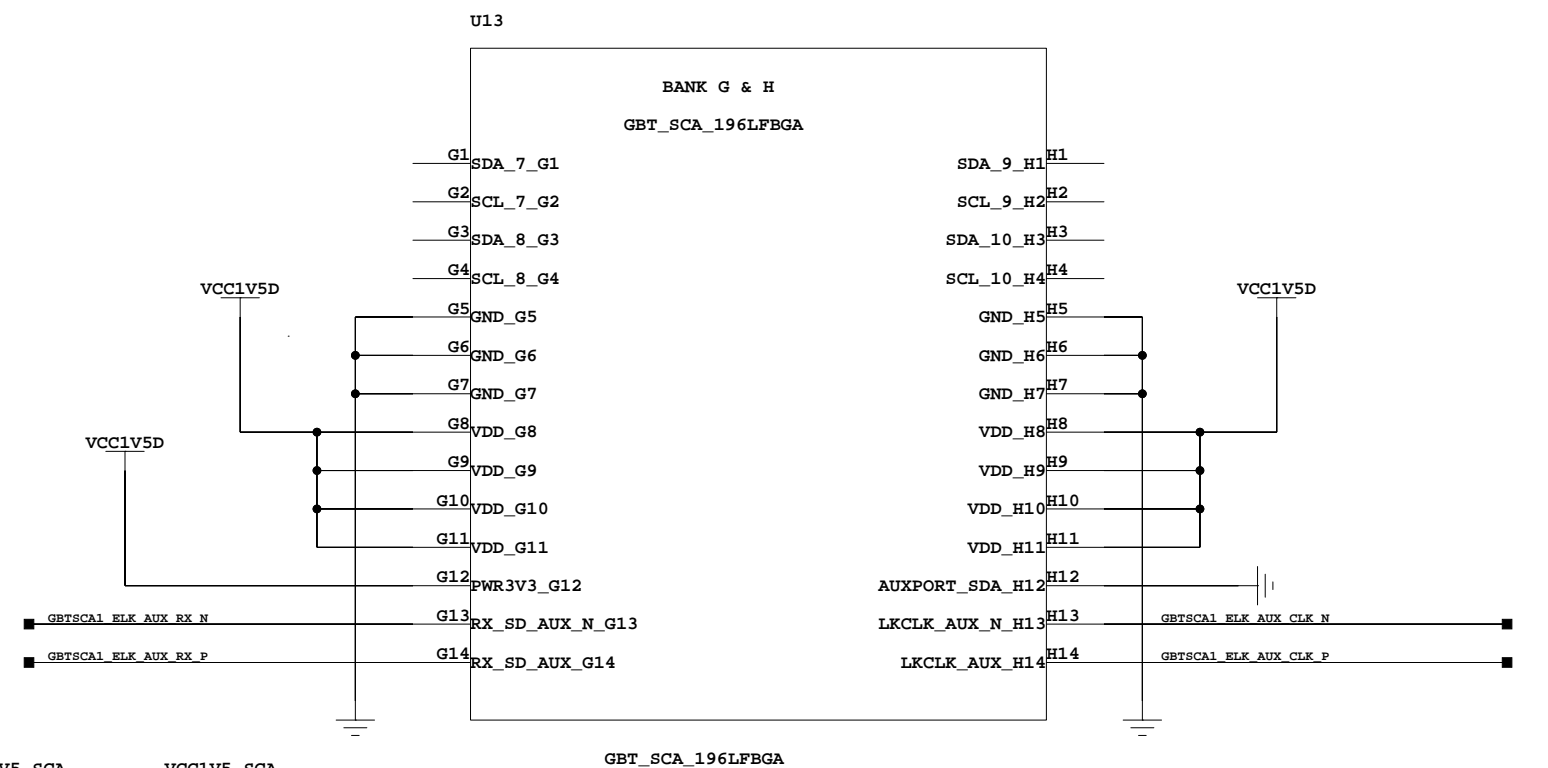
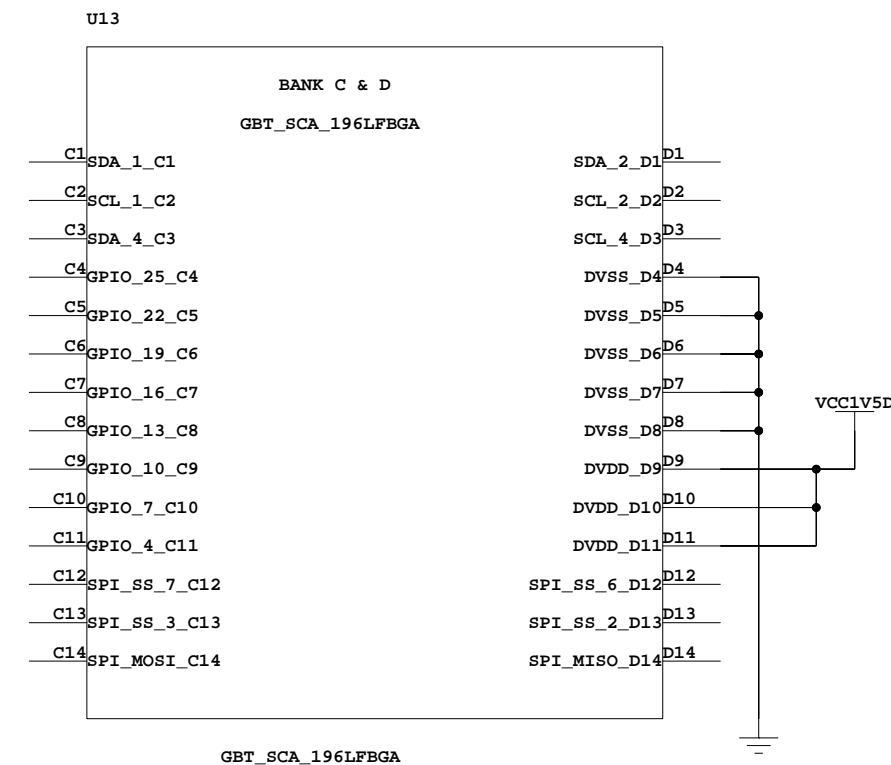
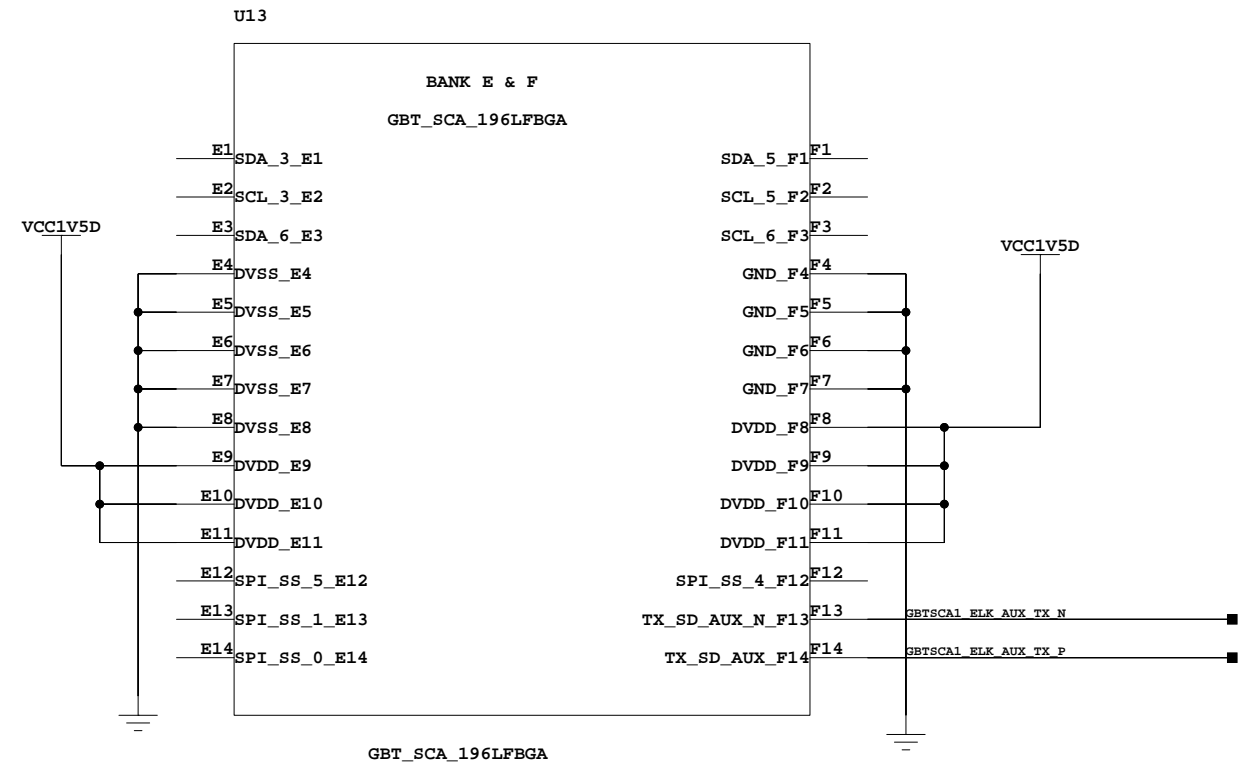
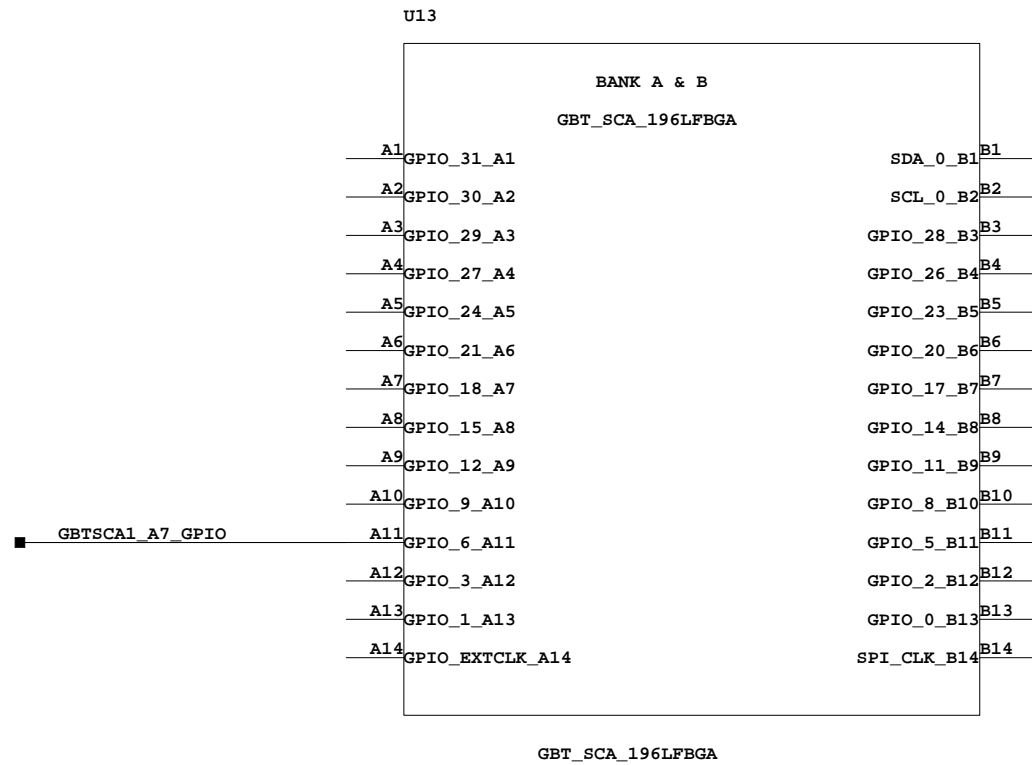
COMPANY							
University of Michigan							
TITLE							
LpGBT_CSM Prototype v2							
SIZE	B	REV	SHEET		11	OF	N
DRAWN	XUEYE HU		DATE		22/05/2023:16:46		

GBT-SCA fusing not allowed

Note: AGND=GND; DVSS=GND; DVDD=1V5D;AVDD=1V5_SCA;VDD=1V5D

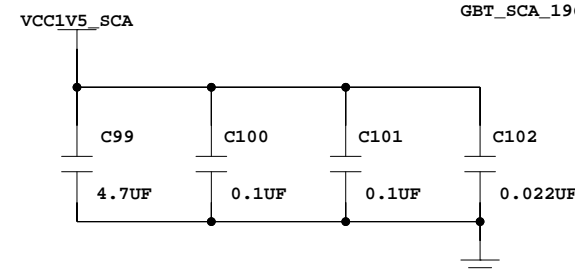
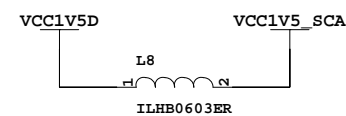
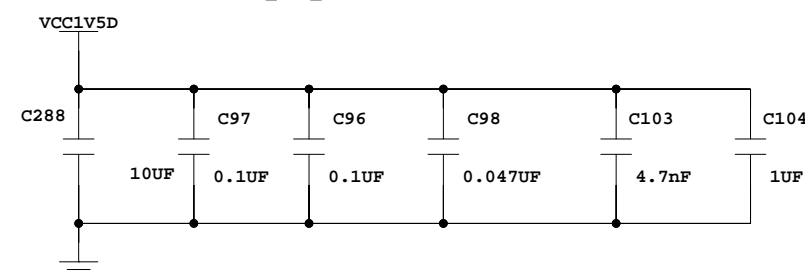
GBT-SCA IO PAD: 0-DVDD

GBT-SCA BANK A-H




GBT-SCA Decoupling

VDD & DVDD Decoupling

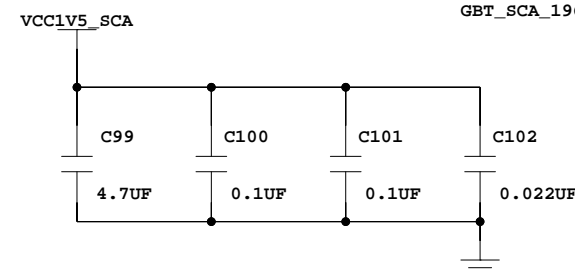
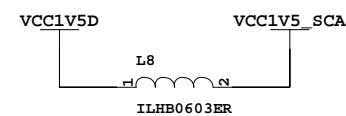
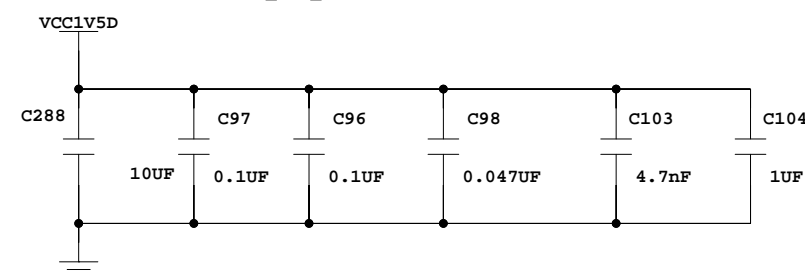


GBT-SCA 1


COMPANY		University of Michigan			
TITLE					
LpGBT_CSM Prototype v2					
SIZE	B	REV	SHEET	12	OF N
DRAWN	XUEYE HU		DATE	27/06/2022:00:40	

GBT-SCA Decoupling

VDD & DVDD Decoupling



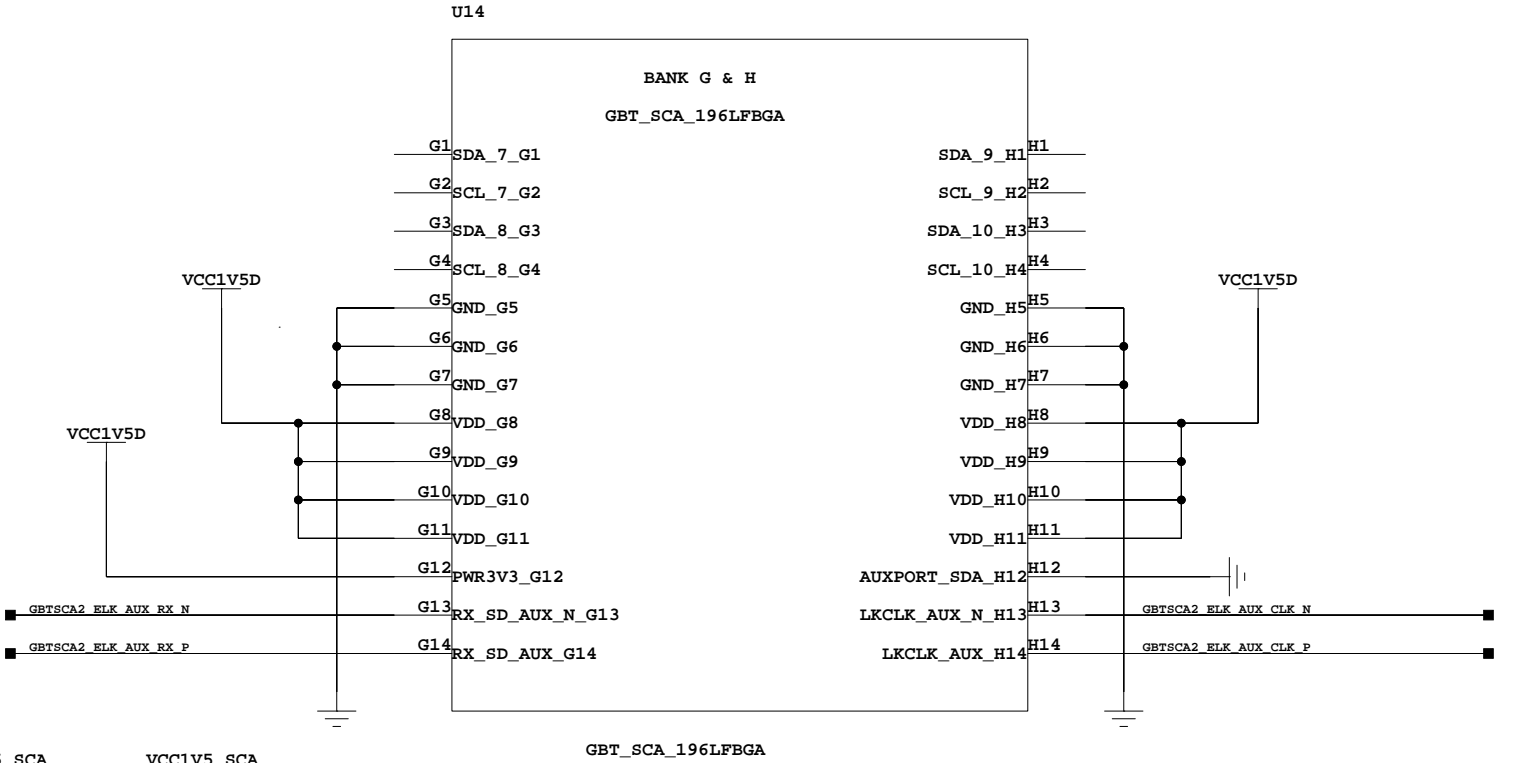
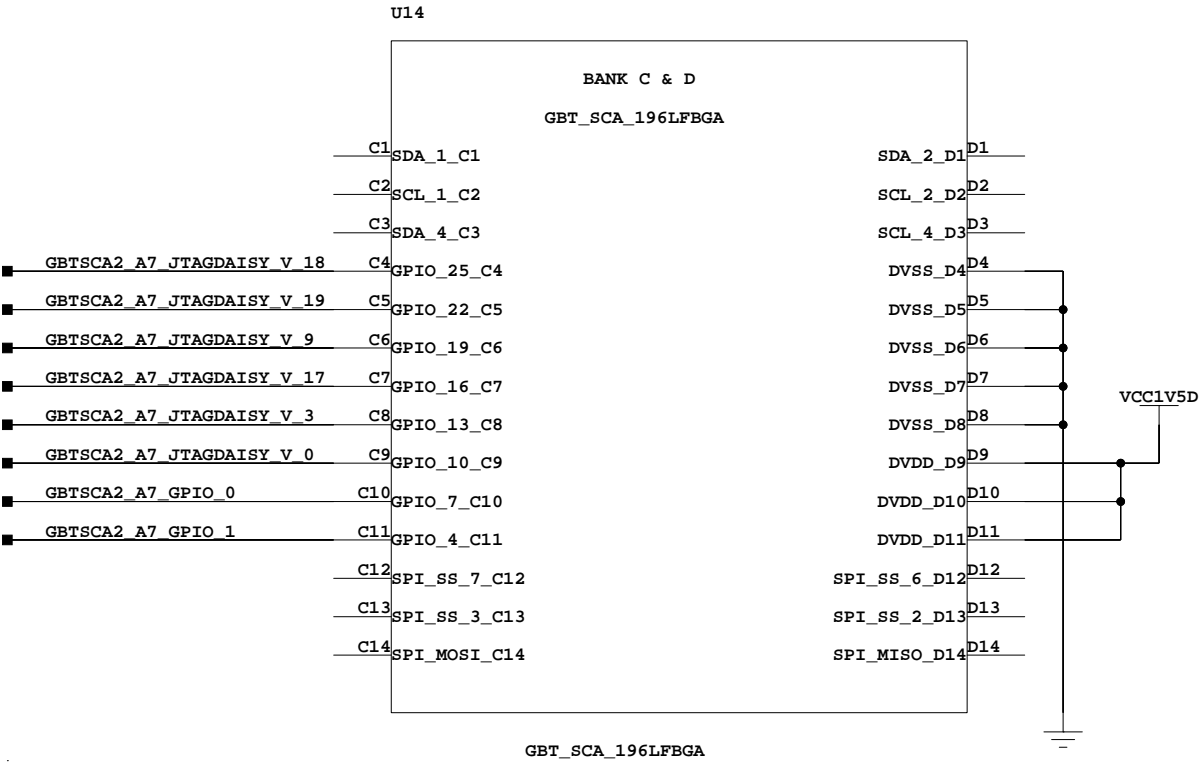
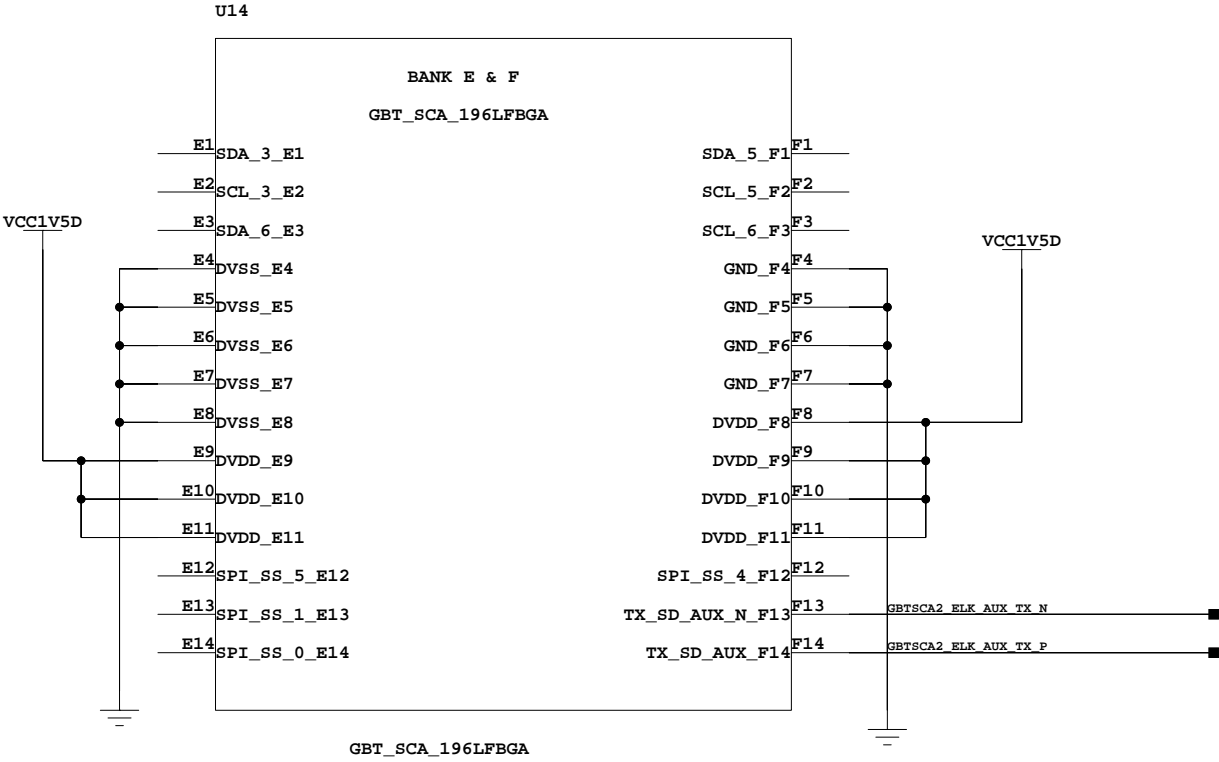
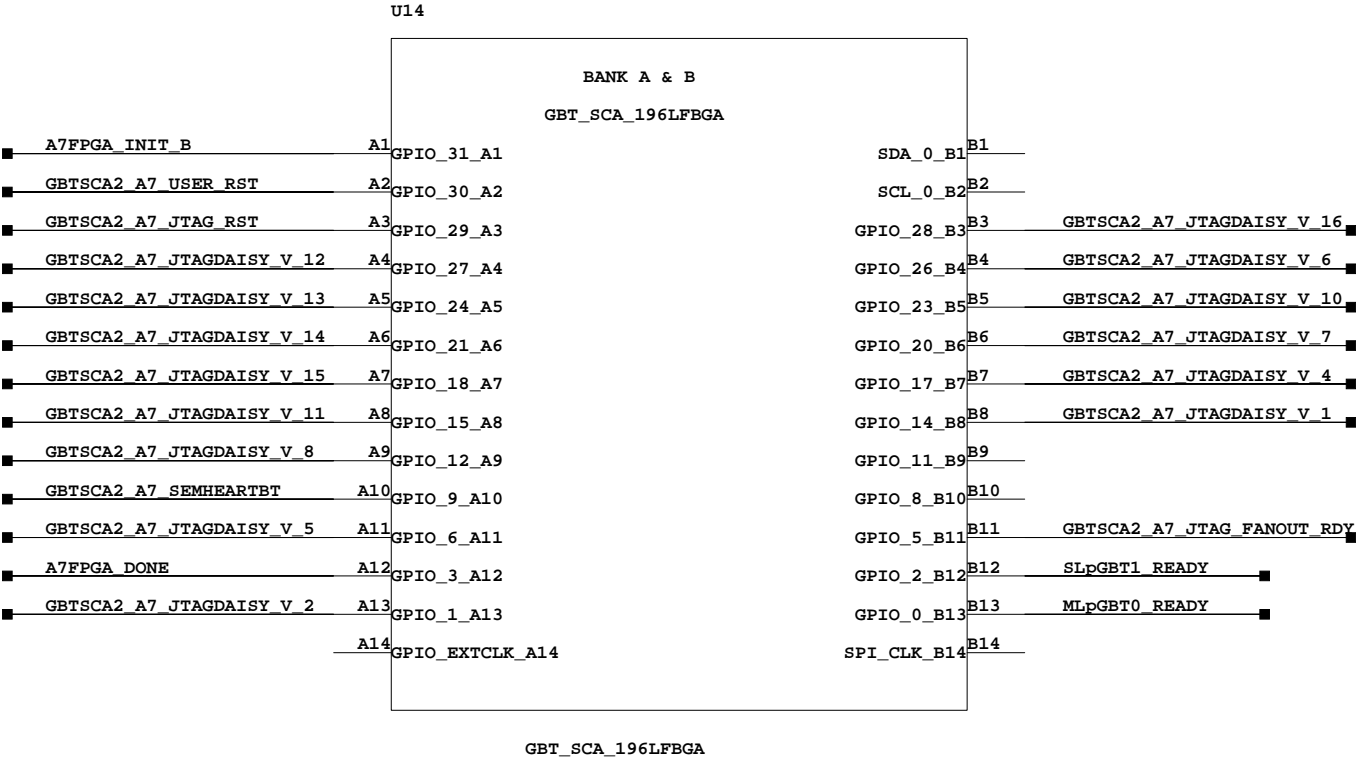
GBT-SCA 1

COMPANY		University of Michigan			
TITLE					
LpGBT_CSM Prototype v2					
SIZE	B	REV	SHEET	12	OF N
DRAWN	XUEYE HU		DATE	27/06/2022:00:40	

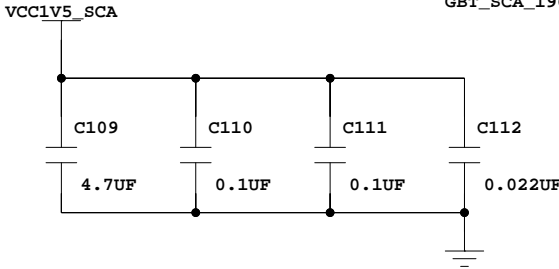
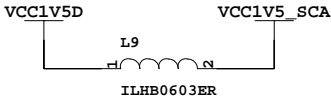
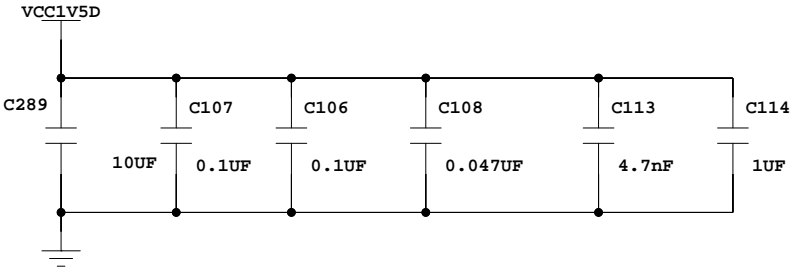
Note: AGND=GND; DVSS=GND; DVDD=1V5D;AVDD=1V5_SCA;VDD=1V5D

GBT-SCA IO PAD: 0-DVDD


GBT-SCA BANK A-H



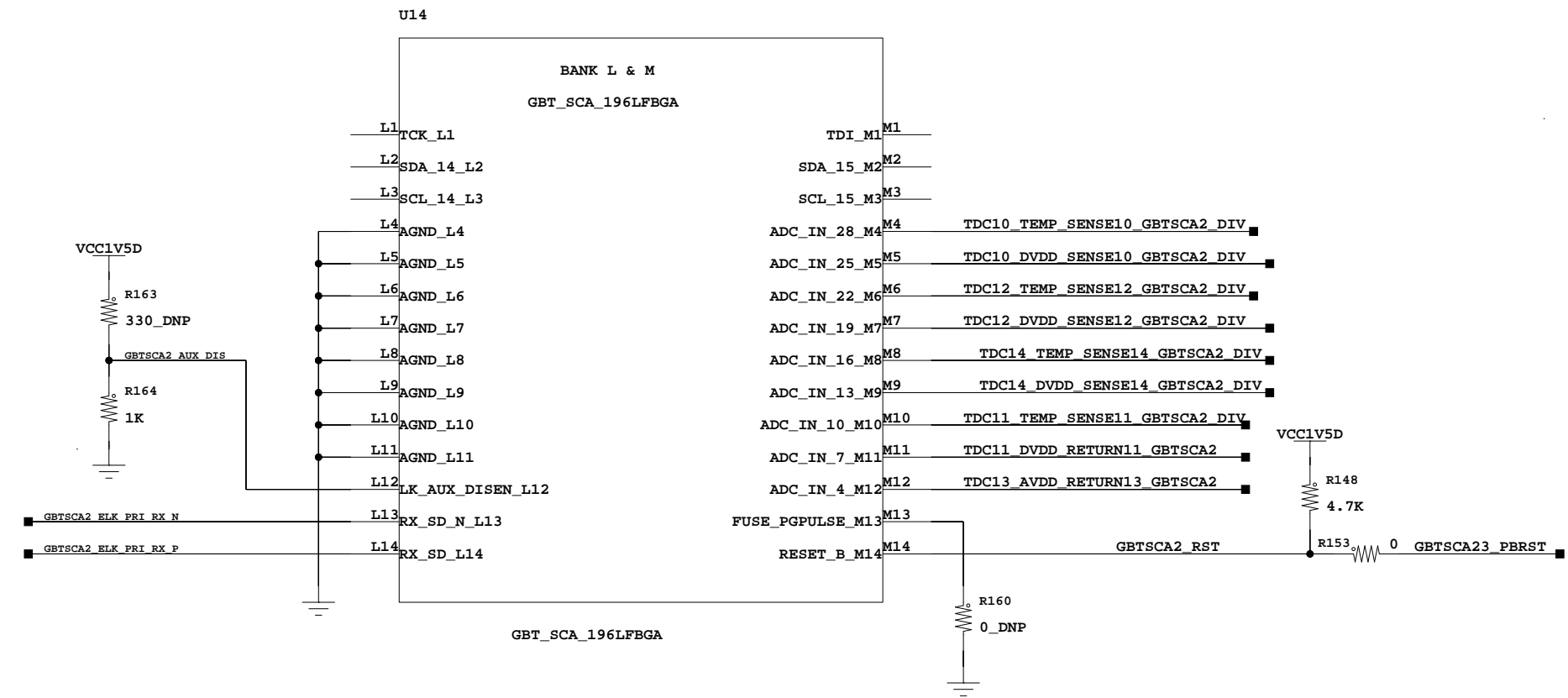
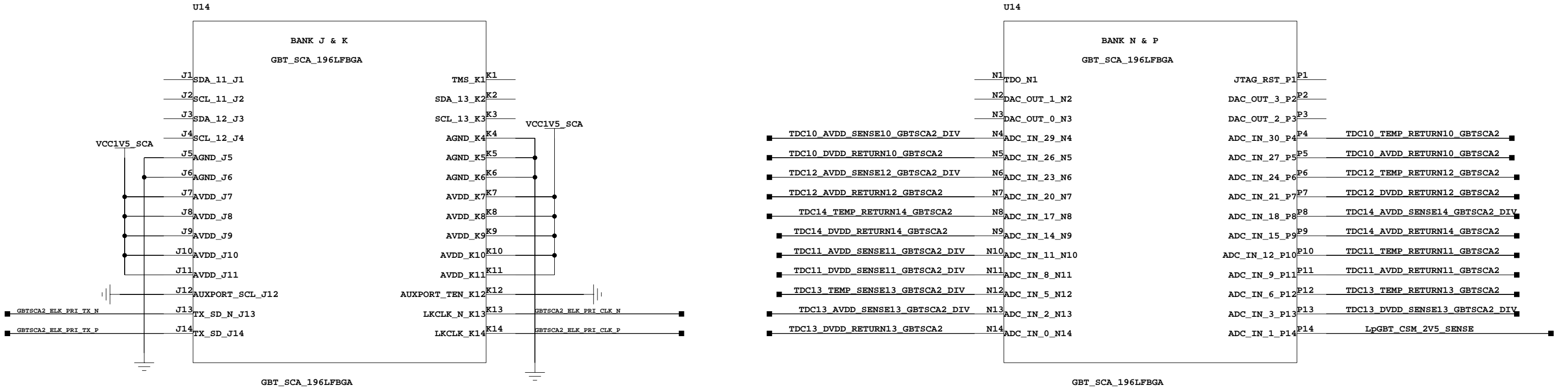
GBT-SCA Decoupling
VDD & DVDD Decoupling




GBT-SCA 2

COMPANY					
University of Michigan					
TITLE					
LpGBT_CSM Prototype v2					
SIZE	B	REV	SHEET	14	OF N
DRAWN	XUEYE HU		DATE	27/06/2022:00:40	

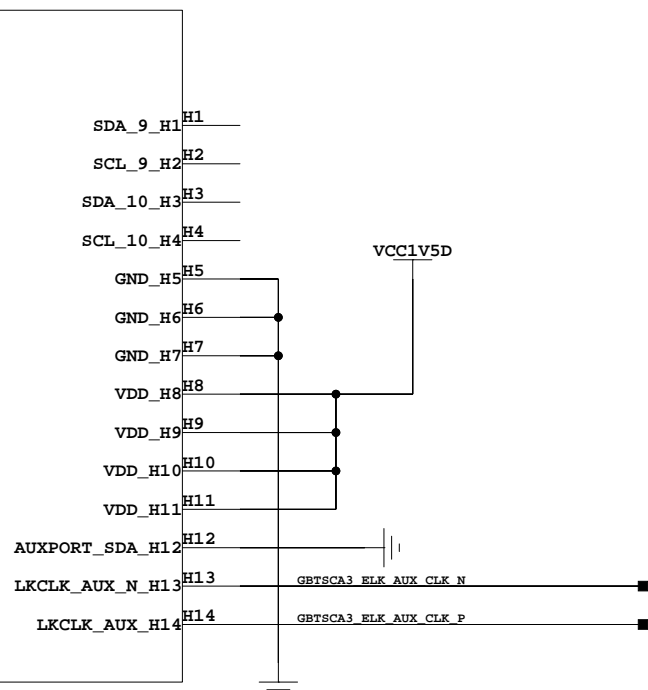
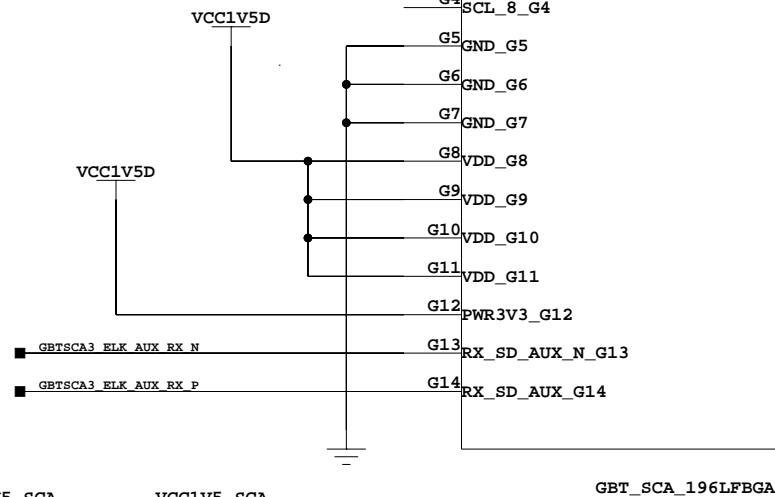
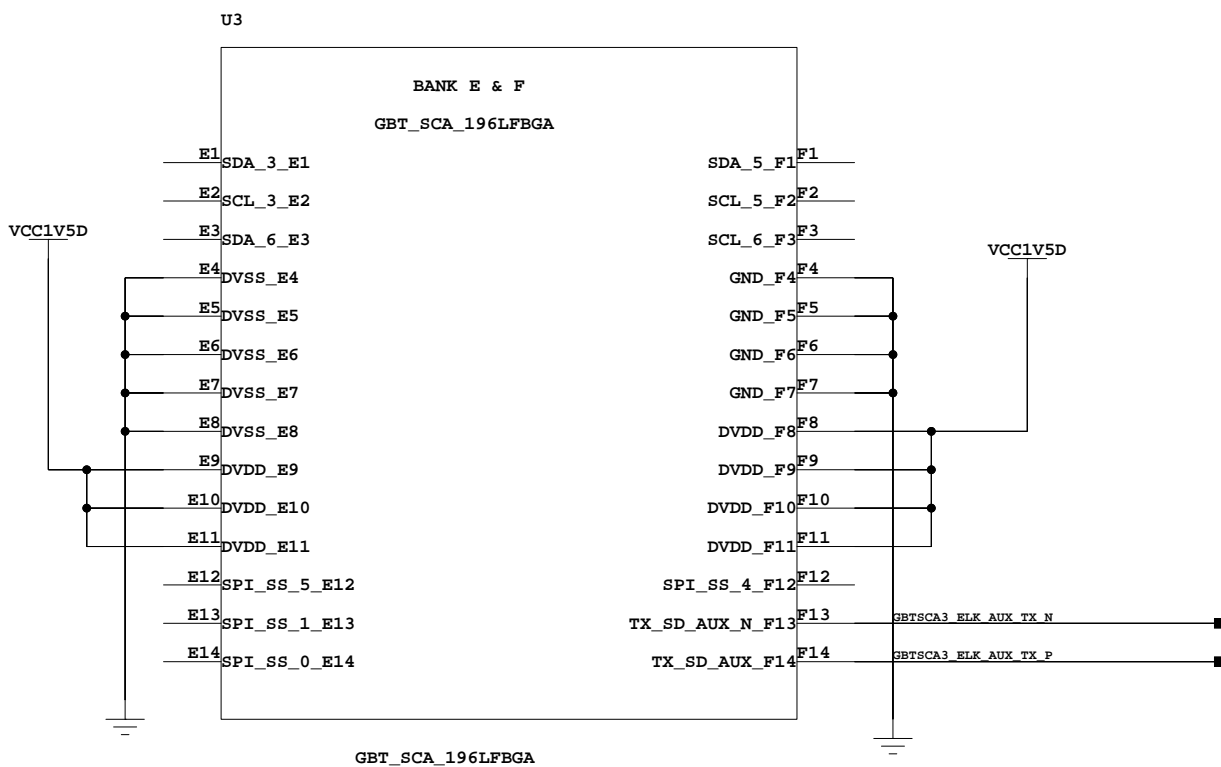
GBT-SCA BANK J-P




GBT-SCA 2

COMPANY		University of Michigan			
TITLE		LpGBT_CSM Prototype v2			
SIZE	B	REV	SHEET	15	OF N
DRAWN	XUEYE HU		DATE	26/08/2022:23:59	

GBT-SCA BANK A-H



GBT-SCA 3

COMPANY		University of Michigan			
TITLE					
LpGBT_CSM Prototype v2					
SIZE	B	REV	SHEET	16	OF N
DRAWN	XUEYE HU		DATE	05/07/2022:17:17	

4

3

2

1

4

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2

1

GBT-SCA BANK J-P

U3

BANK J & K

GBT_SCA_196LFBGA

J1 SDA_11_J1

J2 SCL_11_J2

J3 SDA_12_J3

J4 SCL_12_J4

VCC1V5_SCA

J5 AGND_J5

J6 AGND_J6

J7 AVDD_J7

J8 AVDD_J8

J9 AVDD_J9

J10 AVDD_J10

J11 AVDD_J11

J12 AUXPORT_SCL_J12

J13 TX_SD_N_J13

J14 TX_SD_J14

GBT_SCA_196LFBGA

K1 TMS_K1

K2 SDA_13_K2

K3 SCL_13_K3

K4 AGND_K4

K5 AGND_K5

K6 AGND_K6

K7 AVDD_K7

K8 AVDD_K8

K9 AVDD_K9

K10 AVDD_K10

K11 AVDD_K11

K12 AUXPORT_TEN_K12

K13 LKCLK_N_K13

K14 LKCLK_K14

VCC1V5_SCA

GBT_SCA3_ELK_PRI_TX_N

GBT_SCA3_ELK_PRI_TX_P

U3

BANK N & P

GBT_SCA_196LFBGA

N1 TDO_N1

N2 DAC_OUT_1_N2

N3 DAC_OUT_0_N3

N4 ADC_IN_29_N4

N5 ADC_IN_26_N5

N6 ADC_IN_23_N6

N7 ADC_IN_20_N7

N8 ADC_IN_17_N8

N9 ADC_IN_14_N9

N10 ADC_IN_11_N10

N11 ADC_IN_8_N11

N12 ADC_IN_5_N12

N13 ADC_IN_2_N13

N14 ADC_IN_0_N14

P1 JTAG_RST_P1

P2 DAC_OUT_3_P2

P3 DAC_OUT_2_P3

P4 ADC_IN_30_P4

P5 ADC_IN_27_P5

P6 ADC_IN_24_P6

P7 ADC_IN_21_P7

P8 ADC_IN_18_P8

P9 ADC_IN_15_P9

P10 ADC_IN_12_P10

P11 ADC_IN_9_P11

P12 ADC_IN_6_P12

P13 ADC_IN_3_P13

P14 ADC_IN_1_P14

TDC19_DVDD_SENSE19_GBTSCA3_DIV

TDC19_TEMP_SENSE19_GBTSCA3_DIV

TDC17_DVDD_SENSE17_GBTSCA3_DIV

TDC17_TEMP_SENSE17_GBTSCA3_DIV

TDC15_DVDD_RETURN15_GBTSCA3

TDC15_TEMP_RETURN15_GBTSCA3

TDC18_DVDD_RETURN18_GBTSCA3

TDC18_TEMP_RETURN18_GBTSCA3

TDC16_DVDD_RETURN16_GBTSCA3

TDC16_AVDD_SENSE16_GBTSCA3_DIV

TDC16_TEMP_SENSE16_GBTSCA3_DIV

TDC19_AVDD_SENSE19_GBTSCA3_DIV

TDC19_AVDD_RETURN19_GBTSCA3

TDC17_AVDD_SENSE17_GBTSCA3_DIV

TDC17_AVDD_RETURN17_GBTSCA3

TDC15_DVDD_SENSE15_GBTSCA3_DIV

TDC15_TEMP_SENSE15_GBTSCA3_DIV

TDC18_DVDD_SENSE18_GBTSCA3_DIV

TDC18_TEMP_SENSE18_GBTSCA3_DIV

TDC16_DVDD_SENSE16_GBTSCA3_DIV

TDC16_TEMP_RETURN16_GBTSCA3

LpGBT_CSM_1V2_SENSE

U3

BANK L & M

GBT_SCA_196LFBGA

L1 TCK_L1

L2 SDA_14_L2

L3 SCL_14_L3

L4 AGND_L4

L5 AGND_L5

L6 AGND_L6

L7 AGND_L7

L8 AGND_L8

L9 AGND_L9

L10 AGND_L10

L11 AGND_L11

L12 LK_AUX_DISEN_L12

L13 RX_SD_N_L13

L14 RX_SD_L14

GBT_SCA_196LFBGA

M1 TDI_M1

M2 SDA_15_M2

M3 SCL_15_M3

M4 ADC_IN_28_M4

M5 ADC_IN_25_M5

M6 ADC_IN_22_M6

M7 ADC_IN_19_M7

M8 ADC_IN_16_M8

M9 ADC_IN_13_M9

M10 ADC_IN_10_M10

M11 ADC_IN_7_M11

M12 ADC_IN_4_M12

M13 FUSE_PGMPULSE_M13

M14 RESET_B_M14

VCC1V5D

R149 330_DNP

GBT_SCA3_AUX_DIS

R157 1K

GBT_SCA3_ELK_PRI_RX_N

GBT_SCA3_ELK_PRI_RX_P

TDC19_DVDD_RETURN19_GBTSCA3

TDC19_TEMP_RETURN19_GBTSCA3

TDC17_DVDD_RETURN17_GBTSCA3

TDC17_TEMP_RETURN17_GBTSCA3

TDC15_AVDD_RETURN15_GBTSCA3

TDC15_AVDD_SENSE15_GBTSCA3_DIV

TDC18_AVDD_RETURN18_GBTSCA3

TDC18_AVDD_SENSE18_GBTSCA3_DIV

TDC16_AVDD_RETURN16_GBTSCA3

VCC1V5D

R154 4.7K

R161 0

GBT_SCA3_RST

GBT_SCA23_PBRST

Pushbutton

EVPBB2A9B000

SW4

R44 0_DNP

GBT-SCA fusing not allowed

GBT-SCA 3

COMPANY

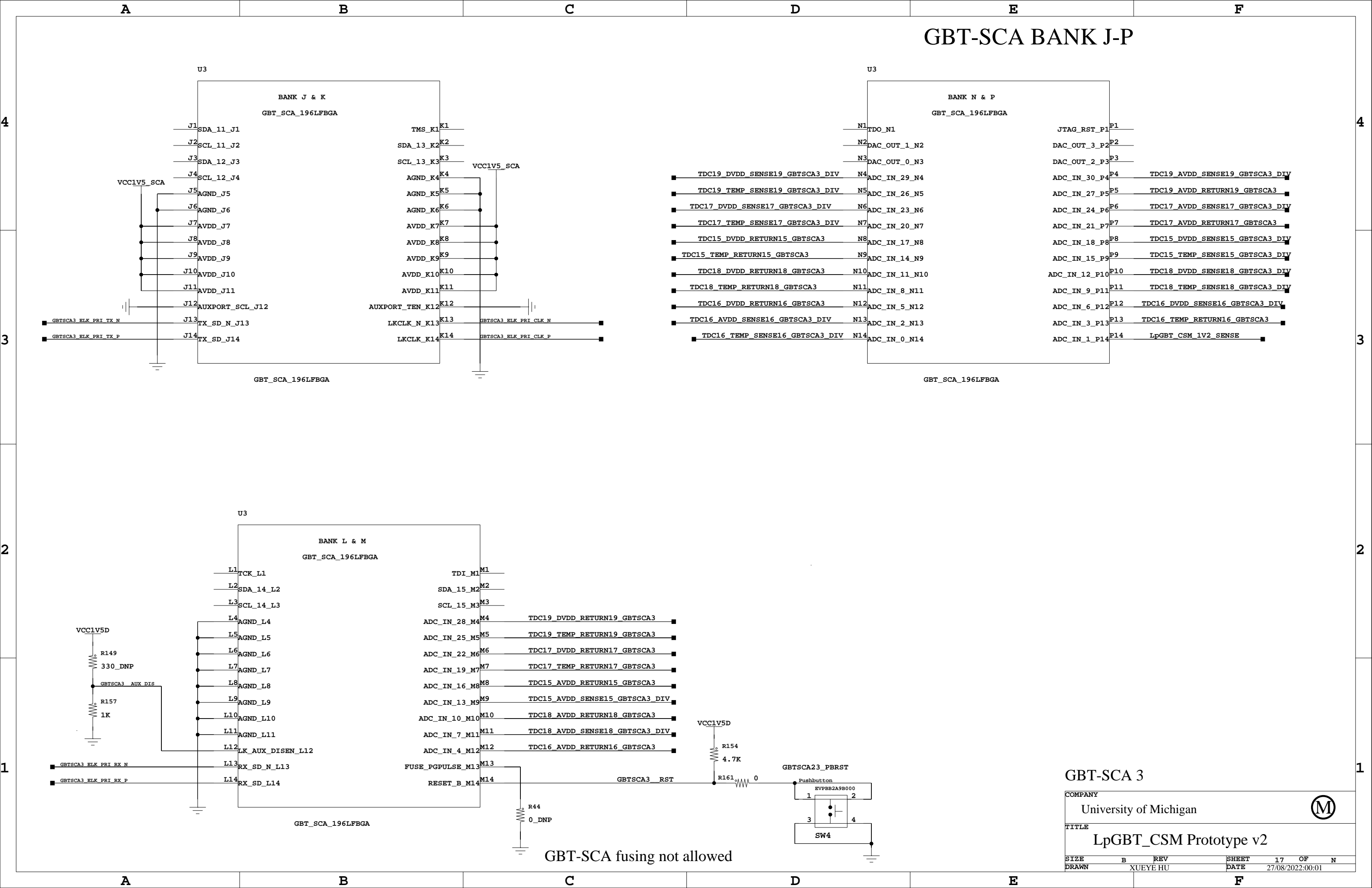
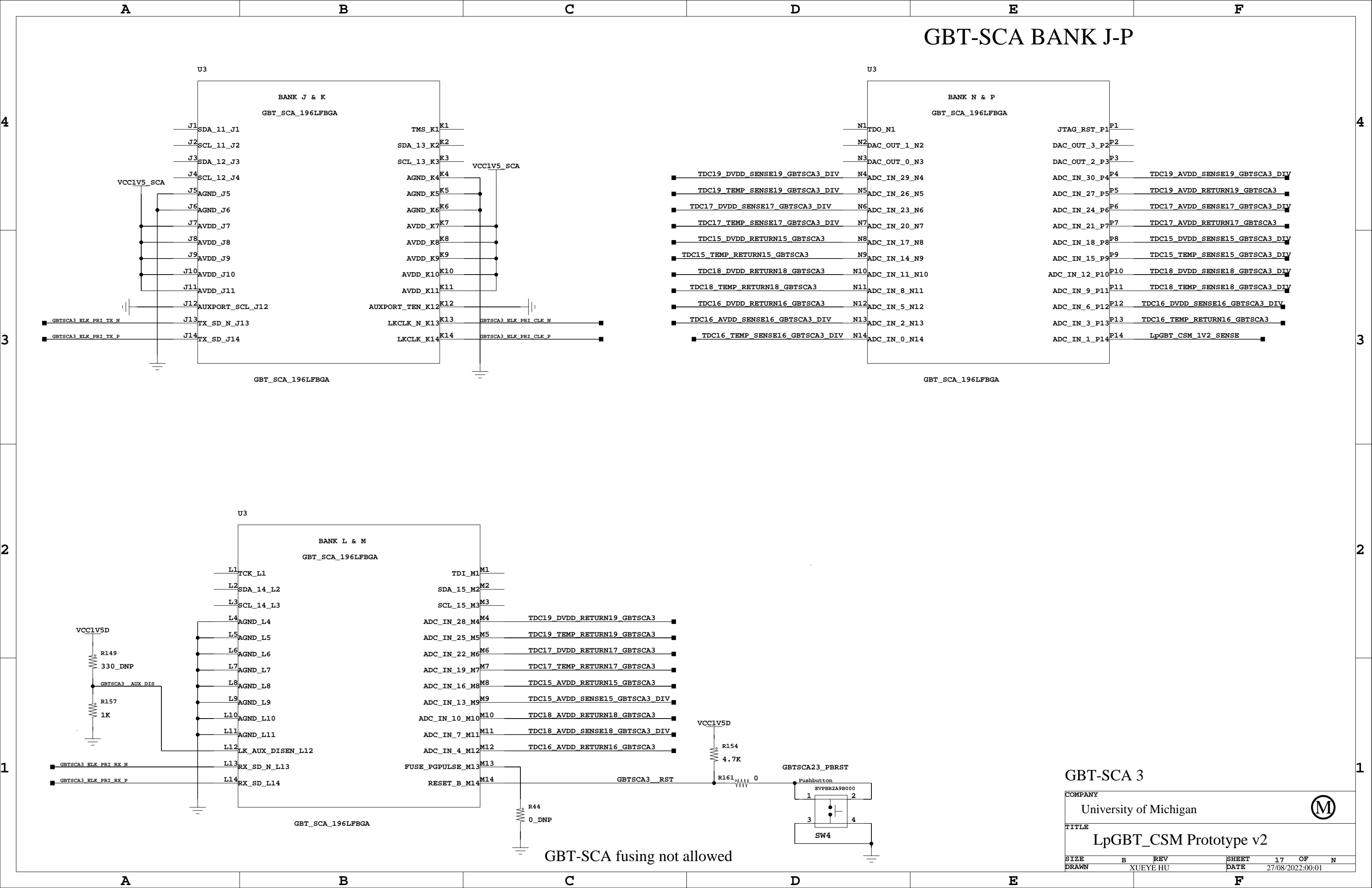
University of Michigan

TITLE

LpGBT_CSM Prototype v2

SIZE B REV SHEET 17 OF N

DRAWN XUEYE HU DATE 27/08/2022:00:01



GBT-SCA BANK J-P

Bank J & K
 GBT_SCA_196LFBGA

Bank N & P
 GBT_SCA_196LFBGA

Bank L & M
 GBT_SCA_196LFBGA

GBT-SCA 3

Company: University of Michigan

Title: LpGBT_CSM Prototype v2

Size: B **Rev:** **Sheet:** 17 **Of:** N

Drawn: XUEYE HU **Date:** 27/08/2022:00:01

GBT-SCA fusing not allowed

GBT-SCA BANK J-P

Bank J & K
 GBT_SCA_196LFBGA

Bank N & P
 GBT_SCA_196LFBGA

Bank L & M
 GBT_SCA_196LFBGA

GBT-SCA 3

Company: University of Michigan

Title: LpGBT_CSM Prototype v2


Size: B **Rev:** **Sheet:** 17 **Of:** N

Drawn: XUEYE HU **Date:** 27/08/2022:00:01

GBT-SCA fusing not allowed

Note 1a: GBT-SCA 1.5V. BANK0,14,15 ->1.5V CFGBVS set to low to get 1.8v/1.5v operation



<div> <div>COMPANY</div> <div>University of Michigan</div> <div>  </div> </div>				
<div> <div>TITLE</div> <div>LpGBT_CSM Prototype v2</div> </div>				
SIZE	B	REV	SHEET	18 OF N
DRAWN	XUEYE HU		DATE	05/07/2022:17:19

4

3



A



3

1

4

3

2

1

4

3

2

1

SOC_IRON_FGG484_CSM

BANK 35
XC7A35TFGG484

IO_0_35_F4
IO_L1P_T0_AD4P_35_B1
IO_L1N_T0_AD4N_35_A1
IO_L2P_T0_AD12P_35_C2
IO_L2N_T0_AD12N_35_B2
IO_L3P_T0_DQS_AD5P_35_E1
IO_L3N_T0_DQS_AD5N_35_D1
IO_L4P_T0_35_E2
IO_L4N_T0_35_D2
IO_L5P_T0_AD13P_35_G1
IO_L5N_T0_AD13N_35_F1
IO_L6P_T0_35_F3
IO_L6N_T0_VREF_35_E3
IO_L7P_T1_AD6P_35_K1
IO_L7N_T1_AD6N_35_J1
IO_L8P_T1_AD14P_35_H2
IO_L8N_T1_AD14N_35_G2
IO_L9P_T1_DQS_AD7P_35_K2
IO_L9N_T1_DQS_AD7N_35_J2
IO_L10P_T1_AD15P_35_J5
IO_L10N_T1_AD15N_35_H5
IO_L11P_T1_SRCC_35_H3
IO_L11N_T1_SRCC_35_G3
IO_L12P_T1_MRCC_35_H4
IO_L12N_T1_MRCC_35_G4
IO_L13P_T2_MRCC_35_K4
IO_L13N_T2_MRCC_35_J4
IO_L14P_T2_SRCC_35_L3
IO_L14N_T2_SRCC_35_K3
IO_L15P_T2_DQS_35_M1
IO_L15N_T2_DQS_35_L1
IO_L16P_T2_35_M3
IO_L16N_T2_35_M2
IO_L17P_T2_35_K6
IO_L17N_T2_35_J6
IO_L18P_T2_35_L5
IO_L18N_T2_35_L4
IO_L19P_T3_35_N4
IO_L19N_T3_VREF_35_N3
IO_L20P_T3_35_R1
IO_L20N_T3_35_P1
IO_L21P_T3_DQS_35_P5
IO_L21N_T3_DQS_35_P4
IO_L22P_T3_35_P2
IO_L22N_T3_35_N2
IO_L23P_T3_35_M6
IO_L23N_T3_35_M5
IO_L24P_T3_35_P6
IO_L24N_T3_35_N5
IO_25_35_L6

F4
B1
A1
C2
B2
E1
D1
E2
D2
G1
F1
F3
E3
K1
J1
H2
G2
K2
J2
J5
H5
H3
G3
H4
G4
K4
J4
L3
K3
M1
L1
M3
M2
K6
J6
L5
L4
N4
N3
R1
P1
P5
P4
P2
N2
M6
M5
P6
N5
L6

R345 33 Mezz2 JTAG TDI 2
Mezz2 IN ENC GEBRST P 2
Mezz2 IN ENC GEBRST N 2
Mezz8 IN ENC GEBRST P 8
Mezz8 IN ENC GEBRST N 8
R346 33 Mezz0 JTAG TMS 0
R347 33 Mezz0 JTAG TDI 0
R310 33 Mezz0 JTAG TCK 0
Mezz0 JTAG TDO 0 2V5
R348 33 Mezz6 JTAG TDI 6
Mezz6 JTAG TDO 6 2V5
R349 33 Mezz2 JTAG TMS 2
R309 33 Mezz2 JTAG TCK 2
Mezz6 IN ENC GEBRST P 6
Mezz6 IN ENC GEBRST N 6
R350 33 Mezz6 JTAG TMS 6
R312 33 Mezz6 JTAG TCK 6
Mezz0 IN ENC GEBRST P 0
Mezz0 IN ENC GEBRST N 0
Mezz8 JTAG TDO 8 2V5
R311 33 Mezz8 JTAG TCK 8
R351 33 Mezz8 JTAG TMS 8
MLpGBT0 ECLK FPGAsys P
MLpGBT0 ECLK FPGAsys N
A7FPGA MLpGBT0 TTC EDCLK3 P
A7FPGA MLpGBT0 TTC EDCLK3 N
Mezz17 IN ENC GEBRST P 17
Mezz17 IN ENC GEBRST N 17
Mezz13 IN ENC GEBRST P 13
Mezz13 IN ENC GEBRST N 13
Mezz19 IN ENC GEBRST P 19
Mezz19 IN ENC GEBRST N 19
A7FPGA MLpGBT0 TTC EDOUT00 P
A7FPGA MLpGBT0 TTC EDOUT00 N
R352 33 Mezz8 JTAG TDI 8
Mezz2 JTAG TDO 2 2V5
GPIO LED 1
Mezz10 IN ENC GEBRST P 10
Mezz10 IN ENC GEBRST N 10
R353 33 Mezz18 JTAG TMS 18
R354 33 Mezz18 JTAG TDI 18
GPIO LED 0
GPIO LED 2
GPIO LED 3
GP_RST A7

LpGBT TTC Elink

VCC1V5D
AA17
AB14
V16
W13
Y10

SOC_IRON_FGG484_CSM

BANK NC13
XC7A35TFGG484

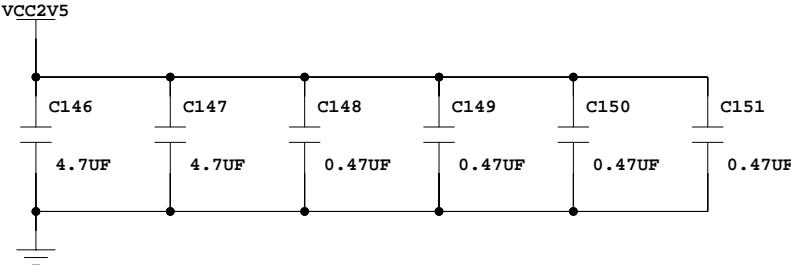
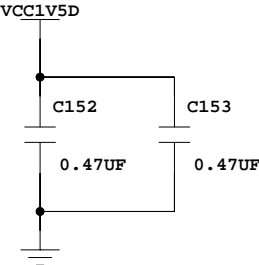
NC_13_T14
NC_13_T15
NC_13_T16
NC_13_U15
NC_13_U16
NC_13_V10
NC_13_V13
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NC_13_V15
NC_13_W10
NC_13_W11
NC_13_W12
NC_13_W14
NC_13_W15
NC_13_W16
NC_13_Y11
NC_13_Y12
NC_13_Y13
NC_13_Y14
NC_13_Y16
NC_13_Y17
NC_13_AA9
NC_13_AA10
NC_13_AA11
NC_13_AA13
NC_13_AA14
NC_13_AA15
NC_13_AA16
NC_13_AB10
NC_13_AB11
NC_13_AB12
NC_13_AB13
NC_13_AB15
NC_13_AB16
NC_13_AB17

T14
T15
T16
U15
U16
V10
V13
V14
V15
W10
W11
W12
W14
W15
W16
Y11
Y12
Y13
Y14
Y16
Y17
AA9
AA10
AA11
AA13
AA14
AA15
AA16
AB10
AB11
AB12
AB13
AB15
AB16
AB17


U17

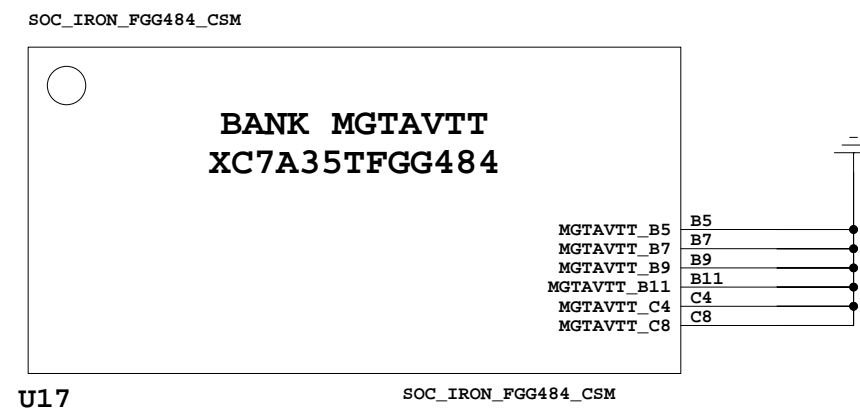
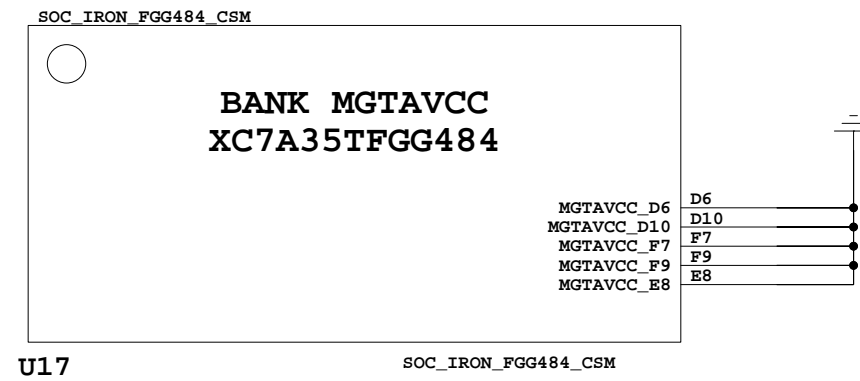
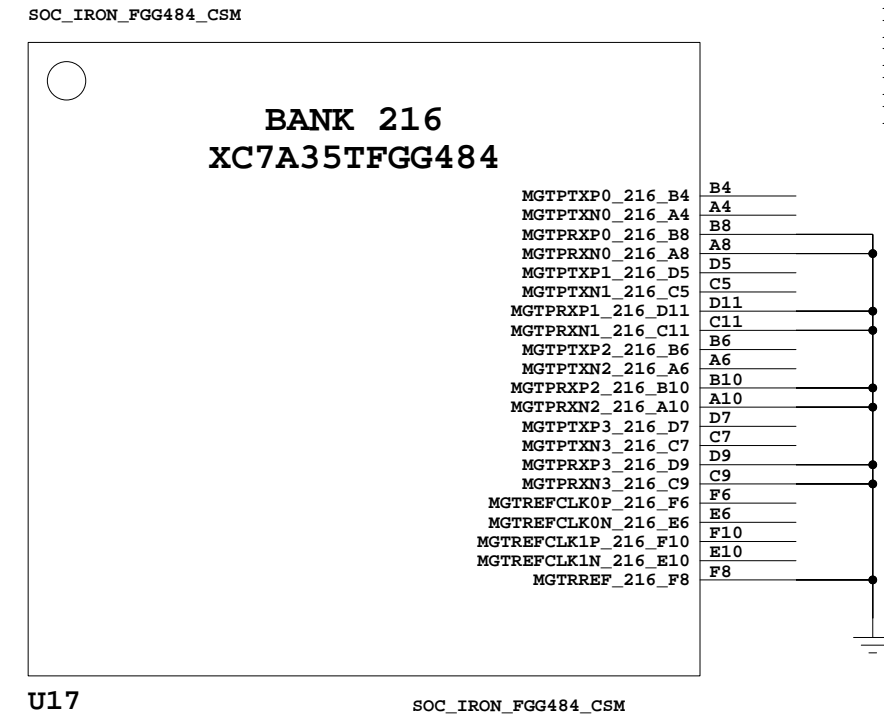
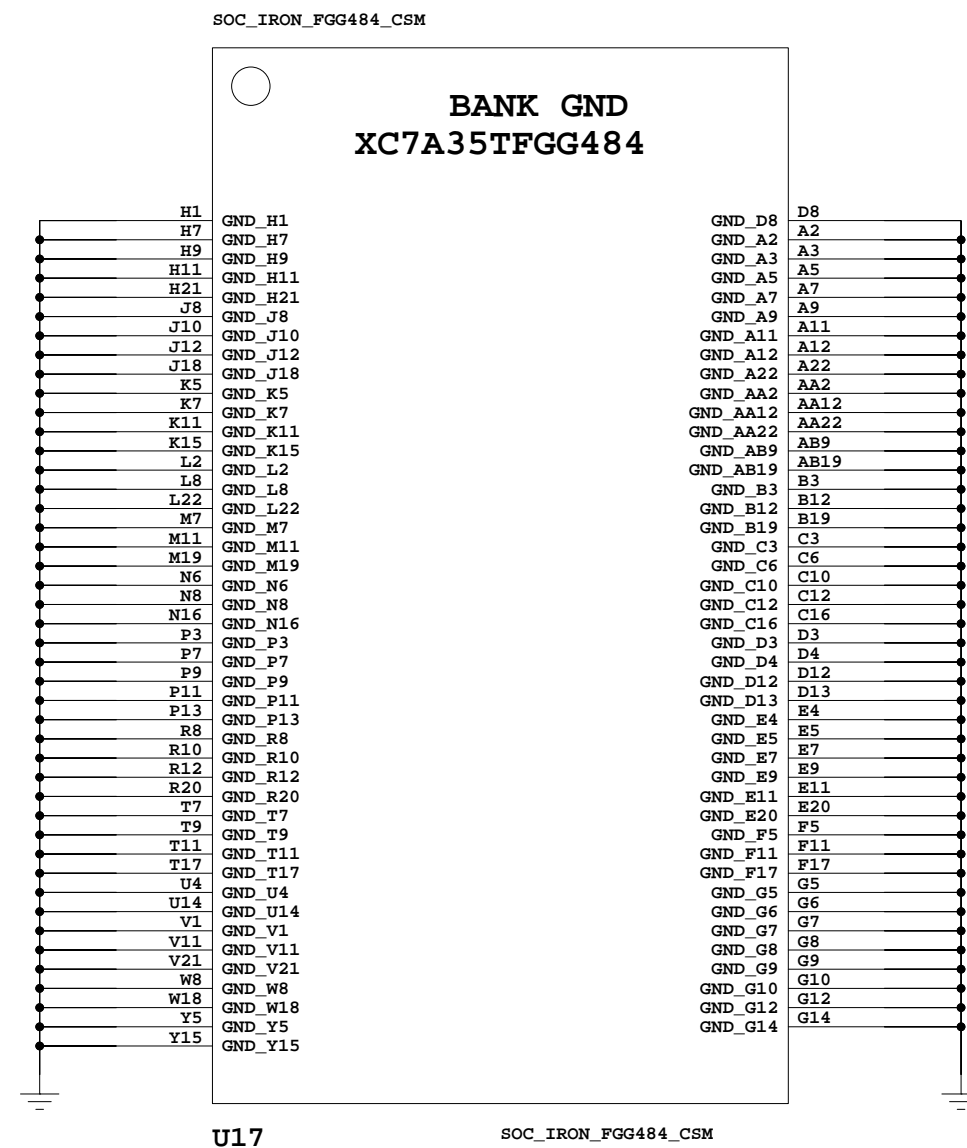
SOC_IRON_FGG484_CSM

Note: VCCO of unused I/O banks
connect to VCCAUX or any available VCCO
but do not require decoupling




XC7A35T FPGA BANKS 35, NC13

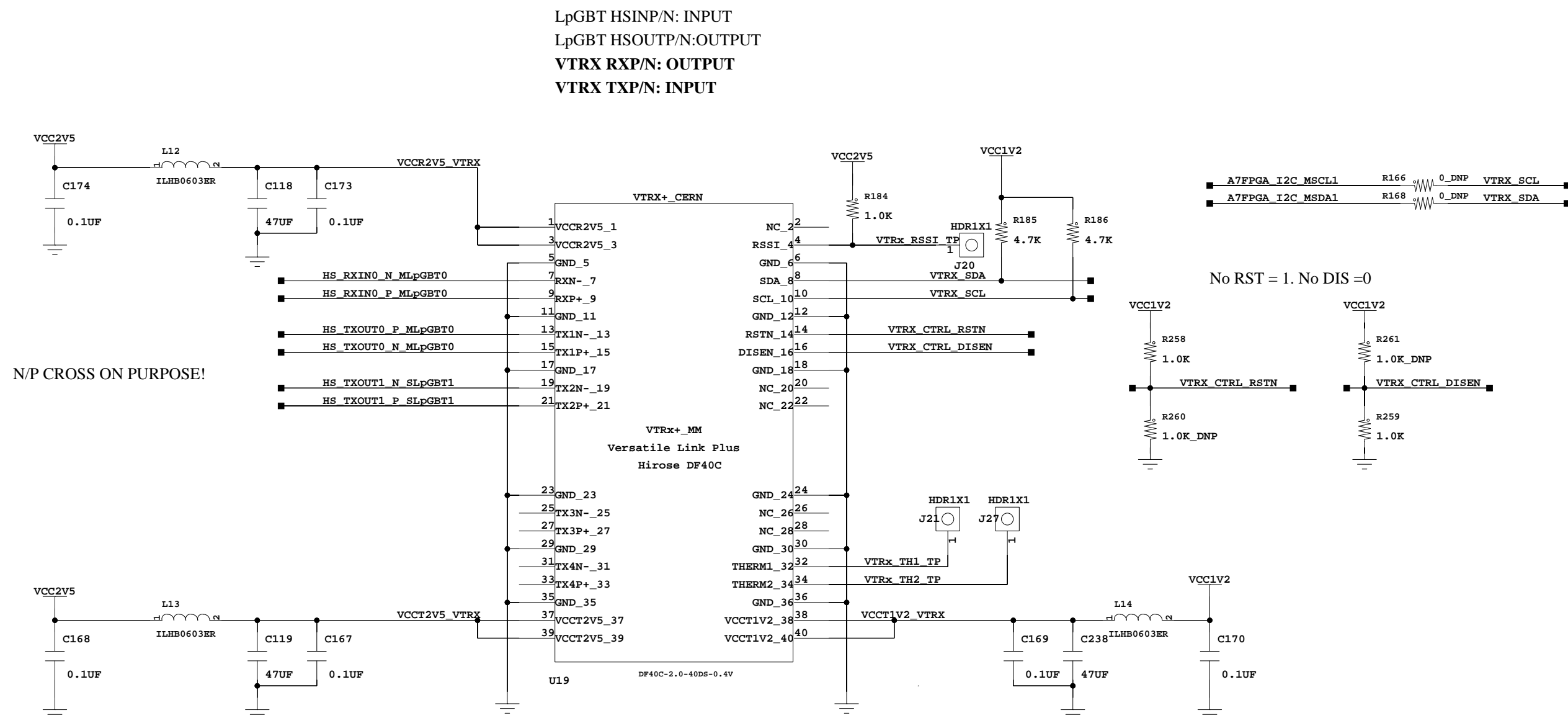
COMPANY					
University of Michigan					
TITLE					
LpGBT_CSM Prototype v2					
SIZE	B	REV	SHEET	21	OF N
DRAWN	XUEYE HU		DATE	30/09/2022:00:21	



MGTVCC: GND
MGTREFCLK: FLOAT
MGTRX: GND
MGTTX: FLOAT
MGTRREF: GND

XC7A35T FPGA GND&PWR BANKS

COMPANY		University of Michigan			
TITLE					
LpGBT_CSM Prototype v2					
SIZE	B	REV	SHEET	22	OF N
DRAWN	XUEYE HU		DATE	05/07/2022:23:07	




LpGBT HSINP/N: INPUT
LpGBT HSOUTP/N: OUTPUT
VTRX RXP/N: OUTPUT
VTRX TXP/N: INPUT

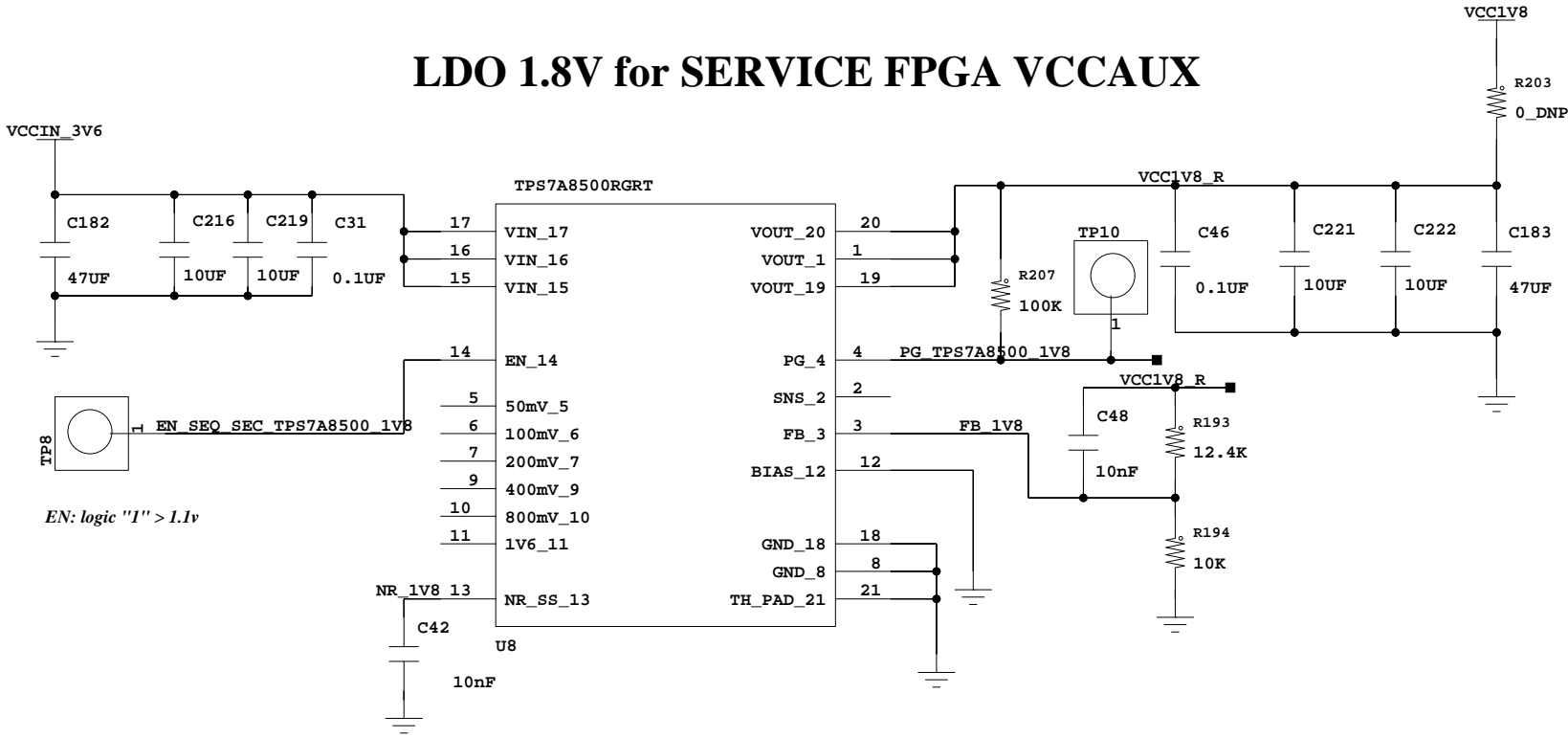
N/P CROSS ON PURPOSE!

No RST = 1. No DIS =0

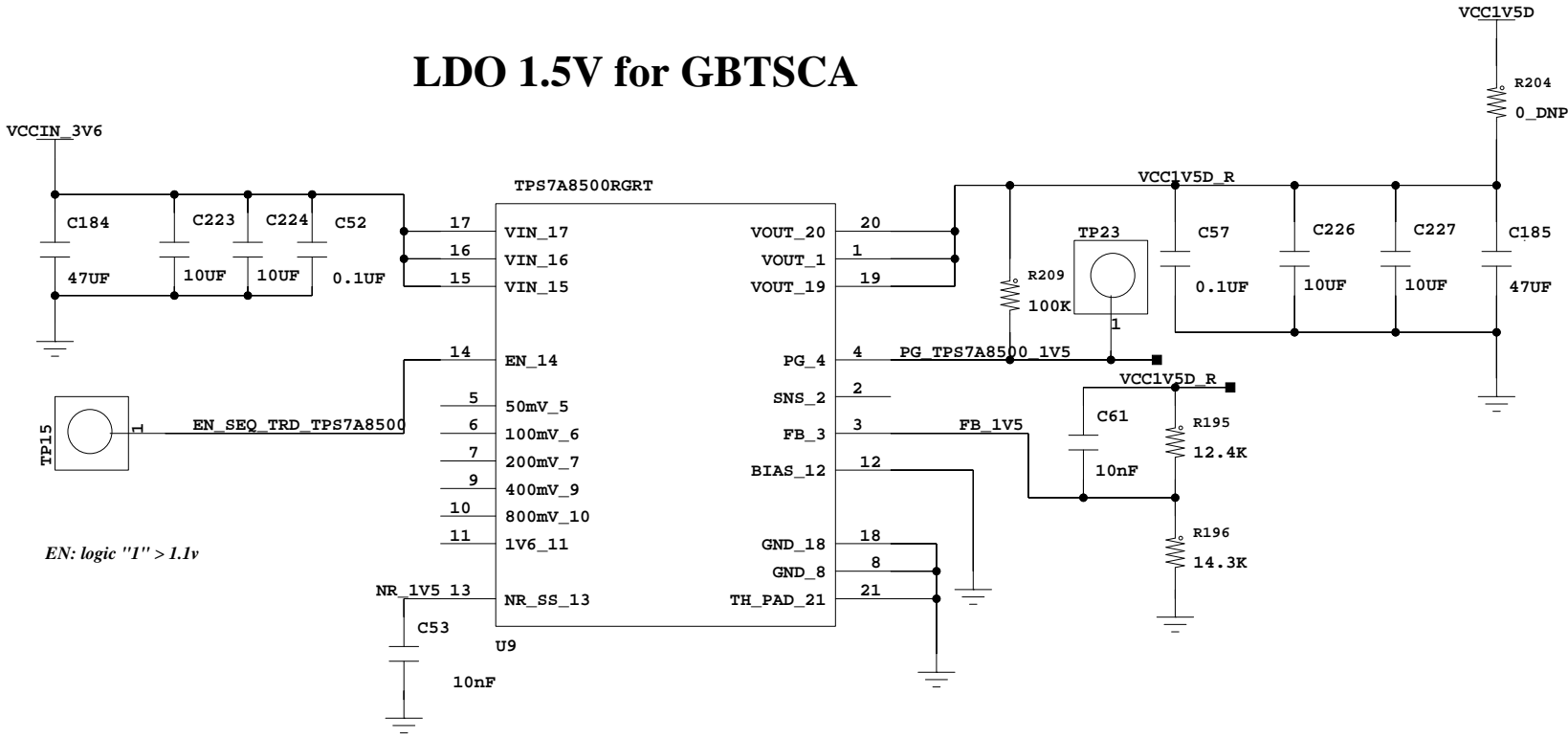
Hirose DF40C-2.0-40DS-0.4V
<https://edms.cern.ch/ui/file/2149674/1/VTRxPlusApplicationNote.pdf>
 Digikey: H11772CT-ND

VTRX+

COMPANY	University of Michigan	
TITLE	LpGBT_CSM Prototype v2	
SIZE	B	REV
DRAWN	XUEYE HU	SHEET 24 OF N DATE 22/05/2023:13:55



PULL-UP RES ON POWER-ON SEQ. Page




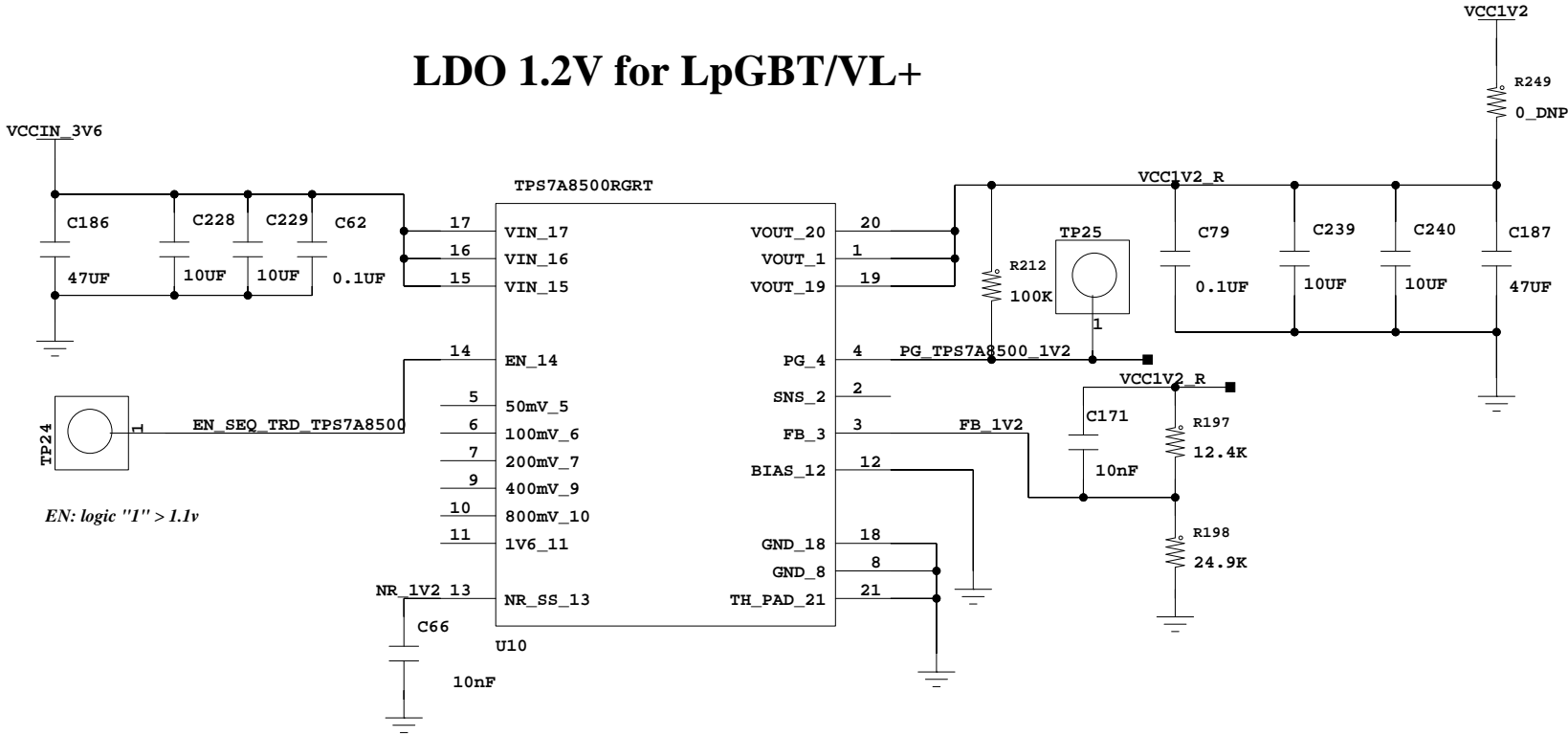
PULL-UP RES ON POWER-ON SEQ. Page

1. VIN Range 1.4V to 6.5V (W/O BIAS)
2. To ensure adequate thermal relief for 4A operation, a 3 x 3 grid of vias to GND MUST be placed under U1
3. PG NEEDS EXTERNAL PULLUP RES 10kohm to 100kohm
4. Cff from FB TO OUT CAN OPTIMIZES NOISE, PSRR. 10nF is recommended
5. PG EN CONTROL ON POWER-ON SEQ PAGE
6. VEN >0.5V ON; <0.5V OFF

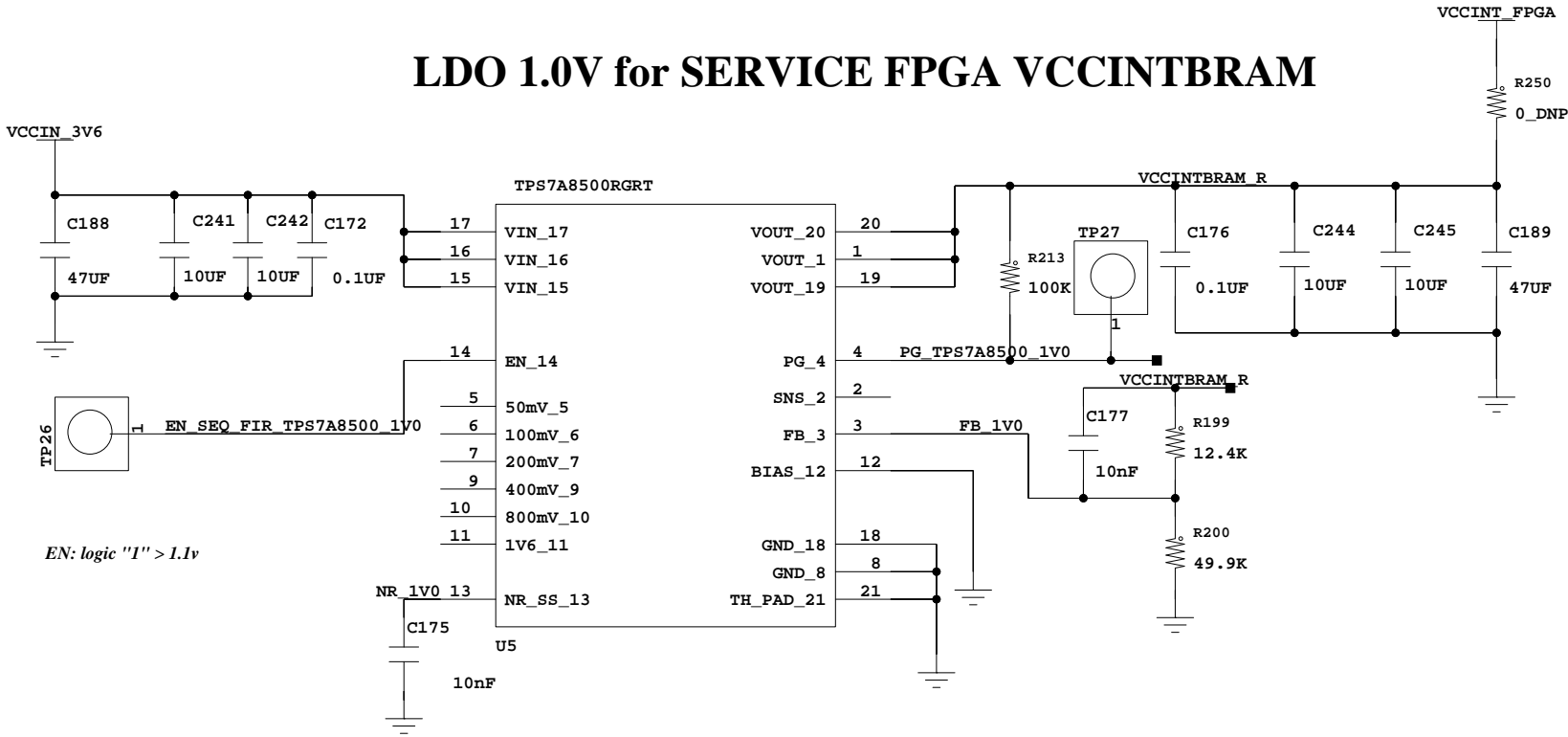
$V_{out}=0.8V*(R_O/R_G + 1))$

LDOs 1.8V & 1.5V

COMPANY					
University of Michigan					
TITLE					
LpGBT_CSM Prototype v2					
SIZE	B	REV	SHEET	26	OF N
DRAWN	XUEYE HU		DATE	22/05/2023:13:54	



PULL-UP RES ON POWER-ON SEQ. Page



PULL-UP RES ON POWER-ON SEQ. Page

1. VIN Range 1.4V to 6.5V (W/O BIAS)
2. To ensure adequate thermal relief for 4A operation, a 3 x 3 grid of vias to GND MUST be placed under U1
3. PG NEEDS EXTERNAL PULLUP RES 10kohm to 100kohm
4. Cff from FB TO OUT CAN OPTIMIZES NOISE, PSRR. 10nF is recommended
5. PG EN CONTROL ON POWER-ON SEQ PAGE
6. VEN >0.5V ON; <0.5V OFF

$$V_{out}=0.8V*(R_O/R_G + 1))$$

LDOs 1.2V & 1.0V

COMPANY		University of Michigan		M	
TITLE		LpGBT_CSM Prototype v2			
SIZE	B	REV	SHEET	27	OF N
DRAWN	XUEYE HU		DATE	22/05/2023:13:54	

FPGA Power-on Sequence

LDO TPS7A8500: PGOOD, En: 0V-VIN+0.3V
EN TH 0.5V

First Stage

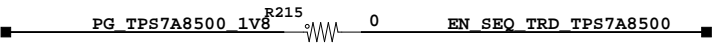
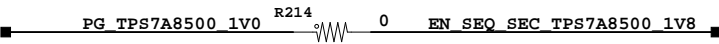
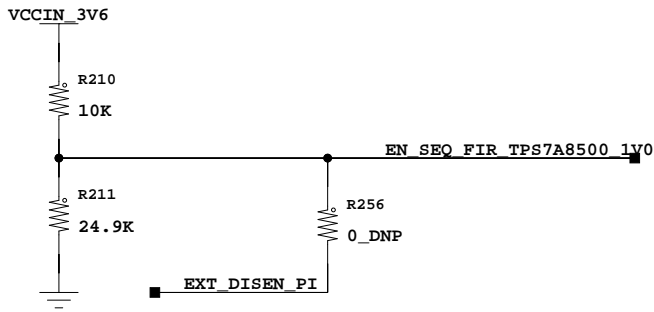
EN 1V0 VCCINT VCCBRAM

Second Stage

EN 1V8 VCCAUX

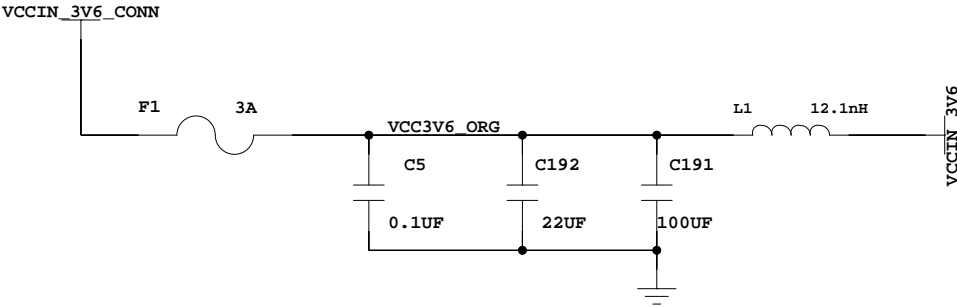
Third Stage

EN 1V2, 1V5D, 2V5, 3V3




Power from AMP140 CONN -- CSM MB

Fuse added for protection

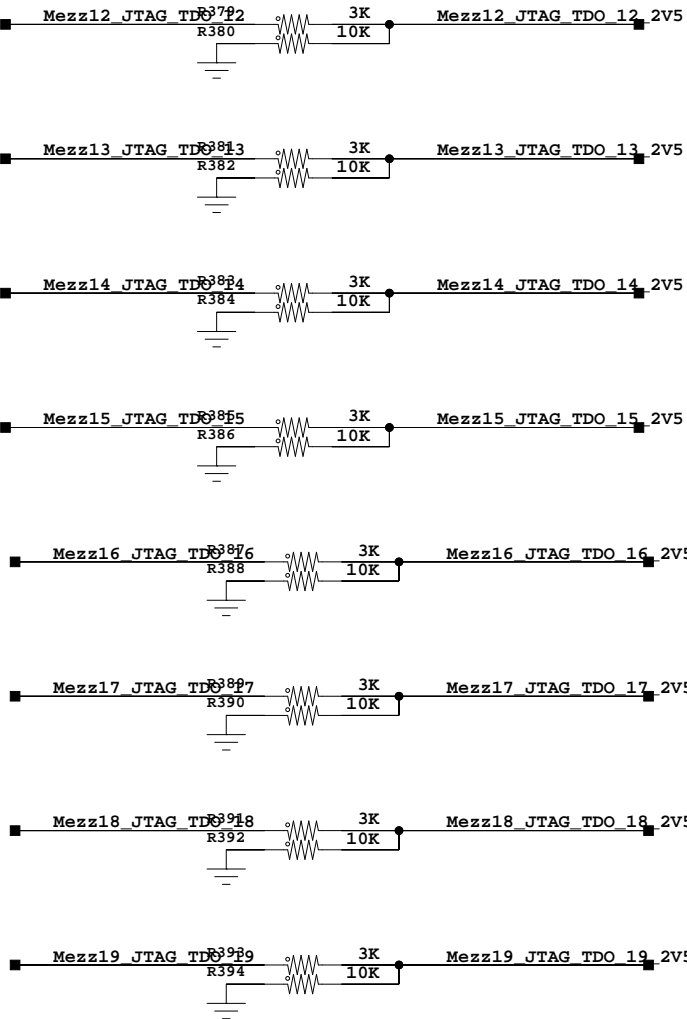
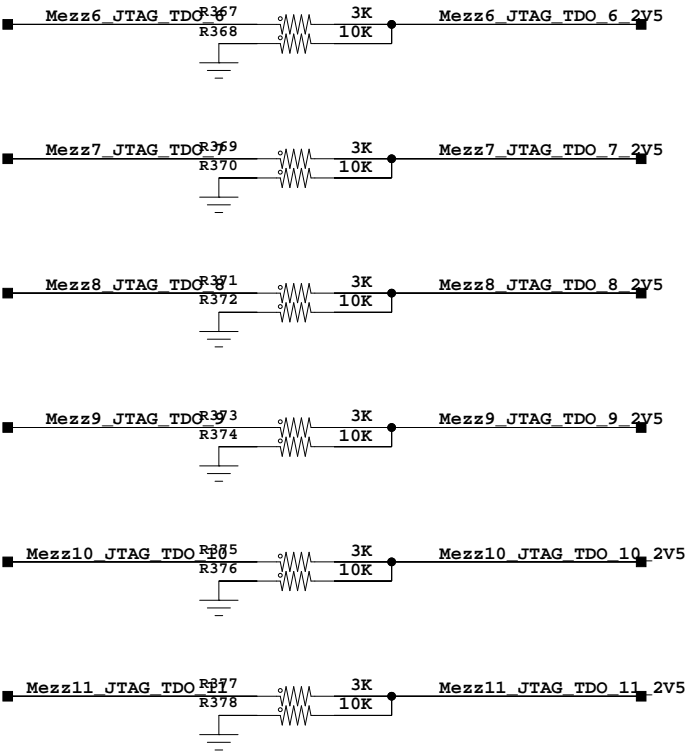
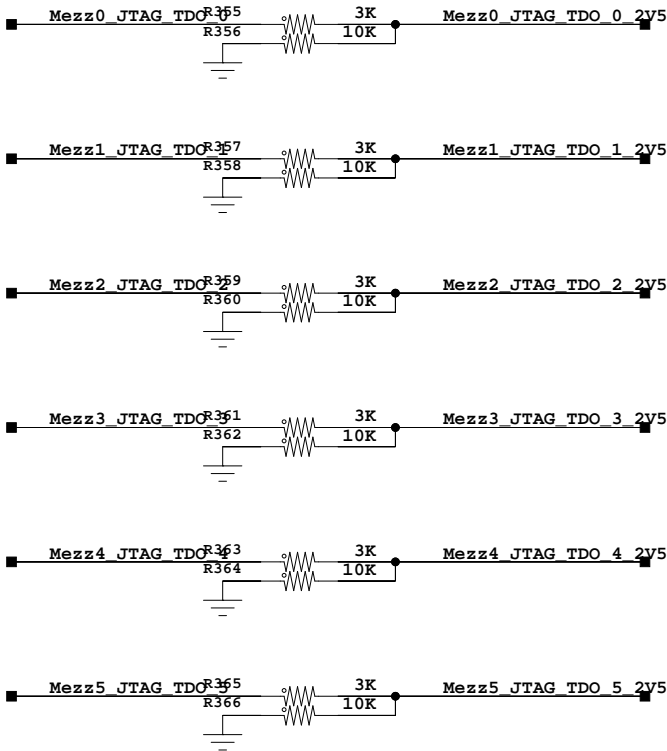


POWER ON SEQ. & CONNECTOR

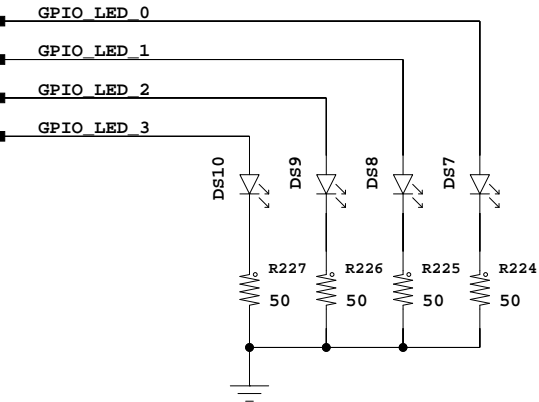
COMPANY				
University of Michigan				
TITLE				
LpGBT_CSM Prototype v2				
SIZE	B	REV	SHEET	28 OF N
DRAWN	XUEYE HU		DATE	22/05/2023:13:54

Mezz 3.0/3.3V, CSM 2.5V

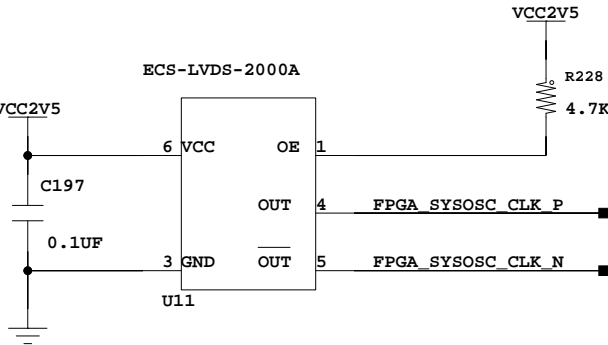
$(10k/10k+3k)*VOH(2.4v\ min) = 1.85V > VIH\ min\ 1.7V$




LED INDICATION FOR A7



200MHz OSC FOR A7

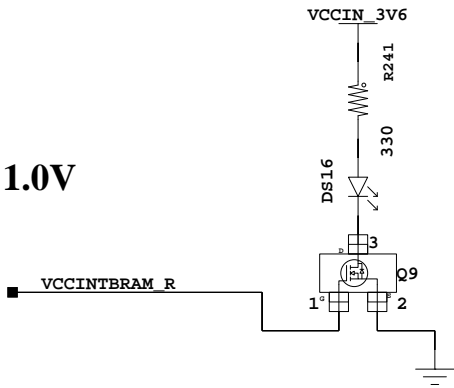


FPGA OSC
TDO Res Divider 3.3V-->2.5V

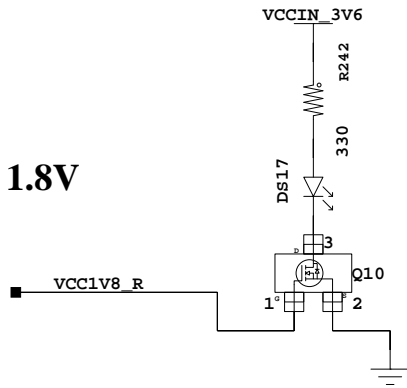
COMPANY					
University of Michigan					
TITLE					
LpGBT_CSM Prototype v2					
SIZE	B	REV	SHEET	29	OF N
DRAWN	XUEYE HU		DATE	22/05/2023:13:52	

Voltage Indication

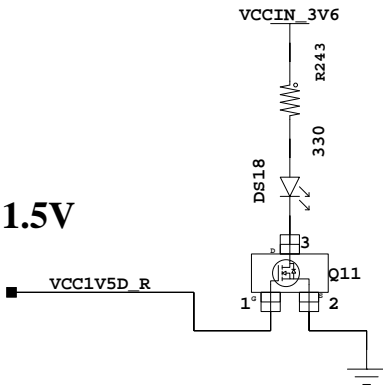
1.0V



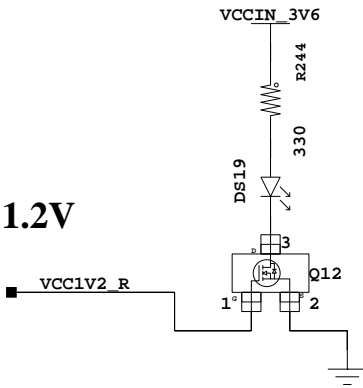
1.8V



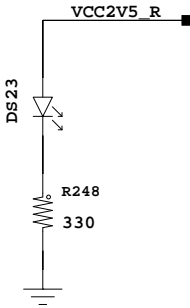
1.5V



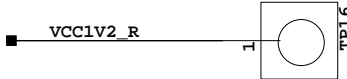
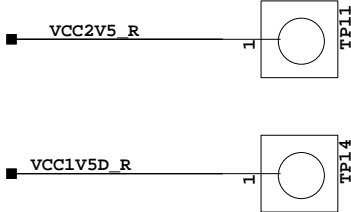
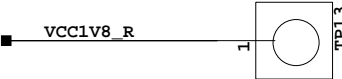
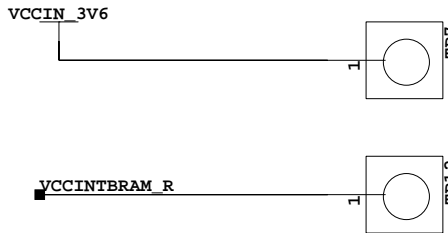
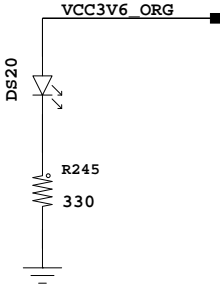
1.2V



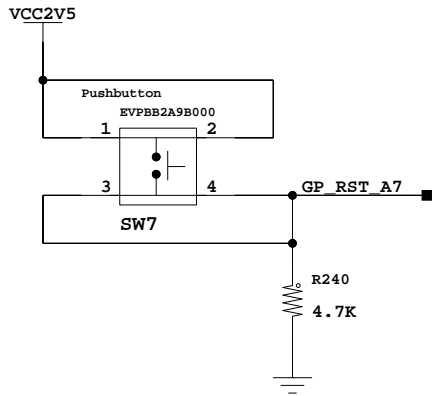
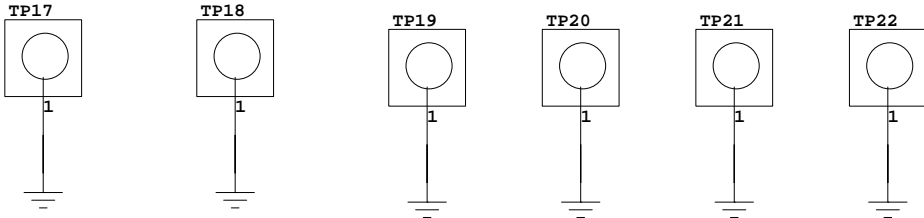
2.5V




3.6V



Ground test points



FPGA TEST POINTS

COMPANY					
University of Michigan					
TITLE					
LpGBT_CSM Prototype v2					
SIZE	B	REV	SHEET	30	OF N
DRAWN	XUEYE HU		DATE	30/09/2022:00:04	

