



Microp

2022

Department of  
Microelectronics and VLSI  
Technology

ISSUE – 1  
(February, 2022)

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## ABOUT THE UNIVERSITY

**Maulana Abul Kalam Azad University of Technology (MAKAUT), West Bengal** is the nodal University that provides affiliation to more than 200 Colleges spread throughout the state offering courses in Engineering & Technology, Pharmacy, Architecture, Management, Applied Sciences and various professional courses. The courses offered by the University are approved by the **All India Council for Technical Education** (AICTE) and UGC. The University has a twin character, viz. (a) as an affiliating University to provide and renew affiliation to more than 200 Colleges after duly carrying out the

process of inspection to satisfy themselves about the presence and quality of the infrastructural and human resources, to get the students in all the affiliated Colleges as well as the In-House courses registered, conduct the examination process, keep a tab on the teaching-learning process and help enhance employability of the students; (b) to conduct In-House courses, particularly in different cutting edge areas of Engineering, Technology, Management, and Applied Sciences, run funded projects leading to publications and patents, offer consultancy activities etc.

## **ABOUT THE DEPARTMENT OF MICROELECTRONICS & VLSI TECHNOLOGY**

The Department of Microelectronics & VLSI Technology at Maulana Abul Kalam Azad University of Technology offers two postgraduate programmes: **1). M. Tech in Microelectronics and VLSI Technology and 2). M. Tech. in VLSI and Embedded Systems.** The Programmes are initiated to create motivated, innovative, creative and thinking graduates to fill the roles of Electronic Engineers who can conceptualize, design, analyze and develop VLSI and Embedded systems to meet the modern day requirements. The number of product and service based semiconductor industry are growing, thus various career opportunities exist in product development companies including mobile and consumer electronics, computing, telecommunications, networking, data processing, automotive, healthcare and industrial applications. In this context, the Department of Microelectronics & VLSI Technology at Maulana Abul

Kalam Azad University of Technology would like to add to the growing human resources needs of VLSI and Embedded system sector as engineers through its M. Tech. programmes. During the programmes the theoretical foundation is built through courses like Digital VLSI design, High speed VLSI design, Low power VLSI Design, Analog and mixed mode design, system on chip design. The practice includes skill development in both Front end and Back end designs, verification and testing. The program also offers strong knowledge and practical skills in developing embedded solutions on varied platforms such as FPGA, Advanced microcontrollers and processors. Students learn to implement real time embedded systems. The designers gain practical knowledge through mini and major projects in both VLSI and Embedded system design domains.

**MISSION:**

- To apply knowledge and skill to solve engineering problems specific to the field of Microelectronics , Embedded Systems and VLSI Technology.
- To provide the framework for industrialization of the nation and the state of West Bengal based on knowledge based economy and intellectual resources.
- Be able to address the contemporary industrial issues with the advancement of technology.
- To participate in the Special Human Resource Development Program to meet the challenge of the global semiconductor industry.

**VISION:**

- To promote a global center of excellence in the field of Microelectronics , Embedded Systems & VLSI Technology.

## LIST OF FACULTY MEMBERS

Sl No	Name of the Faculty Member	Present Designation	Area of Specialization/Research Interest
1	Prof. Amitabha Sinha (HOD)	Director ( Academic reforms) & U.G.C. Adjunct Faculty	Processor Architecture and System-on-chip Design, DSP, VLSI Design, Advanced Architecture and VLSI design for Machine Learning and Neural Network.
2	Dr. Madhumita Das Sarkar	Associate Professor	Modeling of Semiconductor Devices, Photovoltaic Circuit and System Design
3	Dr. Mihir Kumar Mahata	Assistant Professor	III-V heterostructure semiconductor devices (Sensors, Solar cell, HEMT, etc.); Analog VLSI Design.
4	Mr. Sabyasachi Sen	Faculty	Advanced Microelectronic devices, Advanced Photo Voltaic cells and Sensors.
5	Mr. Sowvik Dey	Assistant Professor	Design and Implementation of Fault-Tolerant Memory Systems
6.	Mrs. Chumki Das	Technical Assistant	Microelectronics and VLSI Design.

## MESSAGE FROM HON'BLE VICE-CHANCELLOR'S DESK



I am glad to know that the Department of Microelectronics and VLSI Technology is going to publish the first issue of Departmental magazine Microp 2022. It is indeed a phenomenal achievement given the disruptions that we all have faced during the last couple of years and the huge amount of effort that is necessary to capture the variegated activities undertaken by the faculty members, students and staff members in the forms of reports and articles.

Microelectronics and VLSI Technology is one of the most interesting and challenging disciplines at the cutting edge of scientific and technological research having enormous applications in industry.

Students graduating from this Programme are expected to add value to both academics and industry through the skill and knowledge acquired by them. The publication of this Departmental Magazine is therefore a step in the right direction. I believe that this magazine will capture the attention of all the stake holders through the range and depth of its contents and that it will be a wonderful experience for the readers.

I congratulate all the students, faculty members, staff, HoD and the Director of the School for taking this endeavor in publishing the first issue of the Departmental magazine and wish them all success in future.

## HEAD OF THE DEPARTMENT'S COLUMN,

### MICROELECTRONICS & VLSI TECHNOLOGY, MAKAUT, WB.



**Prof. A. Sinha** The spin of the current revival of Microelectronics and VLSI enables IC designers to add all of the features in one chip. VLSI circuits are used everywhere, including microprocessors in a personal computer, chips in a graphic card, digital camera or camcorder, chips in a cell phone, embedded processors, and safety systems like anti-lock braking systems in an automobile, personal entertainment systems, medical electronic systems etc. VLSI technology is well suited to the demands of today's electronic devices and systems. With the ever-increasing demand for shrinking in size, compactness, performance, reliability, and functionality, VLSI technology is expected to continue to drive electronics advancement.

The very exciting time for the semiconductor industry in India with the government having announced the "Make in India" program following announcements related to National Policy on Electronics (NPE) and several programs to promote the holistic development of the Electronic System Design & Manufacturing (ESDM) ecosystem.

This includes encouraging entrepreneurship, investments in R&D, manpower development, incentives for setting up semiconductor FABs and related manufacturing, among others.

Department of Microelectronics & VLSI Technology of Maulana Abul Kalam Azad University of Technology, West Bengal is involved in the design and implementation of Analog, Digital, RF and Mixed-signal VLSI circuits and systems. Applications in Signal Processing are also being developed. Micro and Nano-scale semiconductor process technologies ranging from  $0.35\mu m$  to 90nm CMOS process technologies are being investigated for various VLSI System-On-Chip implementations. The Department is well equipped with Cadence VLSI design software and TCAD device simulator SILVACO. Growth and characterization laboratory of the department is equipped with Spin Coater, Metallization unit, Probe station, I-V, C-V measurement unit etc. Department is working on different VLSI circuit and advance device design projects. Some of the current undergoing research works are given below.

One group is working on a novel architecture for Analog Digital Signal Processor. The architecture of an Analog-Digital signal processor is a completely new concept. This processor leverages the advantages of both Analog as well as the digital signal processing. The group is also working to patent the idea as soon as possible. Another group is working on reconfigurable switch capacitor based ALU. Also, students are working on Bio-sensors, multi-junction solar cell etc..

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# The Challenge to Reform Engineering Education in the Context of Global Economic Scenario

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**Abstract:** The paradigm shift of engineering education in the context of global economic scenario is a must to provide students with the knowledge of cutting-edge technology. This article aims to review some of the salient attributes cited by renowned academicians across the globe for framing new methodology and conclude with balanced teaching learning process which promotes innovative ideas that best matches with the fast-growing global technological changes.

## I. INTRODUCTION:

The new paradigm for engineering education necessitates to keep students at the cutting edge of technology and requires a balance among domain knowledge clubbed with experimentation & design, knowledge about changes in the society and market driven economy. There are considerable concerns among different stakeholders in various disciplines of engineering schools that retaining old or traditional thoughts and mindset by engineering Institutes/schools may place engineers playing minor roles in the future and cause difficulties in adapting rapidly changed global market scenario. However, it also needs to be kept in mind that this path of transition from the old to the new paradigm may not be trivial.

In the context of our country, it is fact that barring a handful numbers of Institutes of National importance like IITs and IISC, majority of our universities are faced with financial pressures while the urge to make the change lies mostly with those who oppose the change. This situation, coupled

with the fact that there is no specific prescription for making this challenge to change. Still, a number of technological universities/schools have been making attempts for significant changes by adapting innovative approaches in their different undergraduate and graduate programs. It is needless to mention that established scientific methodologies and knowledge gained should be made useful for engineering Institutes/schools to innovate & devise new program or methodologies that fit in the present scenario.

This article aims for a review study of some of the salient attributes cited by renowned academicians for framing new methodology and conclude with balanced teaching learning process which promotes innovative ideas that best matches with the fast-growing technological changes in the context of global market scenario for future reform initiatives in technological universities/schools in our country (India).

## II. REFORMING ENGINEERING EDUCATION:

Reforming engineering education to a new paradigm shift started in the early 1990s, by the National Science Foundation (NSF), U.S.A [1,2] with an aim to keep the engineering education on the track that matches with the effect of globalization. Realizing the New Paradigm for Engineering Education, in Engineering Foundation Conference, held in 1998

(EFC'98), University of South Carolina, and University of Washington, added further stimuli to reform engineering education

Finally, Accreditation Board for Engineering and Technology (ABET) [1] introduced the criteria of Engineering education in 2000 which has been accepted worldwide.

National Academy of Engineering (U.S.A.) [3], described engineering as creative and innovative designing but was constrained by nature, by cost, by concerns of safety, reliability, environmental impact, manufacturability, maintainability, and many other including societal impact. Salient attributes of the New Engineering Education Paradigm have been stressed in many literature [4]. These attributes have been modified to reflect the industrial perspective [5]. They are: 1) Encouragement of diverse student academic backgrounds and faculty dedicated to developing emerging professionals; 2) Emphasize on mathematics and scientific knowledge foundation with engineering practices 3) Maintenance of regular, well-planned interaction with industry – including industry-based projects 4) Integration of subject matter, concepts, issues and principles – including relationships to earlier subject matter 5) Emphasis on inquiry-based learning and preparation for lifelong learning with much less dependence on lectures; 6) Stress on integrative, systems thinking, coping with change 7) Communications skills (listening, speaking, reading, and writing), teamwork and group problem-solving skills (from identification through analysis and resolution); 8) Focus on design issues involving life-cycle economics, environmental impact, sustainable development, ethics, timeliness, quality,

health & safety, 9) Manufacturability, maintainability, social, legal, standards and ad hoc concerns.

Even though it is true that the details of procedure, application and execution in some of the list of attributes may change over time, programs that reflect these attributes will make reformed-engineering graduates to face an unpredictable future with confidence. This in turn will help the society (or the world) where they will live. So, it is obvious that students attending universities/schools with programs that do not reflect these attributes will be lagging behind and finally they will lose interest in attending their schools. This leads to a disaster. As an analogy, just as a lack of diversity can cause disaster during downturns in the economy (like pandemic for an example), lack of flexibility (over specialization) in the engineering disciplines can lead to a disaster. This phenomenon was well addressed in Washington accord and a new Engineering education was recommended for Engineering with interdisciplinary and “all-round” abilities.

### **III. EFFECT OF GLOBALIZATION:**

Globalization has made the market competitive and product needs to be highly flexible, cost effective and capable of offering high performance. So, the graduates in the disciplines of engineering & technology should be highly innovative so that they are able to address these various challenges of the global market. Hence, expectation from “All-rounded” engineers are much more and the focus should be on outcome based education where outcome of the course should be clearly specified to the learners and knowledge that will be imparted must be translated to skill. Unfortunately, students who are deprived to

get this modern outcome-based education from their respective schools/Institutes will be left behind and will have no market value. Until recently, students used to continue to attend such academic institutions is not due to the fact that they liked very much rather they had adjusted to and accepted the condition as "normal," not realizing that they have become redundant. However, the dual effects of globalization and pandemic in recent times, have made the students worldwide more matured. However, the transition from the old to the new paradigm is non-trivial since making the change lies mainly with those who feel paradigm change as threat or those who are unable to give up their traditional age-old views.

#### **IV. SUGGESTED CURRICULUM IN NUTSHELL:**

Traditionally Curriculum for Engineering education has been designed in such a fashion that the importance of theoretical as well as practical classes are almost balanced so that whatever the students learn at theoretical classes will be validated in practical class. This will enhance the understanding of the subject and will create interest among students. Apart from the lab classes project and dissertations is also one of the most important part of engineering curriculum. This if is carried on following a proper scientific approach with a clear vision, the knowledge level as well as the innovation ability of the student can be elevated to a great extent. However, in many cases it is found that students are forced to do the project work according to whims and fancies of the concerned supervisors. Prior to offering projects to the students, if they are reviewed by a forum consisting of industry experts, eminent faculty members

of different universities and carried on the basis of 1) Objective (Motivation behind the Project) 2) Relevance 3) Applications and 4) Deliverables (expectation) then the objective of the project will have many fold gains. They are: 1) development of knowledge, skill and design expertise of the students.

#### **V. CONCLUSION:**

So, it is amply clear that a balanced strategy is the need of the hour and the clear indication is that the focus should be on students centric and the commitment should be on teaching as well as in research. In a developing country like India, to sustain the economic growth, we have to emphasize more on innovation as well as skill development and this can be done by balanced education system in our universities/schools to produce quality graduates in all levels.

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# Device Performance Analysis for Different Gate Locations in AlGaN/GaN HEMT by Silvaco Simulation

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**ABSTRACT:** AlGaN/GaN based high electron mobility transistors (HEMTs) with different gate locations have been simulated in Silvaco. The current-voltage analysis suggests that placing the gate nearer to the source results in higher saturation current. This happens as the voltage nearer to the source is less in comparison with the same nearer to the drain. This causes lesser reverse bias across the gate metal-semiconductor junction. Thus a HEMT with gate contact near the source is very useful for high power applications. At the same time, noise analysis of the devices suggests that the minimum noise figure, for the HEMTs where the gate contact is placed nearer to the source contact is higher than its counterparts. This creates some reliability issues in such semiconductor devices. The possible reason behind such phenomenon has also been discussed in this work.

**KEYWORDS:** Noise Figure, HEMT, Heterostructure, AlGaN/GaN, Power Performance, Device Simulation

## I. INTRODUCTION

AlGaN/GaN high electron mobility transistors (HEMT) are excellent candidates for high power, high frequency and high-temperature application [1] [2] [3]. In RF power applications, this device outperforms its predecessors, due to its larger band gap, high mobility and density of electrons at the 2 dimensional electron gas (2DEG) region at the AlGaN/GaN interface [4] [5]. Their noise performance has also been quite satisfactory [6]. Now, it is a well-known fact that HEMT with higher saturation current has an edge in high power operations. One of commonly applied methods for increasing the saturation current is placing the gate contact nearer to the source. Such devices have been used in many scientific works [7] [8] [9]. However, exactly how

the current changes with a change in gate location have not been explained extensively.

Moreover, the change in device noise with this change is required to be studied. Among the various kinds of noise in semiconductor integrated circuits, the flicker noise and the thermal noise are the ones that dominate [10] [11]. Among these two, thermal noise dominates in higher frequency region; flicker noise dominates in lower frequency region. Thermal noise or the Johnson-Nyquist noise is present in all electrical conductors and is independent of applied bias. But, as the gate to source and gate to drain length is varying, it may cause a change in the conduction path, thus a change in noise figure. Moreover in lower frequency ranges, changing the location of the gate may change the flicker noise of the device. Thus the reliability of the device may suffer if we try to increase the power performance by placing the gate terminal near the source. These issues have been addressed in this work.

In this work, five different AlGaN/GaN HEMTs have been simulated using Silvaco TCAD device simulation software. In each of them, the Gate contact is placed at a different point between the source and the drain contacts. The voltage current analysis has been done and the result suggests that as the gate is moved closer to the source, the current increases. The reason behind such increase has been analyzed. Checking for the rate of increase of current beyond the saturation voltage has also been done. For checking the reliability of the devices, noise figures have been obtained for each of the five samples. The reason for obtaining such results has

been discussed.

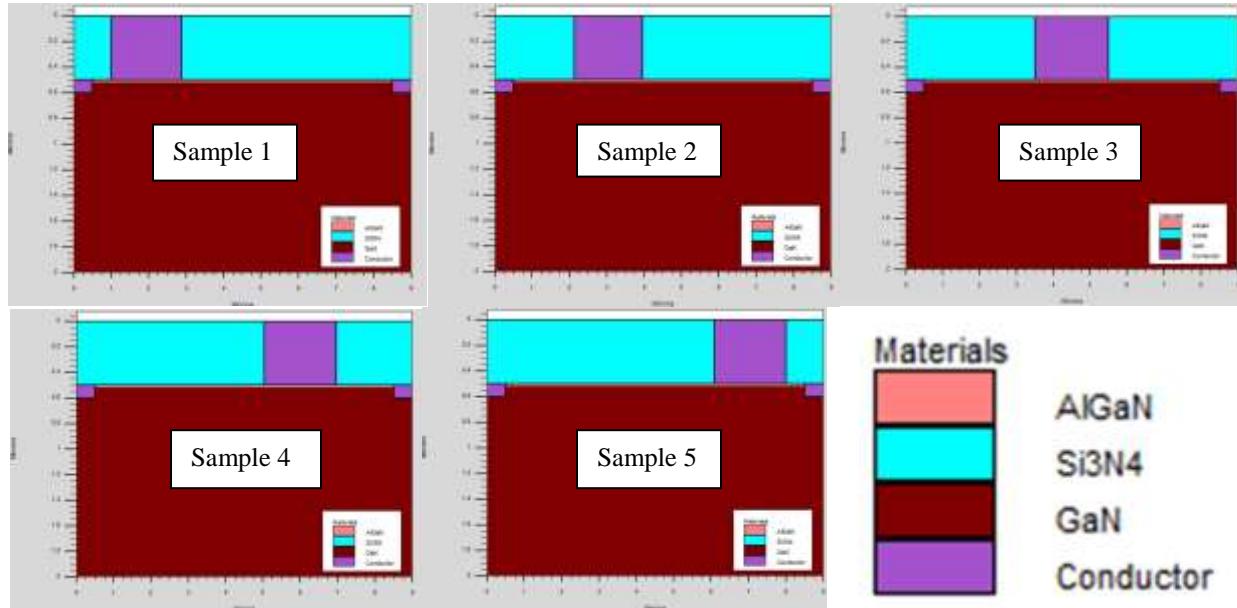
## II. DEVICE STRUCTURES

Five similar samples have been simulated in silvaco TCAD software. These structures were grown on a GaN substrate and  $\text{Si}_3\text{N}_4$  has been

## III. SIMULATION AND ANALYSIS

### a. Simulation of Current-Voltage Characteristics

To check the power performance of the sample HEMTs, both the Gate and drain characteristics have been obtained. The gate characteristic has been obtained by fixing the drain to source

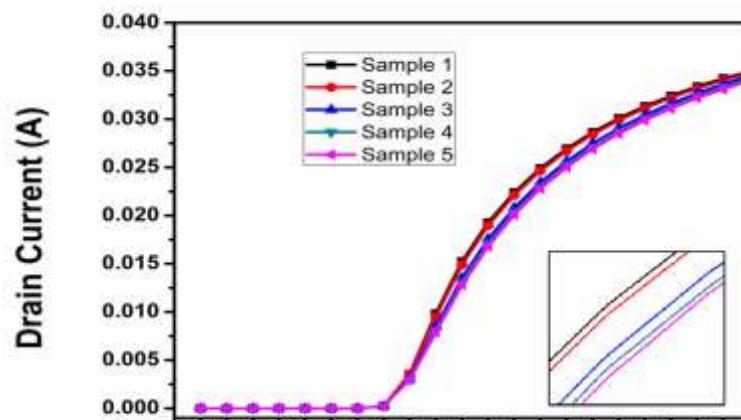


*Figure 1:- Five AlGaN/GaN HEMT samples with different gate locations*

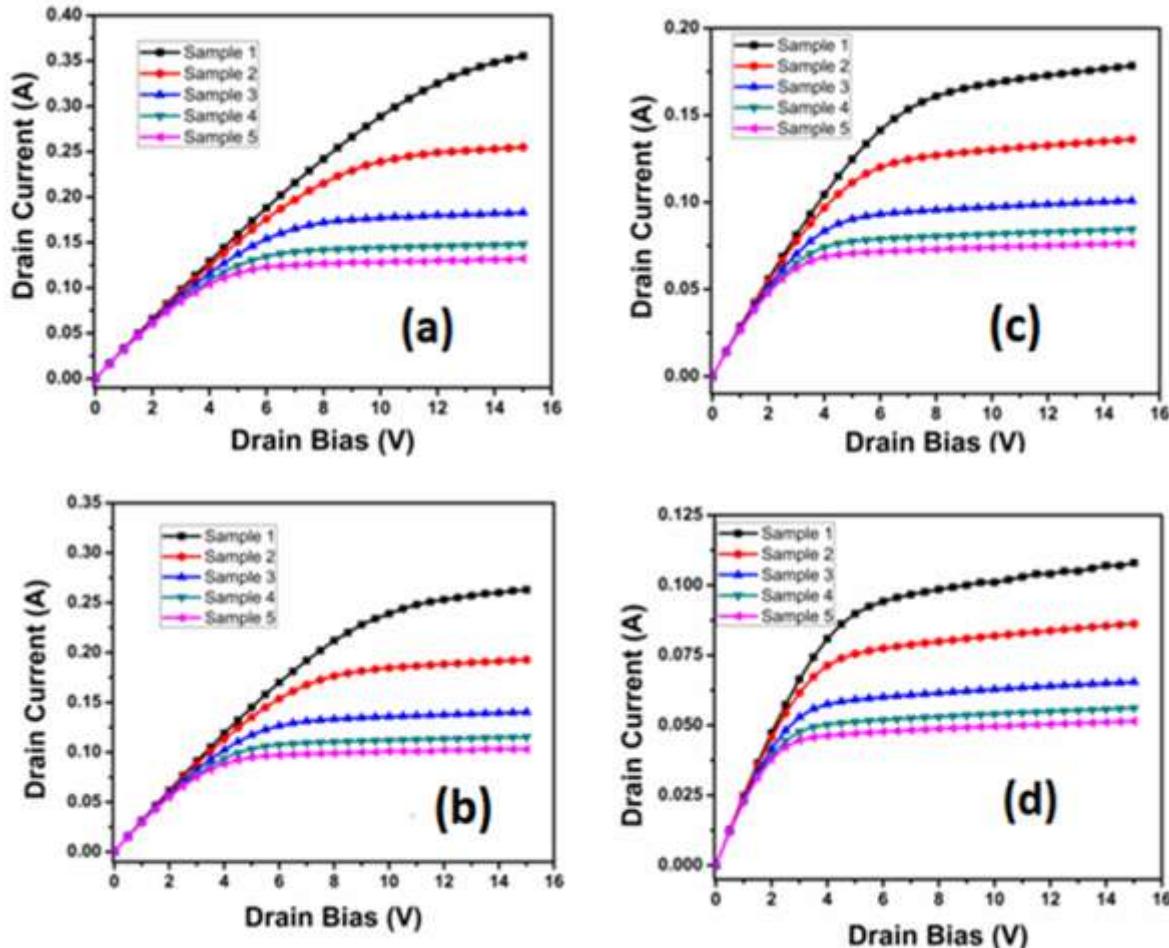
used as the insulator. The nitride insulator has been used for in-situ surface passivation of the devices [12]. The depth of the AlGaN layer is kept at 0.025 micron. The Source and Drain contacts are kept 8 microns apart. To avoid high gate leakage, a minimum distance of 0.5 micron has been maintained between gate and the other two contacts. These five samples with different locations of gate are shown in Figure 1.

voltage at 1 Volts and varying the gate to drain voltage from -9.5 volts to 1 volt. Figure 2 is the graph for gate bias vs. drain current.

From this figure 2, it can clearly be seen that drain current for a particular drain voltage is higher for sample 1. It goes on decreasing in samples 2-4 and is lowest for sample 5. However, this is not affecting the on/off voltage of the device that much. Thus it will reliably provide similar on-off voltage regardless of the physical location of the gate.



Similarly graphs for drain voltage vs. drain current has been obtained for 4 different values of



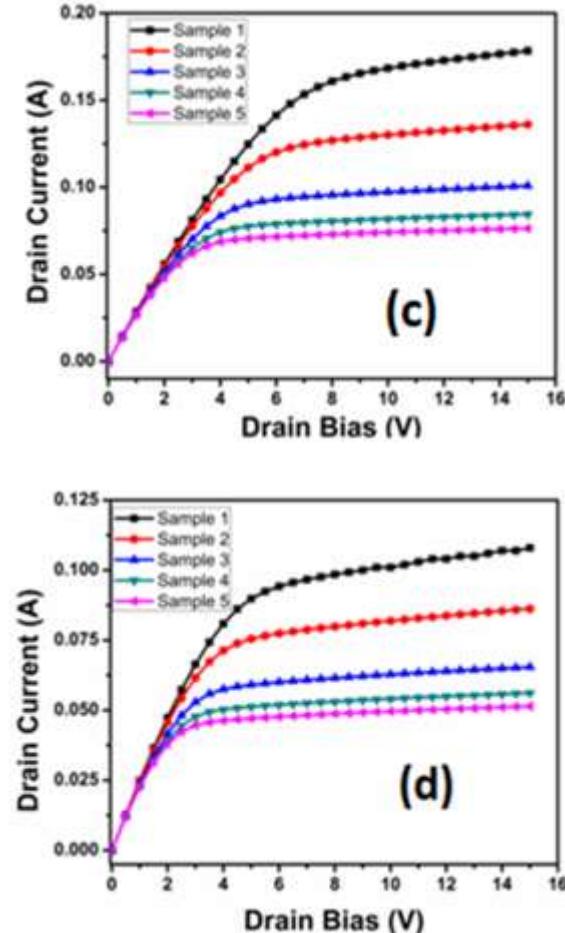
**Figure 3:- Drain Characteristics of the Sample HEMTs for Gate biases of (a) 0V, (b) -1V, (c) -2V, (d) -3V**

gate voltage (0V, -1V, -2V, -3V). These are represented in figure 3.

Now, it is a well known fact that the potential is equally distributed throughout the channel region between the drain and the source. Here, in all the samples the source contact is grounded. If a 5 V potential difference is applied between the drain and source contact, the voltage would have been maximum near the drain terminal and minimum near the source terminal. This situation is explained in figure 4.

In an AlGaN/GaN based HEMT, the gate contact is a schottky contact. This schottky contact is kept at a reverse bias. As the drain to source voltage increases, the reverse bias across the gate contact also increases. This increase in reverse bias widens the depletion region. When

this depletion region touches the 2DEG region, current saturation is achieved. At this point, if the



drain potential is increased further, the depletion region will cover more portion of the channel, which will not allow the current to increase at high rate.

If the Gate is placed near the source contact, the potential drop at any particular drain voltage across the gate is less. This potential drop increases more and more as the gate contact is brought near the drain contact. Thus it takes less voltage for an AlGaN/GaN HEMT with the gate contact near the drain contact to reach the saturation voltage. Similarly saturation voltage in case of AlGaN/GaN HEMT with the Gate contact near the source contact is higher. As the saturation voltage is higher, the saturation current will also be high. This is why, for high power applications, gate contacts are placed nearer to the source



**Figure 4:- The applied potential between the drain and the source distributes evenly in the channel. The potential drop near the source is minimum and the potential drop near the drain is maximum.**

contact.

Now, this increase in current is not a linear increase, it is an exponential looking increase. This can be explained mathematically. Let,  $t$  is the depletion depth required to reach the 2 dimensional electron gas region. Let  $V_a$  be the reverse bias required across the gate schottky contact to have depletion width of  $t$ . Now, if  $L$  is the length of the channel,  $l$  is the distance from the drain contact then saturation voltage for a particular location of gate  $V_{sat}$  will be

$$V_{sat} = \frac{L \times V_a}{L - l} \quad (1)$$

As the saturation current is maintaining a proportional relationship with the saturation voltage, it will also follow similar equation. This will result in a non linear increase in current with position of gate sliding towards the source.

These different potentials across the gate contact will also affect the dynamic resistance of the high electron mobility transistor. The dynamic

From the results in table I, it can clearly be observed that gate contact nearer to the source causes greater slope at the saturation region. But, all the values are quite low and this should not create big reliability issues.

### b. Simulation of Noise Figure

There are various types of noise in a semiconductor device. Out of which two are dominant in high electron mobility transistors. These are thermal noise and flicker noise. The combination of these two adds noise to the input signal. Practically, the input signal is itself noisy. Let the signal to noise ratio for such input be represented as  $\text{SNR}_{in}$ . Similarly noise in the output signal of a device can be represented as  $\text{SNR}_{out}$ . The ratio of these two gives the noise margin. The logarithm of noise margin gives the noise figure. This noise figure is one of the most common measures of device noise. Here, we have used noise figure to detect the noise in different devices. A device with high noise results in lower

**TABLE 1:- Slope of Current-Voltage Curves at Drain Voltage of 14.5 Volts**

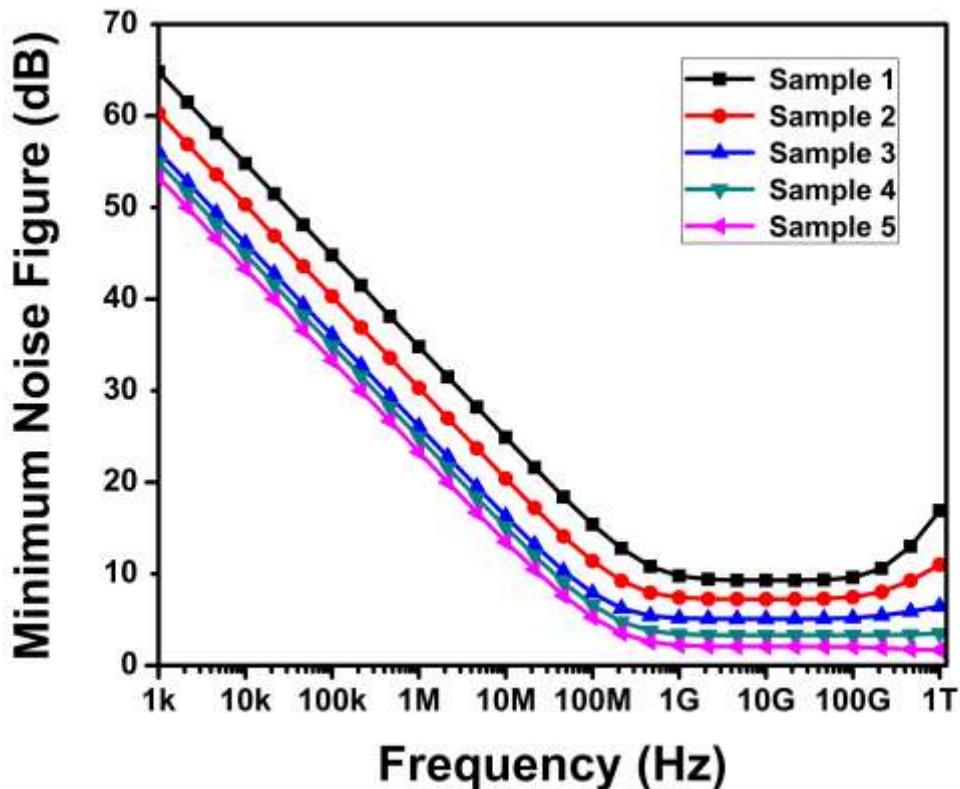
Gate Voltage	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5
0 V	0.0071505	0.0045895	0.0009446	0.0006770	0.0005735
-1 V	0.0026744	0.0021148	0.0008130	0.0005852	0.0004945
-2 V	0.0017768	0.0011208	0.0006449	0.0004691	0.0004091
-3 V	0.0012317	0.0007780	0.0004761	0.0003822	0.0003490

resistance at saturation region is expected to be dependent on the increasing depletion width. The slopes at drain potential of 14.5 Volts are given in Table I.

values of signal to noise ratio at the output, this makes the noise figure higher. The lower is the value of noise figure, the better is the device.

In this work, the minimum noise figure has been calculated for each of the 5 devices keeping the drain to source voltage at 0 volts. The

Now, the thermal noise is the noise in the resistances due to random thermal fluctuations. This fluctuation is not bias dependent; it is



*Figure 5:- Minimum noise figure of five samples at different frequencies*

noise has been calculated from a low frequency (1 kHz) to a very high frequency (1 THz). Generally, at lower frequency ranges the noise is more due to the presence of the flicker noise. The comparative graph for minimum noise figure at different frequencies is given in figure 5.

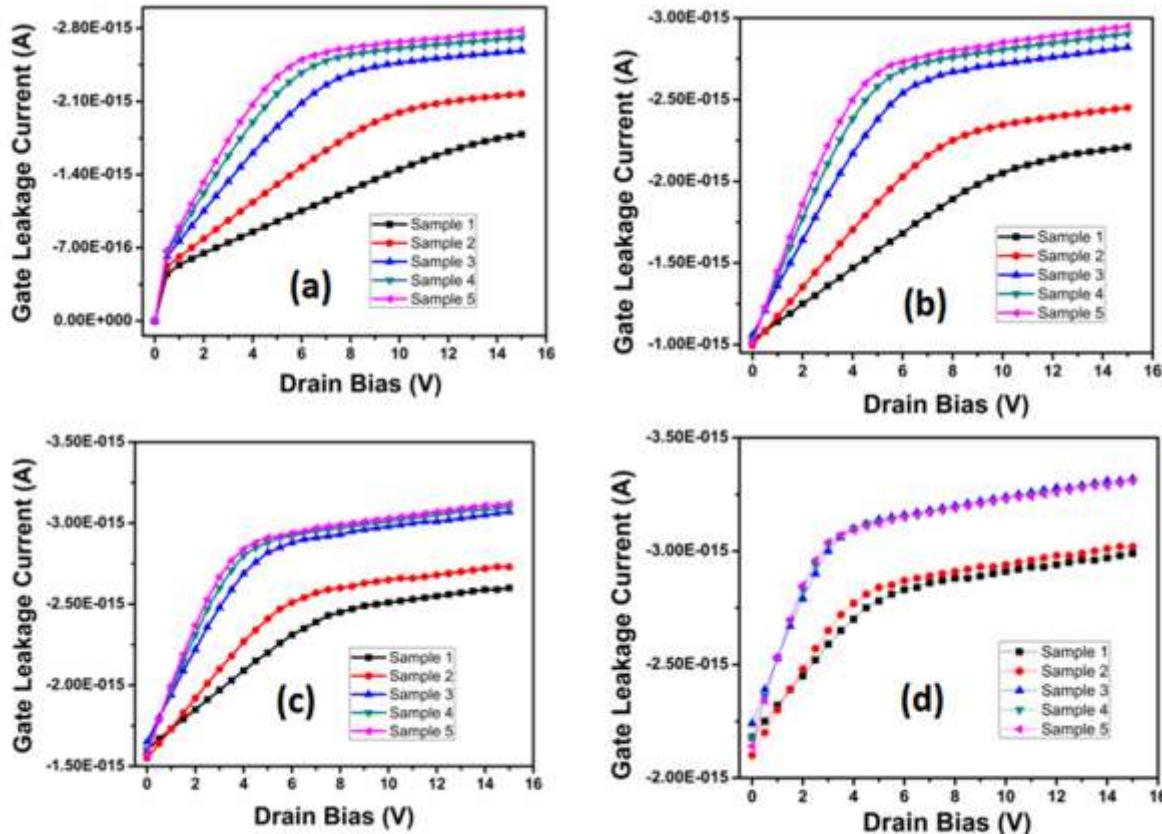
It can be inferred from figure 5 that the value of minimum noise figure is initially very high, and then it drastically falls down. It happens as the flicker noise has a density of  $1/f$ . For this reason the flicker noise is also called the  $1/f$  noise. It can be observed from the figure 5 that the noise performance is worse for the HEMTs with gate contacts nearer to the source. At both high and low frequency regions, the minimum noise figure is highest for sample 1 and lowest for sample 5. It can also be observed that the difference of noise figure is higher at lower frequency ranges. It is lower in higher frequency ranges. Thus, it can be said that both flicker noise and thermal noise becomes higher, if the gate contact is moved towards the source contact.

entirely an internal property of the resistances. Due to random thermal fluctuations, number of electrons in the conduction band changes, creating fluctuation in the current flow. Here, the current is travelling through four different resistances. These are source resistance, drain resistance, resistance of the 2DEG region & the resistance of the depletion region. Among these, the first two are constant in all the samples. The depletion region and the 2DEG region are the ones that change. It has already been shown that the depletion region is narrower in sample 1 & is wider in sample 5. The random fluctuation is more prominent in highly conductive path than the insulating path. This happens due to the energy gap between conduction and valance band. Thus the thermal noise increases as the gate is moved closer to the source contact.

Similarly the flicker noise is also higher in the devices with higher current. The problem with flicker noise is that its physical origin cannot be predicted properly. Several studies have tried to

find a link between the gate leakage current and the flicker noise [13] [14]. According to them, if the gate leakage current is significant in comparison to the drain current, only then the fluctuations in gate current contributes to the output noise of the device.

In this simulated HEMT, for all the five samples, the Gate current is relatively negligible in comparison to the drain current. This means



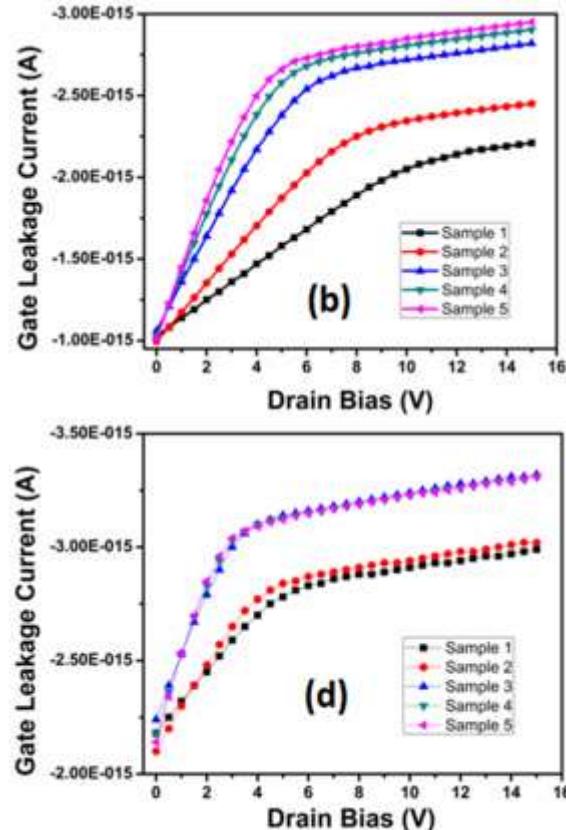
**Figure 6:- Gate Leakage Current vs. drain bias of all the five samples with different gate voltages (a) 0 V, (b) -1 V, (c) -2 V, (d) -3 V**

that the fluctuation in Gate current should not affect the fluctuation in output. The figure 6 is the comparative graphical representation of the gate leakage current at different gate and drain voltages of all the samples.

From figure 6 it can clearly be seen that the gate leakage current is extremely low, thus it should not cause any significant change in the noise figure. Not only that, the gate leakage current becomes higher if the gate contact is placed nearer to the drain contact. This is not happening in case of the noise figure. However, this change is expected to reflect in noise figure in devices with higher leakage current.

Although the actual source of flicker noise is unknown, the overall noise also depends on the

effective gate voltage [15]. Studying gate voltage dependence of the noise has been used as a way of distinguishing different noise source in a device [16] [17]. If the noise in an AlGaN/GaN HEMT is dominated by the channel noise, then the noise spectral density should be a dependent on the effective gate bias. This noise spectral density is inversely proportional to  $1/(V_G)^x$  [17]. Here  $V_G$  is the effective gate voltage. The constant  $x$  varies



from 1 to 3 depending upon the ratio of channel resistance and the series resistance. For this range of values, the noise always decreases with increase in effective gate voltage. It is already known that the effective gate voltage is higher if the gate contact is nearer to the source contact. Thus it can be concluded that the lower effective gate voltage is the cause of higher noise in the AlGaN/GaN HEMT where the Gate contact is nearer to the source contact than to the drain contact.

#### IV. CONCLUSION

The results show that placing the gate contact near the source contact in an AlGaN/GaN HEMT

increases the saturation current, thus making the device more suitable for high power applications. But, at the same time some reliability issues can also pop up. Firstly, the dynamic resistance at the saturation region becomes higher. However, this effect is not significant enough to cause serious reliability issues. The study also shows that the noise figure also increases if the gate contact is placed nearer to the source contact. This happens due to decrease in effective gate voltage. Hence, higher current and better noise performance cannot be achieved at the same time. However, at the higher frequency ranges the height of noise figure is relatively low. Thus, at high frequency operations, the gate contact can be placed near the source contact without much worry. Otherwise application specific optimisation has to be done. While placing the gate nearer to source extra preventive care has to be taken (like the T shaped gate) to keep the noise under desired level.

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# DESIGN AND IMPLEMENTATION OF 32 - BIT MODIFIED RISC ARCHITECTURE

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**Abstract:** One of the prominent features of the RISC processor is that it follows pipelining with compact instruction set that improves the performance and speed considerably and every instruction will return back to the same fetch cycle after completing the execution of each instruction. Every stage must be completed in one clock cycle. As a result, the design will help to improve the speed of the processor as well as provide high performance. The architecture consisting of pipelined control RISC processor consists of 5 stages namely fetch, decode, operand fetch, execution and write back. Instruction set design has been implemented which specifies the operand and opcode sizes as well as the instruction format has also been provided. The important components of the 32 – bit modified RISC architecture include the Program Counter, Instruction Register, Instruction Decoder, Arithmetic Logic Unit, Accumulator, Register File and Control unit. Since the architecture follows the Harvard Architecture model, there will be separate Program memory and separate Data memory blocks. A microoperation table has been shown for each instruction such that the fetch and decode cycle will be same for all the instructions. The instruction set are based on four addressing mode and 7 types of instructions are selected. Simultaneously opcode bits have been generated for each instruction based on four addressing modes. Every microoperation will have one T state and simultaneously in that particular T state, the control signal will be activated and the rest will be low. The design is based on program counter, instruction register, program memory, arithmetic and logical unit and data memory and hence separate modules has been built for analysis and simulation results have been fetched separately. The functionality and performance issues for each separate module like area, power dissipation, clock speed and propagation delay in the form of synthesis report are analysed and presented in this paper using XILINX Version 14.7 software tool.

**Keywords**—RISC processor, pipelining, Program memory, Data memory, simulation

## I. INTRODUCTION

RISC stands for Reduced Instruction Set Computer. RISC Processor is designed to reduce the execution set by simplifying the instruction set computer. In other words, it signifies that the processor requires only one clock cycle. The core features of RISC include the load and store architecture in which memory is accessed. Since the load and store

instruction are frequently used, large number of registers are required for implementation.

The trend for the past few years shows that the RISC Processors clearly outsmarts the CISC Processors. The reason being that these RISC processors has several advantages such as reduced instruction set, fewer instructions and hence few addressing modes. The RISC processor has fixed instruction length that means all the instructions are of same length.

As a result, the instruction format will be fixed while doing the instruction set design. RISC Processor also provides hardwired control unit which faster clock speed by elimination the use of microprogrammed control unit. As a result, RISC Processor are mostly preferred nowadays for simpler operation compared to CISC.

The term RISC V was first designed in the university of California, Berkeley. Prof. Krste Asanović and graduate students Yunsup Lee and Andrew Waterman started the RISC-V instruction set in May 2010 as part of the Parallel Computing Laboratory (Par Lab) at UC Berkeley. The Chisel hardware construction language that was used to design many RISC-V processors was also developed in the Par Lab.<sup>[1]</sup> The paper focuses on the design of 32 – bit Modified RISC Architecture using pipelining process and implementing the design in Verilog programming in XILINX ISE software tool. Pipelining techniques greatly reduce the instruction execution time with machine cycles. [2-3]. The authors Vishal Raj, Rutuja Patil, Alpesh Patil, Vikas Vishwakarma and Preeti Hemnani designed and implemented 32 – bit processor design on FPGA using Von Neuman Architecture. A low cost 32-bit RISC processor has been designed using Verilog and synthesized.<sup>[4]</sup> Almost similar work has been carried out by author Galani Tina G., Riya Saini and R.D.Daruwala, in their paper, “ Design and Implementation of 32 – bit RISC Processor using Xilinx”, where the main objective of this paper is to design and implement of 32 – bit RISC (Reduced

Instruction Set Computer) processor using XILINX VIRTEX4 Tool for embedded and portable applications. However, RISC processor is designed with load/store (Von Neumann) architecture.<sup>[5]</sup> The use of Von Neumann architecture means that all operations are performed on operands held in the processor registers and the main memory can only be accessed through the load and store instructions. In the conventional Von Neumann architecture, program and data are stored in the same memory. With a single memory unit, pipelining will be affected because at any instant, either instruction fetch operation or operand fetch or write back operation will be performed. This reduces the efficiency of the pipelining to a large extent. In order to increase the speed and efficiency, the super Harvard architecture model is required that will consist of dual memory that has been focussed on this paper. The architecture that has been designed consist of separate memories for data and program instruction with separate buses for each. Also, some additional features like instruction cache have been used to improve the speed of the processor. Since the buses operate independently, program instruction and operand (data) can be fetched at the same time, improving the speed over the single bus design. After designing the architecture, all the operation for each instruction can be performed using the modified architecture and microoperation table has been given for each instruction at every T state. Simultaneously, for every T state, the clock signals will be activated. Designing and implementing the 32 – bit Modified RISC Architecture will be done in Verilog programming in XILINX ISE 14.7 Software tool in Spartan 3E FPGA specification where separate modules can be implemented and simulation result will be generated. The complete design has been written using Verilog and then simulated and synthesized. Synthesis report can be extracted from the software where functionality and performance issues like area, power dissipation and propagation delay can be analysed.

## II. DESIGN METHODOLOGY

The following steps are required in order to design and implement a

32 – bit Modified RISC Architecture:

1. Designing the structure of each instruction or instruction format
2. Determine the opcode and operand sizes
3. Determine the type of instructions
4. Determine the type of addressing modes for each instruction
5. Design of instruction set including detailed about each operand and opcode
6. Draw the schematic of the processor including all the control signals
7. Forming the table for microoperation in different T states and corresponding control signals keeping pipelining in view
8. Derive Boolean expressions for all the control signals
9. Write Verilog code for each control signals derived from Boolean expression
10. Perform simulation using test bench
11. Extract detailed synthesis report

### II.1: INSTRUCTION SET FORMAT

The proposed architecture will follow Harvard Architecture for storing program and data separately. Specification of 32-Bit RISC Processor includes the following:

INSRUCITION SIZE = 32 Bit (7 bit for Opcode and  
25-bit for  
operand)

Data memory=  $2^{25} * 16$  bit

Program memory =  $2^{25} * 32$  bit

All registers are 16-bit wide  
 16 Bit ALU  
 Flag Size = 2 bit  
 Address Size= 25 Bit  
 $\text{Memory Address Location} = 2^{25} * 16$

#### Direct Addressing ALU Instruction Set Format:

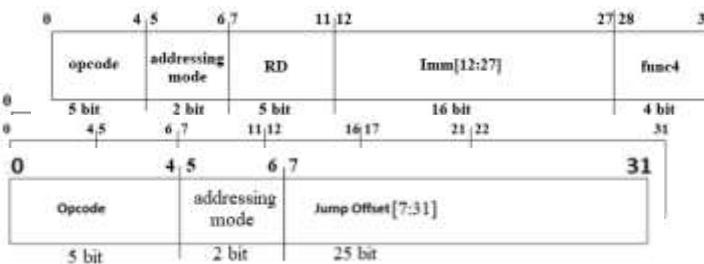
Opcode	Source Operand (1)	Source Operand (2)	Destination address of result	Address of next instruction
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#### Register-Immediate ALU Instruction Format:

#### Register-Register ALU Instruction Format:

#### Register-Register ALU Instruction Format

#### Unconditional Jump Instruction Format:



## II.2: TYPES OF INSTRUCTION:

The following are the list of instructions which are to be executed using the architecture:

- Data Transfer Instruction: LH, LW, SB, SW, LDA, STA, MOVE
- Arithmetic Instruction: ADDI, ADD, SUB, SUBI, DIV, REM
- Logical Instruction: ANDI, AND, ORI, OR, XORI, XOR, NOT, SLT, SGT, SLTI, SEQZ, SRAI, SRA
- Data Manipulation Instruction: SLLI, SLL, SRLI, SRL, RAR, RRC, RLC, RAL
- Transfer of Control (conditional and unconditional): BEQ, BNE, BLE, BGT, BGE, BLTU, JMP, JC, JNC, JZ, JNZ, JP, JN, JPE, JPO
- Subroutine Links: CALL, RET
- Machine Control: Halt

## II.3: TYPES OF ADDRESSING MODE:

The types of addressing mode that has been used in the instruction table are:

- Direct Addressing Mode
- Indirect Addressing Mode
- Immediate Addressing Mode
- Register Addressing Mode

SI No.	Instruction	Opcode Bit (5 bit)	Addressing Mode (2 bit)	Remaining Address (25 bit)
		Contains pure opcode		
<b>Direct Addressing Mode</b>				
1	LW	00000	00 (Direct Addressing)	
2	SW	00001	00 (Direct Addressing)	
3	LDA	00010	00 (Direct Addressing)	
4	STA	00011	00 (Direct Addressing)	
5	MOV	00100	00 (Direct Addressing)	
6	ADD	00101	00 (Direct Addressing)	
7	SUB	00110	00 (Direct Addressing)	
8	MUL	00111	00 (Direct Addressing)	
9	REM	01000	00 (Direct Addressing)	
10	AND	01001	00 (Direct Addressing)	
11	OR	01010	00 (Direct Addressing)	
12	XOR	01011	00 (Direct Addressing)	
13	NOT	01100	00 (Direct Addressing)	
14	SLT	01101	00 (Direct Addressing)	
15	SGT	01110	00 (Direct Addressing)	
16	SEQZ	01111	00 (Direct Addressing)	
17	SRA	10000	00 (Direct Addressing)	
18	SLL	10001	00 (Direct Addressing)	
19	SRL	10010	00 (Direct Addressing)	
20	RAR	10011	00 (Direct Addressing)	
21	RRC	10100	00 (Direct Addressing)	
22	RLC	10101	00 (Direct Addressing)	
23	RAL	10110	00 (Direct Addressing)	
24	JMP	10111	00 (Direct Addressing)	
25	JC	11000	00 (Direct Addressing)	
26	JNC	11001	00 (Direct Addressing)	
27	JZ	11010	00 (Direct Addressing)	

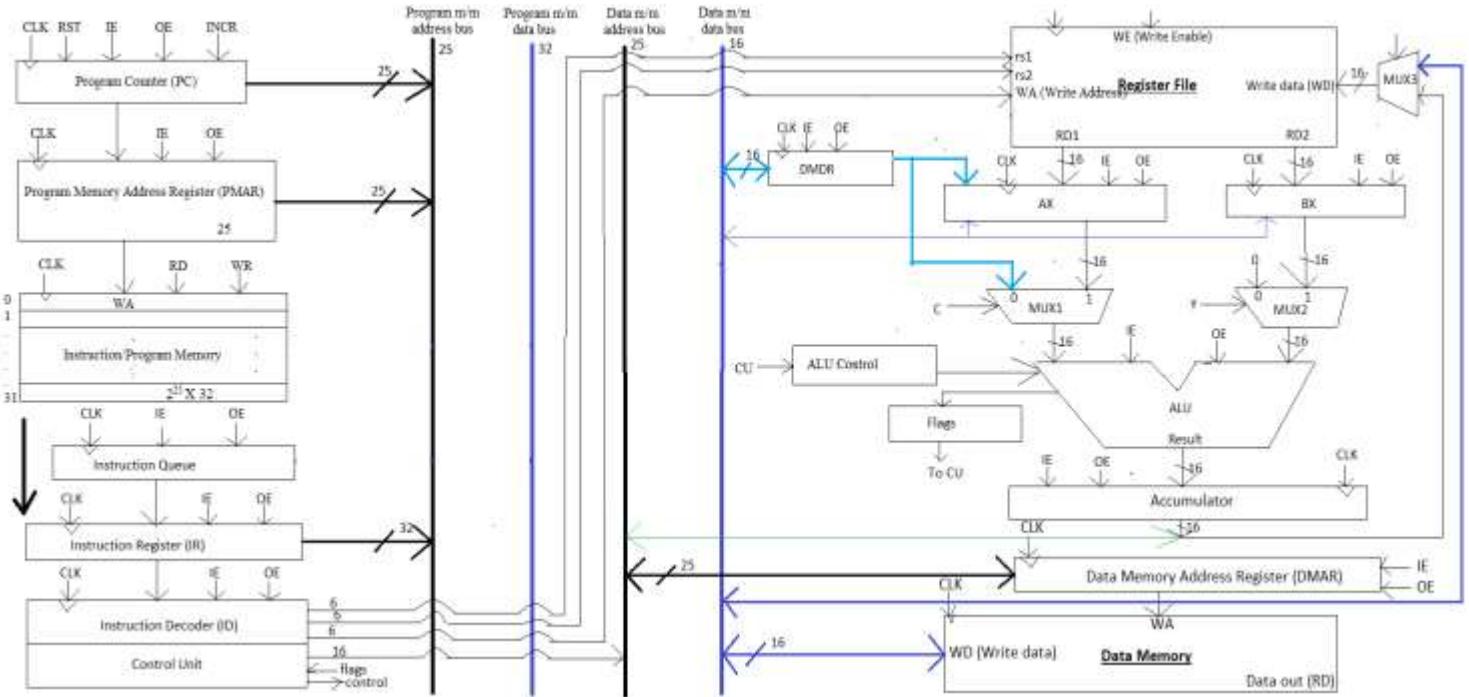
## II.4: INSTRUCTION SET:

The first five bit determines the pure opcode bit and the last two bit determines the type of addressing mode and the remaining bit are for the address bit. Only one type of addressing mode, that is, direct addressing mode is shown here. Similarly for other addressing mode, the instruction set for each instruction can be performed.

## III. ARCHITECTURE OF 32 - BIT MODIFIED RISC CPU:

The above architecture will be used to implement the instruction for any basic arithmetic and logical operation. In the architecture, initially, the Program Counter points to the first instruction starting. As a result, new value gets loaded at the end of cycle. Here, the program counter can be used as memory address.

The general-purpose register used are accumulator and temporary registers, AX and BX of 16 bit each. The special purpose register used are program counter, instruction register, data memory address register and data memory data register.



**Fig 1: Architecture design for different Functional Units of CPU**

Program counter holds the address of the next instruction to be executed. Accumulator to BUS is bi-directional because the data has to come to the accumulator. Other end of the accumulator goes to ALU and the results of the arithmetic or logical operation will come into accumulator. The memory will deliver data for read operation. Two operation, read and write can be performed on memory. For Read operation, some address has to be given to the memory and memory in return will return will deliver the data that will be stored into the register, that is, data memory data register.

The steps required for 1 clock cycle involving pipelining are:

1. Fetch instruction from memory
2. Decode instruction: Using some instruction fields and opcode
3. Opcode Fetch
4. Execute and 5. Write Back

Write Enable is permitting whether to write on to the register or not. If it is permitting then it is set to 1.

Instructions will be kept in the instruction/program memory. So, we have the instructions in the program memory.

To address 32 registers, 5 bits are required. Suppose for 32-bit processor, we have instruction as **ADD x5, x9, x10**.

Out of 32 bits, 5 bits each can be read by the source registers rs1 and rs2 and the rest can be fed to write address of register file.

In register file, rs1 and rs2 are the source registers which are used to receive the instructions from the program memory and RD is the destination register which will give the output data to ALU for arithmetic or logical operation.

In ALU block, the arithmetic and logical operations can be performed similar to the example given and that output (data) can be written onto the register file.

**Data Memory Address Register (DMAR):** Contains the address of a location of main memory from where information has to be fetched or information has to be stored.

**Data Memory Data Register (DMDR):** Contains a word of data to be written to memory or the word most recently read.

**AX** and **BX** are some temporary buffering registers at the boundary of ALU. These registers serve as input registers to the ALU and exchange data with MDR. In the digital front end, the analog signals are converted into digital values. The amplified analog signals that have been received from the pre amplifier stage are passed through a ADC that has been used for parallel interfacing with Spartan FPGA. The ADC will then take the analog input values and provide the binary equivalent decimal values to FPGA. The digital binary values will be processed from FPGA to the input of Digital to Analog Converter and processed through a speaker in an audio amplifier.

### III.1: MAIN COMPONENTS REQUIRED:

The major components required in the architecture are:

1. Registers (Instruction Register, temporary

- register, data memory register, program address register)
2. Multiplexers
  3. ALU
  4. Register File
  5. Memory (Program memory and Data memory)

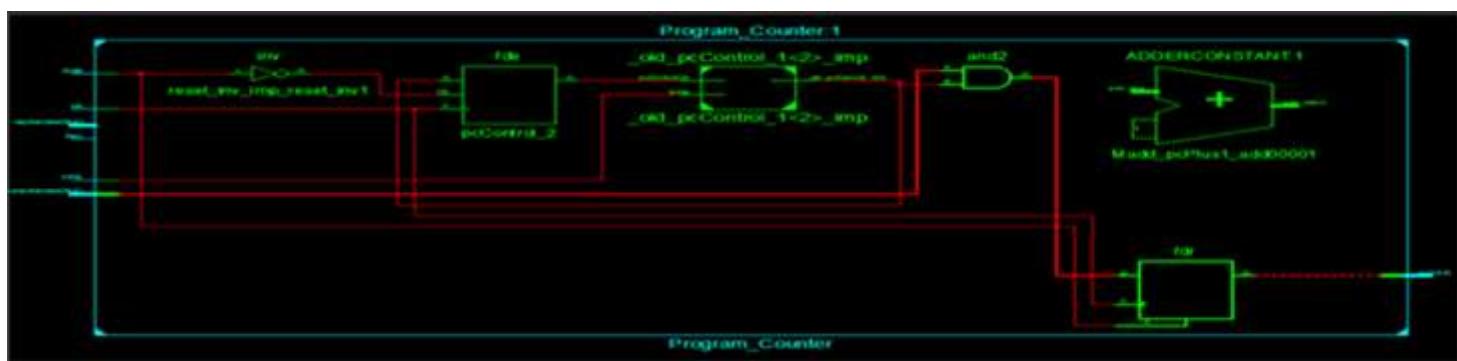
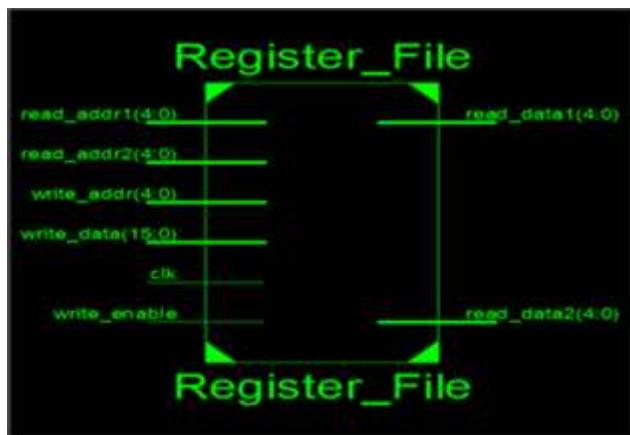
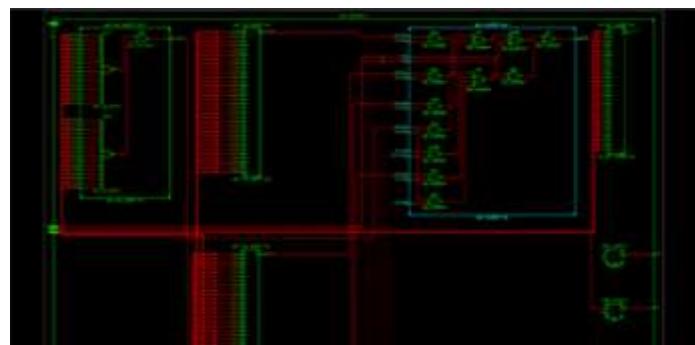
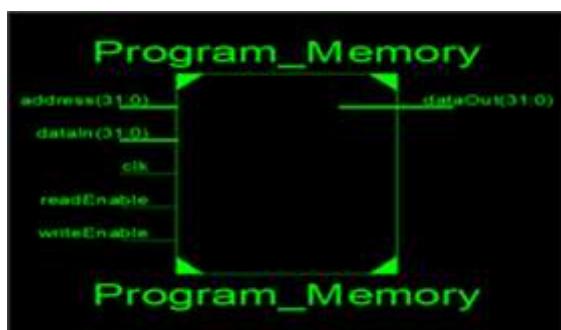
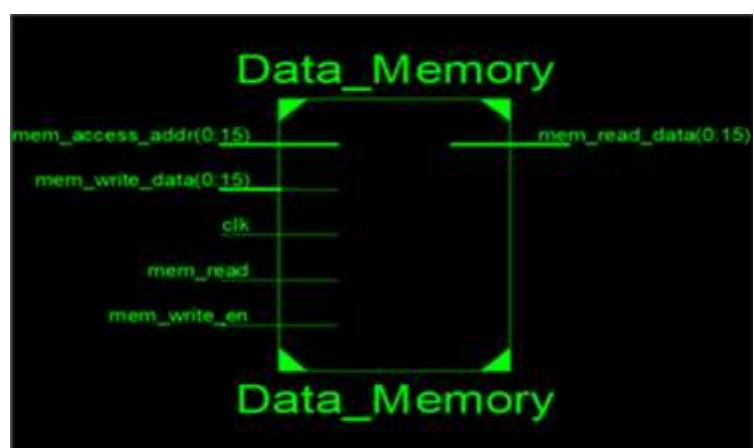
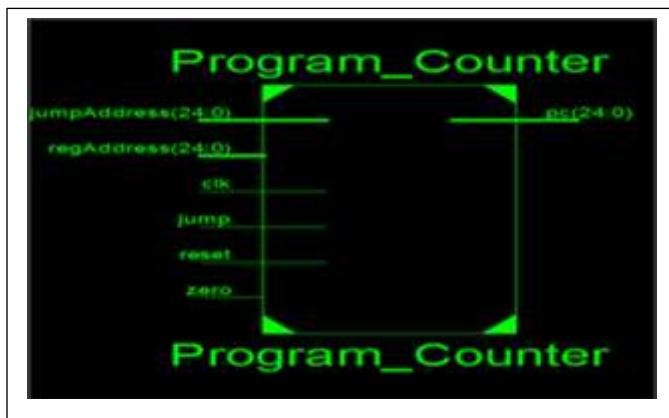
#### IV. MICRO-OPERATION TABLE:

The micro operation table of each instruction for direct addressing mode is shown. Similarly, micro-operation table for remaining addressing mode for each instruction can be performed.

#### V. SIMULATION RESULTS AND ANALYSIS:

S/N	Name of Instruction	T States	Microoperation	Control Signals															
				E (PC)	CH (PC)	E (PMAR)	CH (PMAR)	E (R)	CH (R)	E (AX)	CH (AX)	CH (Y)	RD (mem)	E (Acc)	CH (Acc)	CH (mem)	E (D)	CH (D)	
	FETCH (Common to all)	T1	PC → (PMAR)	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
		T2	PC ← (PC+1)	0	0	0	1	1	0	0	0	0	1	0	0	1	0	0	0
	Decode (Common to all)	T3	IR -> Instruction Decoder	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
Direct Addressing Mode																			
1	LW (Load Word)	T4	IR → PMAR	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1
		T5	PMAR → Addressline	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
		T6	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T7	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T8	GO TO T1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	SW (Store Word)	T4	IR → PMAR	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0
		T5	Acc → DATOWAR	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
		T6	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T7	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T8	GO TO T1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	LD4 (Load Data into Acc)	T4	IR → PMAR	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
		T5	PMAR → Addressline	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
		T6	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T7	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T8	GO TO T1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4		T4	IR → PMAR	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0
		T5	Acc → DATOWAR	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
		T6	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T7	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	STB	T4	IR → [AX]	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
		T5	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T6	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T7	Enable C: Acc ← Acc + [AX]	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0
		T8	GO TO T1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	MUL	T4	IR → [AX]	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
		T5	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T6	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T7	Enable C: Acc ← Acc * [AX]	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0
		T8	GO TO T1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	REM	T4	IR → [AX]	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
		T5	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T6	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T7	Enable C: Acc ← Acc % [AX]	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0
		T8	GO TO T1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	AND	T4	IR → [AX]	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
		T5	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T6	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T7	Enable C: Acc ← Acc (AND) [AX]	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0
		T8	GO TO T1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	OR	T4	IR → [AX]	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
		T5	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T6	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T7	Enable C: Acc ← Acc (OR) [AX]	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0
		T8	GO TO T1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	NOT	T4	IR → [AX]	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
		T5	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T6	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		T7	Enable C: Acc ← Acc (NOT) [AX]	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0
		T8	GO TO T1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The following results are extracted using Verilog programming in XILINX 1SE 14.7 Spartan 3E FPGA specifications.



## VI. CONCLUSION

Thus, in this paper, we have discussed about the design and implementation of 32 – bit modified RISC Architecture. With RISC Processor, the number of instructions in the instruction set gets reduced compared to other processors. Thus, it can be concluded that the architecture is based on Harvard Architecture model since it consists of separate program memory and data memory and it follows the pipelining process. Using the architecture, the operation of all the instructions can be executed. The microoperation table has been designed for every instruction such that each instruction will take the same clock cycle. The Boolean expression has also been derived from the microoperation table for each control signal. For pipelined all the stages like Fetch, decode, operand fetch, execute and write back will work concurrently. Each stage will be working independently. The maximum number of clocks required is 8 for each cycle. All the instructions will be passing through clocks. This is for proper synchronization so that each stage will have same no of clocks. This modified RISC architecture has been implemented and verified on Spartan XILINX 14.7 software tool. Thus, the module functionality and performance issues like area, power dissipation and propagation delay has been analysed using Spartan XILINX14.7 software tool. The RTL Schematic, technology schematic, simulation results of each module have been extracted from Xilinx ISE 14.7.

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# Design & Control of DC-DC Forward Converter

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**Abstract:** The objective of the reported project is to design and control of an isolated DC-DC forward converter. The output voltage of the forward converter is controlled by PWM controller. The control method is chosen in such a way to maintain the output voltage from the converter in voltage control mode.

## I. INTRODUCTION

Now-a-days power electronics is a vast area of modern technology. It is the technology that deals with the conversion and control of electrical power with high efficiency switching mode electronic devices. Among all the devices, converters are the mostly used power device found in many consumer electronic products e.g. battery chargers, personal computers, television set etc.

This project deals with the design and control of an isolated DC-DC forward converter & implementation of voltage mode control for generating isolated and controlled dc voltage from the unregulated dc input supply.

The forward converter is an isolated DC-DC converter that uses a transformer to increase or decrease the output voltage and provide galvanic isolation for the load. With multiple output winding it is possible to provide both higher and lower output voltage simultaneously. The forward converter, when compared with the fly-back circuit, is generally more energy efficient and is used for applications which involve slightly high power output (within 100 – 200 watts).

There are two topologies of forward converter. One is single switch forward converter and the other one is double switch forward converter.

1. The drawback of the single switch approach is that the voltage stress on the switch is the sum of the input voltage, reflected transformer voltage and turn-off voltage spike caused by leakage inductance.

2. Adding a second MOSFET switch on the high end side leads to the double-switch forward or Flyback topology of which the voltage stress on each MOSFET is clamped to the input voltage. The leakage inductance energy is also clamped and recycled back to the input to improve efficiency.

Forward converters are used in many applications such as in solar power system, personal computer, battery chargers and also for generating isolated and controlled dc voltage from the unregulated dc input supply.

## II. TOPOLOGY OF FORWARD CONVERTER

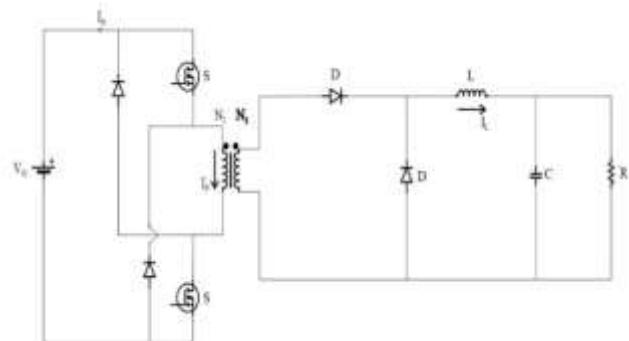
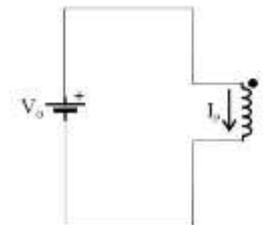


Fig 1. Circuit Diagram of Forward Converter

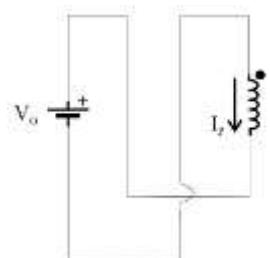
### Mode 1:

*When both the switches are on or two primary side switches are on.*



### Mode 2:

*When both the switches are off or two primary side switches are off.*



### III. MATLAB SIMULATION

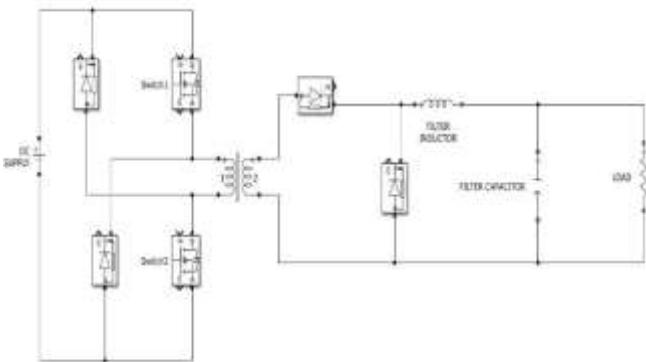


Fig 2. MATLAB Simulation Diagram

### IV. CONTROLLER DESIGN

Suppose a device has to be used with low voltage level and if devices such as laptop or charger are directly connected to the rectifier supplied from the socket at home, the device might not function properly or it might be broken due to over current or overvoltage. Therefore, to avoid unnecessary damage to the equipment's and devices, the voltage level has to be converted to voltage level suitable for the equipment's to function properly.

#### A. PWM Controller

The switch control signal (PWM), controls the state (on or off) of the switch. This control circuit regulates the output voltage against changes in the load and the input voltage. PWM is the method of choice to control modern power electronic circuits. The basic idea is to control the duty cycle of a switch such that a load can see a controllable average voltage.

#### B. Comparator and Voltage to PWM Converter

Switching power supply relies on negative feedback to maintain the output voltages at their specified value. To accomplish this, a differential amplifier is used to sense the difference between an ideal voltage (the reference voltage) and the actual output voltage to establish a small error signal ( $V_{control}$ ).

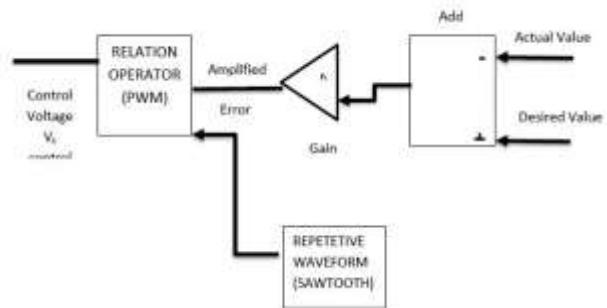


Fig 3. Controller Design

### V. OUTPUT

#### A. Simulation Output without Control

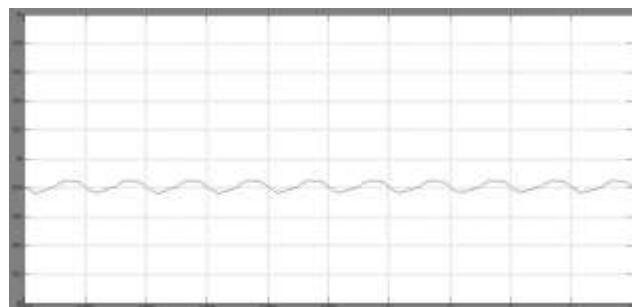


Fig 4. Output Voltage without Control

#### B. Simulation Output with Control

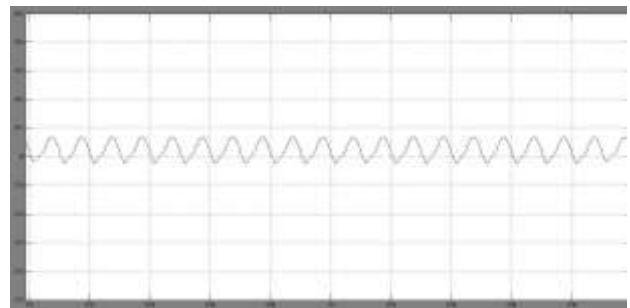
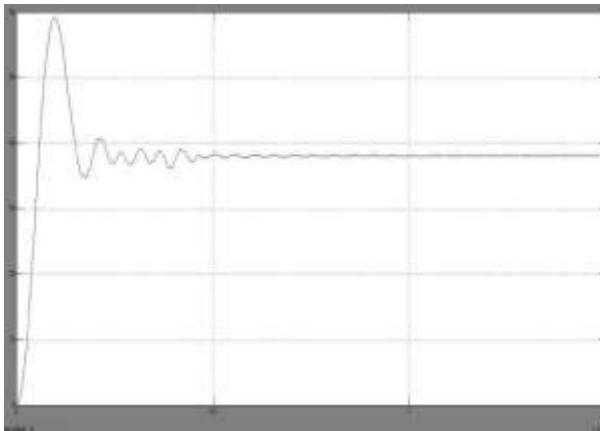


Fig 5. Output voltage with control

#### C. Output Voltage Waveform Including Transient Period



*Fig 6. Transient response of output voltage*

## VI. CONCLUSIONS

In this project firstly the buck converter has been taken care of and analyzed in detail which is subsequently followed by implementation and investigation of forward converter with proper analysis. However its output is not constant for unregulated supply. Thus finally the forward converter is being controlled with PWM controller. Henceforth for a stable input voltage the output voltage becomes stable.

Essentially, when the two switches are ON the input voltage is applied across the transformer and identical voltage is obtained across the secondary one since the transformation ratio here is 1:1. Basically, in our converter without controller circuit the output voltage will change according to the input voltage. Therefore, to obtain constant supply converter with control circuit has to be implemented.

## ACKNOWLEDGEMENT

The implementation of this project has been one of the significant academic challenges we have faced so far and without the support, patience and guidance of the respected faculties and fellow colleagues, this task would not have been accomplished. We hereby take this opportunity to appraise a special note of thanks to **Prof. Debolina Pradhan** for her cherished supervision and also to my colleague **Mr. Souptik Chakraborty**.

Also, I want to express my gratitude to our respected HOD Sir **Prof. Amitabha Sinha** and my respected supervisor **Dr. Madhumita DasSarkar** for giving me this opportunity to represent my project work in the form of a magazine article.

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# Development and Performance Enhancement of a Photovoltaic (PV) System for critical Electronic Load

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**Abstract:** Demands of Global Energy is rising faster than that of population; almost the demand continues round's O clock. The limited fossil fuel is an alarming sign for Energy sector. There are some alternative resources of energy already existing; however, Solar PV technology is most attractive & potential technology now-a-days over those resources. There are huge losses in conversion of AC to DC and vice versa, nonetheless, major loads are DC in nature now-a-days. If we harvest DC source of energy and supply it to dc load there will be hardly any conversion losses. Thus proposed work has been designed here with the help of MATLAB Simulink Simscape environment and Pvsys applications based on fundamental equations and newly designed Simulink circuit. The newly developed system will be useful to calculate the efficiency, P-V and I-V nature under several parameter variations considering the temperature, irradiance, series and shunt resistances. The simulation outcome will be convenient and helpful for the designers to simply design their hardware module.

## I. INTRODUCTION

Today's modern world is energy hungry. The harmful effects of pollutant discharged as a result of fossil-based power generation and strict environmental laws are foremost factors that lead to rapid growth in using renewable energy resources as alternatives to electricity production. Solar cell is a leading and promising renewable technology. A solar PV module is the series connection of various solar cells. The lumped parameter is used to simulate the different behaviors of solar cell in different conditions. Here in this work double diode model has been considered. A comparative study of three different estimation methods for extracting solar cell model parameters is provided in result section.

When a number of photovoltaic cells are linked in series or parallel mode it uses to form a solar module. The basic building block of a PV cell is a p-n junction semiconductor diode which transforms the sunlight directly into electricity. The PV system is extremely modular and can be connected together to supply power from few watts to few megawatts.

Due to several internal physical conversion processes within the solar cell the efficiency is not

very effective. So, the modelling mechanism should be taken care of with utmost priority when someone goes to build the PV module. In this regard modelling and analysis of a solar cell should be properly accomplished with top class accuracy to optimize the design mechanism.

For designing an efficient system we have taken care of the internal as well as external parameters like irradiance, temperature, humidity, wind speed, shading. For modelling and analyzing the electrical characteristics of a solar cell and that of a PV system as well, MATLAB and Pvsys tools are mainly utilized because it helps in forecasting the characteristics of a PV cell and system under several environmental aspects without giving a serious mismatch in terms of output.

Therefore, it helps in generating the P-V and I-V curves smoothly. The general procedure to realize the electrical equivalent circuit of a PV cell can be modeled with a photo-generated current source followed by a diode in parallel for realizing the P-V and I-V attributes.

Photovoltaics are already an established concern in many countries like INDIA. The dynamic factor is load. Several works has been accomplished in PV system without being bothered about the load type. It can be of different types such as electronic load, transient load etc. Since PV source contributes output energy only in day time, therefore, if irradiance is available beyond the threshold value it can be easily deliverable to load.

## II. DIFFERENT TYPES OF DC LOAD

There are several kinds of DC loads of photo-voltaic system. Those are as follows:

- i) LED, ii) Transistor, iii) Amplifier, iv) Router, v) Mobile, vi) Function generator and vii) BLDC Motor

## III. TYPES OF PV SYSTEM

### A. Standalone System

Usually Standalone PV system consists of PV arrays, charge controller, batteries and if required micro-inverter. There is no grid connection availability mostly in the standalone system. It becomes quite a bit costly if it involves a larger number of batteries.

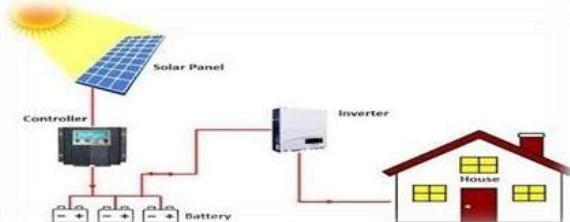


Fig 1. Standalone -PV system

### B. Grid Tied system

In Grid tied system there is no prerequisite of battery which saves the overall system cost. But there is a drawback. If grid power is not available the system doesn't provide output power and the generated power from PV modules becomes wasted.

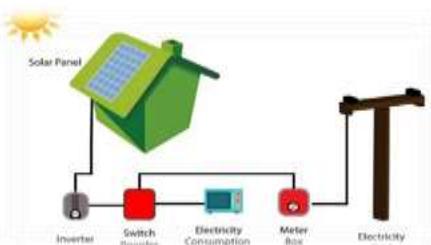


Fig 2. Grid Tied System

### C. Hybrid System

In Hybrid system batteries as well as grid power both are available. It is most suitable where frequent power outage occurs. Here the battery and the PV source provide the power when grid is not available.



Fig 3. Hybrid System

## III. IRRADIATION DATA

In INDIA the solar irradiance is not same in every part of the county. Some region consists of high values of irradiance while other part is getting much lower irradiance. Solar irradiation is usually

measured in watt per meter square.

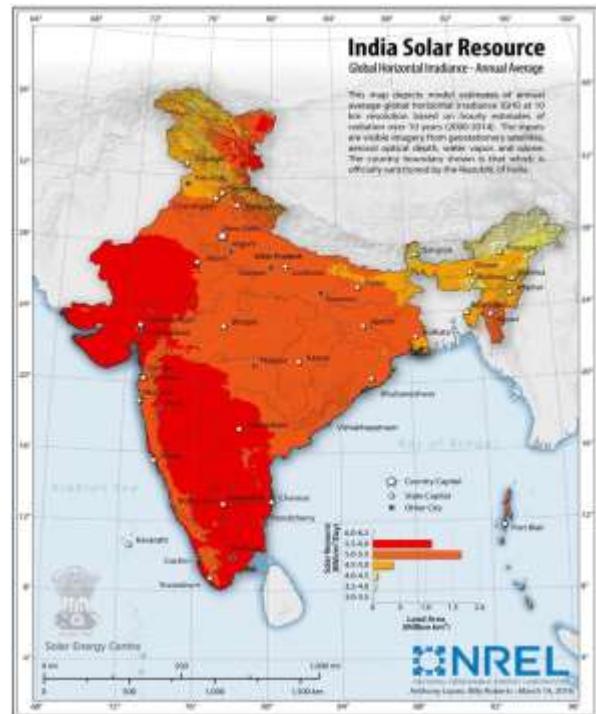


Fig 4. Solar Irradiance data INDIA Source NREL

Table 1. Irradiance data of different INDIAN cities [6]

City	Annual average solar radiation	Monthly average solar radiation over six Indian cities in (kWh/Sq. m/Day)											
		JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
Ahmedabad	6.14	6.41	7.01	7.32	7.09	6.66	5.72	4.26	4.56	5.77	6.90	6.14	5.87
Bhopal	6.05	5.94	7.08	7.07	7.10	6.65	5.53	4.01	3.73	5.74	6.77	6.37	6.23
Chennai	5.80	6.09	6.76	7.20	6.82	6.10	5.59	5.30	5.46	5.74	5.40	4.65	5.42
Delhi	5.46	4.14	5.45	6.55	6.80	6.12	5.49	5.12	4.85	5.74	5.81	5.10	4.31
Kolkata	5.19	4.87	5.78	6.40	6.22	5.54	4.42	4.30	4.29	4.82	5.14	5.61	4.10
Mumbai	5.95	6.51	7.06	7.21	7.11	6.67	4.50	4.10	4.34	5.18	6.00	6.48	6.25

Ref 6: N. M. Kumar, and R. K. Reddy, "Optimal energy performance and comparison of open rack and roof mount mono c-Si photovoltaic Systems", June 2017, Energy Procedia

## IV. EXPERIMENTAL RESULTS

### A. PV Circuit Model

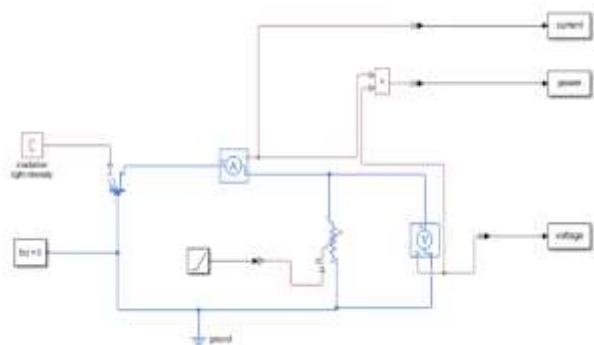
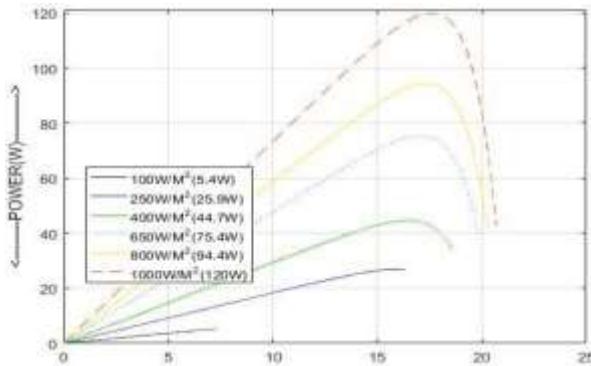


Fig 5. Photo-Voltaic Circuit Model

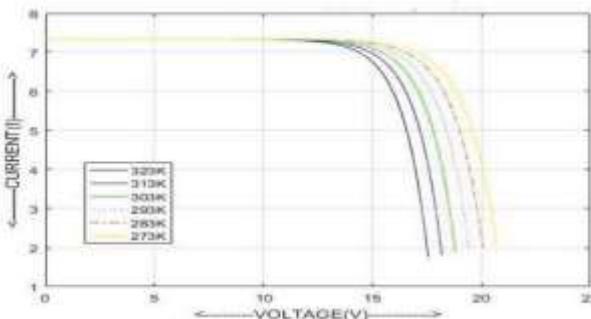
### B. Effect of irradiance on I-V and P-V curve

From Fig. 6 it can be perceived that as irradiance increases the current is increasing and henceforth, more power is delivered from the PV cell. As a consequence, power and current are also increasing when the solar cell is exposed into sunlight with more irradiance.



*Fig. 6. P-V curve of the PV cell beneath the variation of irradiance*

### C. Impact of Temperature on I-V and P-V curve



*Fig. 7. Nature of the PV cell under various conditions of temperature*

The influence of the room temperature on the current and output power is depicted in Fig. 7. Due to the increasing order of short circuit current  $I_{SC}$  and decreasing nature of open circuit voltage  $V_{OC}$  the overall current and power is dropping down after a certain voltage level.

In this report we have anticipated daily household average energy consumption as 4.9 kWh/day. Taking Sessional data for calculation, loads in different session as well as different loads are required.

## D. Different Load and Usage

Table 2. For SUMMER March-May

	Number	Power	Use	Energy
Lamps (LED or fluo)	1	60 W/lamp	6 h/day	360 Wh/day
TV	1	65 W/app	8 h/day	520 Wh/day
Computer	1	120 W/app	8 h/day	960 Wh/day
Fan	1		15 Wh/day	150 Wh/day
Router	1		24 Wh/day	1920 Wh/day
Laptop	1	30 W tot	10 h/day	285 Wh/day
Inverter+Charger	1	120 W tot	4 h/day	480 Wh/day
Stand-by consumers			24 h/day, 7days/7	240 Wh/day
Total daily energy				4915 Wh/day

Table 3. For WINTER Dec-Feb

	Number	Power	Use	Energy
Lamps (LED or fluo)	1	60 W/lamp	6 h/day	360 Wh/day
TV	1	65 W/app	8 h/day	520 Wh/day
Computer	1	120 W/app	8 h/day	960 Wh/day
Router	1		24 Wh/day	1920 Wh/day
Laptop	1	30 W tot	10 h/day	285 Wh/day
Inverter+Charger	1	120 W tot	4 h/day	480 Wh/day
Stand-by consumers			24 h/day, 7days/7	240 Wh/day
Total daily energy				4765 Wh/day

All loads are taken as DC load. LED, TV, computer, fan (BLDC), router, laptop, micro-inverter and charger. According to the session our energy requirement varies. Hourly load distribution is taken into care for this report.

## E. Hourly Load Distribution profile

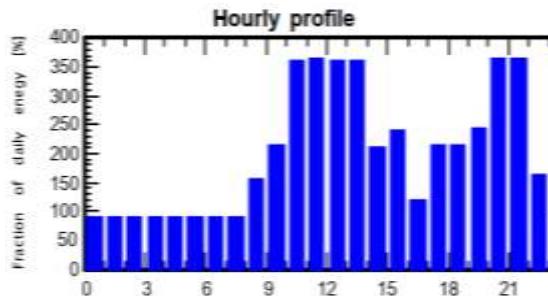


Fig 8. Hourly load distribution having Energy vs time

## F. Available Energy to Load

- Available Energy 2116 kWh/year.
- Used Energy 1720 kWh/year Excess (unused) 347 kWh/year
- Solar Fraction SF 95.70 %.
- Loss of Load Time Fraction 4.6 %.
- Missing Energy 77 kWh/year.

## G. Normalized Production & Performance Ratio

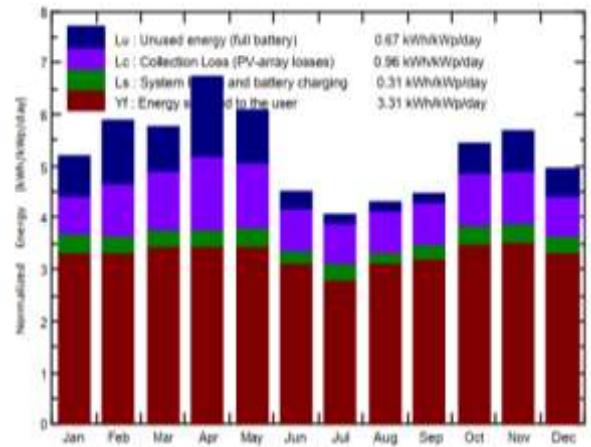


Fig 9. Normalized production with Energy vs Time (month)

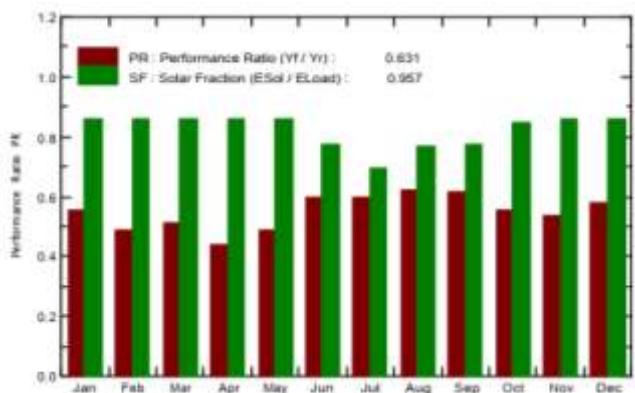
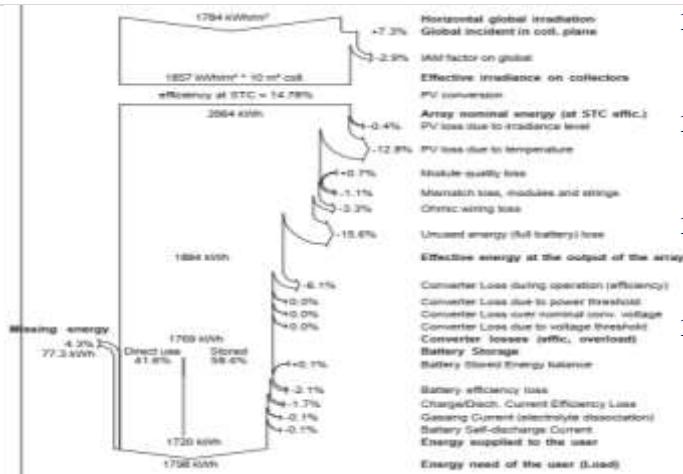


Fig 10. Performance ratio & Solar Fraction

	GLOBAL kWh/m <sup>2</sup>	SUMMER kWh/m <sup>2</sup>	E Avail kWh	Estimated kWh	E Miss kWh	E User kWh	E Load kWh	SF[%]
January	138.3	136.1	180.8	33.28	0.00	147.7	147.7	1000
February	139.3	136.0	184.3	47.67	0.00	123.8	133.4	1000
March	164.5	173.5	194.8	37.91	0.00	132.4	152.4	1000
April	205.0	196.8	216.8	68.42	0.00	147.5	147.5	1000
May	183.7	183.1	203.0	45.21	0.00	132.8	152.4	1000
June	145.4	136.1	147.7	12.62	14.94	113.0	148.8	8.89
July	133.7	121.2	188.4	7.67	29.12	124.8	163.6	8.81
August	136.7	128.8	146.5	7.76	10.77	137.8	163.0	8.89
September	129.5	129.1	146.8	9.62	15.39	136.8	151.8	8.89
October	148.8	163.6	185.3	25.75	2.04	135.0	137.8	3.98
November	136.5	165.1	180.0	33.34	0.00	131.9	131.9	1000
December	129.9	149.1	176.7	24.59	0.00	147.7	147.7	1000
Year	1780.7	1667.3	2116.8	346.99	77.26	1720.1	1787.6	8.957

Legend: Global: Horizontal global irradiation  
GHI: Effective global insolation for GHI and skydome  
E\_Avail: Available Solar Energy  
Estimated: Unused energy (kWh battery) loss  
E\_Miss: Missing energy  
E\_User: Energy supplied to the user  
E\_Load: Energy need of the user (Load)  
SF[%]: Solar fraction (EUser / ELoad)

Fig 11. Balance & Main Results



**Fig 12. Losses in a year**

## V. CONCLUSION

By performing this work exact PV system sizing and losses have been determined precisely under the considerations of different types of critical electronic loads and the system which transfer maximum power for the maximum time.

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# Acoustic Noise & Echo Cancellation Systems

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**Abstract:** An improved and effective design of acoustic echo canceller has been proposed for the advancement in telecommunication which is capable of providing convincing results. In this echo cancellation algorithm an adaptive filter has been considered which uses a fast convolution technique to compute output signal and filter updates. This computation can be executed quickly in MATLAB through frequency-bin step size normalization to obtain better performance .There are different techniques already used for signal processing but proposed design provides advanced features for better quality signal.

## I. INTRODUCTION

The advent of telephony echoes has been a problem in communication networks. The most important factor in echoes is end-to-end delay which is also known as latency. It is the time between generation of the sound at transmitter end and its reception at the receiver end. Echo is a reflected copy of the voice heard sometimes later and delayed version of original sound or electrical signal.

## II. NEEDS OF THE SYSTEMS

Echo and noise related problems are very common in many applications involving speech communications e.g. audio conference and hands-free telephony. In these systems, the speech that comes from the far-end speaker and echoes back with a time delay produces perception problems. In such condition, the perception is further impaired when the speaker is situated in a noisy environment.

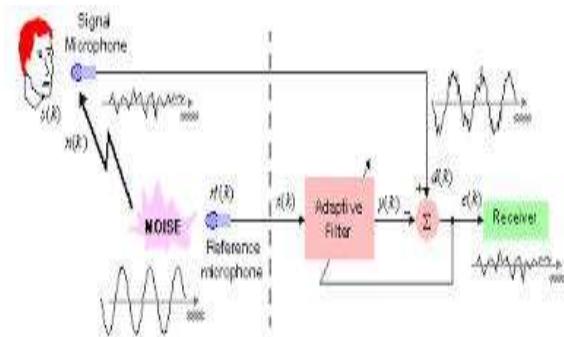
In order to provide a better communication service, an acoustic echo canceller (AEC) is required to cancel the echo returned to the transmitter end and also allow uninterrupted communication between both the ends. A class of promising state of the art techniques exists in which adaptive techniques of several one or two microphones have been proposed to resolve this critical issue of acoustic echo.

Also when microphones and speakers are placed

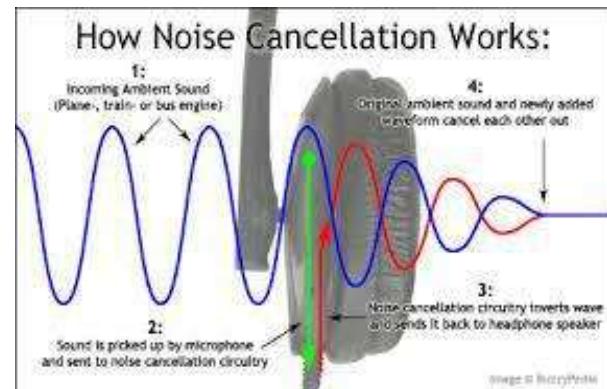
close to each other in that situation dual techniques are used to improve the quality of communication essentially where two acoustical disturbances i.e. echo and noise are present simultaneously. Those two techniques are:

**1) Acoustic Echo Canceller (AEC) for Echo Cancellation**

**2) Active Noise Control (ANC) for removing the Noise**



**Fig 1. Diagram for Echo Cancellation**



**Fig 2. Diagram for Noise Cancellation**

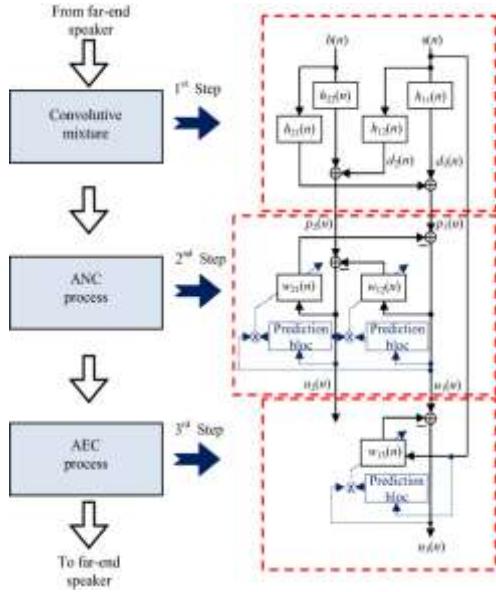
Along with those techniques algorithm like short time Fourier Transform (STFT) and adaptive filter can be used to achieve the resolution.

## III. BACKGROUND OF THE ECHOES

As we all know, velocity of sound is approximately 343 m/s at room temperature,

therefore,

- 1) If any reflected object is situated at 11.3 m far from the sound source yields echo.
- 2) If the delay is more than 32.94m/s then also echo can be generated.
- 3) An echo can be produced when sensitive microphones and speaker volume is turned up to high level.



**Fig 3. Cascade structure of echo cancellation**

#### IV. HOW TO CANCEL AN ECHO

The proposed algorithm for cancelling noise and acoustic echo signal is based on two cascade stages. In ANC phase, BBSS stage is used to cancel noise followed by ACE system which is used to suppress echo signal. Both the stages use efficient SFTF algorithm to take the advantage of adaptive behavior of this algorithm when combined with proposed cascaded system.

#### V. ALGORITHMS FOR ECHO CANCELLATION

In this analysis, we consider two algorithms to update filter coefficients of the proposed system. First one is two channel SFTF which is used to block ANC block and another one is single channel SFTF algorithm which is used to block AEC block . Two channel SFTF algorithm output is,

$$W_{21}(n+1) = W_{21}(n) - u(n) y_1(n) k_1(n)$$

$$W_{12}(n+1) = W_{12}(n) - u_2(n) y_2(n) k_2(n)$$

And prediction error can be estimated as

$$E_1(n) = u_2(n) - a_1(n)u_2(n-1)$$

Forward prediction co-efficients are,

$$a_1(n) = p[a_1(n-1) - E_1(n) y_1(n) k_1(n-1)]$$

$$a_2(n) = p[a_2(n-1) - E_2(n)y_2(n)k_2(n-1)]$$

Calculated like hood variable is,

$$y_1(n) = \frac{1}{1-k_2^T(n)}u_1(n)$$

$$y_2(n) = \frac{1}{1-k_2^T(n)}u_1(n)$$

Output of Single channel SFTF algorithm is,

$$W_{13}(n+1) = W_{13}(n) - u_3(n)y_3(n)k_3(n)$$

And Estimated Error is,

$$E_1(n) = s(n) - a_1(n)s(n-1)$$

$$E_2(n) = u_1(n) - a_1(n)u_1(n-1)$$

#### VI. CONCLUSION

With the world shrinking into a global village because of superior communications, telephones, both conventional and hands free sets, occupy a prominent position in solving people's communication needs. One of major problems in a telecommunication application over a telephone system is echo. The echo cancellation algorithm has been presented in this paper successfully. The entire investigation consists of complete software approach rather than utilizing any DSP hardware components .The algorithm is capable of being executed with MATLAB software.

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# Designing a 16-Bit RISC Processor

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**Abstract:** Design of 16 bit Reduced Instruction Set Computer (RISC) is a methodology which supports lesser and simpler set of instructions that requires the same amount of time to execute. A design of 16-bit RISC processor is presented in this paper using the Verilog HDL. The processor comprises of the various functional blocks such as the Control Unit, Data Memory, Instruction Decoder, Instruction Register Unit and Arithmetic and Logical Unit (ALU) which can be designed using the ISE Xillinx 14.7 Tool. The proposed processor here has been carried out with the help of Harvard Architecture i.e. having separate memory for instruction and data. The processor support four addressing mode. It has ALU which is capable of arithmetic and logical operation and also incorporates with a flag register which indicates carry, zero and parity status of the result.

## I. INTRODUCTION

In today's world the trend of using RISC processor is clearly increasing compare to that of earlier CISC processor. The motives have been the advantages of RISC processor, such as its simple, flexible and fixed instruction format, hardware controlled logic, higher clock speed, elimination of the necessity for micro programming. Moreover, the benefits of high speed, low power, area efficient and operation-specific design possibilities have made the RISC processor universal. The leading feature of the RISC processor is its ability to support single cycle operation i.e. the instruction is fetched from the instruction memory at a maximum speed. RISC processors, in general, are designed to achieve this objective by method of pipelining where there is a possibility of stalling of clock cycles due to wrong instruction fetch when "jump" instructions are encountered. Thus it reduces the efficiency of the processors.

## II. WHY SHOULD WE USE RISC?

Various attempts have been made to increase the instruction execution rates by overlapping the executions of more than one instruction since the very beginning of computer brainchild. The most common ways of overlapping are pre-fetching, pipelining and superscalar operation.

### A. Pre-fetching

The process of fetching next instruction/instructions into an event queue before the execution of current instruction is completed is called pre-fetching.

### B. Pipelining

Pipelining instructions signifies starting or issuing an instruction prior to the completion of the currently executing instruction.

### C. Superscalar operation

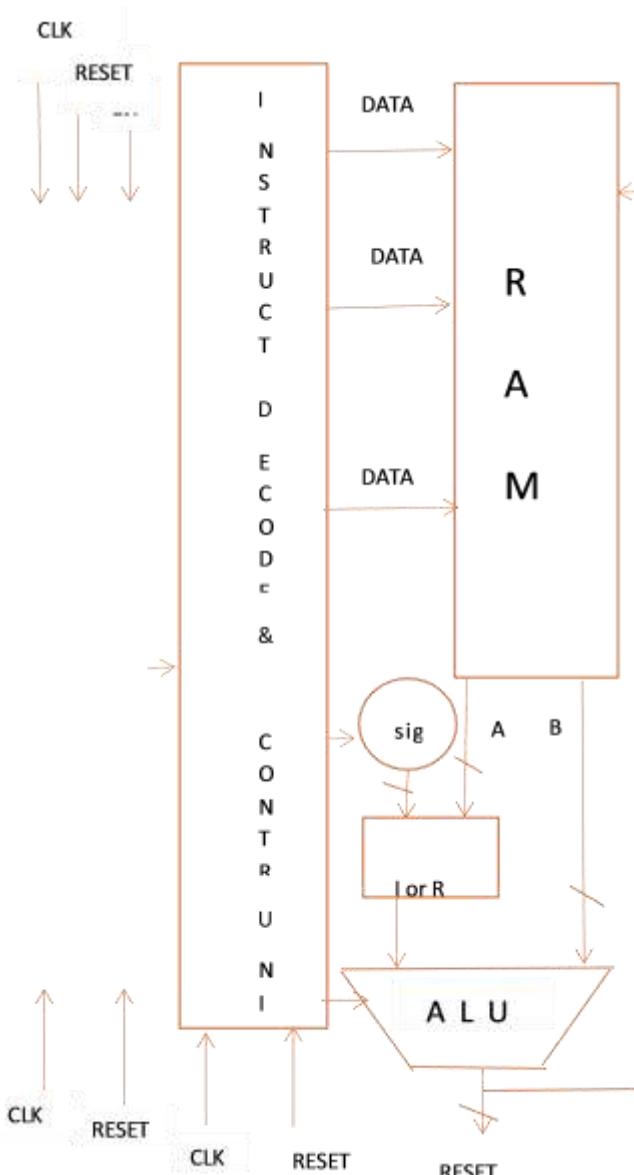
Superscalar operation refers to a processor that can issue more than one instruction simultaneously.

## III. DETAIL OF BLOCKS

The block diagram of the 16-bit RISC CPU is shown in fig 1. The proposed 16-bit RISC processor consists of five blocks namely Arithmetic and Logical Unit (ALU), Program Counter (PC), Register file (REG), Instruction Decoder Unit (IDU) and Clock Control Unit (CCU)

### A. Program Counter

Program Counter (PC) is a 16-bit latch that holds the memory address of location from which the next instruction will be fetched by the processor. It controls the flow of instruction executions and ensures the logical operation flow of the processor. It basically performs two operations: (i) first operation is increment and (ii) second operation is loading.



**Fig 1. RISC Block Diagram**

### B. Arithmetic & Logic Unit (ALU)

Arithmetic and logic unit (ALU) performs arithmetic and logic operations. It also performs the bit operations such as rotate and shift by a defined number of bit positions. The ALU contains two blocks: (i) Arithmetic block and (ii) logic block. The arithmetic unit involves the execution of addition, subtraction, multiplication and division operations and generates Sign flag and Zero flag as per the result of the process. In order to reduce the complexity of the adder circuits used in the arithmetic unit of the RISC CPU a very fast and low power carry select adder circuit is usually introduced.

### C. Instruction Decoder Unit

The instruction decoder is used to decode the opcode part of the instruction and helps to generate the control signals. The instruction set of this decoder unit is essentially comprehensive. To execute the instruction, the processor copies the instruction code from the program memory into the instruction register. It can then be decoded by instruction decoder which is a combinatorial logic block.

### D. Control Unit

It provides the timing and control signals. All computer resources are controlled by the Control Unit. It directs the flow of data between different functional units of CPU like ALU, Register File, Instruction Register, Program Counter etc. Crystal oscillators are typically used to generate the Clock frequency. Besides, instructions are fetched, decoded and executed at the positive edge or negative edge of the clock.

### E. Register File

The register file consists of number of general purpose registers (8, 16 or 32) of 16-bits capacity each. These register files are utilized during the execution of ALU and data transfer instructions. It can be addressed as both source and destination register using a n-bit identifier which is also known as register select where no. of registers are  $2^n$ . The load instruction is used to load the values into the registers and store instruction is used to retrieve the values back to the memory.

## IV. CONCLUSION

The 16 bit RISC processor should be designed in such a way so that it can work using minimum functional units. The proposed design is mainly based on Harvard architecture. The design entry and synthesis can be accomplished by using Xilinx ISE or Vivado. The simulation output should be compared with the anticipated result and functionality can be further tested. Data path can also be designed using Xilinx ISE tool. The design can be further improved in number of ways. To realize more sophisticated design additional features can be added to the current design. The number of

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instructions that the processor supports can be increased.

#### **ACKNOWLEDGMENT**

I would like to express my cordial gratitude to Prof. Amitabha Sinha, Director (Academic Reforms) and Head of the Department (Microelectronics and VLSI Technology), Maulana Abul Kalam Azad University of Technology (MAKAUT). Further I would like to convey my vote of thanks to our project Supervisor Mr. Sowvik Dey for his proficient guidance and support in my Project work.

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# Scope Creep in Project Management

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**M. Tech 2020-2022**

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**Abstract:** The Scope creep in project management refers to changes, continuous or uncontrolled growth in a project's scope at any point after the initiation of the project. This can occur when the scope of a project is not properly defined, documented, or controlled. It is generally considered quite harmful.

## I. INTRODUCTION

This scope creep (sometimes called feature creep in product management) refers to a tendency for the requirements and deliverables of a project to slowly expand or to become distracted over time.

A project's scope will often broaden over its lifecycle as requests from customers and stakeholders come in for new features and functionality. This is a natural as well as essential part of any product development process; however, issues arise whenever the teams get side-tracked on the wrong things.

Customer requirements for the product can also change after the setting of initial requirements. Therefore, effective product management requires a high degree of flexibility. Any changes made must align with the overarching product vision – otherwise, there could be team's risks in wasting resources and crafting poor quality products by focusing on the wrong things.

Consequently, Scope creep can be a outcome of:

- (i) poor change control
- (ii) Lack of proper initial identification which leads to project objectives
- (iii) Weak project manager or executive sponsor
- (iv) Poor communication between parties
- (v) Lack of initial product versatility

## II. WHY DOES SCOPE CREEP HAPPEN?

Scope creep can emerge in different ways, but most typically it occurs when teams start adding supplementary functionalities or features that haven't been properly highlighted in the roadmap.

While the roots of scope creep are typically found in external factors, it sometimes occurs as the outcome of lack of consensus within teams, internal miscommunication or weaknesses in product or (or project) management.

## III. HOW TO MANAGE SCOPE CREEP

To stay on top of scope creep, it's vital to have clearly prioritized product roadmap in place of the documents which demonstrates tuning according to project requirements and displays their impact on priorities or timelines.

An effective product roadmap can also be the basis of a modified control process, which includes:

- (i) Monitoring a product's current status
- (ii) Understanding the original scope of a project and its core objective
- (iii) Apprehending authentic progress & thereafter comparing it to the core objective to identify how much the current project has deviated from the original plan
- (iv) Specifying the bases of changes in requirements and defining how much product development has altered as a result
- (v) Evaluating transformation requests to recommend actions or decide if they should be challenged

(vi) Ensuring all changes should be processed, documented, and broken down into actionable tasks.

While talking about realistic project scope, the role of project scope creep that may lead to failure must have to be studied. That is why a research study where different issues were discussed responsible for project failure usually is considered as a primary source of evidence. On the other hand, the documented papers demonstrate the gap or distinction between project success and failure. Besides, the performance has been estimated based on issues already defined. Similar research was performed to enlist major project failure causes. These causes were then analyzed with comprehensive research on literature and therefore, the degree of complexity related to periodicity, emergence and non-monotonicity had been discussed.

## IV. PROPOSED METHOD

### *A. Make a clearly defined statement of work*

To avoid those long drawn out projects, an adequately defined Statement of Work (SOW) is very much required. SOW should function as a detailed building plan and roadmap of what has to be executed on a project. It should be as specific as possible. A SOW should include the preparations necessary for every role working on each task within the project. Thus the potential risk of the client demanding for one kind of features and the assigned vendor is fabricating something else by realizing some other thing can easily be avoided. Eventually, at the end the product is not anywhere close to what the client has envisioned and demanded in the first place. If the mutually signed SOW can't be referred back, then those corrections could quickly turn out to be much more comprehensive. As a consequence, it could make the project to be run overtime, make the resources to be stretched and push other projects and clients further delayed from their completion dates.

### *B. Assume there will be change*

Project scope is never set in stone. Change happens even before the ink is dry, regardless of how detailed the scope and requirements are. What can be accomplished from the very beginning is to

learn how to embrace the mindset of change and live with it in harmony.

Whenever there's the case of change, requests for change has to be controlled, process is to be managed and a good governance has to be confirmed. Every change should be supported by the evidence of necessity. Therefore, it is to be made sure that the change is of value to the project. Management processes involving scope change have to be set up upfront and you probably already have these in place. But there is no such management process, possible scenarios have to be realized and developed on how to respond to changes. Here are a few critical steps not to miss:

#### **1) Log changes**

Changes should not go unnoticed. Record of every additional requirement to the scope has to be kept in detail. Therefore, it will lead to the benefit of reporting easily to the client and ask for additional resources when necessary.

#### **2) Re-plan**

Keeping baseline up-to-date can assist to communicate progress of project and lack of resources among other things.

#### **3) Request additional funding**

If both the above steps are followed, there will be solid proof for requesting additional funding or resources from the client.

#### **C. Educate the clients**

To prevent scope creep, discovery sessions have to be set up with the clients in the early stages even before the project begins and processes and strategies have to be developed around change requests. Letting the clients in the processes and agreeing what's best for both sides are essential for the success and future collaboration of vendor.

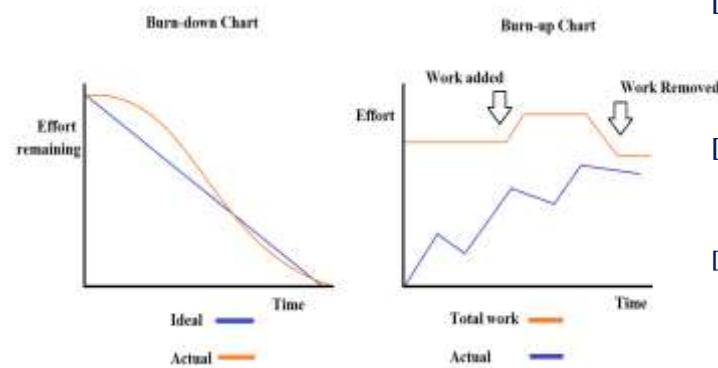
#### **D. Filter simple adjustments from new tasks**

This one is very specific and critical for both avoiding scope creep and not becoming a control freak. Whenever the feedback is received on project deliverables, it has to be made sure to distinguish the input from what is a simple adjustment to the work from an entirely new task. Adjustments can be alright, of course, but new tasks are most often out of the initially defined scope.

The difference is in what the client is asking to alter. An adjustment is a simple change to adapt the experience slightly, i.e., the design of a button in a

mobile app. A new task is if the nature of this button is asked to be changed, i.e. creating an entirely new flow or building a new feature around it.

Suggestions and demand of features can be alright, however, significant modifications lead to an extended agreement. Of course, this is in the case that the feature or change is clearly out of the scope and not just a simple adjustment of the current project. If it is indeed a new task, then it has to be realized something like that that it can be accomplished definitely, however, this is out of the initially agreed scope of the project. Thereafter, time and costs have to be estimated to do that further efficiently. Thus, it is opened to the adjustment as well as can be made sure that project remains profitable.



*Fig 1. Burn-down vs. Burn-up Charts*

## V.CONCLUSIONS

Scope creep is the size of a project in terms of effort, cost, and schedule instigates to grow beyond what was originally expected. There are many causes of scope creep, but, basically it can happen any time when the original estimate of the project goes wrong. Probably the biggest source is to fit a project forcibly which is full of uncertainties with a traditional plan-driven model having fixed cost and schedule estimates instead of recognizing that the project is full of uncertainties and using a more flexible and adaptive model to manage it.

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# Activated Carbon: A Savior in Disguise

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**Abstract:** The concern to raise awareness about the environment has been a subject of interest to many, irrespective of the field. People from all walks of life, with their own form of capabilities, have contributed in a way to preserve the vast greenery amidst those concerns. Even researchers have successfully implemented numerous formulations to keep a check on the efforts of the above-mentioned problem through science and technology. Industries, of how they changed the scenario of human progression, have also ceased the portfolios of saving the environment. In this Article, there will be a discussion about a essential constituent, Activated Carbon, although may not be quite substantial, but has serious impacts on filtering out the impurities released into the environment. Its brief description, composition and how it has affected the latest trends, is also to be discussed.

## I. INTRODUCTION

Human kind has witnessed rapid progress in all fields, and has shown cumulative development in all sectors. Such progress gave us a giant leap to enhance our capabilities but it comes with some consequences. Industrialization along with numerous inventions has somehow been both a boon and a curse. A curse due to its outcomes. Environmental degradation is one of the key outcomes of such progress which not only harms our surroundings but also our individual daily life. As a consequence to resolve those out scientists have developed multiple components and products to prevent such degradations. One such important component is Activated Carbon.

## II. ACTIVATED CARBON: A COMPONENT WITH INFLUENCE

Activated Carbon is a form of carbon that is generally processed in such a way to have pores of low volumes which thereby increases the surface area. Consequently it can adsorb harmful toxins and

impurities in different environment and thus purifies the ambient. It finds its usage in various sectors ranging from healthcare to industries. In Healthcare, it is consumed orally to treat diseases such as indigestion. The Activated carbon adsorbs all the harmful toxins in our intestine without affecting our body. In industries, the harmful gases released can be controlled through its usage. Several Studies demonstrate the activated carbon as a prospective agent with good adsorbing capabilities against gases like Carbon Monoxide, Nitrogen and other greenhouse gases. Volatile Organic Compounds are compounds that can be both men made or released due to natural activities. VOCs will act as both a source of environmental degradation i.e. they can somehow reduce plant growths and can cause other harmful activities as well as it can also degrade human health. It affects us through nausea, liver damage and even irritation in eyes and noses. Activated Carbon has shown high potentiality to eliminate such harmful VOCs.

For urban usage municipalities have shown interest to use activated carbon in sewage treatment plants and also for water purification. The overview shows how useful it is. Thus, it demonstrates the enormous prospect in scope of research in this field.

## III. RESEARCH TRENDS

Activated Carbon due to its potentiality has been studied thoroughly and different counterparts have been created. Coconut Shells is the most common and a natural form of activated carbon. Adsorption efficiency and the surface area are the two parameters that lead to better usage. More the adsorption efficiency will be more the capability will be to adsorb toxins into its surface. Bamboo activated carbon has an adsorption efficiency of 71% compared to 50% of a normal Charcoal form. From the environmental point of view its usage

exhibits better results and less toxic end products if any. In oil industries palm shells have been found to be a leading source of adsorbents for gas separation. The rise in concern for a “Go Green” initiative has resulted in an increase for products usage that minimizes the degradation of environment. Henceforth, the research trend in this area is quite a vast.

#### IV. CONCLUSION

The main purpose of the article was to enlighten the necessity of consciousness for a green environment. Activated Carbon is just an example; the first priority of recent trends should be to put a limit or to check any form of harmful end products. Also as a consumer the following norms have to be maintained as per our capability. Besides, Science and Technology are always on the verge to upgrade themselves; Thanks to the trait of curiosity. But along with that we should also keep a check to protect our ‘home’ through various means. It is us who are basically responsible for environmental degradation and henceforth, can also be responsible to find out the way to rectify all sorts of degradations in forms of activated carbon.

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# “THE GAME CHANGER” Open Source RISC-V Hardware

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**Abstract:** In this article we have discussed about the importance of “RISC-V”. RISC-V is a free and open instruction set architecture which provides innovative operational mechanisms. This ISA provides a new level of free and extensible software as well as hardware freedom on architecture; offering the way for the next 50 years of computing design and innovation. It has a large amount of advantages like its openness, simplicity, clean-slate design, modularity, extensibility and stability etc.

## I. INTRODUCTION

It is quite well known to us that RISC implements a revolution in efficient and low cost processors and expedites the creation of our modern connected world. However, there are many drawbacks like if we need a chip for a new device, we can find something close to that but not exactly and some time it is highly restricted, complex and also expensive. One of the major limiting factor is the basic processor code or ISA (Instruction Set Architecture). Designing a new ISA is a big endeavour. After that “RISC-V” comes into picture with ISA for anyone i.e. ISA is designed to be flexible. We can add functionality and also can select the features that we want. Therefore, the value of open source hardware varies in the field of hardware designs. Several authentic open source hardware have limited impact on the chip design while RISC-V is not the first open source hardware project, probably the best known and the one that has the largest impact on the industry. UC Berkley has first started “RISC-V” as a project where the first RISC design occurred is RISC-I. For many other open source softwares the standard is open but the CPU design on it doesn’t have to be open or free. On the contrary, “RISC-V” Offers very low

cost of entry; a fresh, clear and very flexible architecture.

## II. IMPORTANCE

### A. What Makes the “RISC-V” So Eminent

- (i) It is originally used in the field of teaching or as a research tool.
- (ii) The instruction set design of RISC-V is very ordinary simple, clean, contemporary and free of IP entanglements.
- (iii) Due to open source, it allows to build chips, enlarge the architecture and explore new instruction sets.
- (iv) So it is quite easily comprehensible for student and also for designing it.
- (v) It not only reduces risk and development expenses, but also makes sure the companies to resource designs to the market much faster.

## III. CONCLUSION

At the end of the day, there are a few things that really matter: having the ability to run the same application binaries and to be able to run the same Operating Systems on different implementations. Therefore, a successful future will be waiting with exploration of applications that are designed with RISC-V.

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# Li-Fi: A New model in Communication system

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**Abstract:** Communication is one of the most important parts of our life for exchanging information from one to another by wired or wireless networks. Now-a-days with the introduction of new mobile devices wireless communications have become the basic necessity of our daily lives. We are mainly familiar with Wi-Fi (Wireless Fidelity), which uses 2.4 GHz – 5 GHz RF to give us wireless internet access around our homes, schools, colleges and offices. We are mostly dependent with this ubiquitous service. This increased number of users and thus the usage of bandwidth has led to obstruction in the radio spectrum. Besides its major limitation is that it can just cover only inside the house or building. We can solve this problem by using Li-Fi (Light Fidelity).

## I. INTRODUCTION

We are mainly familiar with Wi-Fi (Wireless Fidelity) which uses 2.4 – 5 GHz RF to give us wireless internet access for our daily life. We are mostly dependent with this ubiquitous service. This increased number of users and thus the usage of bandwidth has led to obstruction in the radio spectrum and some hindrance makes us unhappy with this. Its major limitation is in the inadequacy of area coverage which is only inside the house or building means it gives a limited facility service. To resolve this problem now-a-days communication uses more flexible protocol which is known as Li-Fi (Light Fidelity).

## II. HOW LI-FI WORKS

Lightning reaches nearly everywhere, so communication can ride along for nearly free by using Li-Fi. This is governed by visible part of spectrum which is more than 10,000 times faster than that of radio part being used in Wi-Fi. Li-Fi basically depends upon the subset of Visible Light Communication (VLC). Li-Fi uses visible light region of the electromagnetic spectrum, transmitting

data through highly bright LED bulbs. Here LED bulbs are basically used as hotspots and provides higher data rates with comparatively larger range of scope. It works on very simple principle. If the LED is on it transmits a digital '1' whereas when it is off digital '0' is transmitted.

Suppose yourself walking in to a mall where GPS signals are unavailable but the mall is equipped with ceiling LED bulbs that create their own 'constellation' of navigation beacons. As your cell phone camera automatically receives these signals it connects your navigation software to use this

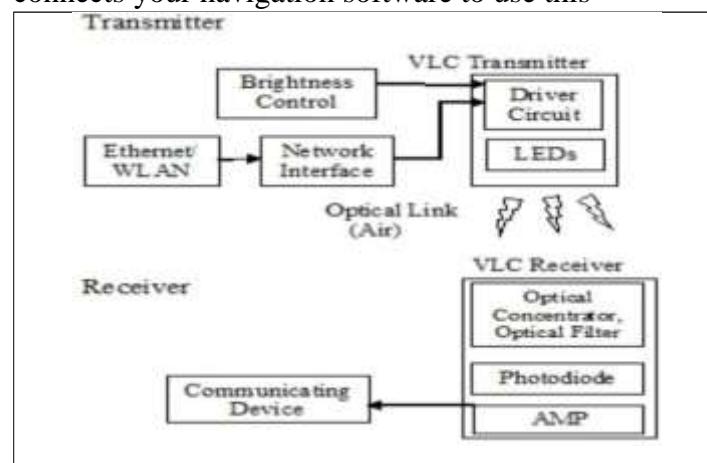


Fig 1. Block Diagram of Li-Fi

information to guide you to the nearby ATM machine, what you're looking for. Then as soon as your ATM transaction is finished the Giga Spot sign can be noticed easily for instant digital movie downloads. Thus a new HD movie can be picked out instantly using phone's payment facility and can be downloaded into the Giga Link flash drive plugged into your mobile USB port within a few seconds. Thereafter, as you walk away, you will be notified by your phone that the leather jacket featured by a movie's character is on sale nearby. Then when you start walking over towards the show window your image will come up on the screen wearing that desirable jacket. You can turn and pose

while the image matches your intention and body gestures for ‘digital fitting’. Thereby when you reach to the store the sales man will hand over the actual jacket to you.

### **III. CONCLUSION**

Li-Fi can makes our daily communication process more easier because of using subset of Visible Light Communication (VLC) which is more than 10,000 times faster than that radio communication using Wi-Fi. So we can say by using Li-Fi we can significantly improve our communication process and data transmission speed. It is best suitable for those areas where optical fiber installation is not possible and it is cheaper as well as reliable compared to that of Wi-Fi. But main disadvantage of Li-Fi is connection problem, when light is turned off or if it is blocked by any obstacle then it will lost its connection.

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# Digital Signal Processor in FPGA

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**Abstract:** Computer architecture is built not only with the components of a computer, but much more consists of suitable instruction sets, compilers, and operating systems with appropriate technologies of chip design. With VLSI design moving up and computer architecture moving down, both areas have come very close, and even cover each other in many aspects. A processor ISA can easily be implemented using any HDL languages like Verilog HDL, System C etc. The most radical change in the field of computer architecture in the last decade was the appearance of RISC V processors. These are marked by Open source ISA that are efficiently executable in parallel pipe-lines. Moreover signal processing application can easily be implemented in FPGA using FFT to design & optimize a Digital Signal Processor.

## I. INTRODUCTION

A classical Von-Neumann architecture enables a low pin-count and less no. of registers for the processor chip, however, with the disadvantage caused by a single common data and instruction bus to the main memory. On the other hand, RISC processors are simple and challenging at the same time [1]. They are simple due to their considerably fewer instruction sets and variants as is indicated by their abbreviated nomenclature RISC (Reduced Instruction Set Computer) than that of Complex Instruction Set Computer (CISC). On the contrary, their design is a bit challenging due to higher degree of parallelism in their implementations and therefore, they become superior just in connection with well-tuned compilers. Henceforth, in this article we will focus on design & implementation of DSP Processor based on RISC architecture using FPGA.

There are lots of platform on which DSP algorithms i.e. FFT, FIR and IIR filters can be implemented. Specifically, it can be implemented in DSP processor [2], a microprocessor specially

designed to execute DSP algorithms & its applications within an ASIC (Application specific integrated circuit) or in a FPGA. Among all these ASIC is the fastest followed by FPGA which is further followed by DSP processor. Since both ASIC and FPGA are hardware based therefore they are faster than DSP processor which executes the instruction sets sequentially i.e. software based. Comparatively ASIC is much faster than FPGA as it doesn't comprehend switching blocks & it consists of less hardware for reconfiguration.

Digital signal processing has a long range of application like image processing, communication etc. A typical DSP processor consists of several noteworthy features like MAC unit (Multiply and accumulate unit), circular addressing scheme, zero overhead looping and pipelining. These features are most important for implementation of DSP algorithm along with which there can be other features like barrel shifter [3].

## II. PIPELINING

Pipelining is a process in which hardware element of the CPU is arranged such that overall performance is increased. Suppose there is an 8 point FFT having 3 stages. Let us suppose each butterfly takes T unit of execution time. For each stage the butterfly (2 point FFT) can be executed parallelly so that each stage takes T unit of execution time. The first instruction will take 3T units of execution time while the rest of the instructions will have single cycle execution for pipelined FFT.

Suppose if a bucket has to be filled by carrying water from well with the help of mug then it will take large time whereas if we have a pipe and motor that fetches water then it will yield very less time. Similar concept is applied in pipelined processor. Modern memory components often have a fast burst

mode increasing the average data transfer rate which requires an efficient memory interface. Thus, it enables the loading of two instructions per cycle, which then should be executed in parallel by duplicate pipeline stages e.g. parallel ALUs (superscalar system). The only disadvantage in this system is the necessity for a more complex & new compiler and a more complex hardware control.

### III. MAC UNIT (MULTIPLY AND ACCUMULATE)

This unit is used in most of the DSP processor. The basic MAC operation is  $R = R + xy$ , where  $R$  is an accumulator register, and  $x$  and  $y$  are the source operands from A and B registers respectively. It can also be implemented using Verilog HDL. Thus MAC which is an important instructional unit of any DSP processor can be easily implemented in FPGA.

### IV. ZERO OVERHEAD LOOPING

Zero overhead looping is a feature in which hardware can repeat the loops i.e. using register rather than software instruction being executed sequentially and increasing computational time.

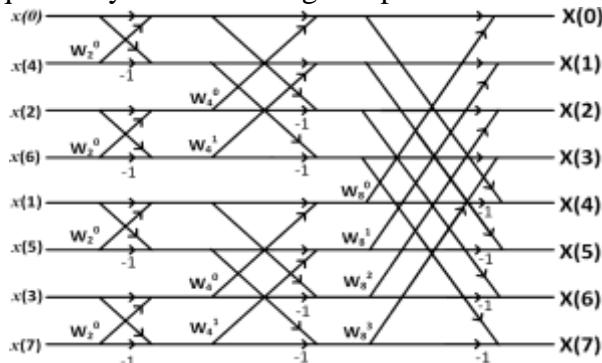


Fig 1. FFT Algorithm [4]

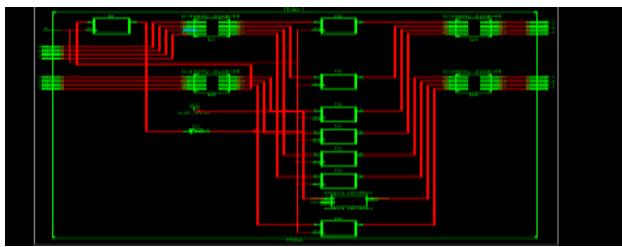


Fig 2. RTL Schematic of 4 point FFT

### V. CIRCULAR ADDRESSING

Circular addressing is used to create circular buffer such that it consists of pointer to point data

without creating overhead due to post shift updated time.

### VI. BARREL SHIFTER

It provides the capability to scale the data during an operand read or write. No overhead is required to implement the shift needed for the scaling operations. Let us observe an example how DSP algorithm is implemented in FPGA.

### VII. FFT IMPLEMENTATION IN FPGA

FFT can be easily implemented in FPGA designing it in Xilinx 14.7 ISE [5]. We got the correct output for a given input  $X_0=1, X_1=2, X_2=3j, X_3=4$ . Hence 4 point FFT algorithm is implemented on Xilinx 14.7 ISE. Thus 4 point FFT as well as other DSP algorithms and FIR filters can be easily implemented in FPGA.

The main advantage of FPGA lies in its flexibility but its cost is its main disadvantage which is recently coming down. In future we can expect FPGA will have major role not only in academia and industry as well as in all parts of life. We can also design a dedicated processor for DSP. It could also have static or dynamic data path to implement signal processing application.

### VIII. CONCLUSIONS

Therefore, we can design a dedicated processor for DSP as well as it could also have static & dynamic data path to implement signal processing application.

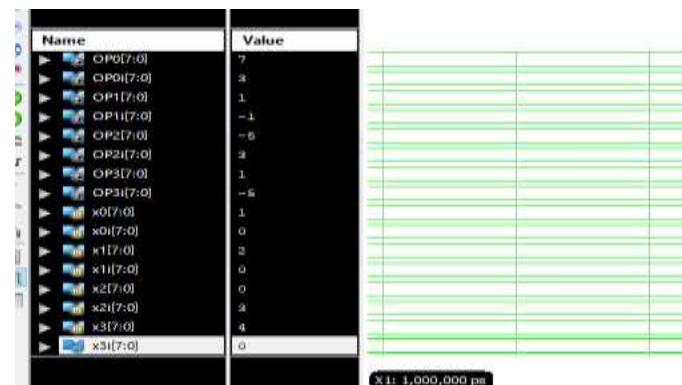


Fig 3. Simulation of 4 point FFT

### ACKNOWLEDGMENT

This article provides an overview of DSP processor in

FPGA which is heavily influenced by the classroom teaching of Processor Architecture and Digital Signal Processing by my respected professor and mentor Prof. A. Sinha.

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# Reconfigurable Analog ALU Design using OP-AMP

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**Abstract:** A reconfigurable analog ALU has been designed & presented here using OP-AMP. A circuit has been proposed which will be able to perform arithmetic operations i.e., Addition, Subtraction, Integration, Differentiation and Multiplication. For designing this circuit Operational-Amplifier and switched capacitor have been used. For the construction of the circuit weighted Summer circuit, difference Amplifier circuit, integrator Circuit, differentiator circuit and multiplier circuit has been implemented and analysed properly using Op-Amp along with its transfer functions. Thereafter, the above-mentioned circuits are merged together to build an integrated singular circuit so that the circuit can be used to perform all the five operations as stated before. Here for different operations different components are required to be connected and few components are required to be disconnected. To fulfil the purpose a logic-controlled switch or 5-volt relay module has been used which can be controlled by the microcontrollers such as Arduino, AVR, PIC, ARM etc.

## I. INTRODUCTION

Before designing the main circuit one should discuss about the construction of weighted summer circuit, differential amplifier circuit, integrator Circuit, differentiator circuit and multiplier circuit using Op-Amp along with its transfer function [1]. After analysis the transfer function of weighted adder circuit is found to be

$$V_0 = - \left[ \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 + \dots + \frac{R_f}{R_n} V_n \right],$$

that of differential amplifier is found to be

$$V_0 = \frac{R_2}{R_1} [V_2 - V_1],$$

output of integrator circuit

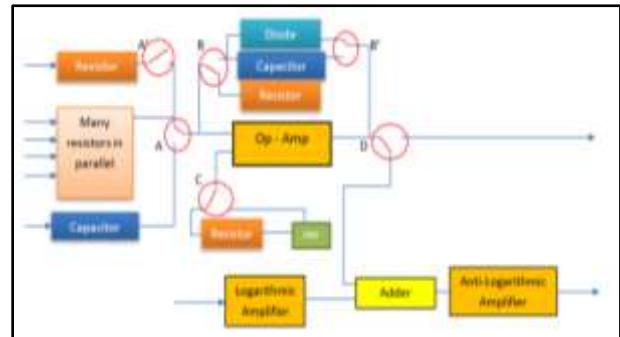
is found to be  $V_0 = -\frac{1}{RC} \int_0^t V_{in} dt + C$ , that of differentiator circuit is  $V_0 = -C R_f \frac{dV_1}{dt}$  and output of multiplier circuit is found to be  $V_0 = -\frac{1}{R I_S} \times (V_1 \times V_2)$ . So, all the circuits

that has been entirely merged together to form a complete integrated circuit which can be used as

adder, subtractor, integrator, differentiator and multiplier.

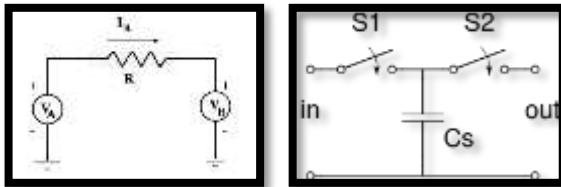
## II. CIRCUIT DIAGRAM

As discussed above aforesaid discrete Op-Amp circuits are merged together to design the final integrated circuit. The circuit has been designed here in an optimized way by using minimum number electronic components with probable objective to design it in a very small area and with minimum costing. Therefore, in this circuit four Op-Amps are used whereas the total count of required Op-Amps in all the discrete circuits before merging is eight. Besides, six switches have been used here for controlling the circuit for performing different operations.



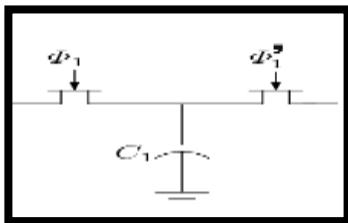
*Fig 1. Proposed ALU Circuit diagram*

Here the main objective is to design the circuit with the help of switched capacitor since those switched capacitors provides high resistance value in very small area. Moreover, it is temperature and process independent. It also provides high tolerance and better voltage linearity. Therefore, switched capacitors have been used here in place of resistors during IC fabrication [2].



**Fig 2. (a) Resistor and (b) Switched capacitor**

In the above diagrams of fig 2(a) and (b) it has been shown that how to connect a switched capacitor in place of resistor. The resistor ( $R$ ) in fig 2(a) is replaced with switched capacitor in fig 2(b).



**Fig 3. Switched Capacitor with MOSFET Switches**

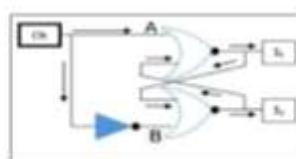
$$\text{Resistance value in fig 2(a)} \quad R = \frac{V_A - V_B}{I_R}$$

$$\text{Resistance value in fig 2(b)} \quad R = \frac{T_{clk}}{C_s}$$

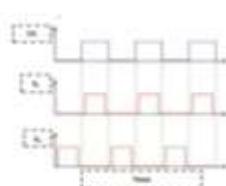
$$\text{Therefore, } \frac{V_A - V_B}{I_R} = \frac{T_{clk}}{C_s}$$

Now, if we compare with the fig 2(b) and fig 3 we can see that normal switches are replaced with the MOSFET switches. This is the authentic diagram of a switched capacitor where MOSFET are used as switches. Thus two MOSFETs  $M_1$  and  $M_2$  and one capacitor  $C_s$  complete one Switched Capacitor. Now, final circuit has been designed by replacing the resistor with switched capacitors as shown in the earlier circuit diagram.

### III. CLOCK GENERATOR FOR SWITCHED CAPACITOR



Clik	A	B	S <sub>1</sub>	S <sub>2</sub>
1	1	0	0	1
0	0	1	1	0



**Fig 4. (a) Clock Generator, (b) Truth Table and (c) Time Line of Clock Generator**

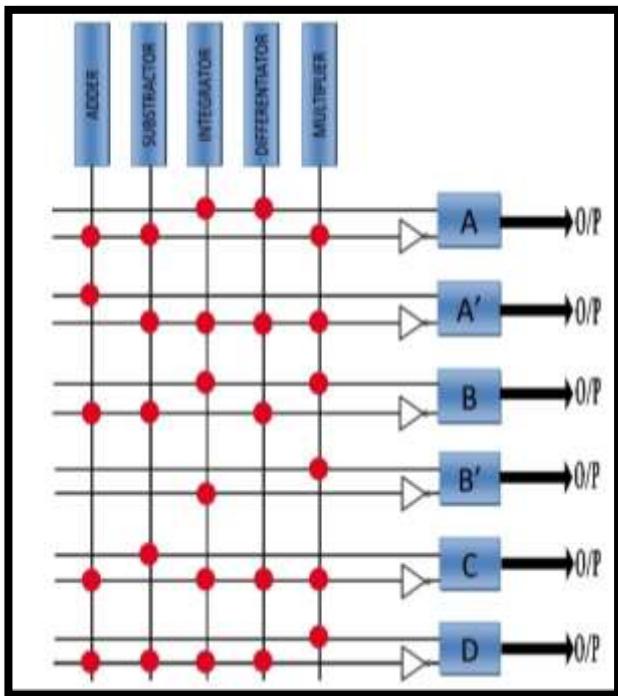
Already we have seen that switched capacitor is basically used for designing a circuit. Therefore, for using switched capacitor the switches need to be controlled by a clock pulse. As shown in fig. 2(b) there are two switches i.e.,  $S_1$  and  $S_2$  which cannot remain ON or OFF simultaneously. If  $S_1$  is ON then  $S_2$  should be OFF and if  $S_1$  is OFF then  $S_2$  should be ON. For achieving this a non-overlapping clock generation is required [3].

### IV. CONTROL UNIT

As mentioned before that this circuit can be used as Adder, Subtractor, Integrator, Differentiator and Multiplier. An Arduino based control unit has been designed following the concept of the diagram given below [4]. The control unit is controlled by logic-controlled switch or 5-volt relay module for performing the operations [5].

### V. WORKING PRINCIPLE

The Circuit Diagram as well as the Control Unit has been exhibited in fig 5 for demonstrating ALU's working principle. The working of the circuit is totally controlled by the six switches/relays i.e., A, A', B, B', C and D. When the mode of operations i.e., addition, subtraction, integration, differentiation or multiplication is selected the switches changes their positions as instructed by the control unit for performing the operation. As for addition the weighted adder circuit is required to be designed. For achieving so the non-inverting terminal of the Op-Amp is grounded through switch C and the inverting terminal is connected to the numbers of parallel resistors through



*Fig 5. Control Unit*

switches A and A'. Then the feedback of the Op-Amp is connected to resistors through switches B and B'. Thereafter finally the output is taken through switch D. All the other operations are executed by repeating the same concept.

## VI. CONCLUSION

In conclusion, it can be inferred that Operation Amplifier and Switched Capacitor based circuits can be used as Adder, Subtractor, Integrator, Differentiator and Multiplier. Proposed circuit reduces number of hardware components. It leads to reduce power dissipation and silicon area. Complexity of this reconfigurable circuit will increase. Proposed Control Unit will control the designed ALU circuit for executing multifunctional activities.

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# Design of FIR Filter Using Genetic Algorithm

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**Abstract:** Filtering is a process by which the frequency spectrum of a signal can be modified, reshaped or manipulated to achieve some desired objectives such as to eliminate noise to avoid contamination of signal, to remove signal distortion due to imperfection in the transmission channel, to resolve the signal into its frequency component, to demodulate the signal which was modulated at the transmitter side and to limit the bandwidth of a signal. Genetic algorithms are search algorithms based on the mechanics of natural selection and genetics. They combine survival of the fittest among string structures with a structured yet randomized information exchange to form a search algorithm with some of the innovative flair of human search. In every generation, a new set of artificial creatures (strings) is created using bits and pieces of the fittest of the old; an occasional new part is tried for good measure.

## I. INTRODUCTION

Genetic Algorithm (GA) can be used for the design of FIR Filters which is based on the concept of “survival of the fittest” [1,4]. This Algorithm is the optimization method that resembles natural selection. In GA a set of numbers which can be a solution to the problem at hand is called genome (chromosome). A set of genomes is called population. The GA creates new generations by applying some genetic operators to the individuals of a population.

In order for genetic algorithm to surpass their more traditional cousins to surpass in the quest for robustness, GA’s must differ in some very fundamental ways. Genetic algorithms are different from more normal optimization and search procedures in four ways:

- (i) GA’s work with a coding of the parameter set, not the parameters themselves.
- (ii) GA’s search from a population of points, not a single point.

(iii) GA’s use payoff (objective function) information, not derivatives or other auxiliary knowledge.

(iv) GA’s use probabilistic transition rules, not deterministic rules.

Figure 1 shows a standard procedure of a Canonical Genetic algorithm.

## II. STEPS OF GENETIC ALGORITHM (GA)

GA involves mainly three steps: Selection, Crossover & Mutation. The Genetic Algorithm loops over an iteration process to make the population evolve. Each consists of the

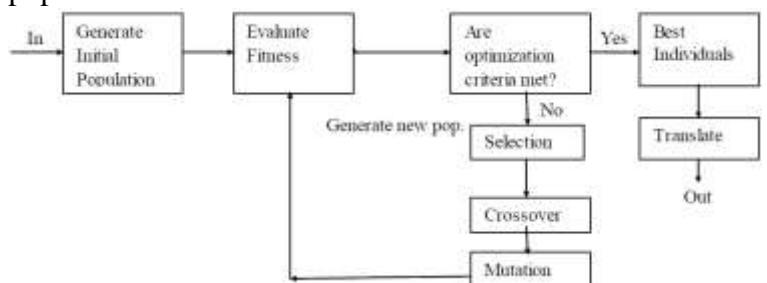


Fig 1. Standard procedure of Canonical Genetic Algorithm

following steps:

### A. Selection

The first step consists of selecting individuals for reproduction. This selection is done randomly with a probability depending on the relative fitness of the individuals so that best ones are often chosen for reproduction than poor ones [5].

### B. Reproduction

In the second step offspring are bred by the selected individuals. For generating new chromosomes the algorithm can use both recombination and mutation.

### C. Evaluation

Then the fitness of the new chromosomes is evaluated.

#### D. Replacement

During the last step individuals from the old population are killed and replaced by the new ones. The algorithm is stopped when the population converges towards the optimal solution [6].

### III. PROPOSED METHODOLOGY

In ideal case for FIR Filter there should be flat pass band, flat stop band and a very small transition band width. It can be seen that in case of Blackman window technique of filter design. There is a flat pass band, large ripples in stop band and transition band width is very large. In case of Parks McClellan technique there are small ripples in pass band, very large ripples in stop band and transition band width is very small.

But when Genetic Algorithm is used instead of the above two techniques there are small ripples in pass band, very small ripples in stop band and transition band width is very small. Magnitude response is approximately same as ideal response [7]. Hence GA has relatively better magnitude response in comparison to Blackman Window and Parks McClellan techniques. Phase response of FIR filter designed using GA approaches towards zero. Hence, there is a very small phase change [8].

### IV. CONCLUSION

Thus in conclusion, out of all three techniques GA offers a quick, simple and automatic method of designing low pass FIR filters that are very close to optimum in terms of magnitude response, frequency response and in terms of phase variation. FIR filter design using Blackman window provide good magnitude response, however, transition bandwidth is very high, phase deviation is quite large and lack of control of critical frequencies  $\omega_p$  and  $\omega_s$ . To overcome this problem, Parks McClellan is used. But as the order of the filter increases, this method is not suitable. Therefore, to resolve out all these problems Genetic Algorithm (GA) is used. With the help of GA the number of operations in design process is reduced and coefficient calculation can be easily realized.

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Women's day Celebration 2020



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Teachers' Day Celebration 2021



Teachers' Day Celebration 2021



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