Setting Up Direct Serial Links

Ronique Young

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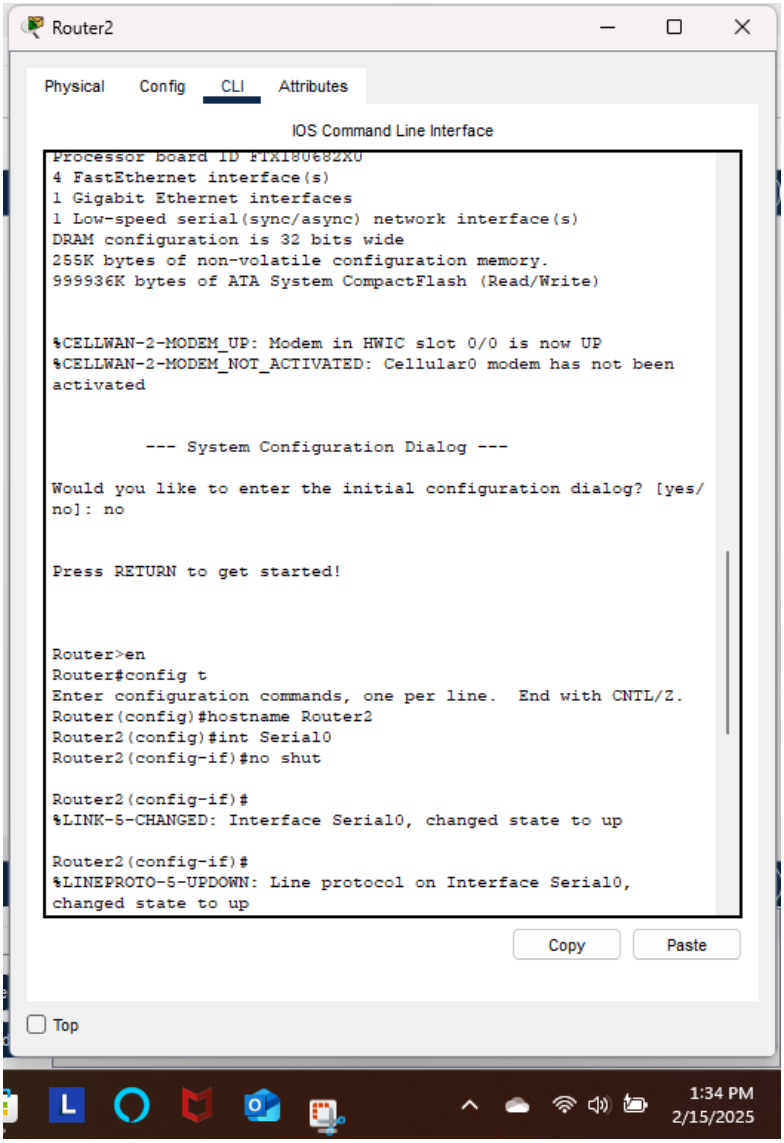
Project Title: Network Setup and Configuration

Enabling Serial Interfaces on R1 and R2

Objective: To enable and verify the Serial0/0 interfaces on Routers R1 and R2, with R2's Serial0/0 identified as the DCE (Data Communications Equipment) in our network topology.



In this part of the network setup, I initially accessed privileged EXEC mode by entering Router>en followed by Router#config t to enter global configuration mode. Here is the sequence of commands:

Changed the router's hostname from 'Router' to 'Router2' with Router(config)#hostname Router2.

Entered interface configuration mode for the Serial0 interface using Router2(config)#int Serial0.

Activated the Serial0 interface with Router2(config-if)#no shut.

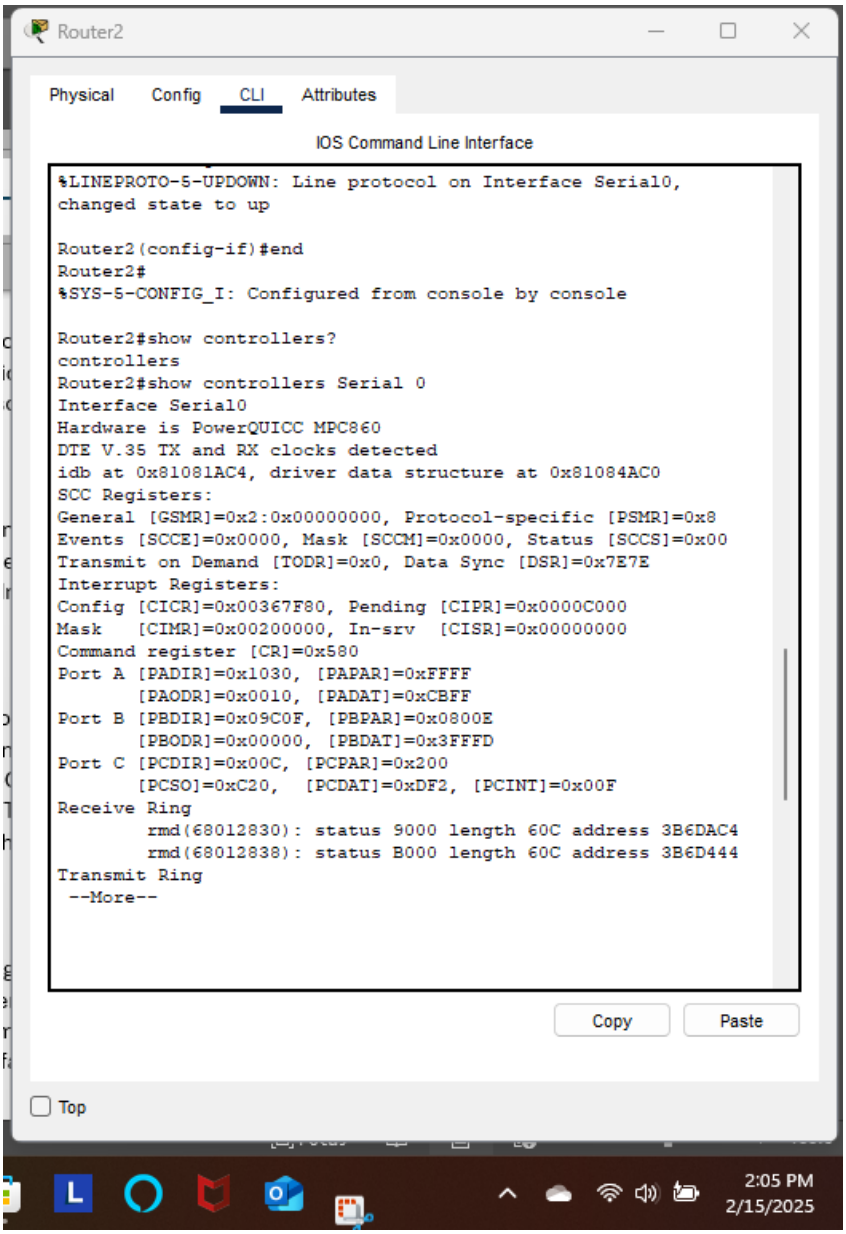
The immediate feedback from the router after enabling the Serial0 interface was:

%LINK-5-CHANGED: Interface Serial0, changed state to up, indicating the physical link of the Serial0 interface was now active.

%LINEPROTO-5-UPDOWN: Line protocol on Interface Serial0, changed state to up, showing that the line protocol on the Serial0 interface has also transitioned to an "up" state, meaning it's now operational at the data link layer.

These log messages confirm that the Serial0 interface on Router2 is now up and functioning, ready to transmit and receive data. This step ensures connectivity between routers or devices connected via this serial link, setting the stage for further network configuration or testing.

Project Documentation: Router2 Serial Interface Configuration



In this phase of the network project, I executed the show controllers Serial0 command on Router2 to delve into the specifics of the Serial0 interface's configuration and operational status. This command output provides comprehensive details about the hardware and software settings of the Serial0 interface.

The interface is identified as using Power QUICC MPC860 hardware, operating in DTE mode with both TX and RX clocks detected, which ensures proper synchronization for serial data transmission. The Interface Descriptor Block (IDB) is located at memory address `0x81081AC4`, while the driver data structure is at `0x81084AC0`.

The Serial Communications Controller (SCC) registers' settings are crucial for the interface's functionality. The General and Protocol-specific Mode Registers (`GSMR` and `PSMR`) are set to values that define the interface's behavior. Notably, the event registers (`SCCE`, `SCCM`, `SCCS`) show no active events or changes, and the Transmit on Demand (`TODR`) and Data Sync (`DSR`) registers are at zero and `0x7E7E`, respectively, which are part of the interface's control mechanism.

The interrupting handling configuration is also detailed, with the Config, Pending, Mask, and In-service registers (`CICR`, `CIPR`, `CIMR`, `CISR`) providing insights into how interrupts are managed. The Command register (`CR`) at `0x580` indicates specific operational commands.

Additionally, the port configurations for `Port A`, `Port B`, and `Port C` outline the interface's pin usage, which is essential for physical layer operations.

Finally, the command output includes a snapshot of the Receive and Transmit Ring buffers. This information shows the memory addresses and status of the buffer entries, which are fundamental for managing data packets moving through the interface. Understanding these buffer details helps in verifying that the data transmission and reception are correctly configured, ensuring robust and efficient serial communication in the network setup.

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