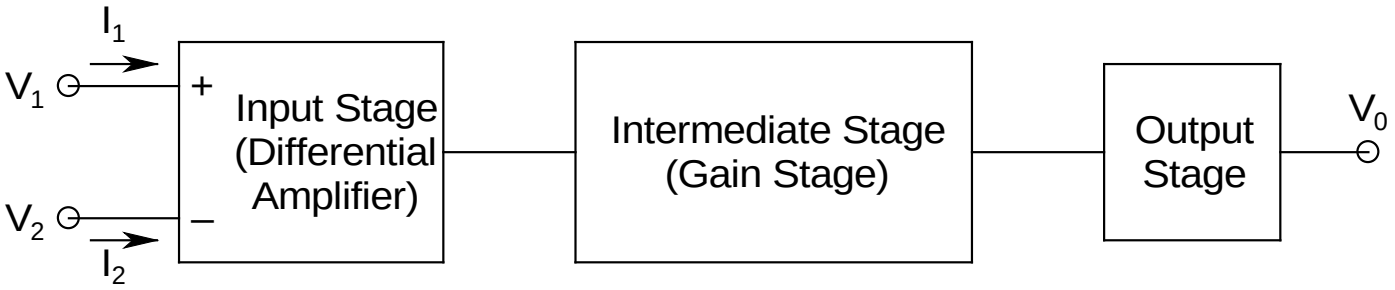
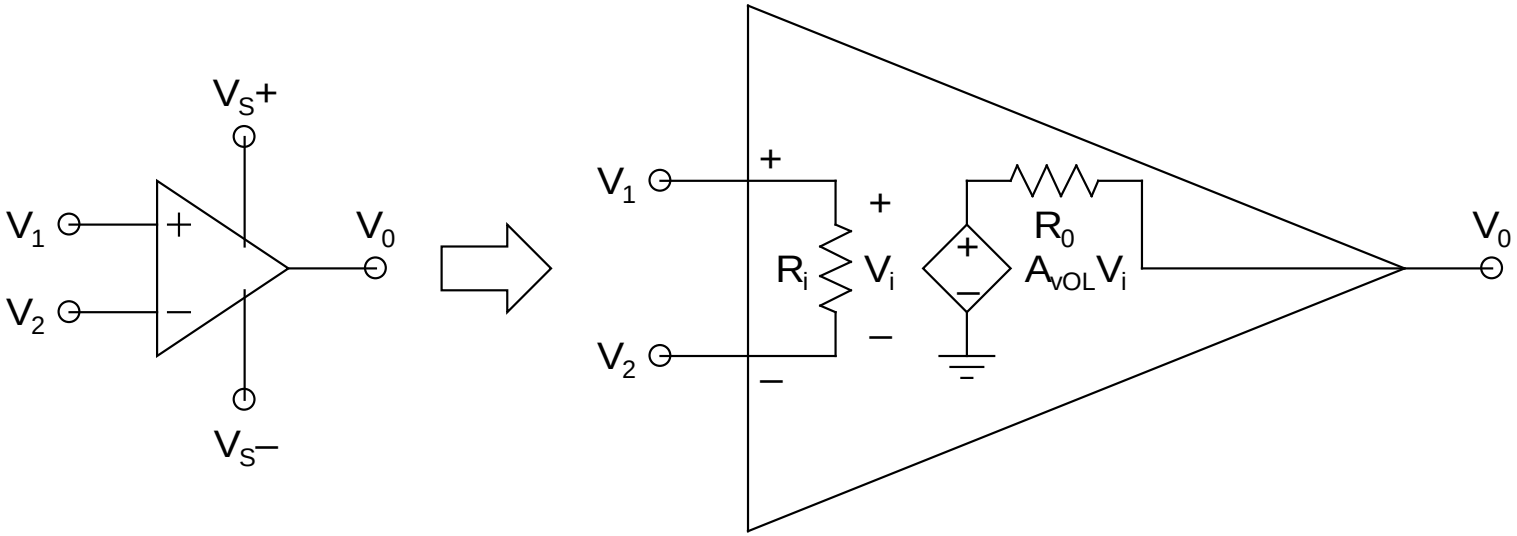


Basic Three-Stage Architecture of an Op-Amp



Symbol

MacroModel

- ***2 Input Terminals***:
  - V_1 (***non-inverting*** [+])
  - V_2 (***inverting*** [–])
- ***1 Output Terminal***: V_0
- V_1, V_2, and V_0 can be ***simply DC***, or ***simply ac,*** or a ***combination of both***
- I_1, I_2: ***Input currents flowing into the + and – terminals respectively***
- ***Dual symmetric power supplies*** (***V_S+ and V_S–***)

- Refer to the ***MacroModel***:
  - R_i: ***Input Resistance***
    - ***Very high*** (***ideally infinite***)
  - R_0: ***Output Resistance***
    - ***Very small*** (***ideally zero***)
  - A_{vOL}: ***Open-Loop Gain***
    - ***Very large*** (***ideally infinite***)
- ***Input-Output Relation***:

$$V_0 = A_{vOL}(V_1 - V_2)$$

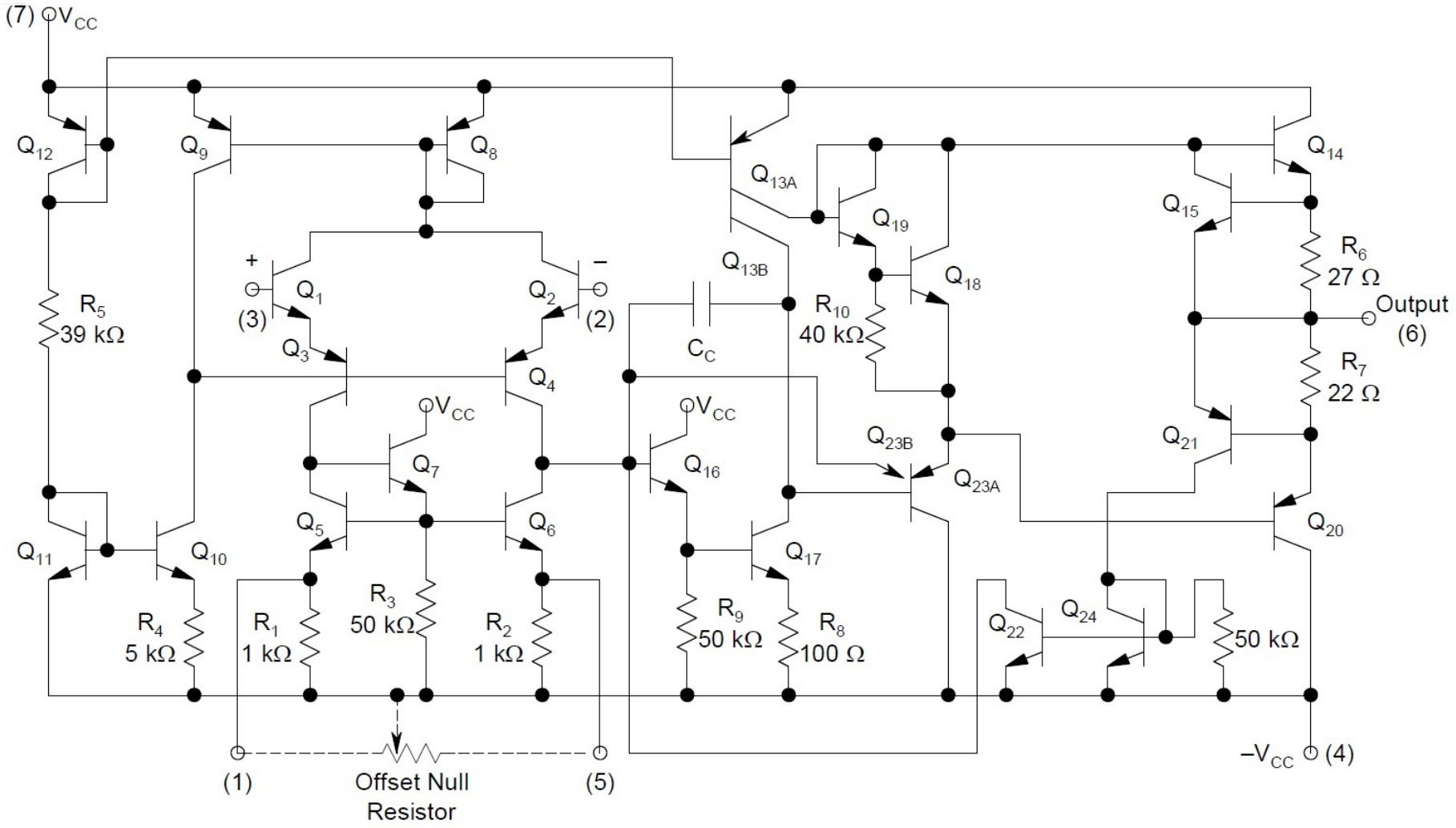
- V_1, V_2, and V_0 are measured ***w.r.t. ground***, but V_i is a ***floating signal*** (***difference*** between V_1 and V_2)
- The ***controlled source*** in the ***MacroModel*** is ***VCVS*** (***Voltage Amplifier***)
- For $V_1 > (<) V_2$, V_0 is ***positive*** (***negative***)
- ***Typical values for 741 op-amp***:
  - $A_{vOL} \sim 10^5$ (***100 dB***), $R_i >$ ***1 MΩ***, $R_0 <$ ***100 Ω***, CMRR ~ ***80-100 dB***, V_S+ and V_S-: ***±3 V to ±15 V***

- ***Uncompensated bandwidth*** typically ***larger than 1 MHz***
- Such a ***large gain*** and ***high bandwidth*** system will be prone to ***oscillations*** (***instability***)
- Need adequate ***compensation***
  - ***Compensated bandwidth*** drops to about ***5-10 Hz***

- ***History of 741 Op-Amp***:
  - In ***1965***, ***Bob Widlar*** (remember ***Widlar current source***?) of ***Fairchild Semiconductors*** (now defunct) first came up with the design of a ***monolithic*** (***single substrate IC***) ***op-amp***

- Named it ***μA 709*** (***μA*** was the ***trademark*** of ***Fairchild Semiconductors***)
- Almost immediately thereafter, ***a number of improvements*** were made on the ***original architecture***, and ***μA 741*** evolved
- It became so ***popular*** that ***the term 741*** became a ***legend***
- ***All subsequent op-amp designs continued to be called 741***!
- ***Initial design*** of course was based on ***bipolar technology***, since at that time, ***MOSFETs were not even there***!

- In ***late 70s***, ***JFET version*** of op-amps came into existence, followed by the ***MOSFET version*** in the ***80s***
- The ***design pedagogy*** of the ***original version*** is a ***real beauty***
- So many ***brilliant innovations*** were ***incorporated*** in the ***design***, that it is a ***learner's paradise***!
- The ***detailed analysis*** of the ***bipolar version*** of the ***741 op-amp*** is given in my book
- Go through it and enjoy! :)



The schematic of the 741 bipolar op-amp (the pin numbers of the 741 chip is shown in parantheses).

Transistor(s)	Magnitude (μA)
I_{C1}, I_{C2}, I_{C3}, I_{C4}, I_{C5}, I_{C6}	9.5
I_{C7}	12.1
I_{C8}, I_{C9}, I_{C10}	19
I_{C11}, I_{C12}	733.3
I_{C13A}, I_{C23A}	183.3
I_{C13B}, I_{C17}	550
I_{C14}, I_{C20}	216
I_{C16}	17.9
I_{C18}	165.7
I_{C19}	17.6

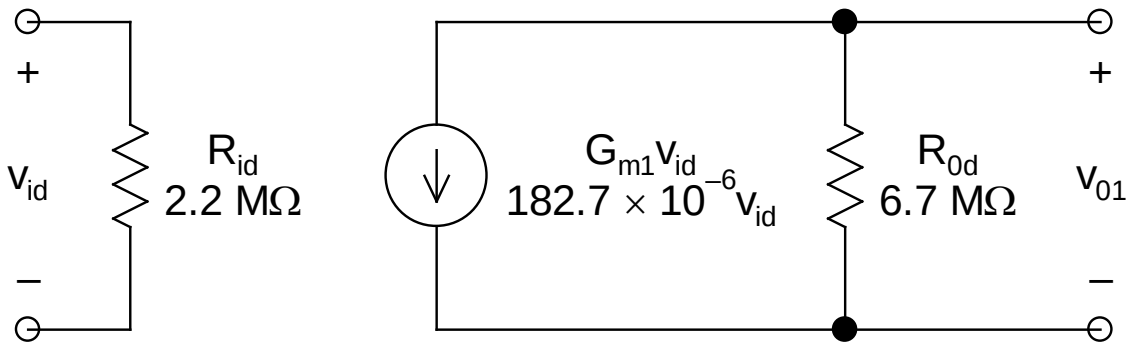
The DC Bias Currents of Different Transistors

- The ***DC power dissipation*** of the circuit:

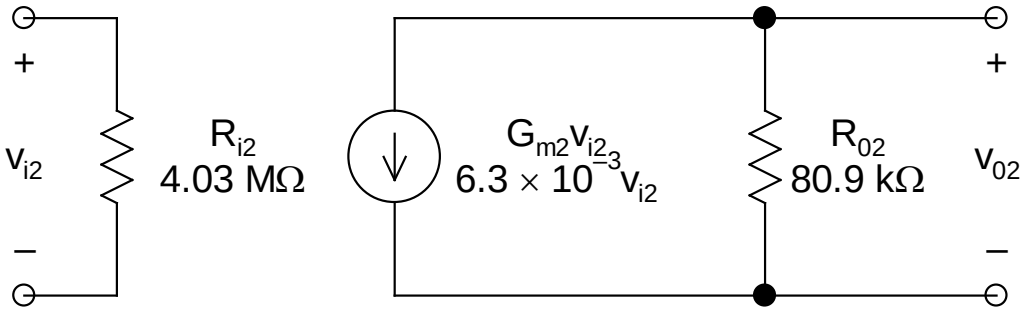
$$P_{DC} = V_{CC} \times (I_{C12} + I_{C9} + I_{C8} + I_{C13A} + I_{C13B} + I_{C14} + I_{C7} + I_{C16}) + |-V_{CC}| \times (I_{C11} + I_{C10} + I_{C5} + I_{C7} + I_{C6} + I_{R9} + I_{C17} + I_{C23A} + I_{C20})$$

$$= 52.3 \text{ mW}$$

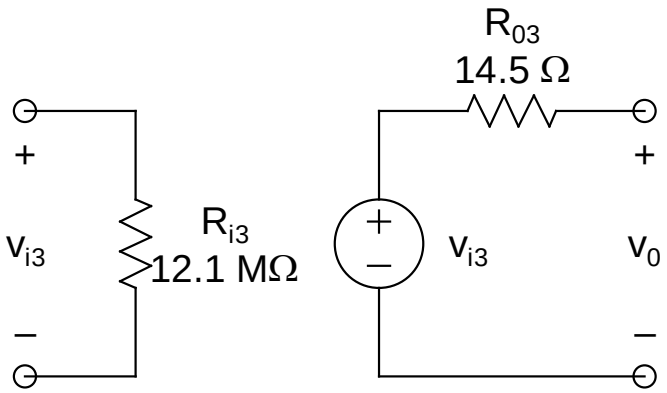
- Note that the ***reference branch*** consumes the ***highest DC power***, followed by the ***Darlington branch***
- On the other hand, the ***least DC power*** is consumed by the ***DA branch***



2-Port Equivalent of the Input Stage



2-Port Equivalent of the Gain Stage

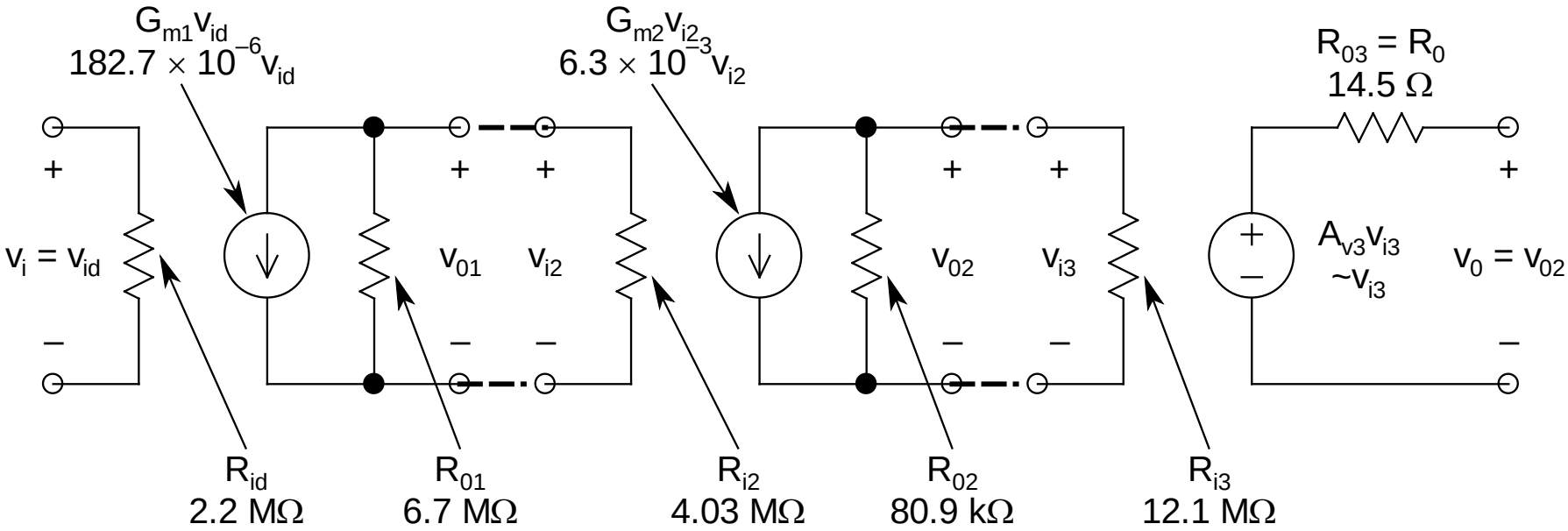


2-Port Equivalent of the Output Stage

(Driving a load of 5 kΩ)

➢ *Overall Performance*:

- Just *cascade* the *2-port equivalents* of the *three stages*



Complete 2-Port Representation of 741 Op-Amp

- ***Voltage gain of the input stage***:

  $A_{v1} = v_{01}/v_{id} = -G_{m1}(R_{01}\|R_{i2}) = -459.7$

- ***Voltage gain of the gain stage***:

  $A_{v2} = v_{02}/v_{01} = -G_{m2}(R_{02}\|R_{i3}) = -506.3$

- ***Voltage gain of the output stage***:

  $A_{v3} \sim 1$

- Thus, the ***overall voltage gain*** of ***741 op-amp***:

  $A_{vOL} = v_0/v_{id} = (v_0/v_{i3}) \times (v_{i3}/v_{i2}) \times (v_{i2}/v_{id})$

  $= 2.33 \times 10^5$ (107.3 dB)

  Note: $v_{i3} = v_{02}$, and $v_{i2} = v_{01}$

- This is an ***excellent value***, in spite of the ***significant loading effect*** of the ***gain stage*** on the ***input stage***

➢ *Observations*:

- A_{vOL} is actually the ***differential-mode gain*** (A_{dm})
- It is ***positive***
  - ❖ ***Positive*** v_{id} produces ***positive*** v_0
  - ❖ ***Bases*** of Q_1 and Q_2 are termed as ***non-inverting*** (+) and ***inverting*** (–) terminals respectively
- ***Input and output resistances*** are 2.2 MΩ and 14.5 Ω respectively, both of which are ***excellent values***
- The ***exact value*** of A_{cm} is ***a bit difficult to evaluate***, but it's quite small
- Has ***extremely high CMRR***, typically more than 80 dB