EE-380 EC Lab-01
Basics of Prototyping, Measurement and Simulation

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Section: C

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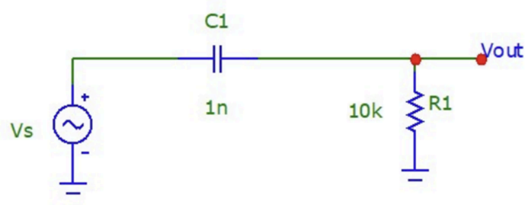
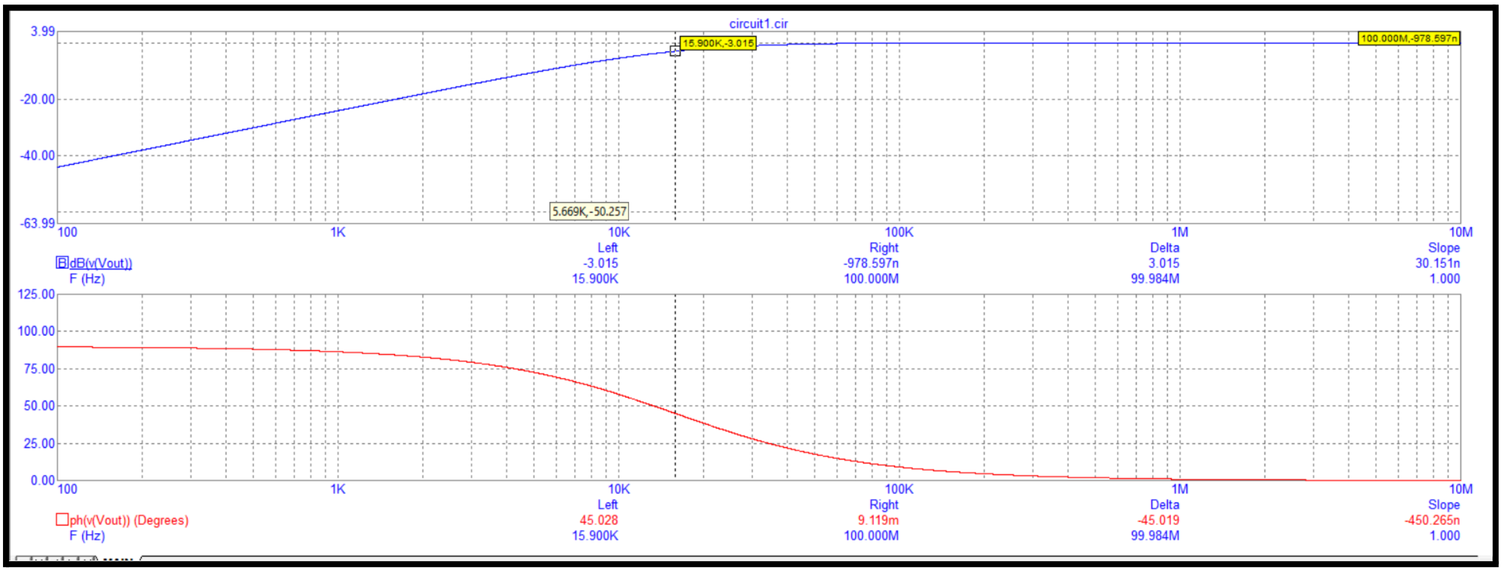
1 Measure the frequency response of the RC circuit

1.1 Pre Lab Simulation

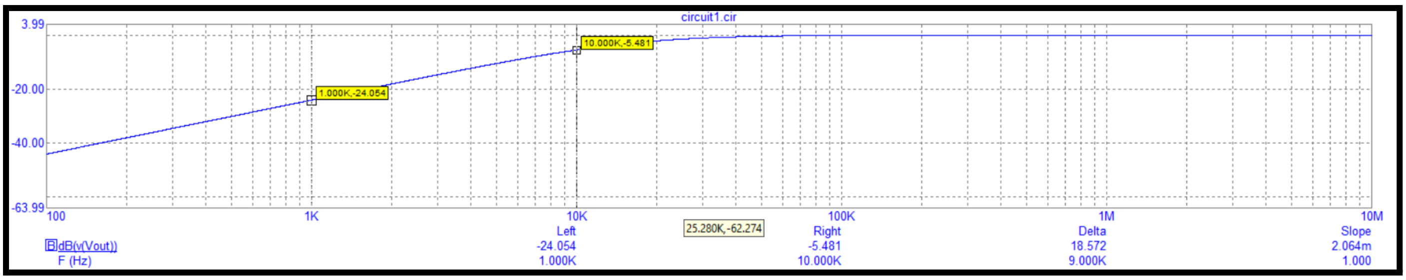




-3db or Cutoff Frequency comes around **15.9 kHz from the plot**

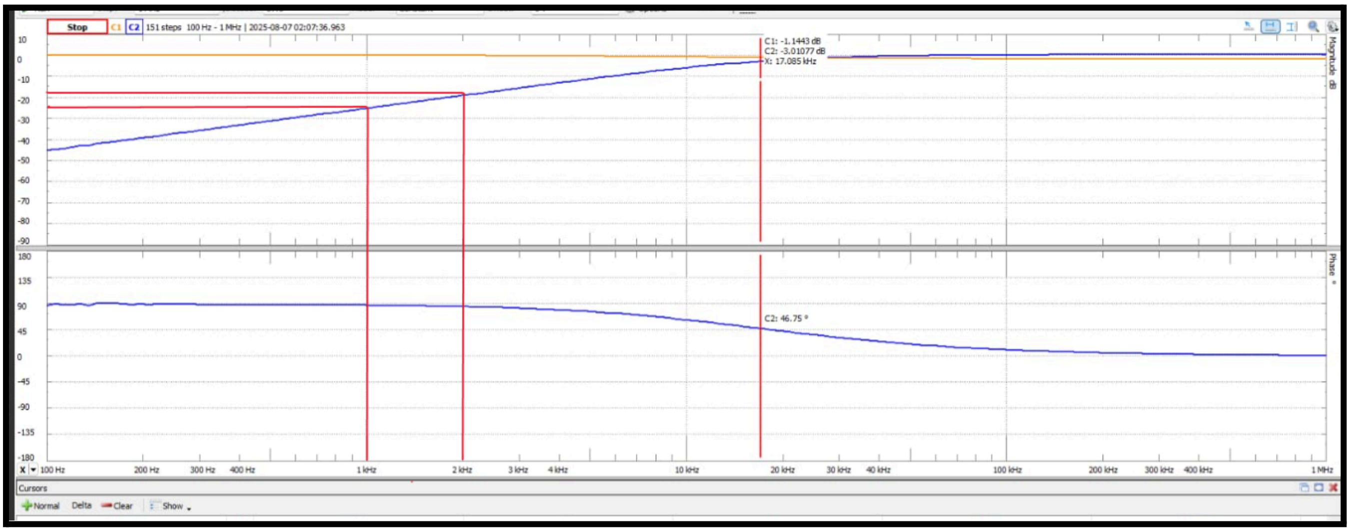
and expected lower cutoff frequency is $f_L = \frac{1}{2\pi RC} = \frac{1}{2\pi 10^4 10^{-9}} = 15915\ Hz\ or\ \sim 15.9kHz$

Rolloff Frequency:



The rolloff comes to be round (-24.054 - (-5.481)) = 18.573 dB/dec that is approximately 20 dB/dec as measured between 1 kHz and 10 kHz, which is expected.
The variation from 20dB/dec is due to the fact that 10kHz is close to corner frequency so the slope starts attaining 0dB/dec.

1.2 In Lab Experimental Result



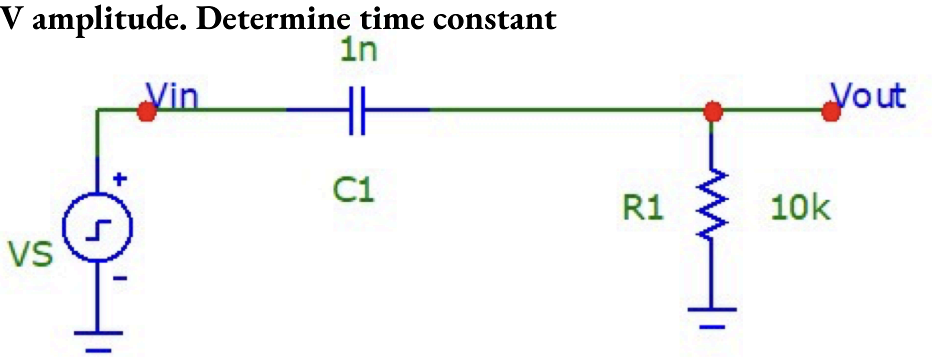
-3db or Cutoff Frequency comes around **17.085 kHz** in lab

And Rolloff $\simeq \frac{-25-(-18.5)}{log(1/2)} \simeq 21.6 dB/dec$

1.3 Post Lab Calculation Discussion

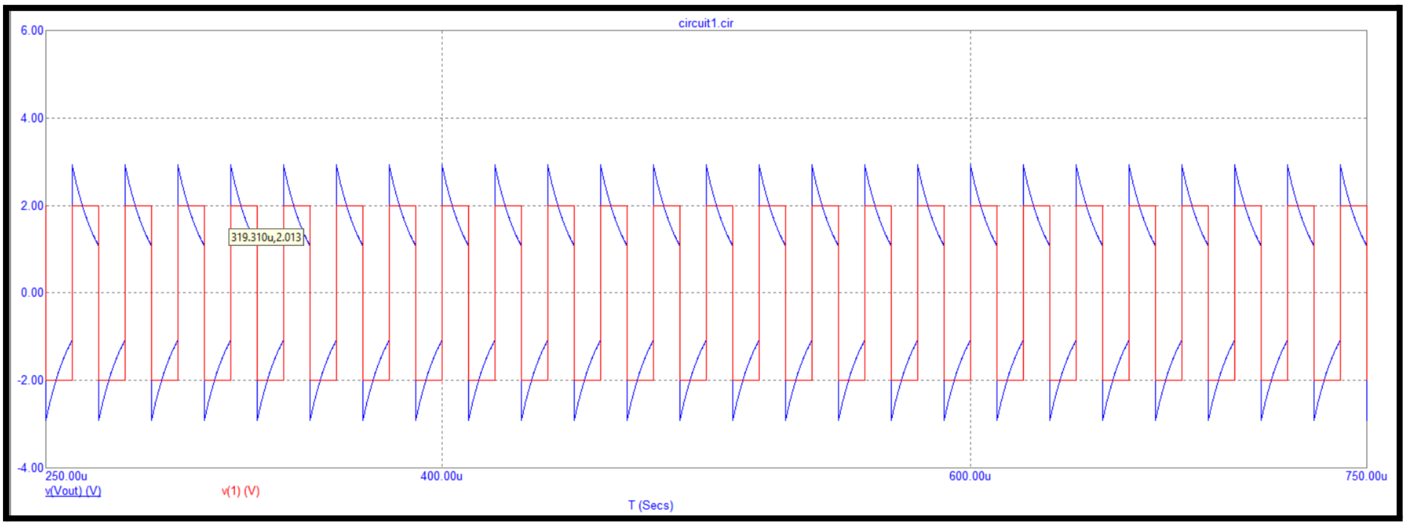
The simulated cutoff frequency was around 15.9 kHz, whereas the experimental measurement was about 17 kHz and the experimental rolloff comes close to the expected 20dB/dec. This slight difference is expected due to component tolerances in resistors and capacitors, parasitic capacitances and inductances from wiring and junctions, and limitations of measurement tools such as oscilloscope bandwidth and probe capacitance. Temperature effects on resistor values and capacitor dielectrics also contribute. Despite these factors, the results are in close agreement, showing that the high-pass filter performs as designed within normal practical variations.

2 Measure the transient response of the given RC circuit with a square-wave input of ±2V amplitude. Determine time constant

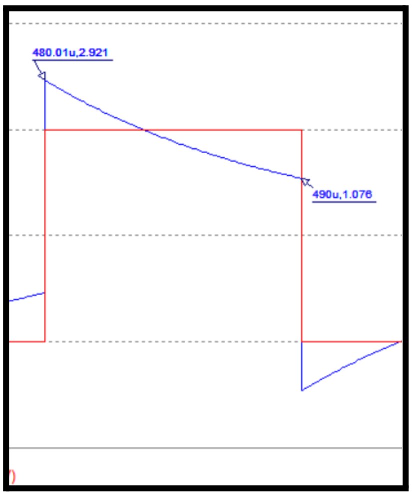


2.1 Pre Lab Simulation Result:

Square wave with 20µs time period and 50% duty cycle was applied



>Determination of Time Constant form simulation

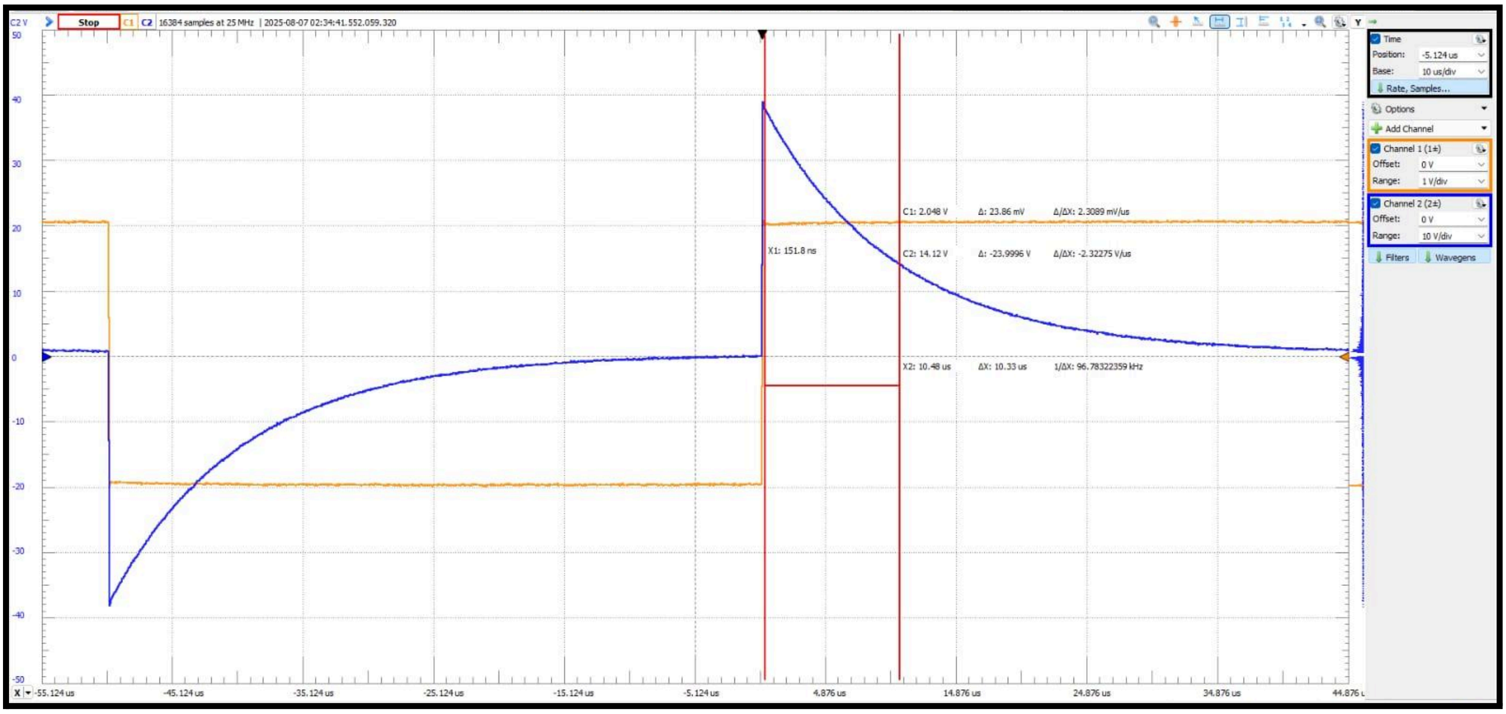


Between 480us and 4900us, the curve should follow capacitor charge decay (discharging) equation $V(\Delta t) = V_0 e^{-\frac{\Delta t}{\tau}}$

$$\Rightarrow \tau = \frac{\Delta t}{ln(\frac{V_0}{V(\Delta t)})} = \frac{10}{ln(\frac{2.921}{1.076})}$$

$\tau = 10.01\mu s$

2.2 In Lab Measurement



Determination of Time Constant form experimental data

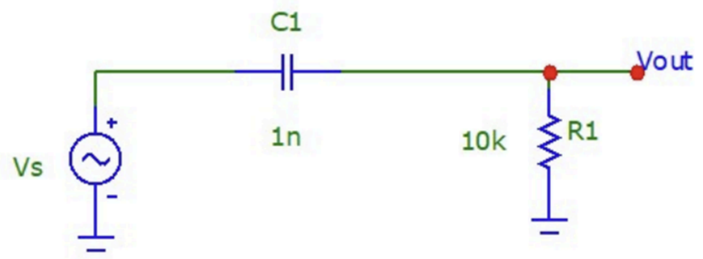
Δt = 10.33 us, v(final) is chosen such that v(final) ≈ V_0 /e

$\Rightarrow \tau = 10.33 \mu s$

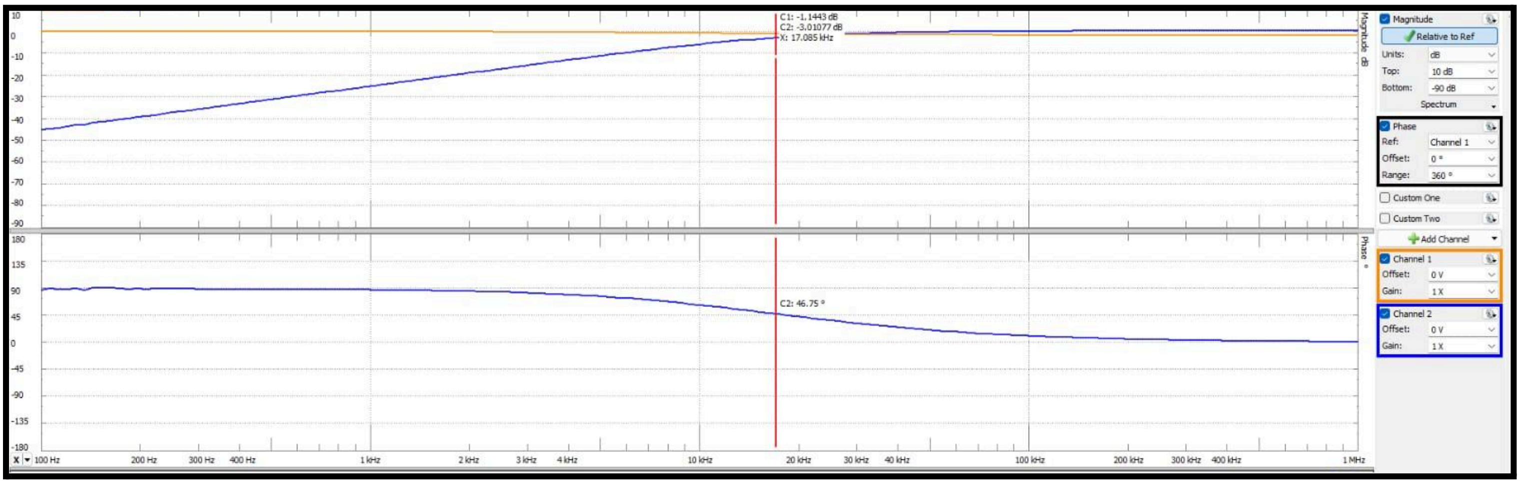
2.3 Post Lab Discussion

The theoretical time constant obtained from the relation $\tau = RC$ was calculated to be 10 µs. In comparison, the measured value during the experiment was 10.33µs, and the value obtained from the simulation was 10.01 µs. The small differences among these results arise mainly due to real-world factors such as manufacturing tolerances of resistors and capacitors, parasitic capacitances and resistances present in the circuit layout and connections, as well as measurement limitations like oscilloscope resolution and probe loading effects. On the other hand, simulations are based on idealized models of components, which neglect these imperfections, leading to results that are closer to the theoretical prediction.

3 Experimentally determine the frequency at which gain is -80dB



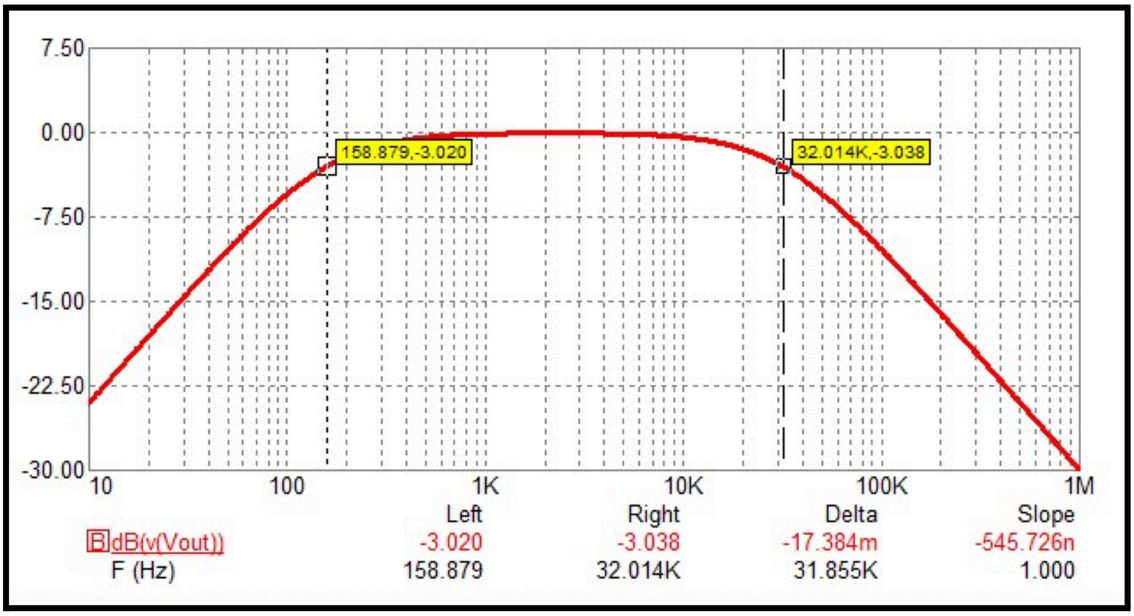
3.1 In Lab Measurements



-80dB frequency was found out to be **1.56 Hz**

4 Design a circuit that has the following frequency response.

4.1 Pre Lab Designing and Simulation

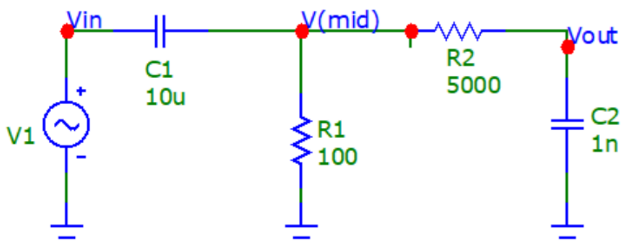


To achieve the desired frequency response, a bandpass filter is constructed by cascading a high-pass filter with a low-pass filter, each designed with appropriate cutoff frequencies. The lower and upper cutoff frequencies corresponding to the -3 dB points on the Bode plot—are approximately 158.9 Hz and 32.0 kHz, respectively. These cutoff points define the bandwidth of the filter and are calculated using standard cutoff frequency formulas:

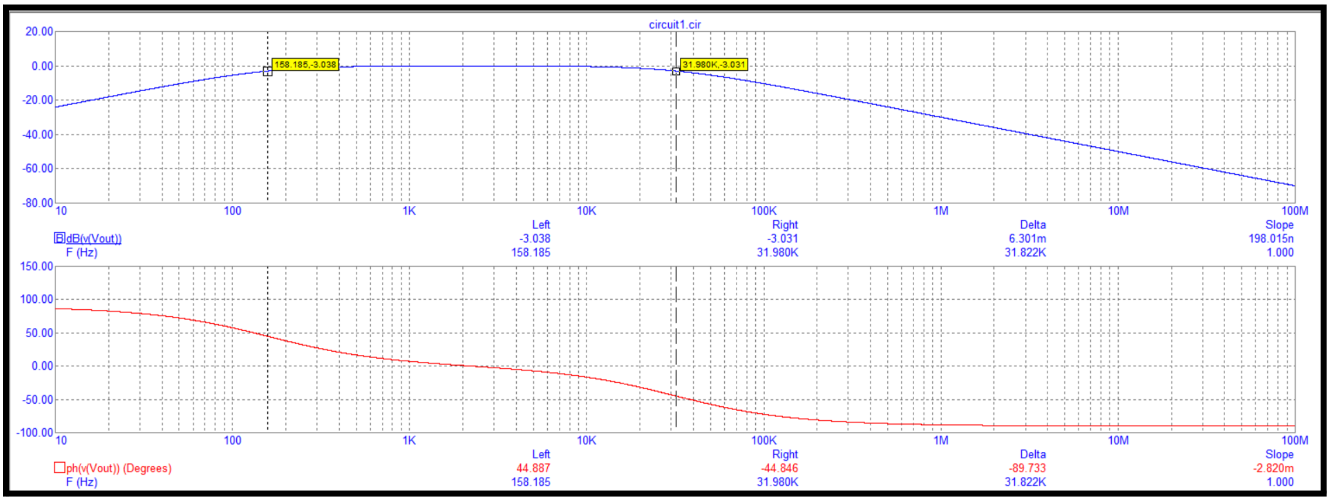
$f_L = \frac{1}{2\pi R_1 C_1}$ and $f_H = \frac{1}{2\pi R_2 C_2}$

$R_1 C_1 = 0.001$ and $R_2 C_2 = 5 * 10^{-6}$

We set $R_1 = 100\ \Omega$ and $C_1 = 10$ uF for the high-pass stage, and $R_2 = 5000\ \Omega$ and $C_2 = 1$nF for the low-pass stage. This configuration effectively produces the desired bandpass response, as reflected in the resulting Bode plot.

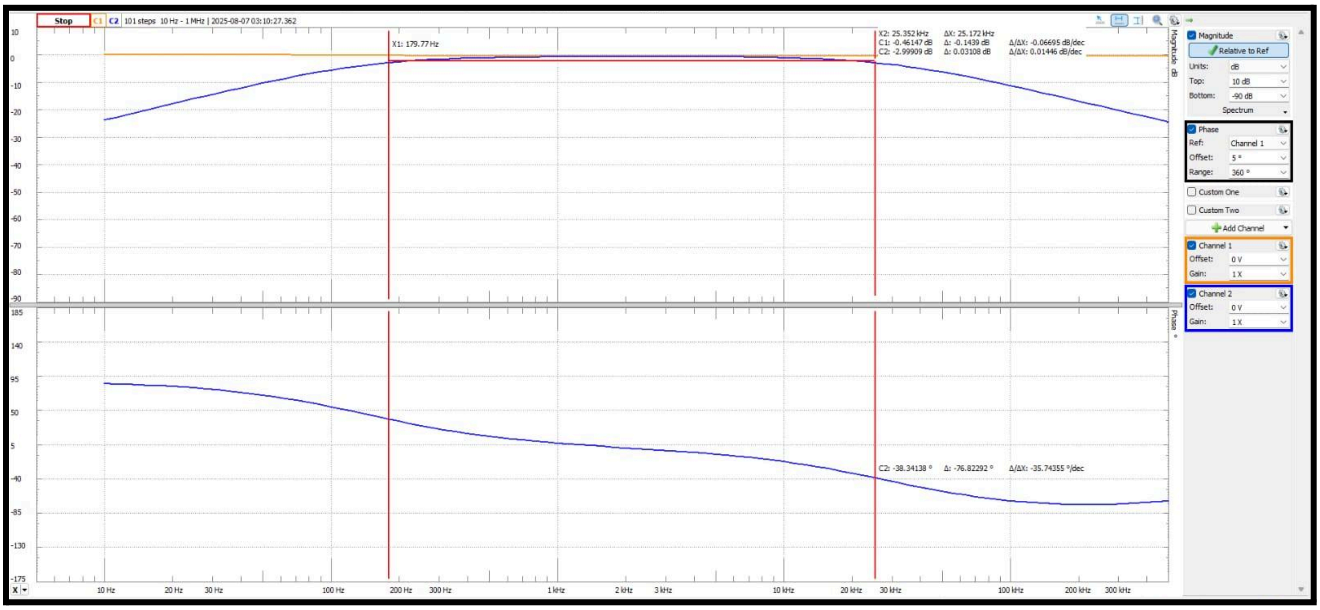


Frequency Response:



4.2 In Lab Measurement

Frequency Response:

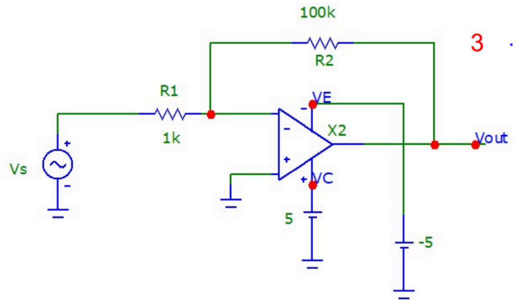


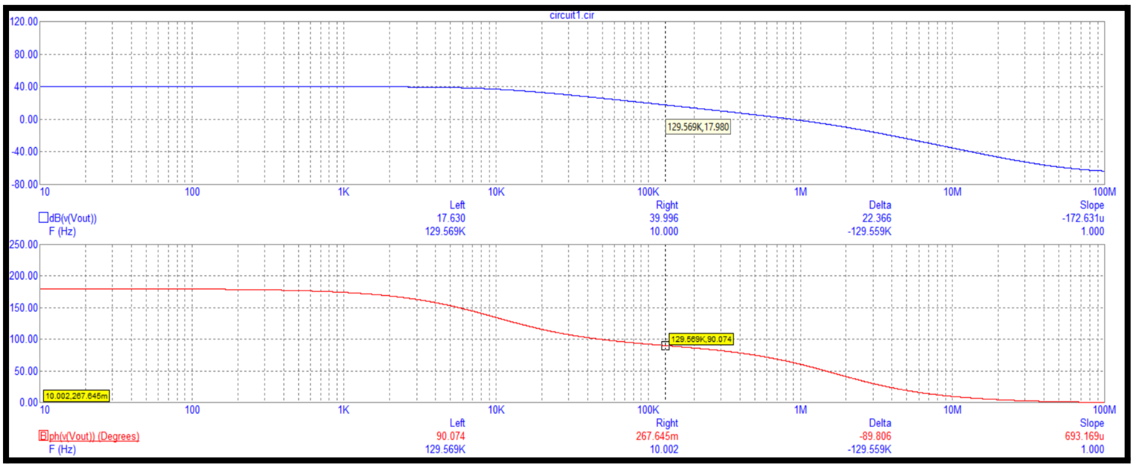
4.3 Post Lab Discussion

The in lab designed circuit exhibited lower and upper cutoff frequencies of approximately 179.8 Hz and 25.35 kHz, compared to the target values of 158 Hz and 32 kHz. This deviation is primarily due to the use of a 5.1 kΩ resistor in place of the intended 5 kΩ, as the exact value was unavailable. The substitution slightly changed the RC time constants, resulting in a shift in the cutoff frequencies.

5 (Bonus) : Find from both simulation and experiment the frequency at which phase difference between input and output is not 180º but 90º. What is the voltage gain at this frequency?

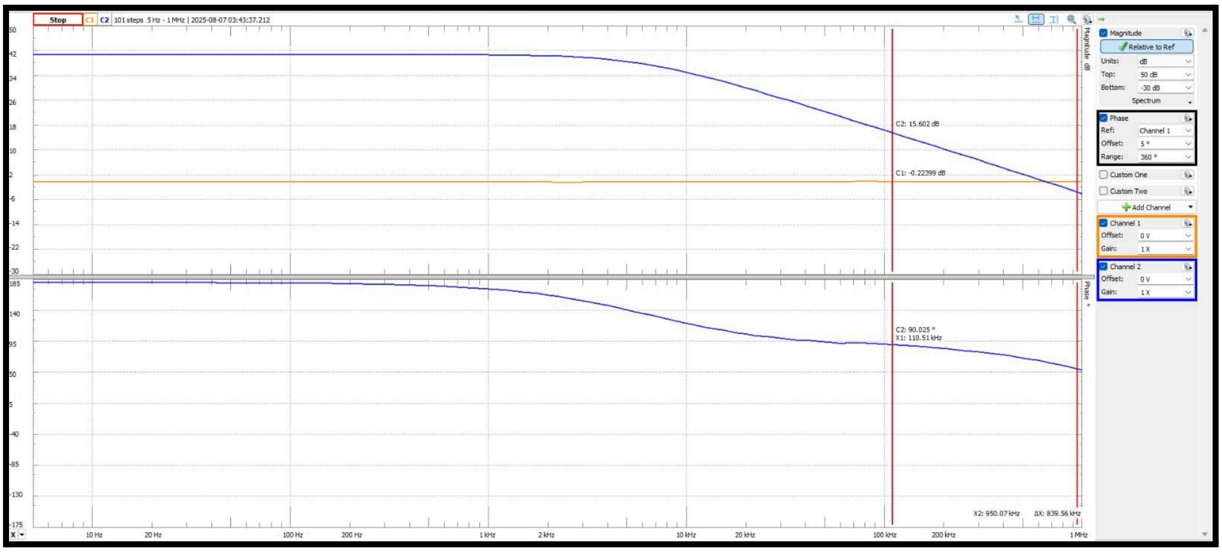
5.1 Pre Lab Simulation





From the simulation, it is evident that the Phase shift is 90º at **frequency = 129.589 kHz**, the Voltage gain at this frequency is **17.98 dB**.

5.2 In Lab Measurement



From the lab measurements, the frequency where phase difference between input and output is 90º is **110.51 kHz** with the gain is **15.602 dB.**

5.3 Post Lab Discussion:

The difference between the simulated and experimental results is primarily due to practical non-idealities not present in the simulation. Factors such as component tolerances, parasitic capacitance and inductance, and loading effects from measurement equipment can alter the circuit's frequency response. Additionally, real-world imperfections like breadboard wiring and temperature variations can shift the 90° phase point and reduce gain slightly, explaining the observed discrepancy.