Small-Signal Model

- The ***electrical equivalent*** of the MOSFET at the ***DC bias point***
- ***Must be biased in saturation***
  - ***Resembles a constant current source***
- ***DC analysis must precede***, since ***need the information regarding the Q-point*** (I_D, V_{DS})
- ***This model for NMOS and PMOS is the same*** (***incremental model***)

Validity of the Small-Signal Model

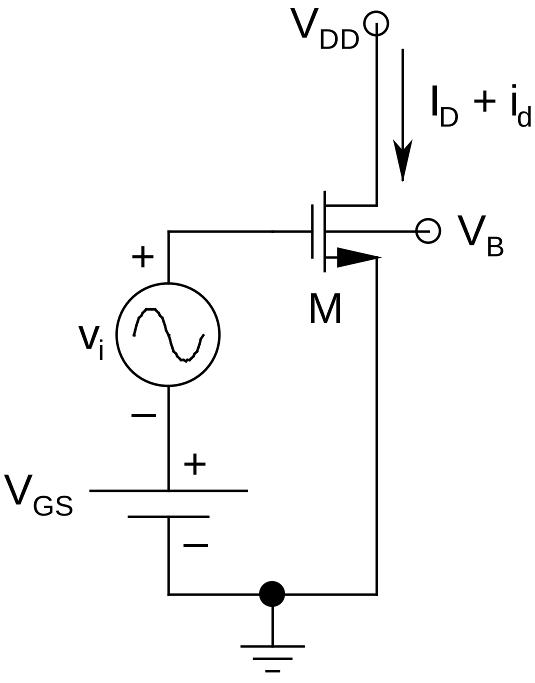
- The ***instantaneous current***

  (***assuming $\lambda V_{DS} < 0.1$***):

$$I_d = \frac{k_N}{2}\left(V_{GT} + v_i\right)^2$$

$$= I_D + \frac{k_N}{2}\left[2V_{GT}v_i + v_i^2\right]$$

$$\Rightarrow \; i_d = k_N V_{GT} v_i \left[1 + \frac{v_i}{2V_{GT}}\right]$$



- Thus, for ***linear relationship*** between i_d and v_i, ***v_i must be << $2V_{GT}$***
- Note that ***V_{GT} (minimum) = $3V_T$***
- Hence, ***v_i should be less than 1/10th of $6V_T$*** (requirement less rigorous than BJT)
- Recall in ***BJT***, for ***linear relationship*** between i_c and v_i, ***v_i has to be less than 1/10th of V_T***
  - ➢ ***Six times less than that for MOSFET***
  - ➢ ***MOSFETs are inherently more linear device than BJT*** (***compare quadratic with exponential***)

Small-Signal Model Parameters

- ***Transconductance*** (g_m):

$$g_m \triangleq \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS} \text{ and } V_{SB} \text{ constant}}$$

$$= k_N V_{GT}\left(1+\lambda V_{DS}\right) = \sqrt{2k_N I_D\left(1+\lambda V_{DS}\right)}$$

  - ***If $\lambda V_{DS} < 0.1$***:

$$g_m \simeq k_N V_{GT} \simeq \sqrt{2k_N I_D}$$

- An important ***Figure of Merit*** is ***transconductance to current ratio***
  - For ***MOSFETs***: $g_m/I_D = 2/V_{GT}$
  - For ***BJTs***: $g_m/I_C = 1/V_T$
  - Thus, ***BJTs produce more g_m per unit current***
- As we will see later, a ***high value of g_m is highly desirable***, since it ***dictates the gain***
- **g_m/I_D *can be changed by changing the bias current and/or aspect ratio***
- **g_m/I_C *is a function only of temperature***

- ***Body Transconductance*** (g_{mb}):

$$g_{mb} \triangleq \left.\frac{\partial I_D}{\partial V_{BS}}\right|_{V_{GS}\ \text{and}\ V_{DS}\ \text{constant}} = \chi g_m$$

$$\chi = \frac{\gamma}{2\sqrt{2\phi_F + V_{SB}}} = \textit{\textbf{Body factor}} \quad (\sim 0.1\text{-}0.3)$$

   - ***Note***: ***As*** $V_{SB}\uparrow$, $V_{TN}\uparrow \Rightarrow I_D\downarrow$
   - $\partial I_D/\partial V_{SB}$ ***would have yielded negative*** g_{mb}
   - ***If both B and S are tied to fixed DC potentials*** (***including ground***), g_{mb} ***won't matter***!

- ***Output Conductance*** (g_0)/ ***Output Resistance*** (r_0):

$$g_0 = r_0^{-1} \triangleq \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS} \text{ and } V_{SB} \text{ constant}} = \frac{\lambda I_D}{1+\lambda V_{DS}}$$

  - ***If $\lambda V_{DS} < 0.1$***:

    $g_0 = 1/r_0 \approx \lambda I_D$
  - ***λ has a very wide range*** ~ 0.01-0.5 V^{-1}
  - ***When $\lambda \rightarrow 0$, $g_0 \rightarrow 0$, and $r_0 \rightarrow \infty$***
    - ***Device starts to behave like an ideal constant current source***

- ***Gate-Source and Gate-Drain Capacitance*** (C_{gs} and C_{gd}):
  - Each has ***two components***: ***intrinsic*** (i) and ***technological*** (t)
  - ***Total intrinsic gate-body capacitance***:

    $$C_{gbi} = C'_{ox} WL$$
  - Using ***Meyer's model***, ***intrinsic component***:
    - In ***linear region***: $C_{gsi} = C_{gdi} = C_{gbi}/2$
    - In ***saturation region***: $C_{gsi} = (2/3)C_{gbi}$, $C_{gdi} = 0$
  - ***Technology component arises due to gate-source and gate-drain overlap*** (L_D)

- ***Technology components***:

$$C_{gst} = C_{gdt} = C'_{gs0} W = C'_{gd0} W$$

Gate-Source/Drain Overlap Capacitance per unit width: $C'_{gs0} = C'_{gd0} = C'_{ox} L_D$

- Thus, ***total capacitance in saturation***:

$$C_{gs} = (2/3) C'_{ox} WL + C'_{gs0} W$$

$$C_{gd} = C'_{gd0} W$$

- $\boldsymbol{C_{gs} >> C_{gd}}$

- ***Source-Body and Drain-Body Capacitance*** (C_{sb} and C_{db}):
  - ***Both reverse-biased n^+p junctions***

$$C_{sb} = \frac{C_{sb0}}{\left(1+V_{SB}/V_0\right)^m} \quad \text{and} \quad C_{db} = \frac{C_{db0}}{\left(1+V_{DB}/V_0\right)^m}$$

$$C_{sb0} = C_{sb}\Big|_{V_{SB}=0} \quad \text{and} \quad C_{db0} = C_{db}\Big|_{V_{DB}=0}$$

$$V_{SB} \text{ and } V_{DB} \geq 0$$

- ***Drain/Source Series Resistance*** (R_S and R_D):
  - ***Due to neutral n^+ source/drain regions***