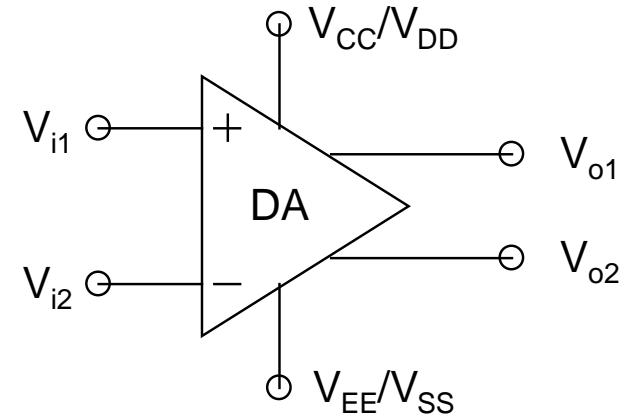


- **Differential Amplifier (DA)/Differential Pair (DP):**

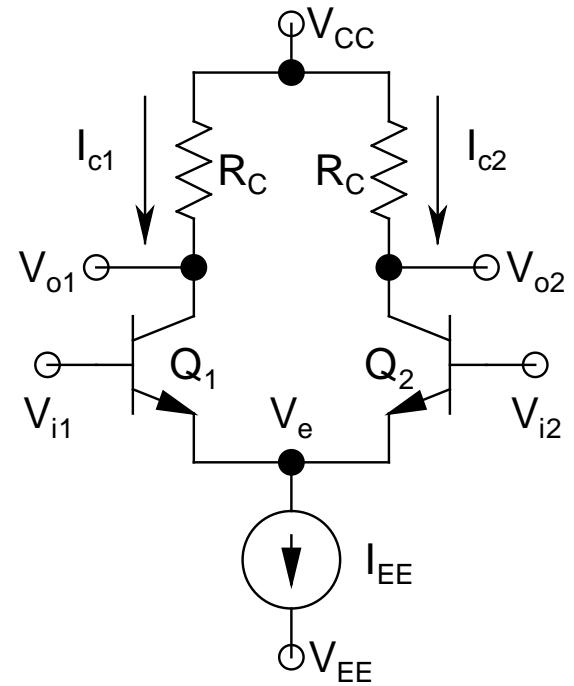
- **Most versatile analog building block**
- **Immensely useful and widely used** (particularly for **sensing/telemetry/instrumentation** applications)
- **Two inputs** (V_{i1}, V_{i2})/**Two outputs** (V_{o1}, V_{o2})
- **Dual Supply** ($V_{CC}/V_{DD}, V_{EE}/V_{SS}$)



Symbol for DA

- ***Unique Property:***
 - *Amplifies the difference between V_{i1} and V_{i2} , while rejecting/suppressing signals common to both V_{i1} and V_{i2}*
 - *Very efficient noise suppressor*
- *The stage can be direct coupled to a similar next stage without the need for any coupling capacitor*
- In *BJT technology*, known as *Emitter-Coupled Pair (ECP)*
- In *MOS technology*, known as *Source-Coupled Pair (SCP)*

- ***npn DA (ECP):***
 - Q_1-Q_2 constitute a a ***matched pair***, and have their ***emitters connected together***, hence, the name
 - I_{EE} : ***DC bias current source***
 - ***All voltages and currents (apart from those used for biasing) are instantaneous (DC + ac)***



npn DA Topology

➤ $V_{be1} = V_{i1} - V_e$, and $V_{be2} = V_{i2} - V_e$

➤ **KVL around Q_1 - Q_2 BE loop:**

$$V_{i1} - V_{be1} + V_{be2} - V_{i2} = 0$$

$$\Rightarrow V_{be1} - V_{be2} = V_{i1} - V_{i2} = V_{id}$$

V_{id} : **Differential-Mode Input Voltage**

➤ **Neglecting Early effect:**

$$V_{id} = V_T \ln(I_{c1}/I_{c2})$$

$$\Rightarrow I_{c1}/I_{c2} = \exp(V_{id}/V_T) \quad (1)$$

➤ **Neglecting base currents:**

$$I_{c1} + I_{c2} = I_{EE} \text{ (*always!*)} \quad (2)$$

This is because I_{EE} is an ideal current source

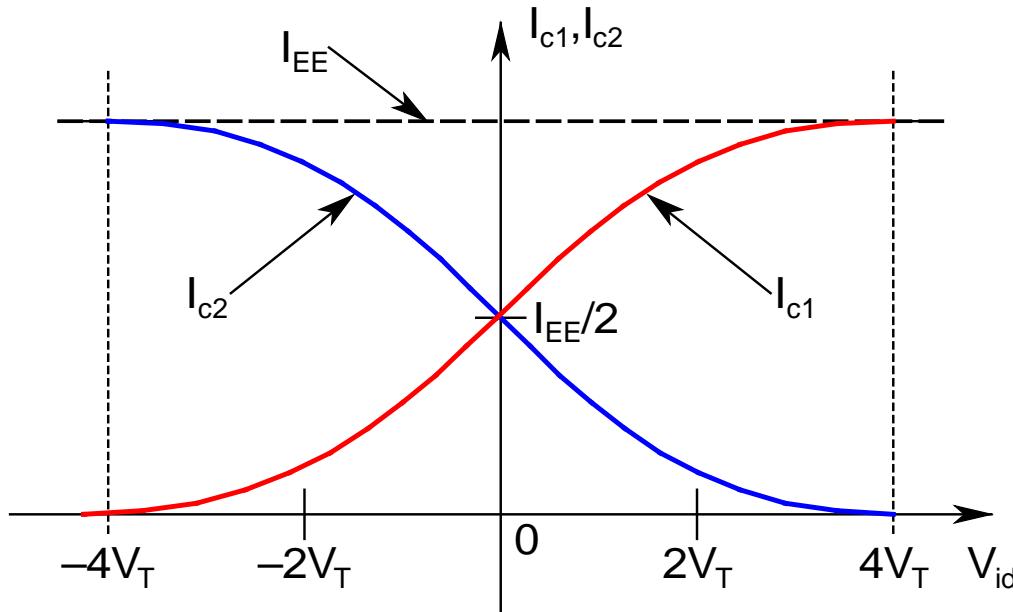
➤ *Solving Eqs.(1) and (2):*

$$I_{c1} = I_{EE}/[1 + \exp(-V_{id}/V_T)]$$

$$I_{c2} = I_{EE}/[1 + \exp(V_{id}/V_T)]$$

➤ *Extremely interesting results:*

- *For $V_{id} = 0$, $I_{c1} = I_{c2} = I_{EE}/2$*
 I_{EE} shared equally between Q_1 and Q_2
- *For positive V_{id} , $I_{c1} \uparrow$ and $I_{c2} \downarrow$*
For negative V_{id} , $I_{c1} \downarrow$ and $I_{c2} \uparrow$
But for both cases, their sum is constant and equal to I_{EE}
- *For $V_{id} > 4V_T$, $I_{c1} \rightarrow I_{EE}$*
For negative V_{id} , with $|V_{id}| > 4V_T$, $I_{c2} \rightarrow I_{EE}$



The Current Transfer Characteristics of an npn DA

- ***Linear Range*** of the circuit $\sim \pm 4V_T$ ($\sim \pm 100$ mV at room temperature)
- This range is known as the ***analog domain***

- For V_{id} out of this range, either Q_1 or Q_2 carries the entire I_{EE} , with the other carrying almost no current \Rightarrow acts as a **Current Switch**
 - This is the *digital domain*
- For analog applications, both devices must be on and in the linear range of the I_c - V_{id} characteristic
- The highest linearity, which is also the region of the highest g_m ($= \partial I_C / \partial V_{ID}$), occurs around $V_{id} = 0$ ($V_{i1} = V_{i2}$)
- This is the most preferred DC bias point

- At this point, $I_{C1} = I_{C2} = I_{EE}/2$, and all small-signal parameters of Q_1 and Q_2 are identical to each other
- This particular biasing scheme leads to a Balanced DA, having properties:
 - Q_1 - Q_2 completely matched
 - R_C s identically equal to each other
 - Both inputs connected to DC ground or to the same DC potential (ground is the best choice, obviously)
 - Both Q_1 and Q_2 biased at $I_{EE}/2$
- We will consider only Balanced DAs

➤ *Unbalanced DAs create anomalies in circuit operation*

➤ Now, the *output voltages*:

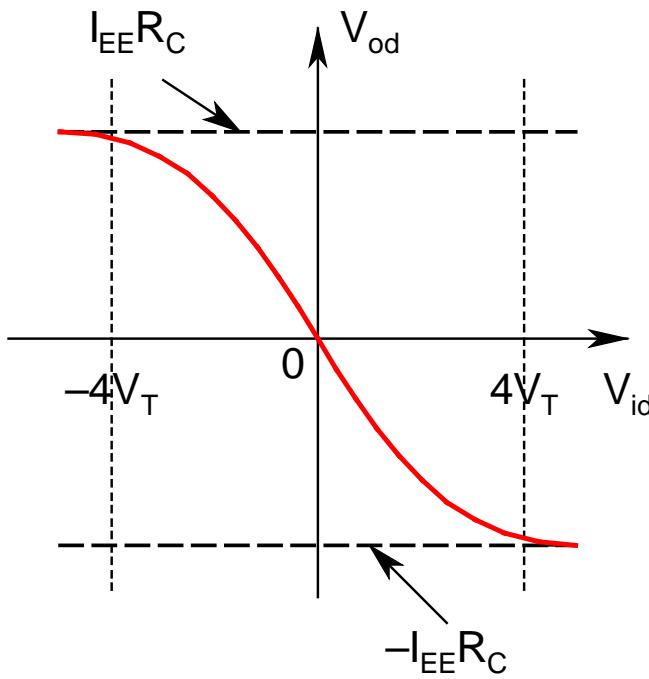
$$V_{o1} = V_{CC} - I_{c1}R_C \text{ and } V_{o2} = V_{CC} - I_{c2}R_C$$

➤ Define *Differential-Mode Output Voltage*:

$$V_{od} = V_{o1} - V_{o2} = I_{EE}R_C \tanh[-V_{id}/(2V_T)]$$

- V_{od} (*positive maximum*) = $I_{EE}R_C$
- V_{od} (*negative minimum*) = $-I_{EE}R_C$
- At $V_{id} = 0$, $V_{od} = 0$

❖ *Permits direct coupling of similar stages without the need of any coupling capacitor*



Linear Range = $\pm 4V_T$
 $(\sim \pm 100 \text{ mV at room temperature})$

The Voltage Transfer Characteristics of an npn DA

➤ ***DC Biasing***:

- $V_i = V_I + v_i$ (V_I : ***DC bias voltage***, v_i : ***ac small-signal voltage***)
- $I_c = I_C + i_c$ (I_C : ***DC bias current***, i_c : ***ac small-signal current***)
- ***The ideal DC bias point should be $V_{I1} = V_{I2}$***
⇒ $I_{C1} = I_{C2} = I_{EE}/2$
- ***Thus, any arbitrary DC voltage can be applied at the bases of Q_1-Q_2 , provided they are same***
⇒ ***Ideal choice: ground***
⇒ ***Necessitates a negative power supply for proper biasing***

- ***Under this condition:***

$$V_{01} = V_{02} = V_{CC} - I_{EE}R_C/2, \text{ and } V_{0d} = 0$$

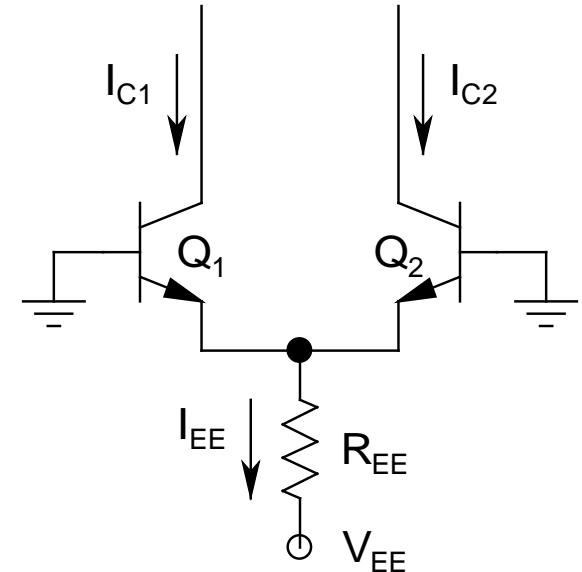
- ***The simplest DC biasing scheme is to attach a resistor R_{EE} from the common emitter point to V_{EE} :***

$$\Rightarrow I_{EE} = (-0.7 - V_{EE})/R_{EE}$$

$$\text{and } I_{C1} = I_{C2} = I_{EE}/2$$

\Rightarrow Both Q_1 and Q_2 have same g_m , r_E , r_π , and r_0

- ***To improve performance, any of the current sources discussed earlier could be used in place of R_{EE}***



- A check is needed to see that Q_1 and Q_2 are biased in the forward active region

- For this circuit, for **best biasing**:

$$V_{CE1} = V_{CE2} = (V_{CC} + |V_{EE}|)/3 \text{ (**3-element o/p branch**)}$$

➤ **ac Analysis:**

- *Balanced DAs have perfect symmetry around the vertical cut-line going through the middle of the circuit*
- *Can be analyzed using heuristics*
 - ❖ Known as the **Half-Circuit Technique**
- *This technique is based on an algorithm*
(Understand it thoroughly to get a clear grasp!)

➤ ***Algorithm for the Half-Circuit Technique:***

- *Apply inputs v_{i1} and v_{i2} at the bases of Q_1 and Q_2 respectively*
- *Outputs v_{o1} and v_{o2} taken from the collectors of Q_1 and Q_2 respectively*
- Define $v_{id} = (v_{i1} - v_{i2})$ as the ***pure differential-mode input***
- Define $v_{ic} = (v_{i1} + v_{i2})/2$ as the ***pure common-mode input***
- Thus:

$$v_{i1} = v_{id}/2 + v_{ic}$$

$$v_{i2} = -v_{id}/2 + v_{ic}$$

- Define $v_{od} = (v_{o1} - v_{o2})$ as the ***pure differential-mode output***
- Define $v_{oc} = (v_{o1} + v_{o2})/2$ as the ***pure common-mode output***
- Thus:

$$v_{o1} = v_{od}/2 + v_{oc}$$

$$v_{o2} = -v_{od}/2 + v_{oc}$$

- *Now, assuming that pure differential-mode and pure common-mode signals are completely non-interacting:*
 - ❖ **Pure differential-mode output can only be caused by a pure differential-mode input**
 - ❖ **Pure common-mode output can only be caused by a pure common-mode input**

- Based on these, define:
 - ❖ **Differential-Mode Gain**: $A_{dm} = v_{od}/v_{id}$
 - ❖ **Common-Mode Gain**: $A_{cm} = v_{oc}/v_{ic}$
- Thus, from the *principle of superposition*:
 - ❖ $v_{o1} = (A_{dm}/2)v_{id} + A_{cm}v_{ic}$
 - ❖ $v_{o2} = - (A_{dm}/2)v_{id} + A_{cm}v_{ic}$
- Thus, *each output carries both differential- and common-mode signals*, however, the *differential-mode signals are out of phase with each other*, whereas the *common-mode ones are in phase*
- *Hence, the difference between the two outputs carries only the differential-mode signal, with a gain double that of a single output*