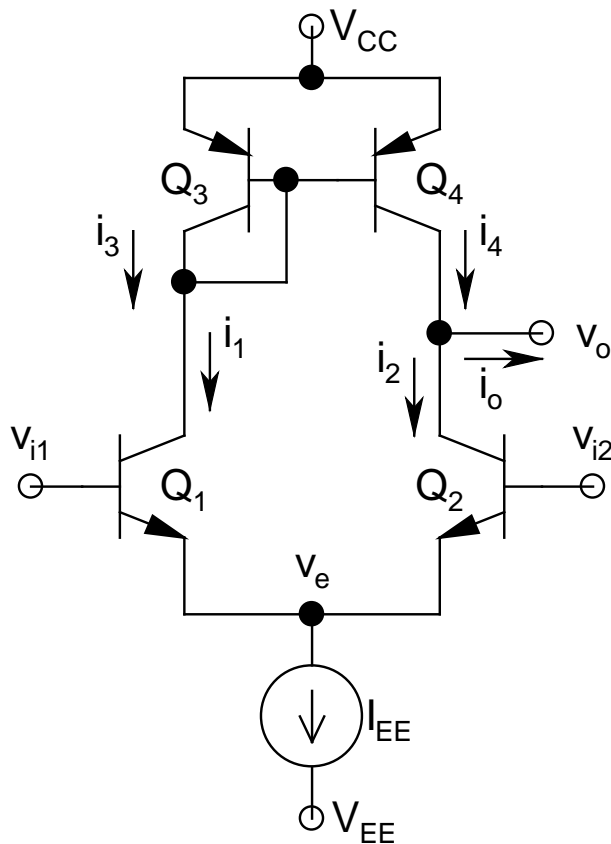
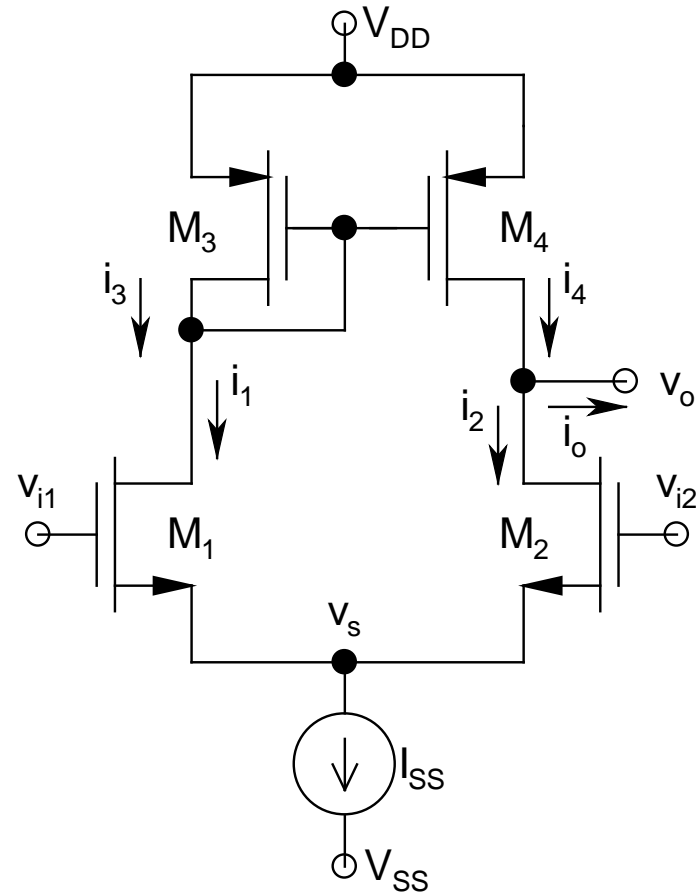


- *Actively Loaded DA:*



BJT Implementation



MOS Implementation

- Absolutely *similar topologies* for *both BJT and MOS implementations*
- *Produces double-ended to single-ended conversion*, i.e., *from two inputs to a single output*
- *Q_1 - Q_2 / M_1 - M_2 / Q_3 - Q_4 / M_3 - M_4 perfectly matched*
- *Output should never be taken from collector/drain of Q_1 / M_1 (Why?)*
- *DC biasing* is *absolutely straightforward* with *all branch currents equal to $I_{EE}/2$ or $I_{SS}/2$*

- **Caution:** *Half-circuit technique can't be used for this circuit*, since *collector/drain circuits of the two sides are coupled*, i.e., $i_{c3} = i_{c4}$ and $i_{d3} = i_{d4}$ (*always*)
- This circuit can be *analyzed by inspection*
- **Define** $v_{id} = v_{i1} - v_{i2}$
- *Apply $+v_{id}/2$ at the base of Q_1 /gate of M_1*
- *Apply $-v_{id}/2$ at the base of Q_2 /gate of M_2*
- From **symmetry** of the circuit *around the BE/GS loops*, the *common emitter/source node* is at **ac ground** (i.e., $v_e = v_s = 0$)

- Since $v_s = 0$, M_1 - M_2 won't have any body effect issue
- Now, $i_3 = i_4$ (*mirror*), $i_3 = i_1$ (*same branch*), and $i_2 = -i_1$ (*symmetry*)
- Also, $i_1 = g_m v_{id}/2$ and $i_2 = -g_m v_{id}/2$
 $g_m = I_{EE}/(2V_T)$ (*BJT Implementation*)
 $= (k_N I_{SS})^{1/2}$ (*MOS Implementation*)
- Hence, the *short-circuit output current* (with the *output terminal shorted to ground*):
 $i_o = i_4 - i_2 = i_1 - i_2 = 2i_1 = g_m v_{id}$

- To find the **output voltage**, we need to use the **Thevenin technique**:
 - **Open-Circuit Voltage** = **Short-Circuit Current** \times **Thevenin Resistance**
- **Thevenin Resistance** (**looking from the output**):

$$R_o = r_{o2} // r_{o4}$$
- Thus, the **output voltage**:

$$v_o = i_o R_o = g_m (r_{o2} // r_{o4}) v_{id}$$
- Hence, the **differential-mode gain**:

$$A_{dm} = v_o / v_{id} = +g_m (r_{o2} // r_{o4})$$
- **$R_i = 2r_{\pi}$** (**BJT Implementation**)

➤ *Ex.:* Prove the expressions for A_{dm} and R_i from the hybrid- π model

➤ A_{cm} for this circuit is a little difficult to evaluate

➤ However, the *CMRR can be safely approximated as:*

$$CMRR \approx 20 \log_{10} (2g_m R_{EE})$$

R_{EE} : Output resistance of the bias current source I_{EE}/I_{SS}

➤ In order to *improve CMRR*, various *current source topologies* can be used

- *Example: Simple npn CM*

- *One of the simpler choices*

- *Q_5 - Q_6 perfectly matched*

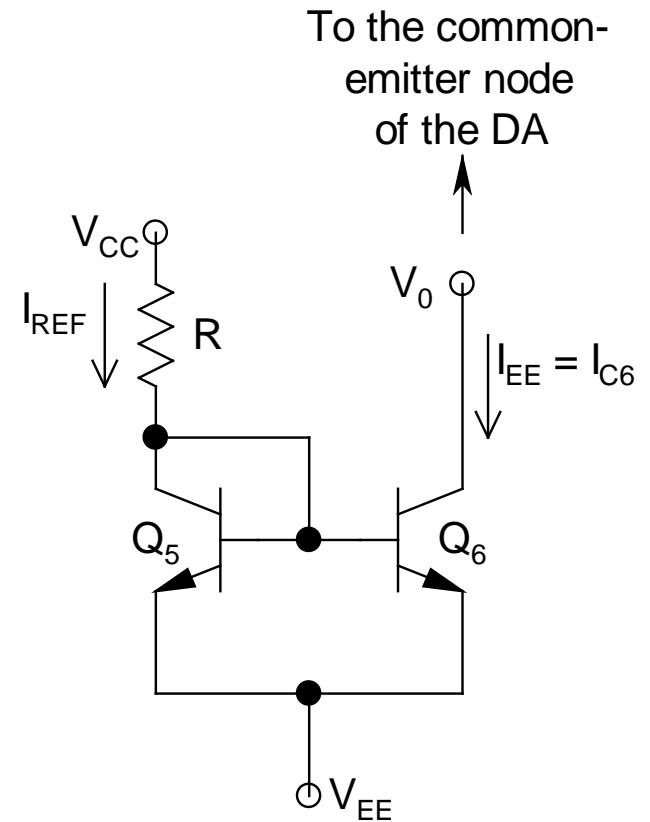
- *Neglecting base currents:*

$$I_{REF} = I_{EE} = I_{C6}$$

$$= (V_{CC} - V_{BE} - V_{EE})/R$$

- $R_{EE} = r_{06} = V_A/I_{EE}$

- Acts as a *current source* of *magnitude I_{EE}* with a shunt *resistance R_{EE}*



- *Insights:*

- *Recall: A_{dm} independent of R_{EE} , but A_{cm} and CMRR strongly depend on R_{EE}*
- *To maximize CMRR, R_{EE} should be increased as much as possible*
- *To increase R_{EE} , other current sources discussed in class, e.g., *ratioed mirror*, *cascode*, *Widlar*, etc., can be used*
- *Note that with more advanced architectures, $V_o(min)$ increases, and may become a limiting factor!*

OUTPUT STAGES

- **Main Purpose:**
 - *To drive load with sufficient current*
- Both **BJT** and **MOS** output stages available
- **BJT** output stages preferred due to their *large current handling capability*
- **BiMOS** circuits use **MOS** devices in the *core* of the circuit, while using **BJT** devices in the *output* stage
 - *Best of both worlds!*

- **Requirements:**
 - *Sufficient drive current/power transfer to load*
 - *Low output distortion*
 - *Ideal voltage source:*
 - *Thevenin equivalent: V_o with $R_o \rightarrow 0$*
 - *Voltage gain A_v independent of load*
 - *Ideally unity with no phase shift*
 - *Low Standby (or Idling) Power*
 - *While not driving any load*
 - *Should not degrade frequency response*

➤ *High power conversion efficiency η*

▪ $\eta = (\text{average power delivered to load}) / (\text{average power drawn from supply})$

• *Classification:*

➤ *Depends on the conduction angle (θ)*

▪ θ : Angle over the complete cycle (360°) for which either both or one of the output transistors are/is on

➤ *Class A:*

▪ $\theta = 360^\circ$ and $\eta_{max} = 25\%$ (*large standby power*)

➤ *Class B:*

▪ θ slightly less than 180° and $\eta_{max} = 78.5\%$ (*zero standby power*)

- **Class AB:**
 - $\theta = 180^\circ$ and $\eta_{max} \approx 78.5\%$ (*very small standby power*)
- **Class C:**
 - $\theta \ll 180^\circ$ (*used in RF applications*)
- There are *other classes* also, namely **D**, **E**, **F**, **G**, and **H**
 - Used only in *special cases*, e.g., *pulse width modulated input*, *lowering of distortion*, etc.
- In this course, we shall be discussing only about **Class B** and **Class AB** output stages

- **Class B:**

- Uses **complementary** set of output transistors (**n_{pn} and p_{np}**, **NMOS and PMOS**)
- One takes care of the **positive half cycle**, while the other takes care of the **negative half cycle**
- **θ slightly less than 180° for each**
- **Both output devices never on simultaneously**
 - **Zero standby power (significant advantage)**
- Also known as **Push-Pull Stage**

- During *positive half cycle*, the stage *pushes current through load*
- During *negative half cycle*, the stage *pulls current away from load*
- *Very high η_{max} of 78.5%*
- However, there is a *very big limitation*, known as *Crossover Distortion*
 - Also known as *Deadband Distortion*
 - *Occurs during zero crossings of the signal*
 - *For BJT/MOS Class B stage*, the *input voltage must at least equal V_γ ($\sim 0.6\text{ V}$)/ V_{TN} ($|V_{TP}|$) ($\sim 0.6\text{-}0.9\text{ V}$)* for the *output stage transistors to turn on*

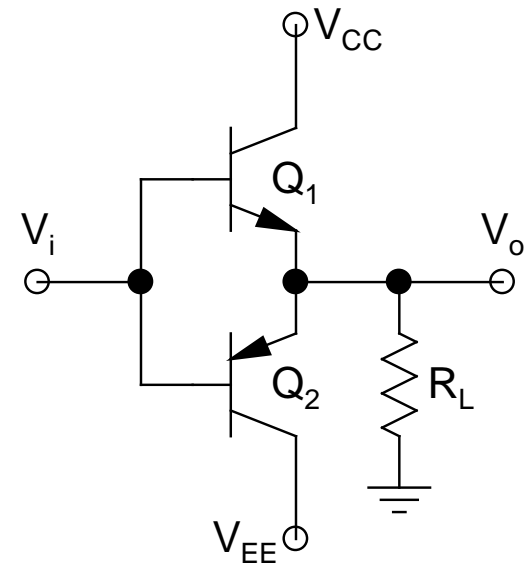
- *Class AB:*

- *Eliminates Crossover Distortion* by *prebiasing the output transistors*
 - *They remain at the verge of conduction in the standby stage*
- *θ exactly equal to 180°*
- *η_{max} slightly less than 78.5% due to a small amount of standby power*
- *Extremely popular and most widely used*

- ***Class B Push-Pull Output Stage:***

- BJT Implementation:***

- Also known as ***Complementary Output Stage***
- ***Uses dual symmetric power supplies***
- ***Typical values used:***
 $\pm 3\text{ V}$, $\pm 5\text{ V}$, $\pm 12\text{ V}$, $\pm 15\text{ V}$
- ***Q-point: $V_i = V_o = 0$***
 $\Rightarrow V_{be1} = V_{eb2} = 0$



Circuit Schematic