EE-380 EC Lab-05
Extraction of MOSFET Model parameters and Design/Characterization of NMOS Amplifiers

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Section: C

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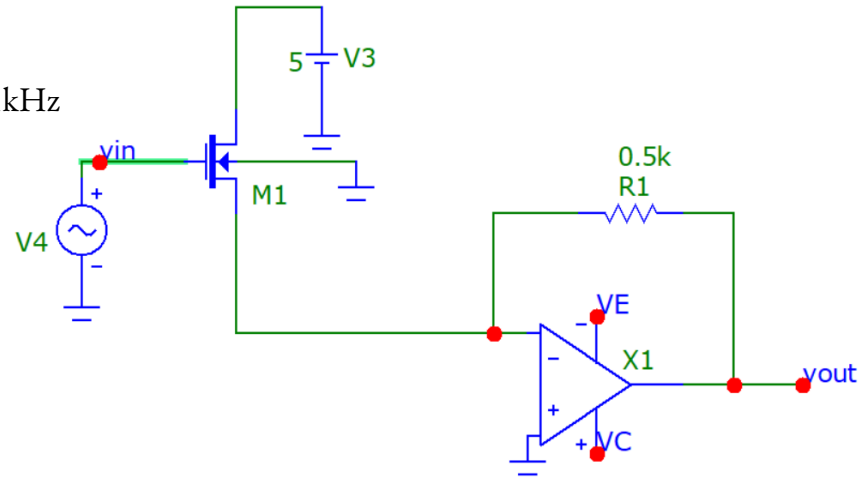
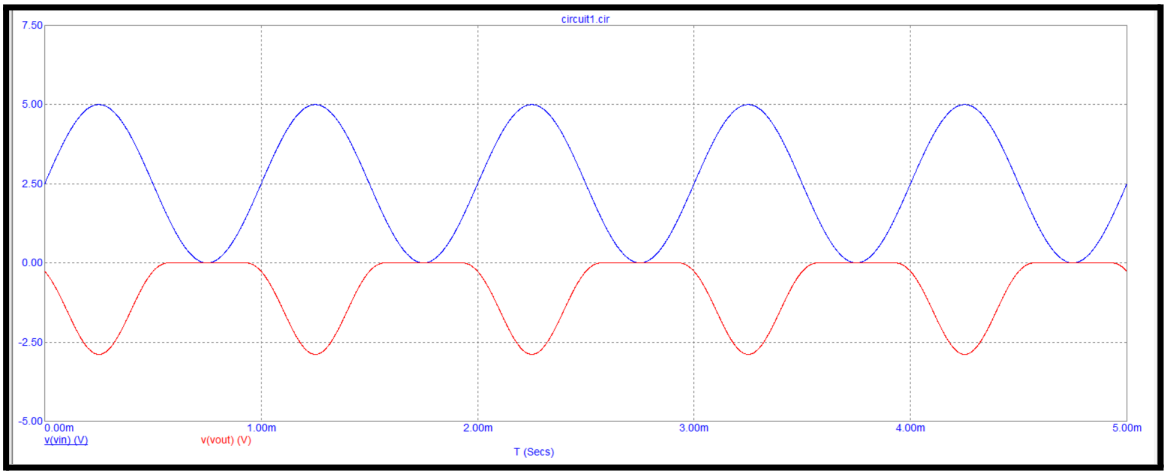
1 Measurement of NMOS Transfer Characteristics

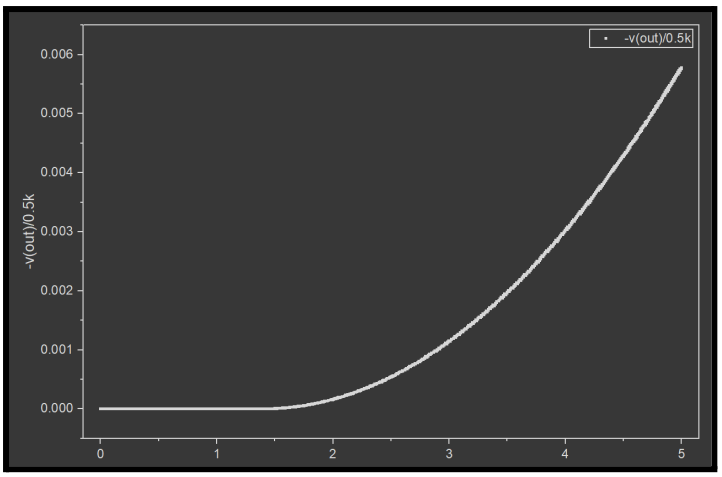
1.1 Pre Lab

Input : 2.5+2.5sin(2πft) V ; f=1kHz

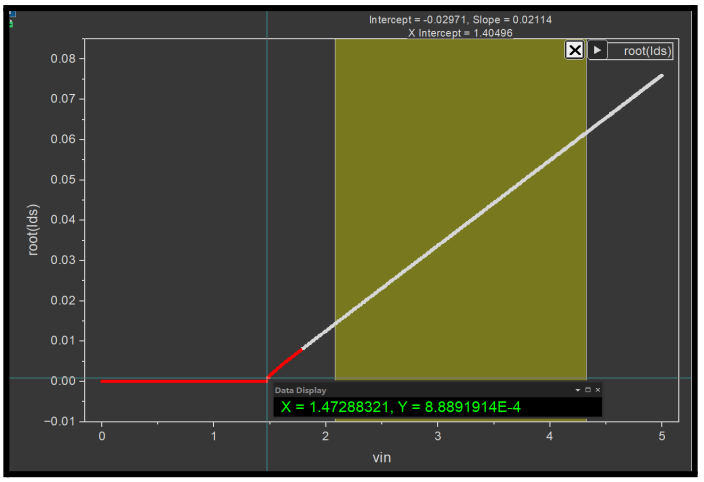


Input / output wave forms





$\mathbf{I_{DS}}$ **vs** $\mathbf{V_{in}}$



$\sqrt{(\mathbf{I_{DS}})}$**vs** $\mathbf{V_{in}}$

$$equation\ of\ the\ line\ is\ \sqrt{I_{DS}} = 0.02114V_{in} - 0.02971$$

$$and\ we\ know\ that\ in\ saturation\ ,\ I_{DS} = \beta_N \frac{(V_{GS}-V_{TN})^2}{2}$$

$$\Rightarrow \sqrt{I_{DS}} = \sqrt{\frac{\beta_N}{2}}(V_{in} - V_{TN}) \qquad since\ V_{GS} = V_{in}$$

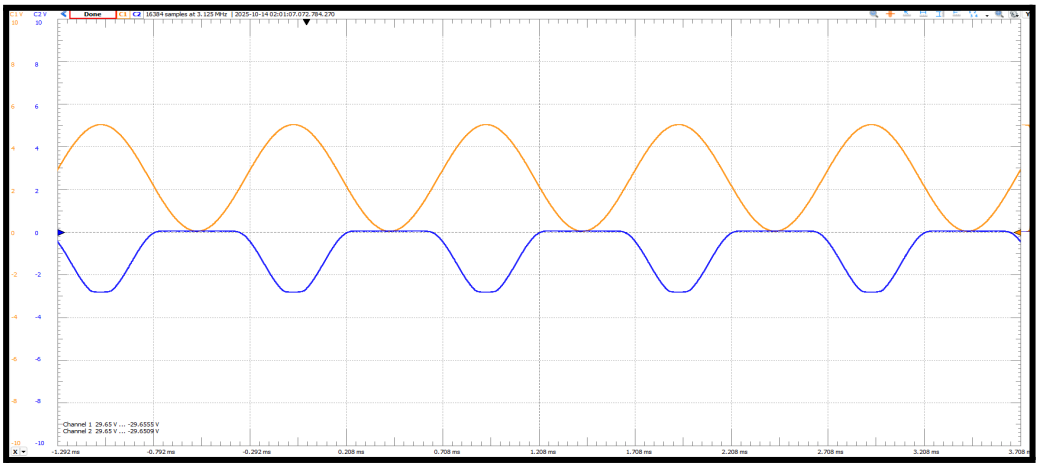
$$so,\ on\ comparing\ with\ the\ obtained\ equation\ of\ line,\ we\ get:$$

$$\sqrt{\frac{\beta_N}{2}} = 0.02114\ \ and\ \sqrt{\frac{\beta_N}{2}}V_{TN} = 0.02971$$

$$\Rightarrow \beta_N \simeq 8.93 * 10^{-4}\ V^{-1}\Omega^{-1}\ and\ V_{TN} \simeq 1.40V$$

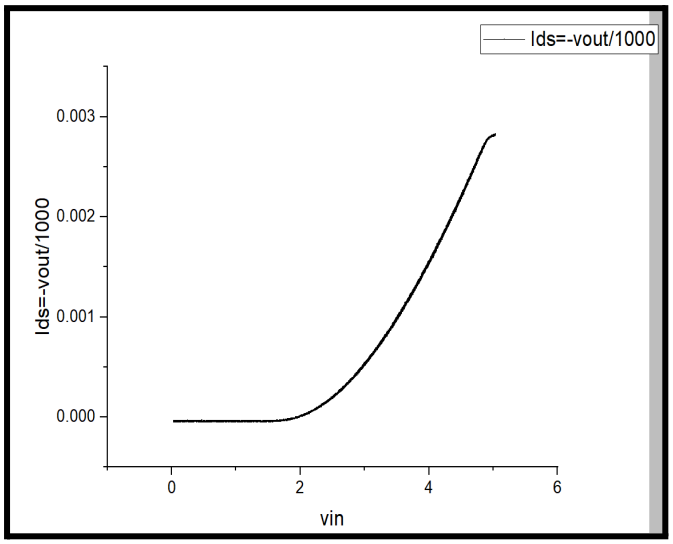
1.2 In Lab

Input / output wave forms:

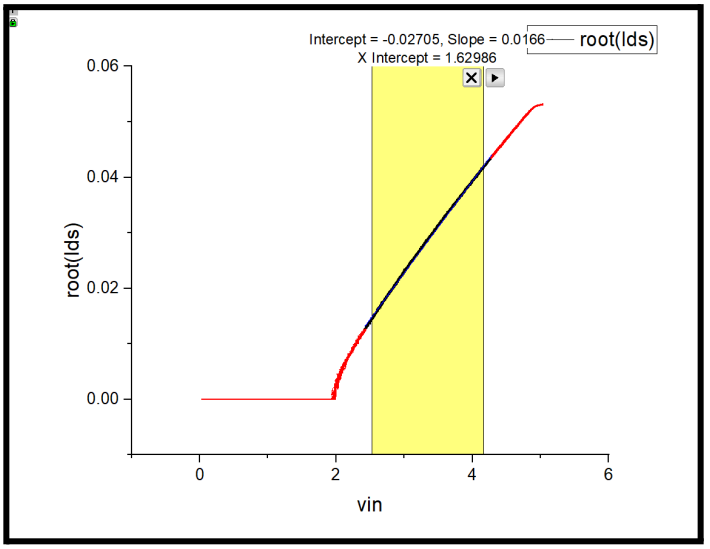


1.3 Post Lab

The data was analysed using *origin* and the following results were obtained



I_{DS} vs V_{in}



√(I_{DS})vs V_{in}

$equation\ of\ the\ line\ is\ \sqrt{I_{DS}} = 0.0166V_{in} - 0.02705$

$and\ we\ know\ that\ in\ saturation\ ,\ I_{DS} = \beta_N \frac{(V_{GS}-V_{TN})^2}{2}$

$\Rightarrow \sqrt{I_{DS}} = \sqrt{\frac{\beta_N}{2}}(V_{in} - V_{TN}) \qquad since\ V_{GS} = V_{in}$

$so,\ on\ comparing\ with\ the\ obtained\ equation\ of\ line,\ we\ get:$

$\sqrt{\frac{\beta_N}{2}} = 0.0166\ and\ \sqrt{\frac{\beta_N}{2}}V_{TN} = 0.02705$

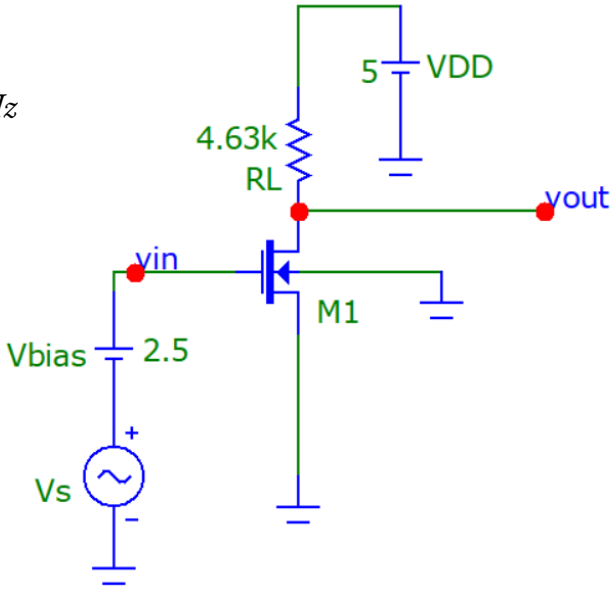
$\Rightarrow \beta_N \simeq 5.51 * 10^{-4}\ V^{-1}\Omega^{-1} and\ V_{TN} \simeq 1.63V$

These obtained parameters will be used for further calculations.

2 CS Amplifier with Resistive Load

2.1 Pre Lab

Input : 2.5V+$50sin(2\pi ft)mV$; f=1kHz

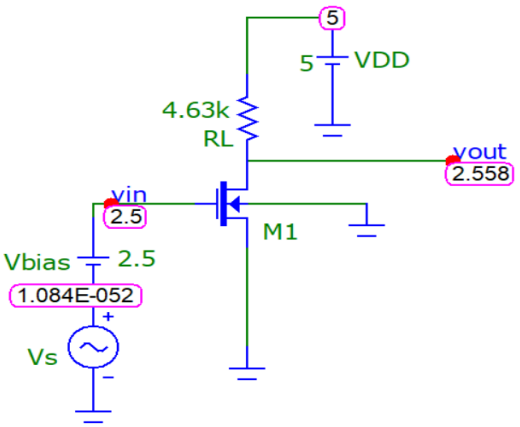


Since, here the transistor operates in saturation region and if V_{DS}=2.5V then

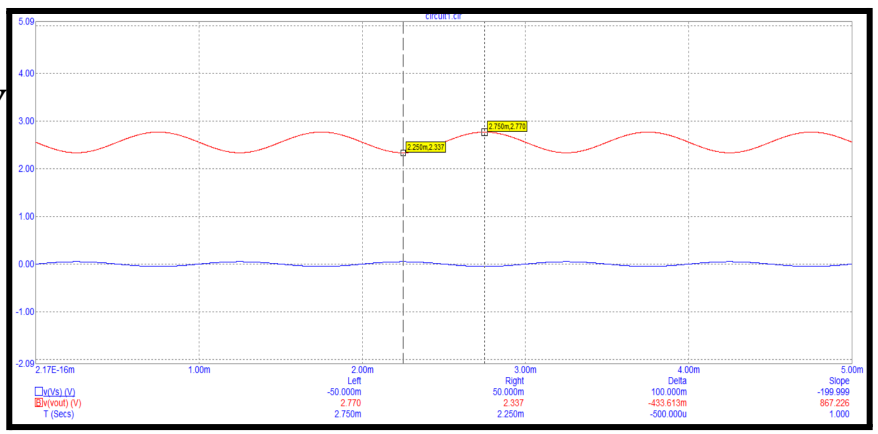
$I_{DS} = \frac{2.5}{R_L}$, *and also* $I_{DS} = \beta_N \frac{(V_{bias} - V_{TN})^2}{2}$. *Now, putting the values we obtained in part* 1

we get, $I_{DS} = 0.54mA$, *so* $R_L = \frac{2.5}{0.54} k\Omega \Rightarrow R_L \simeq 4.63k\Omega$

I. DC analysis:
Bias point (V_{DS} , I_{DS}) is
(2.558V , 0.527mA)

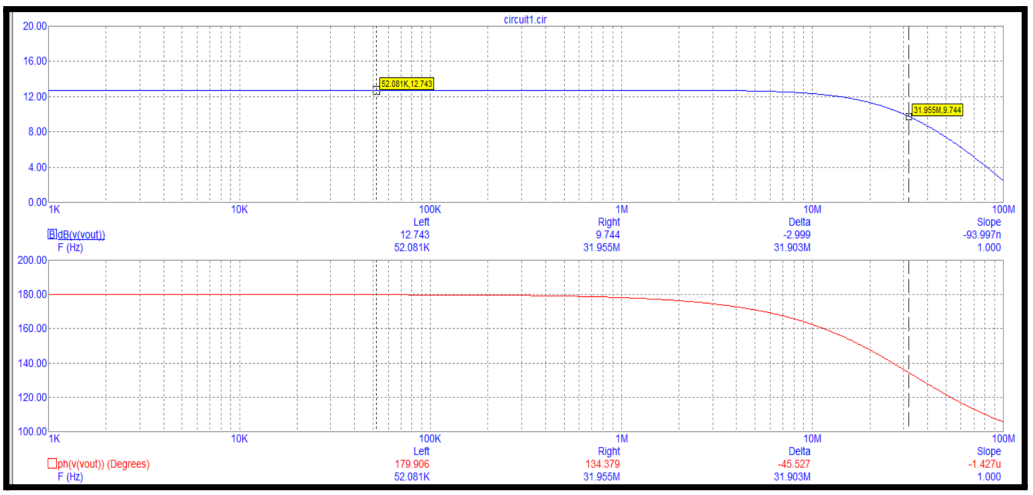


II. Voltage Gain:
$A_{out} = \frac{2.77 - 2.337}{2} = 0.2165V$
And $A_{in} = 50mV$ *or* $0.05V$
so , Gain = 4.33

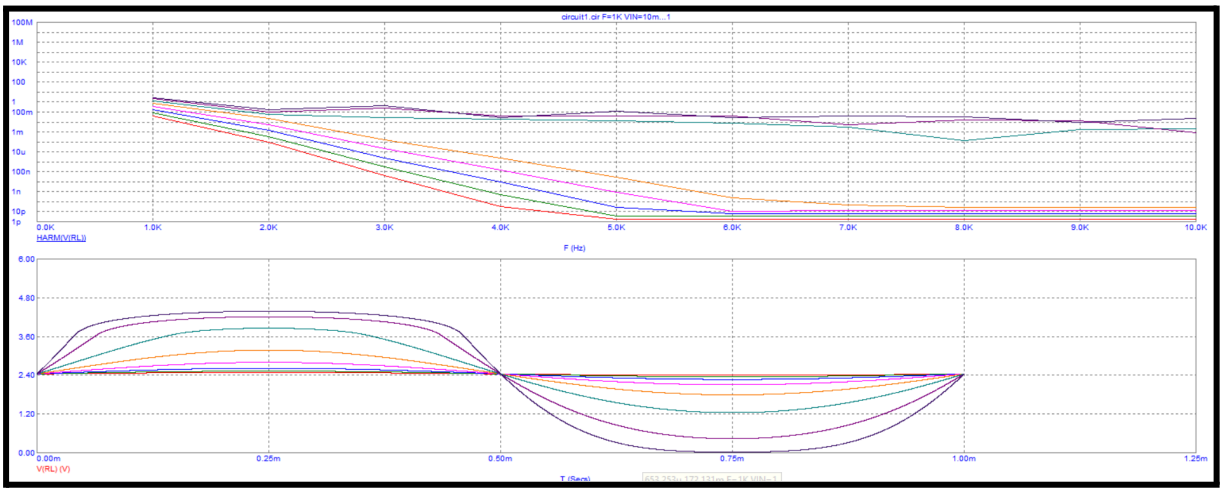


III. Frequency response

f_{3dB} = 31.95MHz



IV. Output voltage swing and distortions



The upper plot (HARM(V(RL)) vs Frequency) shows the harmonic content of the output. The fundamental component dominates, while higher-order harmonics (2nd, 3rd, etc.) appear at lower frequencies and decrease with frequency, reflecting reduced distortion at higher frequencies.

The lower plot (V(RL) vs Time) illustrates how the output waveform changes with increasing input amplitude. For small signals, the output is clean and sinusoidal, but as the amplitude increases, the waveform begins to flatten at the peaks, and we get a distorted output.

2.2 In Lab

The transistor operates in saturation region here, and if V_{DS}=2.5V then

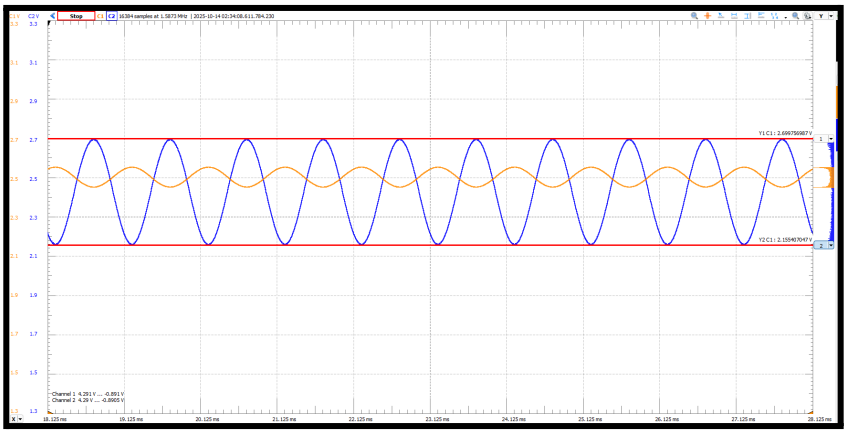
$I_{DS} = \frac{2.5}{R_L}$, *and also* $I_{DS} = \beta_N \frac{(V_{bias} - V_{TN})^2}{2}$. *Now, putting the values we obtained in part* 1

we get, $I_{DS} = 0.21mA$, *so* $R_L = \frac{2.5}{0.21} k\Omega \Rightarrow R_L \simeq 11.9k\Omega$

But a resistor of $10k\Omega$ seems to work the best, these 1st order calculations just gave us an estimate and our estimate was indeed close to what we saw in the lab. So, $R_L \simeq 10k\Omega$

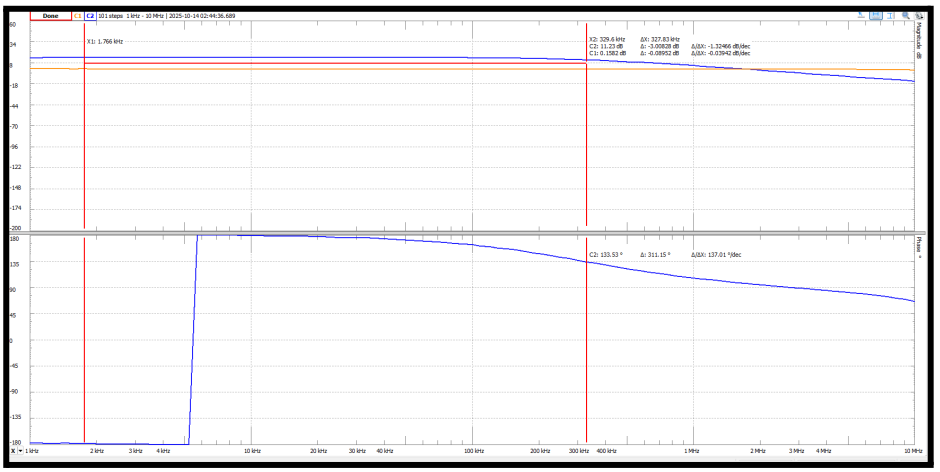
I. DC analysis:
Bias point (V_{DS} , I_{DS}) is
(2.43V , 0.257mA)

II. Voltage Gain:
$A_{out} = \frac{2.70 - 2.155}{2} = 0.2725V$
And $A_{in} = 50mV$ *or* $0.05V$
so , Gain = 5.45



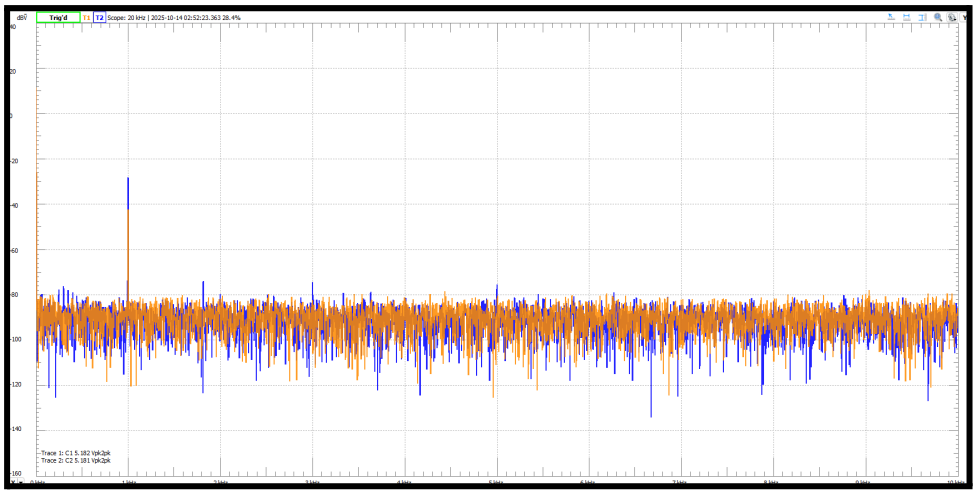
III. Frequency response

f_{3dB} = 329.6kHz

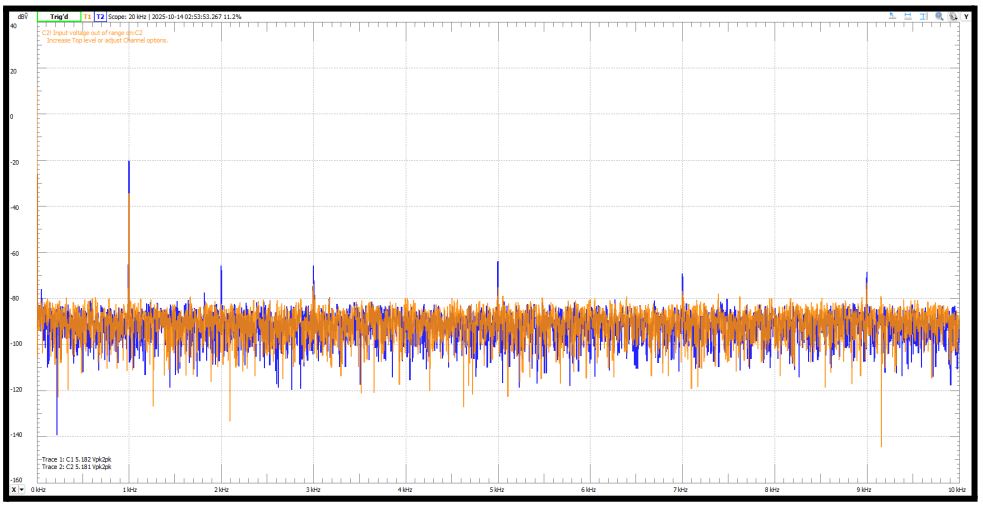


IV. Studying Output Voltage Swings and Distortions

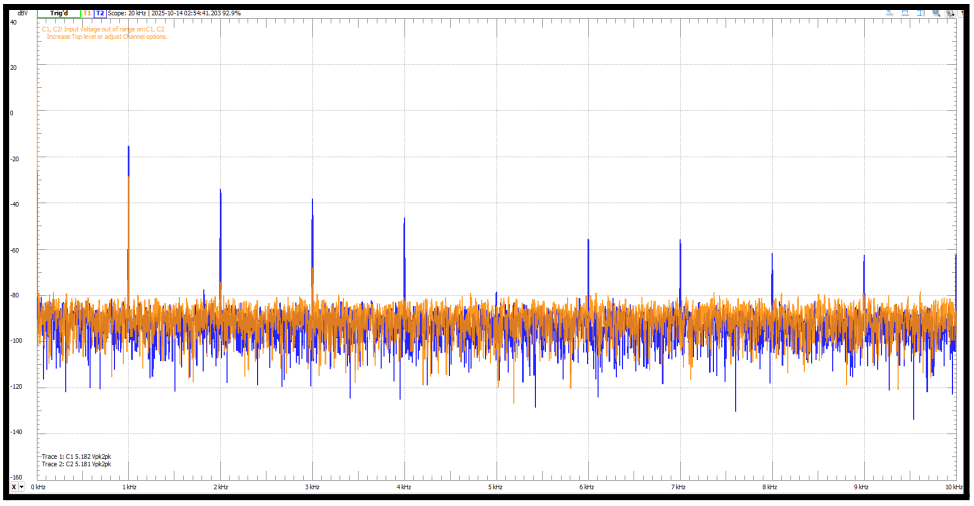
Input amplitude : 10mV



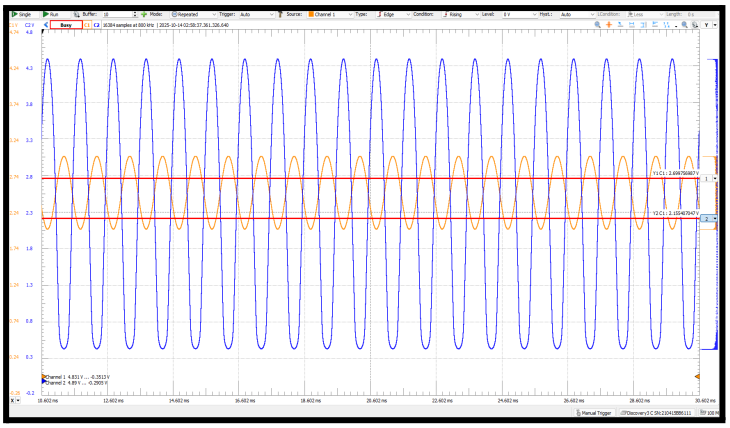
Input amplitude : 25mV

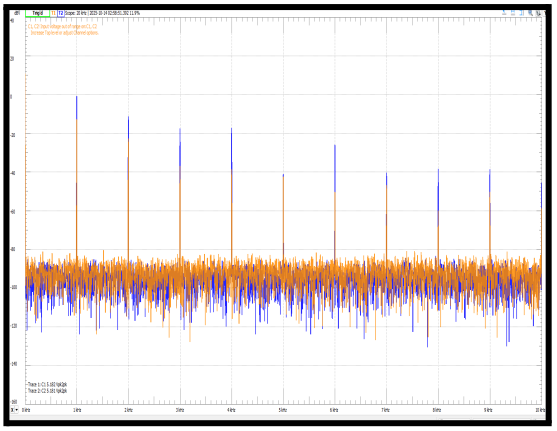


Input amplitude : 50mv

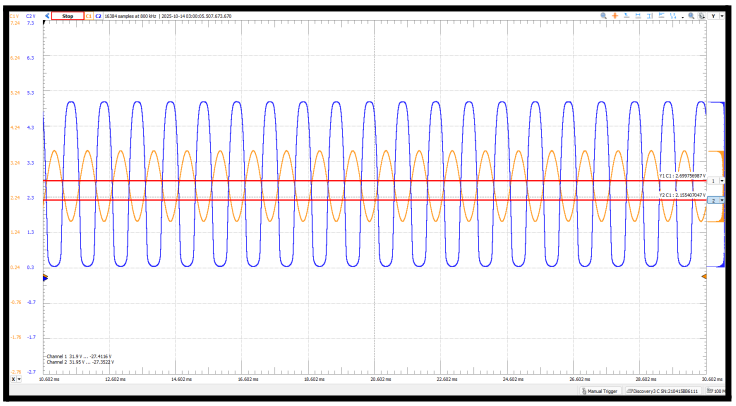


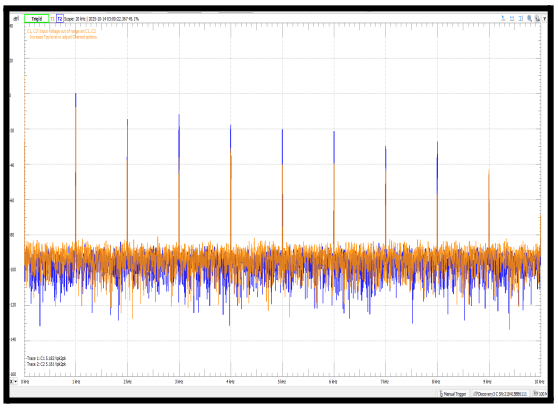
Input amplitude : 500mV





Input amplitude : 1V



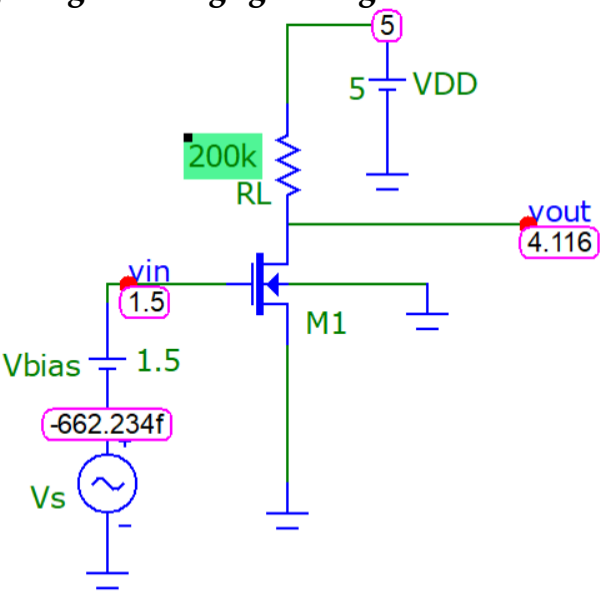


2.3 Post Lab

As the input amplitude increases the distortions become more and more significant and are easily observable in the waveforms too. The maximum voltage swing we were able to achieve was around 4.65V, that we got when the i/p was 1S sine wave, so the gain reduced to just 2.3 times in this case.

3 Modify the Design to give Voltage gain larger than 15

Input signal: +-50mv



3.1 Pre Lab

Choose R_L = 200k and V_{Bias}=1.5V

I. DC analysis:

Bias point (V_{DS} , I_{DS}) is

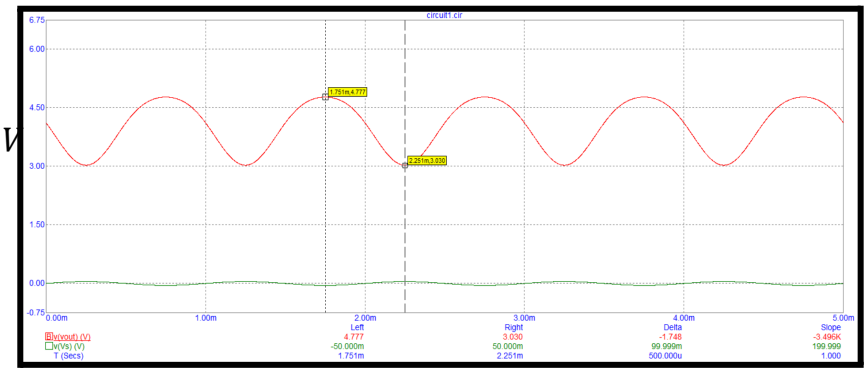
(4.116V , 0.004mA)

II. Voltage Gain:

$A_{out} = \frac{4.777-3.030}{2} = 0.8735V$

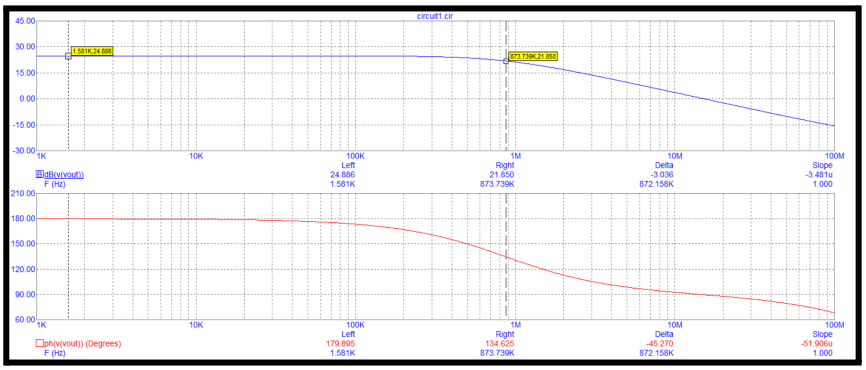
And $A_{in} = 50mV \; or \; 0.05V$

so , Gain = 17.47

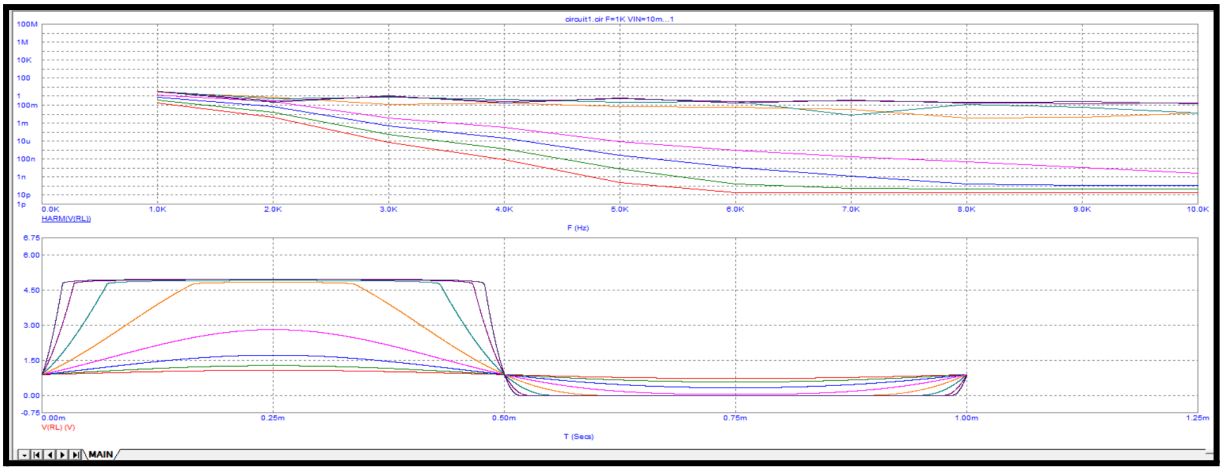


III. Frequency response:

f_{3dB} = 873.739kHz



IV. Output voltage swing and distortions:



Same inference can be drawn from this plot too as done in part 2, but here the distortion starts for a relatively smaller input.

3.2 In Lab

We Chose $R_L = 510k\Omega$ and V_{Bias}=1.65V

I. DC analysis:

Bias point (V_{DS} , I_{DS}) is

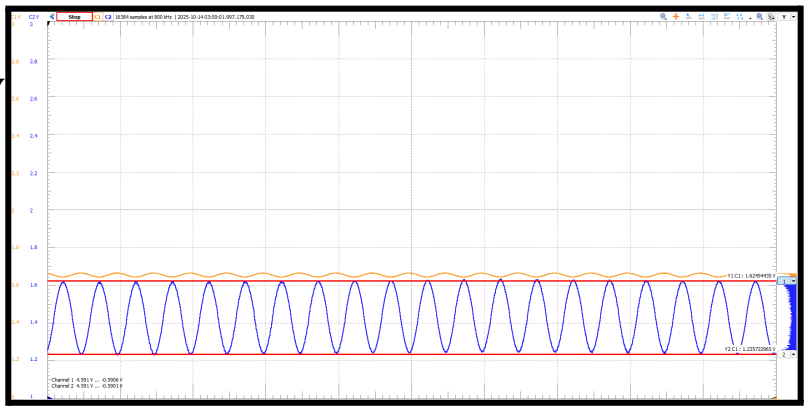
(1.418V , 0.0069mA)

II. Voltage Gain:

$$A_{out} = \frac{1.6245-1.2357}{2} = 0.1944V$$

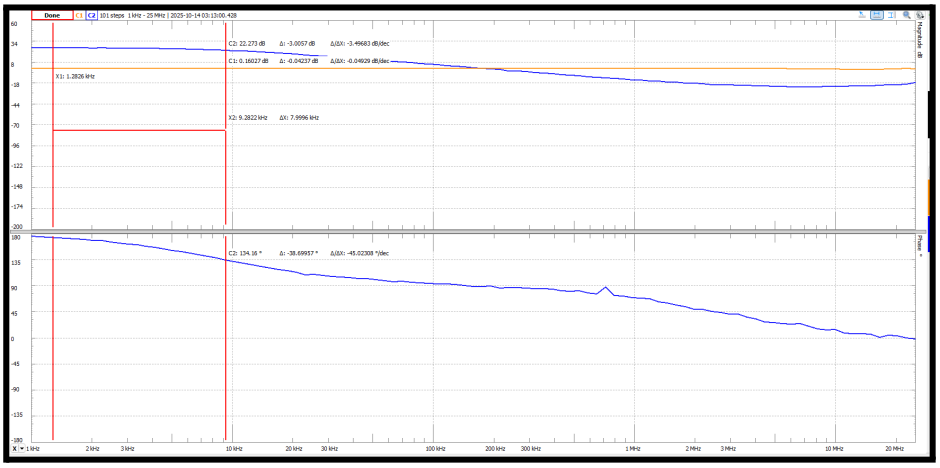
And $A_{in} = 10mV \; or \; 0.01V$

so , Gain = 19.44



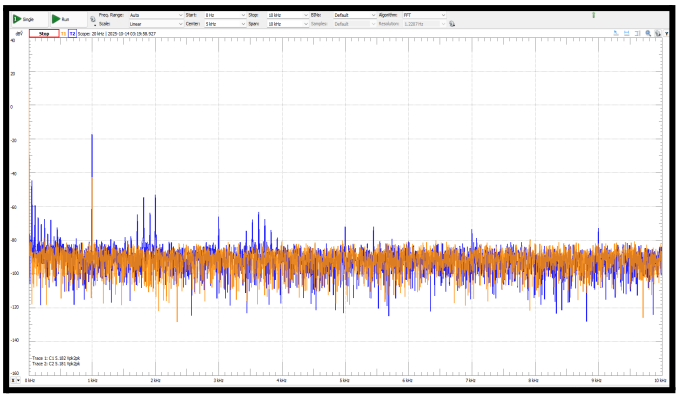
III. Frequency response:

f_{3dB} = 9.28kHz

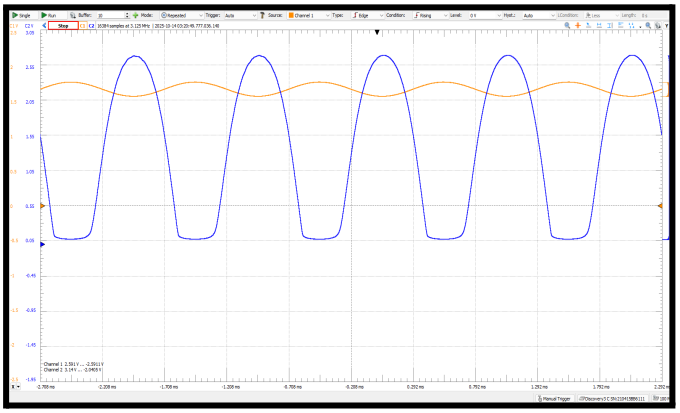


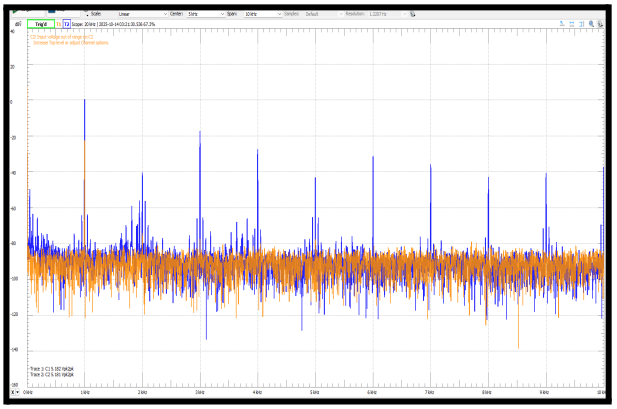
IV. Studying Output Voltage Swings and Distortions

Input amplitude : 10mV

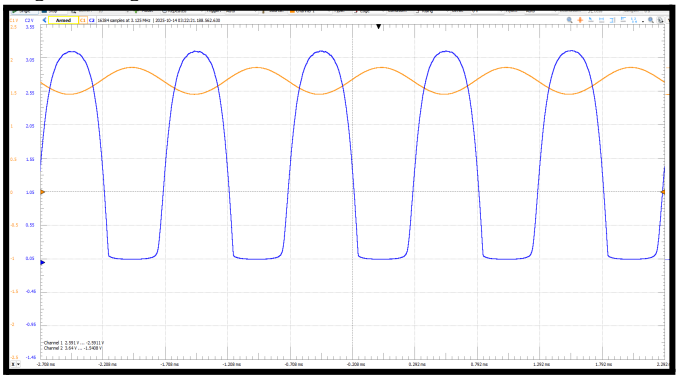


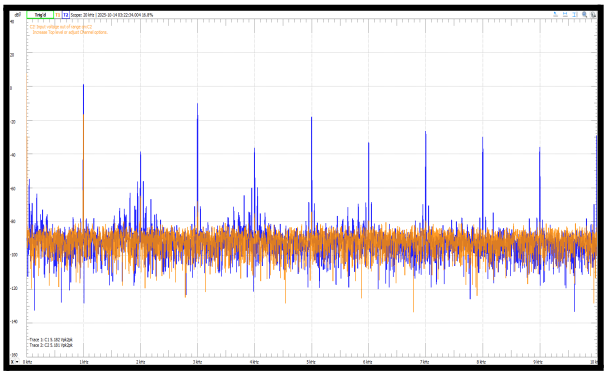
Input amplitude : 100mV





Input amplitude : 200mV



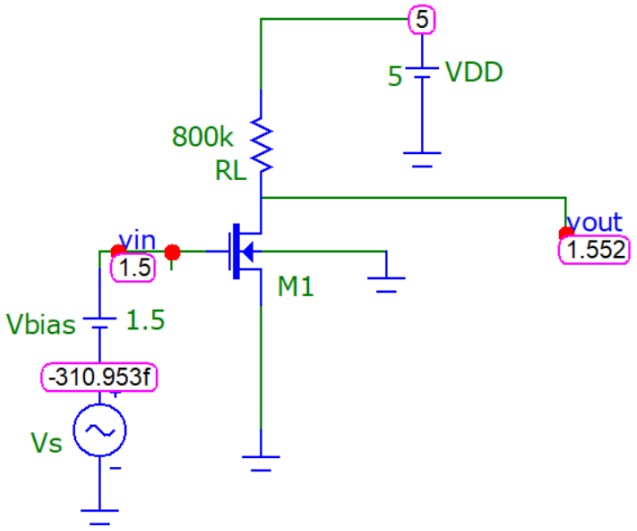


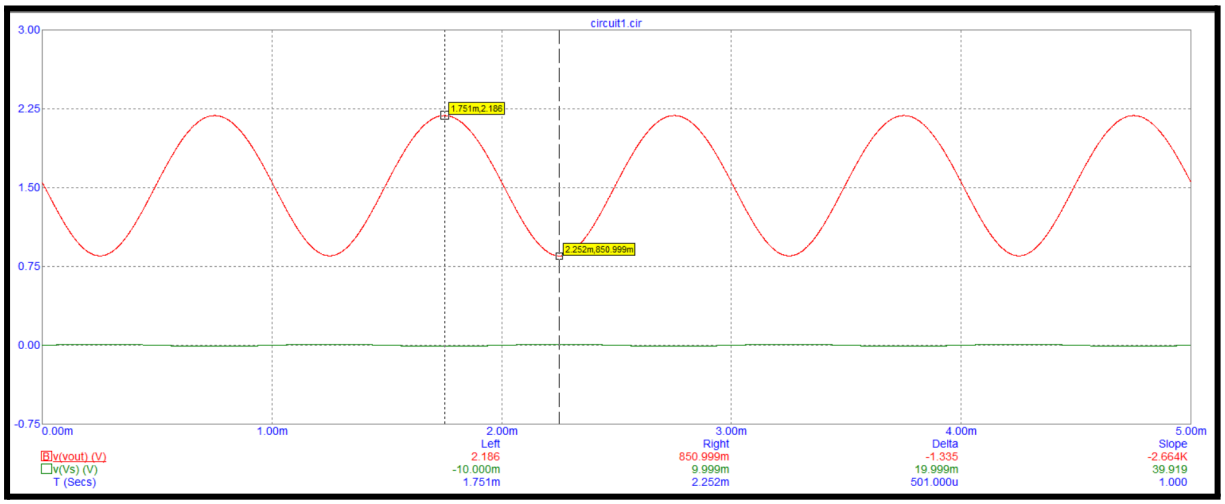
3.3 Post Lab

Increasing the gain comes at a cost – bandwidth! We lost our bandwidth significantly here. Also the distortion can be seen for relatively smaller inputs here.

4 Design to maximize Voltage Gain

4.1 Pre Lab





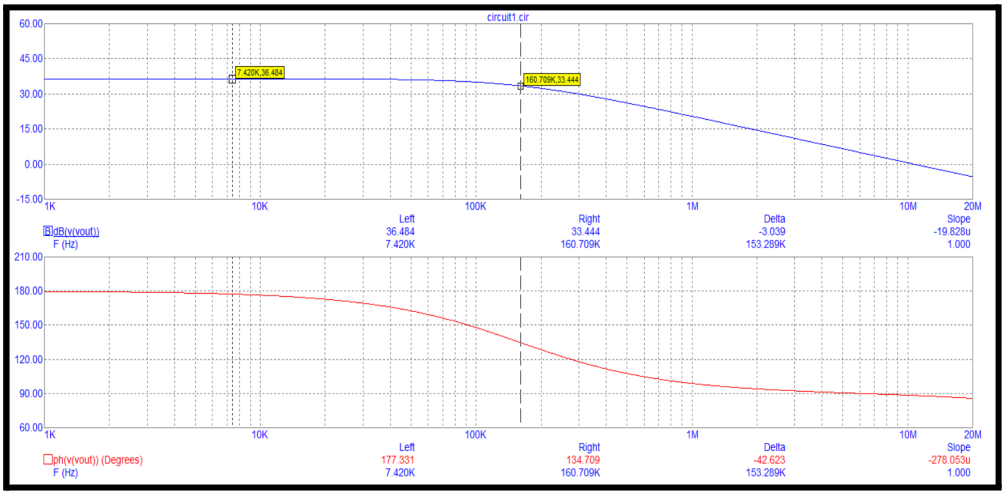
$A_{out} = \frac{2.186-0.851}{2} = 0.6675V$

And $A_{in} = 10mV \; or \; 0.01V$

so , Gain = 66.75

Frequency Response:

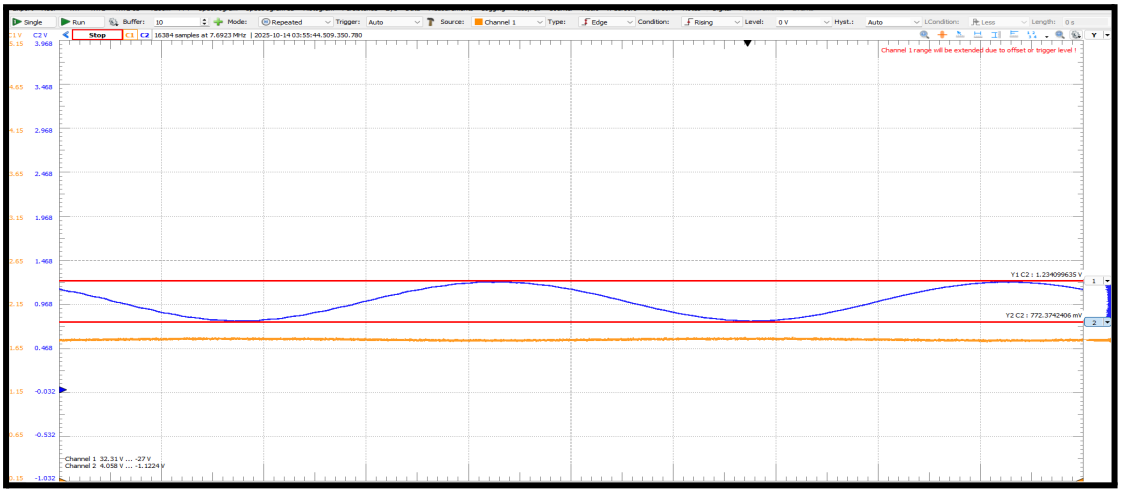
f_{3dB} = 160.7KHz



4.2 In Lab

We Chose $R_L = 390k\Omega$ and $V_{Bias}=1.7V$

Input - output waveforms:



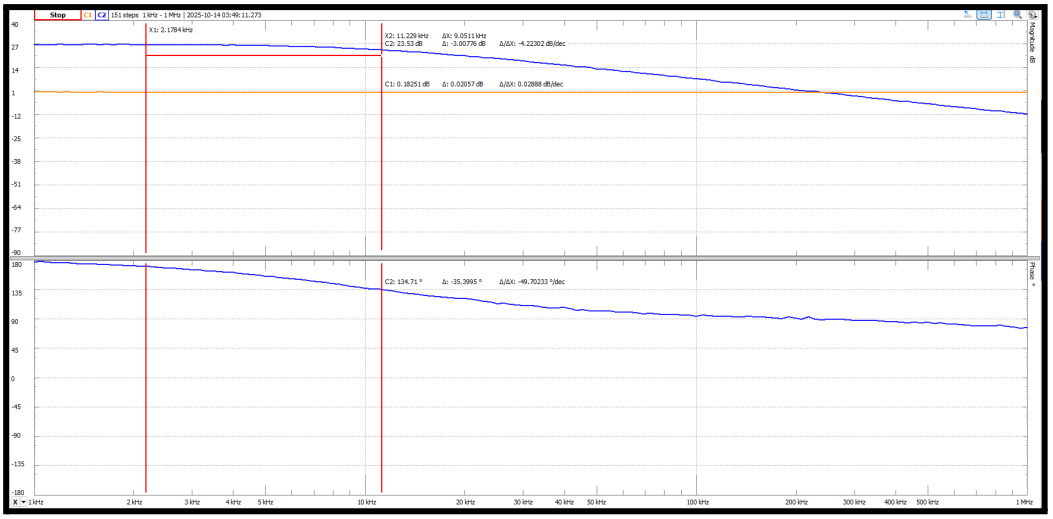
$$A_{out} = \frac{1.234-0.772}{2} = 0.231V$$

And $A_{in} = 10mV \; or \; 0.01V$

so , Gain = 23.1

Frequency Response:

f_{3dB} = 11.23KHz



4.3 Post Lab

After experimenting with various combinations of increasing R_L and minimising I_{DS} we achieved a maximum gain of 23.1 .

5 (Bonus) Explore two stage design for higher Gain

5.1 Pre Lab

Stage M_1 (input stage) :

Provides voltage gain and amplifies the small input signal, but the trade off is of bandwidth. The amplifier designed in part 4 can be directly used here, as the VDS is at 1.5V, more than V_{TN}.

Stage M_2 (Output Stage) :

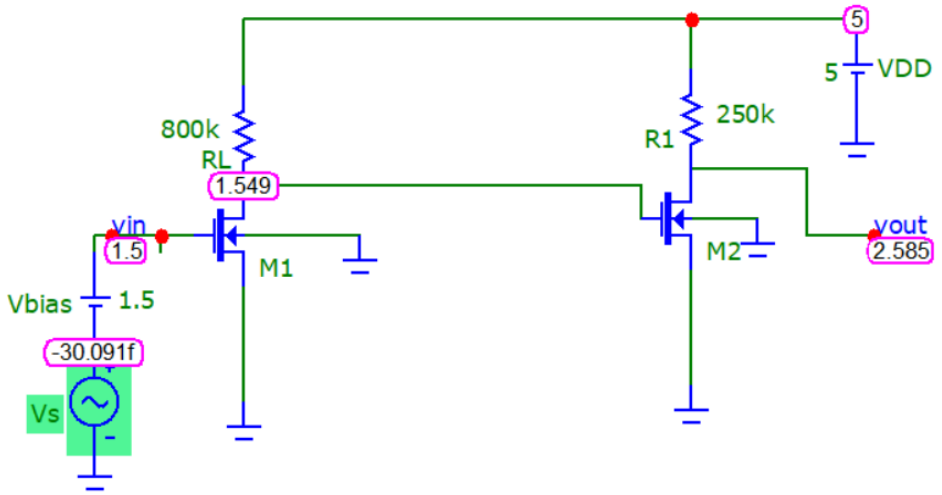
Designed for High output swing and Typically biased at mid-supply.

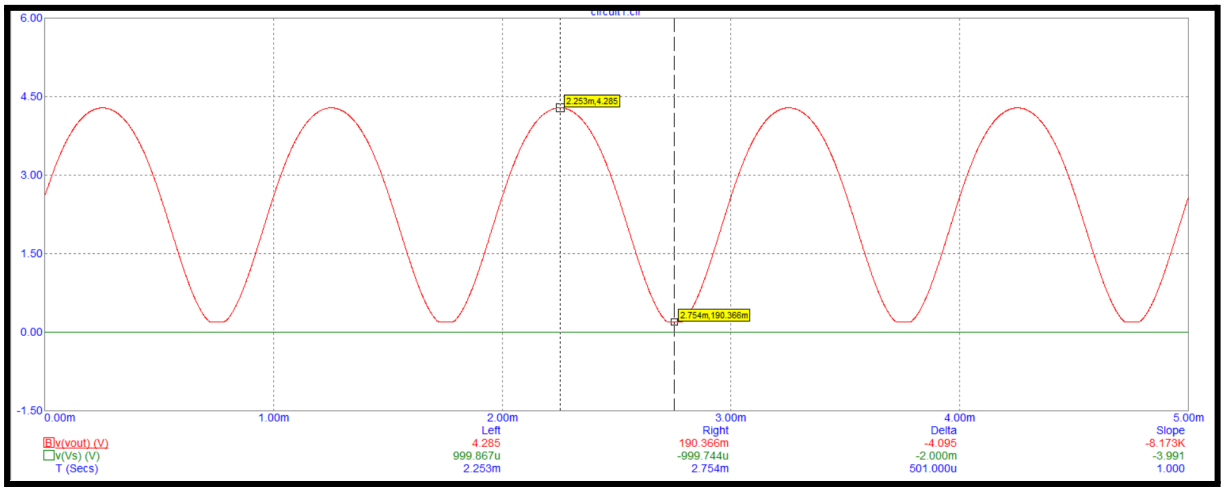
Calculator R_L for the output stage

Since, here the transistor operates in saturation region and if V_{DS}=2.5V then

$I_{DS} = \frac{2.5}{R_L}$, *and also* $I_{DS} = \beta_N \frac{(V_{bias} - V_{TN})^2}{2}$. *Now, putting the values we obtained in part* 1 *and*

$take\ V_{bias} \simeq 1.55V,\ so,\ I_{DS} = 0.0103mA,\ so\ R_L = \frac{2.5}{0.01} k\Omega \Rightarrow R_L \simeq 250k\Omega$





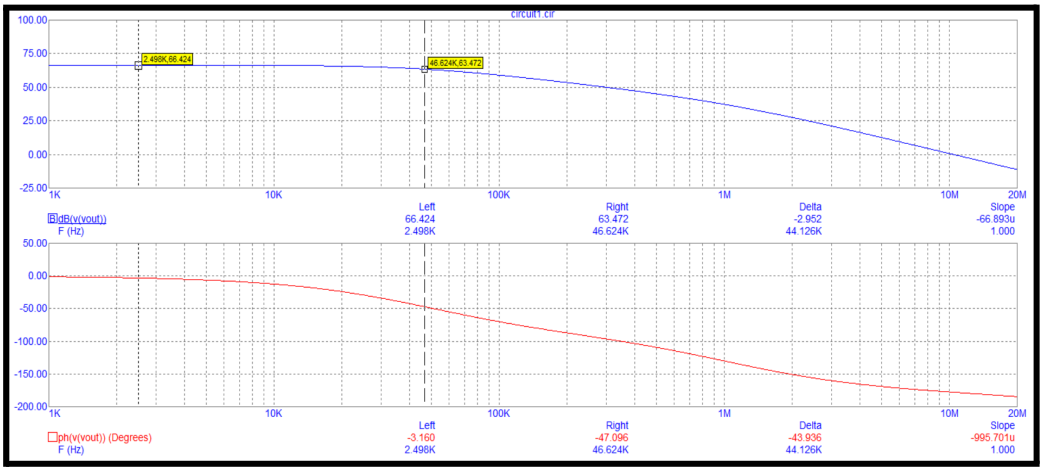
$A_{out} = \frac{4.285-0.19}{2} = 2.0475V$

And $A_{in} = 1mV \; or \; 0.001V$

so , Gain = 2047.5

Frequency Response:

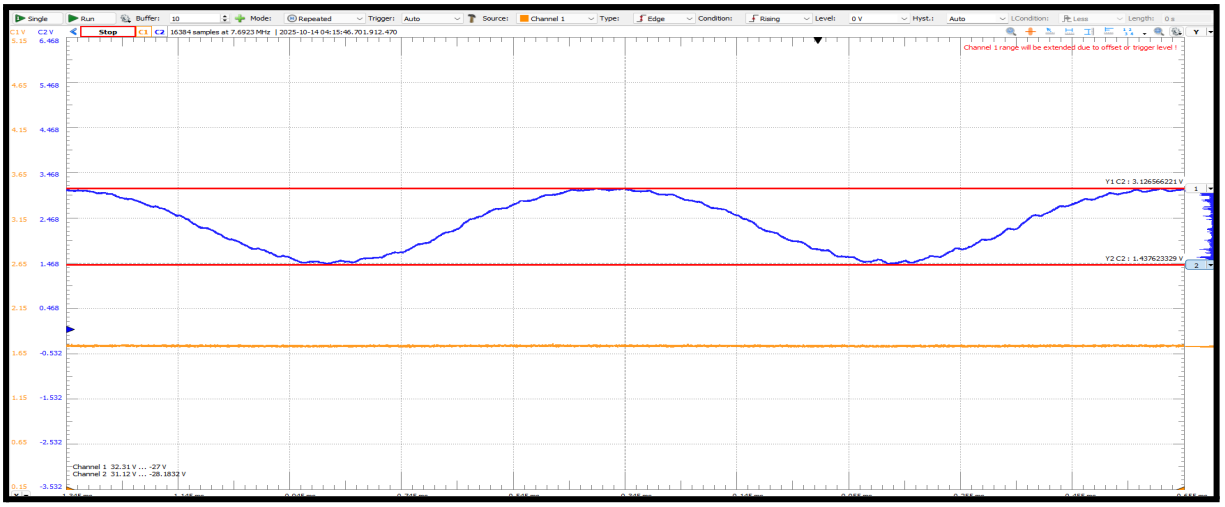
f_{3dB} = 46.6kHz



5.2 In Lab

We chose R_1=390kΩ and R_2 = 100kΩ and V_{bias}=1.685V

The following amplification was obtained from an input of a mere 2 mV sinusoidal signal.

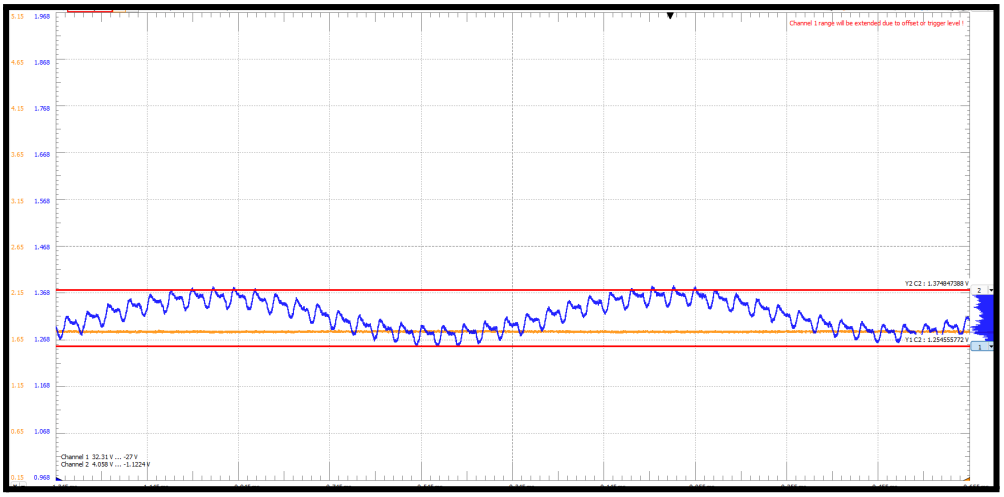


$A_{out} = \frac{3.127-1.437}{2} = 0.845V$

And $A_{in} = 2mV \; or \; 0.002V$

so , Gain = 422.5

Following is the gain of just the 1st stage:



$A_{out} = \frac{1.375-1.254}{2} = 0.0605V$

And $A_{in} = 2mV \; or \; 0.002V$

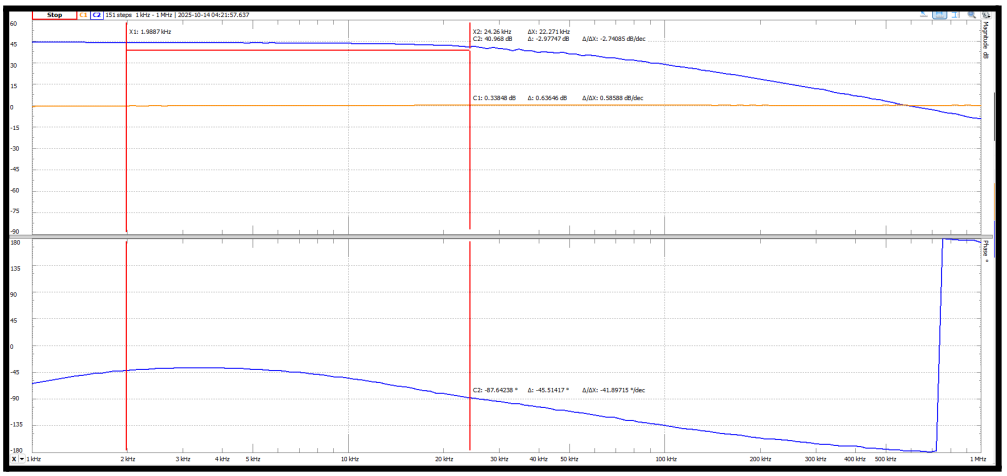
so , $Gain_{1st\ stage} = 30.25$

So, gain of 2nd stage can be estimated as $Gain_{2nd\ stage} = \frac{Gain}{Gain_{1st\ stage}}$

So, $Gain_{2nd\ stage} = 14$

Frequency Response:

f_{3dB} = 24.26kHz



5.3 Post Lab

The majority of the gain is contributed by the first stage, while the second stage is biased around $V_{DD}/2$ V to provide a large output voltage swing. The second stage primarily acts as a buffer and gain stage for driving the load.