IC Stage Biasing

- ***Avoids resistors as much as possible***
  - ➢ ***Resistors take up very large area on IC chips, which is at a premium***
- ***Uses transistors as biasing elements***
  - ➢ ***Much more compact than resistors***, and ***area consumption is almost negligible as compared to resistors***
- Also known as ***active biasing***

- ***Parameters***:
  - ***Output Current I_0***
    - ***As per specification***
  - ***Output Resistance R_0***
    - $R_0 = \Delta V_0/\Delta I_0 = dV_0/dI_0 = v_0/i_0$ (***ac***)
    - ***As large as possible*** - ***ideally infinite***
  - ***Minimum Allowed Output Voltage $V_{0,min}$***
    - ***As small as possible*** - ***ideally zero***
    - ***Dictated by***:
      - ***For BJT***: $V_{CE}(\text{min}) = V_{CE}(\text{SS}) = 0.2$ V
      - ***For MOSFET***: $V_{DS}(\text{min}) = V_{GT}(\text{min}) = 80$ mV

- ***I_0 should be independent of power supply and temperature***
  - ***Temperature and Supply Independent Biasing***
- ***Should use minimum number of circuit elements***
  - ***Economization of space***
- ***Should not affect frequency response***

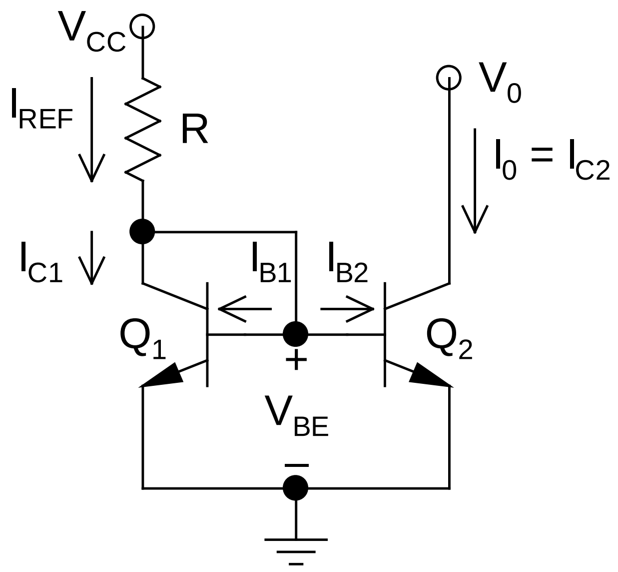
- It is ***almost impossible to satisfy all these constraints simultaneously***
  - ***Look for optimization***

Current Sources/Sinks

- Also known as ***Current Mirrors*** (CM)
- Can be used for ***biasing*** as well as ***load elements*** (known as ***active load***)
- Designed based on ***required specifications***
- ***Two sources of errors***:
  - ***Systematic***: ***Even when devices are matched***
  - ***Random***: ***When there is a random mismatch between devices***

- ***Simple npn CM***:
  - Q_1 has its ***B and C shorted***
    - ***Can never saturate*** ($V_{BC} = 0$)
    - Known as ***diode-connected BJT***
  - Q_1 and Q_2 have ***same*** V_{BE}
  - I_{REF} = ***Reference Current***

    $= (V_{CC} - V_{BE})/R$
  - I_0 = ***Output Current*** $= I_{C2}$
  - V_0 = ***Output Voltage***
    - ***Variable***, ***depends on the load connected to it***



- ***General Analysis***:

$$I_{REF} = I_{C1} + I_{B1} + I_{B2} = I_{C1}\left(1+\frac{1}{\beta_1}\right)+\frac{I_{C2}}{\beta_2}$$

- Now:

$$V_{BE} = V_T \ln\left(\frac{I_{C2}}{I_{S2}}\right) = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right)$$

$$\Rightarrow I_{C2} = KI_{C1} \quad \left(K = I_{S2}/I_{S1}\right)$$

- Thus:

$$I_{REF} = I_{C2}\left[\frac{1}{\beta_2}+\frac{1}{K}\left(1+\frac{1}{\beta_1}\right)\right]$$

- ***Finally***:

$$I_0 = \frac{I_{REF}}{\dfrac{1}{\beta_2} + \dfrac{1}{K}\left(1 + \dfrac{1}{\beta_1}\right)}$$

- This is the ***exact expression*** of I_0, ***without making any assumptions/approximations whatsoever***
- The ***only assumption*** so far is that we have ***neglected Early effect***, which we would include soon

- Now, we ***make approximations/assumptions***:

1. $\beta_1 = \beta_2 = \beta$:

$$\Rightarrow I_0 = \frac{KI_{REF}}{1 + \dfrac{1+K}{\beta}}$$

2. $I_{S1} = I_{S2} = I_S$ $(K = 1)$:

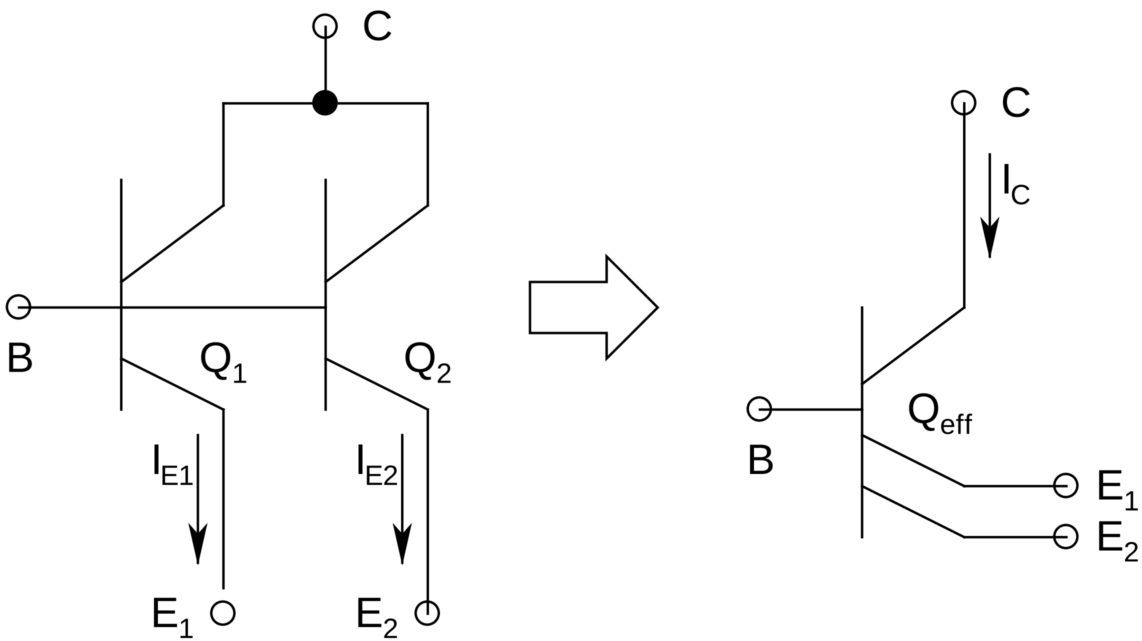
$$\Rightarrow I_0 = \frac{I_{REF}}{1 + 2/\beta}$$

3. And finally $\beta >> 2$:

$\Rightarrow I_0 = I_{REF} \Rightarrow$ ***Current Mirror***!

- For this to happen, Q_1 and Q_2 must have ***same β*** (***>> 2***), and ***same I_S***
- If two BJTs have ***same β, I_S, and V_A***, they are known as a ***matched pair***
- If $I_{S1} \neq I_{S2}$ and/or $\beta_1 \neq \beta_2$, then $I_0 \neq I_{REF}$
  - Leads to ***random error*** (***process induced***)
- If $\beta_1 = \beta_2$, but $I_{S1} \neq I_{S2}$, then $I_0 = KI_{REF}$
  - ***K or 1/K can only be integers***
    - ***I_0 and I_{REF} become integer multiples of each other***

- ***Multi-Emitter BJT***:



- $I_{S1} = I_{S2} \Rightarrow I_{E1} = I_{E2} = I_E \Rightarrow I_C \approx 2I_E$
    - *This does not imply that $\alpha = 2$*, *since there are two emitters*

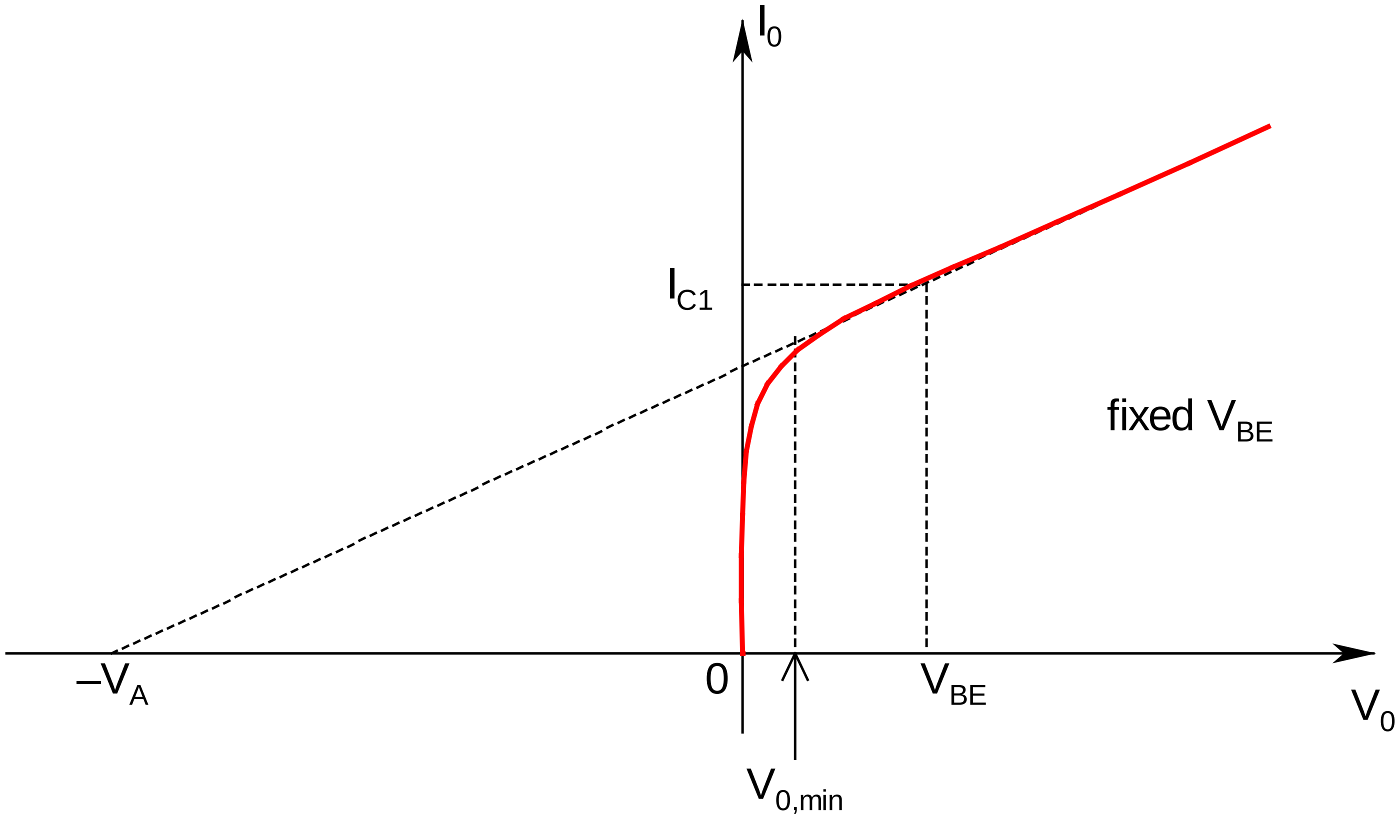
- ***Systematic Error***:
  - ***Even if Q_1 and Q_2 are perfectly matched and $\beta >> 2$***, ***still I_0 may not equal I_{REF}***!
  - ***Recall***:

$$I_C = I_S[\exp(V_{BE}/V_T)](1 + V_{CE}/V_A)$$

  - ***Thus***:

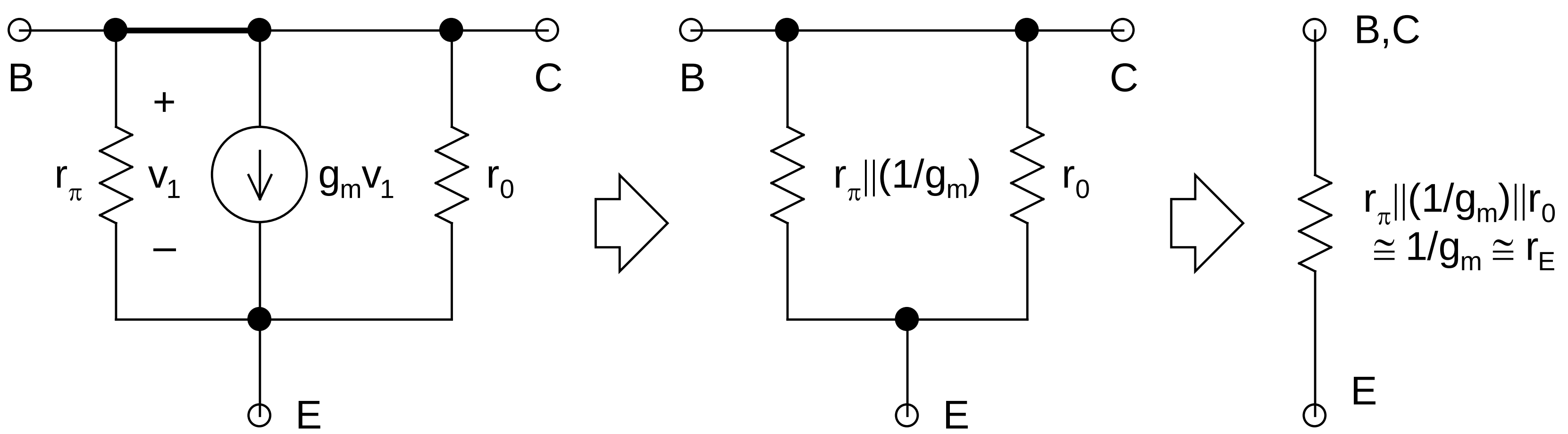
$$\frac{I_{C2}}{I_{C1}} = \frac{I_0}{I_{C1}} = \frac{1 + V_{CE2}/V_A}{1 + V_{CE1}/V_A} = \frac{1 + V_0/V_A}{1 + V_{BE}/V_A}$$

  - Therefore, ***$I_0 = I_{C1}$ only when $V_0 = V_{BE}$***



$$V_{0,min} = V_{CE2}(SS) = 0.2\ V$$

- ***Output Resistance R_0*:**
  - First, ***investigate Q_1***



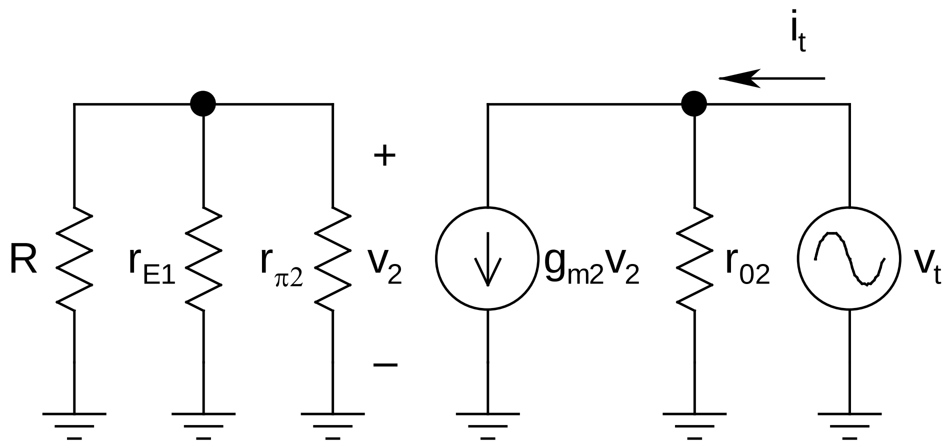
- The ***small-signal equivalent*** consists simply of r_E, which is the same as that for a ***diode***
  - Hence the name ***diode-connected transistor***

- ***Algorithm to find R_0*:**
  - ***Short all independent DC voltage sources***
  - ***Open all independent DC current sources***
  - ***Replace the active device by its low-frequency hybrid-π model***
  - ***Excite the output terminal by a test voltage source (ac) v_t***
  - ***Find the current (ac) i_t drawn from v_t***
  - ***Then, $R_0 = v_t/i_t$***

- ***For the complete circuit*:**
  - ***Left part of the circuit has no source***

    $\Rightarrow v_2 = 0$

    $\Rightarrow g_{m2}v_2 = 0$



  - Thus, $R_0 = v_t/i_t = r_{02} = V_{A2}/I_0$
  - For a ***good current source***, ***R_0 should be as large as possible*** (***ideally infinite***)

    $\Rightarrow$ ***V_{A2} should be as large as possible*** and/or ***I_0 should be as small as possible***