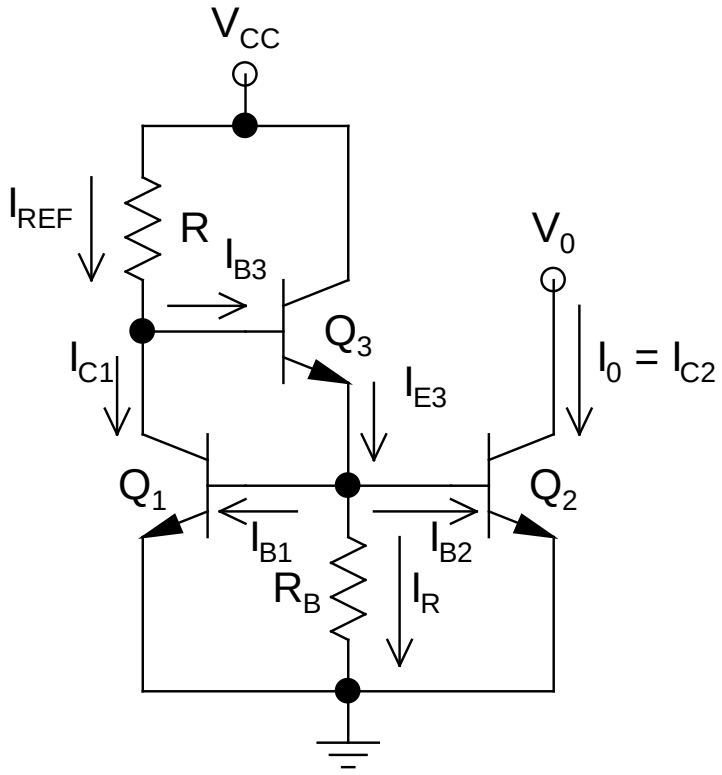
- ***More on W/L Ratio***:
  - ***Generally, in technology, W/L is kept between 0.01 and 100***
  - ***The ideal ratio is between 0.02 and 50***
  - ***Minimum Feature Size*** (MFS):
    - ***Minimum dimension that can be resolved in an IC chip***
      - ***Has gone down from 10s of μm in 80s to a few nm now***!
  - ***For W/L > 1 (or < 1), L (or W) is chosen equal to MFS***
    - ***Yields minimum possible device area*** (W × L)

- ***npn CM With Better β Insensitivity***:
  - $I_{REF} = (V_{CC} - 2V_{BE})/R$
  - Neglecting I_{B3}:

    $I_{C1} = I_{REF}$
  - ***If Q_1 and Q_2 are matched***:

    $I_0 = I_{C2} = I_{C1} = I_{REF}$

    $\Rightarrow$ ***Simple CM***
  - ***The actual advantage of the circuit lies elsewhere***!



- First, assume ***R_B is absent***

$$\Rightarrow I_{E3} = I_{B1} + I_{B2} = I_{C1}/\beta_1 + I_{C2}/\beta_2 = 2I_0/\beta_1$$

(***assuming $\beta_1 = \beta_2$***)

$$\Rightarrow I_{B3} = \frac{I_{E3}}{\beta_3 + 1} = \frac{2I_0}{\beta_1(\beta_3 + 1)}$$

$$I_{REF} = I_{C1} + I_{B3} = I_0\left[1 + \frac{2}{\beta_1(\beta_3 + 1)}\right]$$

$$\Rightarrow I_0 = \frac{I_{REF}}{1 + \dfrac{2}{\beta_1(\beta_3 + 1)}}$$

- Now, if $\beta_1 = \beta_3 = \beta$, and $\beta >> 1$:

  $I_0 \approx I_{REF}(1 - 2/\beta^2)$
- Compare with that of simple CM:

  $I_0 \approx I_{REF}(1 - 2/\beta)$
- ***The advantage is obvious***!
- ***Further Insights***:
  - I_{E3} (= $I_{B1} + I_{B2}$) ~ ***few 10s of μA***
  - ***At such a low current, β drops significantly from its nominal value***
  - ***Thus, full advantage of the circuit can't be exploited***

- ***Here comes the role of R_B***:
  - ***It drains a constant current*** (= V_{BE}/R_B), ***which gets added to*** ($I_{B1} + I_{B2}$), and ***boosts*** I_{E3} (and, thus, I_{C3})
  - ***Thus, β_3 gets pulled up to its nominal value***
  - ***This resistor has a special name***: ***Keep Alive***, ***since it keeps Q_3 alive***!
- ***However, it creates some issues as well***:
  - ***Additional power drain due to the additional current flowing through R_B***
  - ***If $I_{E3} \uparrow$, so would I_{B3}***

    $\Rightarrow$ ***I_{C1} may depart from I_{REF}***
  - ***Design optimization needed***

- ***Now, for R_0***:
  - ***Looking at C_2***
  - ***E_2 grounded***
  - ***No connection between C_2 and B_2*** (***no feedback***)
  - ***Therefore, by inspection***:

    $R_0 = V_{A2}/I_0$

- ***Also, by inspection***:

  $V_{0,min} = V_{CE2}(SS) = 0.2\ V$

- ***There is no MOS counterpart for this circuit for obvious reasons***!

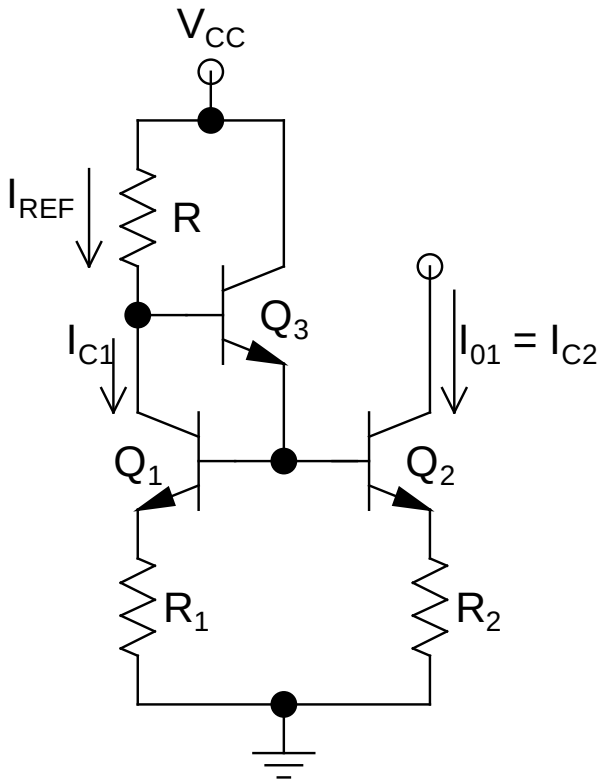
- ***npn Ratioed CM***:
  - ***Q_1-Q_2 matched pair***
  - ***Neglecting all I_B***, $I_{E1} = I_{C1}$ $= I_{REF}$, and $I_{E2} = I_{C2} = I_0$
  - $I_{REF} = (V_{CC} - 2V_{BE})/(R + R_1)$
  - ***KVL around Q_1-Q_2 BE loop***:

$$V_{BE1} + I_{REF}R_1 = V_{BE2} + I_0R_2$$

$$\Rightarrow I_0 = (I_{REF}R_1 + \Delta V_{BE})/R_2$$

$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$

$$= V_T \ln(I_{REF}/I_0)$$



- ***Note the ln dependence***:
  - ***For $I_{REF}/I_0 = 2$, $\Delta V_{BE} = 18$ mV***
  - ***For $I_{REF}/I_0 = 10$, $\Delta V_{BE} = 60$ mV***

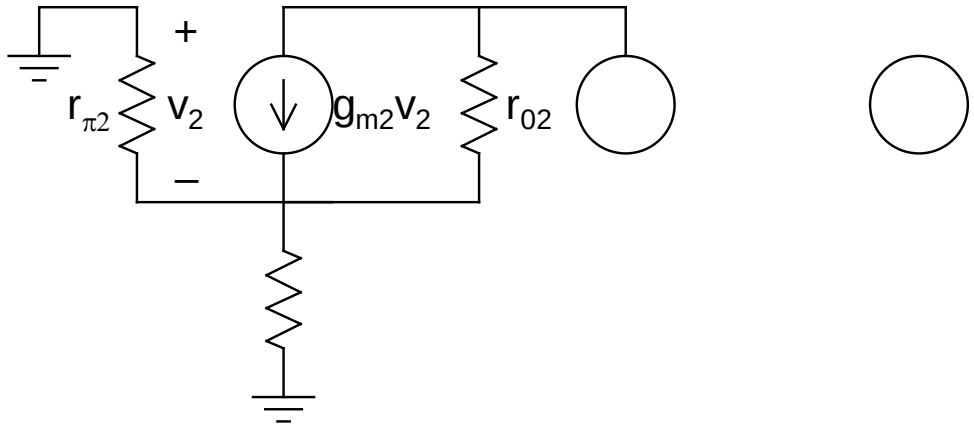
  $\Rightarrow \Delta V_{BE}$ can be neglected if $I_{REF}R_1 > 10\Delta V_{BE}$

  $\Rightarrow I_0 = (R_1/R_2)I_{REF}$ (Ratioed Mirror)
- ***Thus, by tinkering R_1 and R_2, any ratio between I_0 and I_{REF} can be obtained***
  - ***Tremendous advantage***
    - ***Widely used***
- ***By inspection***:

$$V_{0,min} = V_{CE2}(SS) + I_0R_2 = 0.2 + I_0R_2$$

- ***Calculation of R_0:***
  - ***Golden Rule can't be used since emitter of Q_2 is not grounded (R_2 present there)***
  - ***Needs analysis***

    $\Rightarrow$ Leads to a module that is frequently encountered
  - ***Base of Q_1-Q_2 at a fixed DC potential $\Rightarrow$ ac ground***



$$i_t = g_{m2} v_2 + \left(v_t + v_2 \right) / r_{02}$$

$$= v_t / r_{02} + \left(g_{m2} + 1/r_{02} \right) v_2 \qquad v_t / r_{02} + g_{m2} v_2$$

$$v_2 = -i_t R_{eff}$$

$$\Rightarrow i_t = v_t / r_{02} - g_{m2} R_{eff} i_t$$

$$\Rightarrow R_0 = v_t / i_t = r_{02}(1 + g_{m2} R_{eff})$$

- This is a ***Golden Equation***, which would be ***used frequently***
  - ***Carefully note the topology that produces this result***
- ***Exercise***: ***Reverse v_2 and show that the expression for R_0 remains invariant***