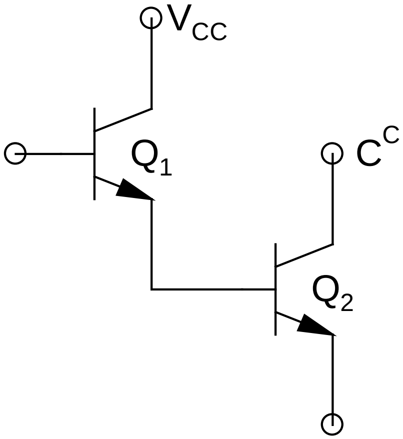
Compound Connections

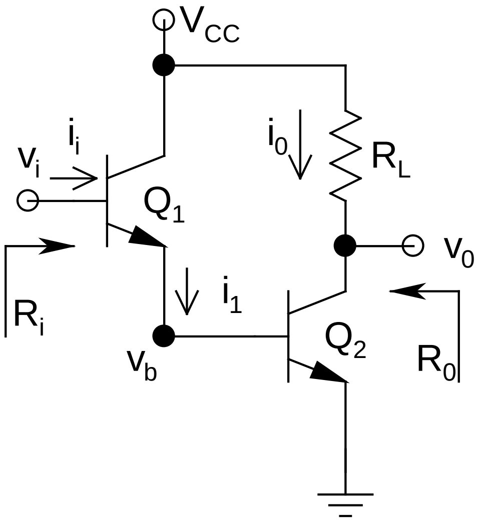
- ***Multi-Stage***
- Have some ***special properties***
- ***Popular Topologies***:
  - ➢ ***Darlington***
  - ➢ ***Cascode***
  - ➢ ***DP*** (or ***DA***)
- ***Modules by themselves***

- ***Darlington***:
  - Cascade of a ***CC*** stage, followed by either a ***CE*** or a ***CC*** stage
  - ***Two biggest advantages***:
    - ***Extremely large*** R_i
    - ***Extremely large*** A_i
  - ***These two advantages are automatic for MOS stages***

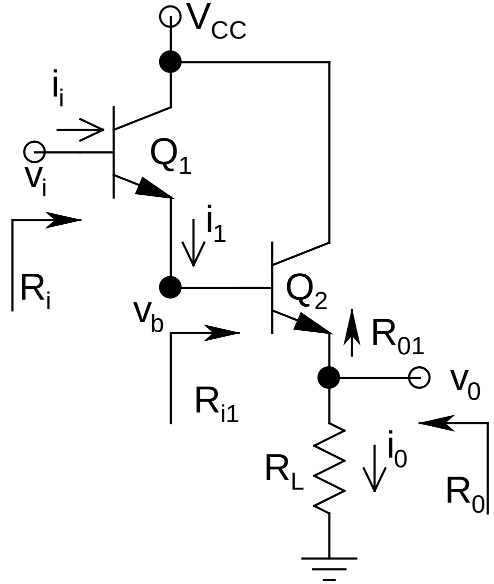
  $\Rightarrow$ ***MOS Darlington has no special use***



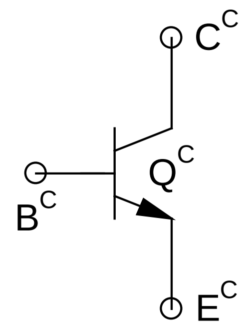
Generic Circuit



CC-CE Stage



CC-CC Stage



Compact Representation

- For ***DC biasing***:

$$I_{C2} = \beta_2 I_{B2} = \beta_2 I_{E1} \approx \beta_2 I_{C1}$$

$$\Rightarrow r_{\pi 2} = \beta_2 r_{E2} = \beta_2 V_T/I_{C2} = V_T/I_{C1} = r_{E1}$$

- For ***ac analysis***:

  CC-CE:

  - $i_1 = (\beta_1 + 1)i_i$ and $i_0 = \beta_2 i_1 = \beta_2(\beta_1 + 1)i_i$

    $\Rightarrow A_i = i_0/i_i = \beta_2(\beta_1 + 1) \approx \beta^2$ (***Huge***!)
  - $R_i = r_{\pi 1} + (\beta_1 + 1)r_{\pi 2} \approx 2r_{\pi 1}$
    - I_{C2} ~ mA, I_{C1} ~ 10s of μA, r_{E1} ~ kΩ, $r_{\pi 1}$ ~ 100s of kΩ (***Huge***!)
  - $v_0/v_b = -R_L/r_{E2}$ and $v_b/v_i = r_{\pi 2}/(r_{\pi 2} + r_{E1}) = 1/2$

    $\Rightarrow A_v = v_0/v_i = -R_L/(2r_{E2})$ (***Moderate***)
  - $R_0 = R_L||r_{02} \approx R_L$ (***Moderate***)
- Thus, this stage has ***huge A_i and R_i***, and ***moderate A_v and R_0***

- For ***ac analysis***:

  CC-CC:

  - $i_1 = (\beta_1 + 1)i_i$ and $i_0 = (\beta_2 + 1)i_1 = (\beta_2 + 1)(\beta_1 + 1)i_i$

    $\Rightarrow A_i = i_0/i_i = (\beta_2 + 1)(\beta_1 + 1) \approx \beta^2$ (***Huge***!)
  - $R_i = r_{\pi 1} + (\beta_1 + 1)(\beta_2 + 1)(r_{E2} + R_L)$

    $\approx r_{\pi 1} + \beta^2(r_{E2} + R_L)$ (***Astronomical***!)
  - $R_{i1} = r_{\pi 2} + (\beta_2 + 1)R_L$
  - $v_0/v_b = R_L/(R_L + r_{E2})$
  - $v_b/v_i = R_{i1}/(r_{E1} + R_{i1})$
  - $A_v = v_0/v_i \approx \beta_2 R_L/(2r_{E1} + \beta_2 R_L)$ (***Show***!)

- Thus, this stage has ***extremely large A_i and R_i***, and ***A_v is ≤ 1 with no phase shift***

- $R_0 = R_L || R_{01}$

  $R_{01} = r_{E2} + r_{E1}/(\beta_2 + 1)$ (***by inspection***)

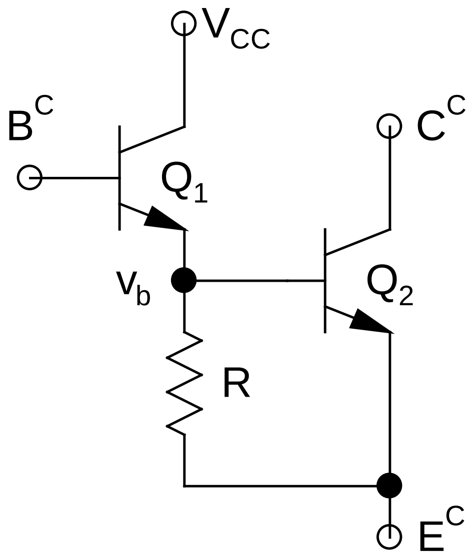
  $\approx 2r_{E2}$

  $\Rightarrow R_0 \approx R_L || (2r_{E2})$ (***Small***)
- Above analysis is ***pretty straightforward***, and ***assumes that both β_1 and β_2 are high***
- ***In reality, Q_1 operates with a very low value of I_C*** (~ ***10s of μA***)

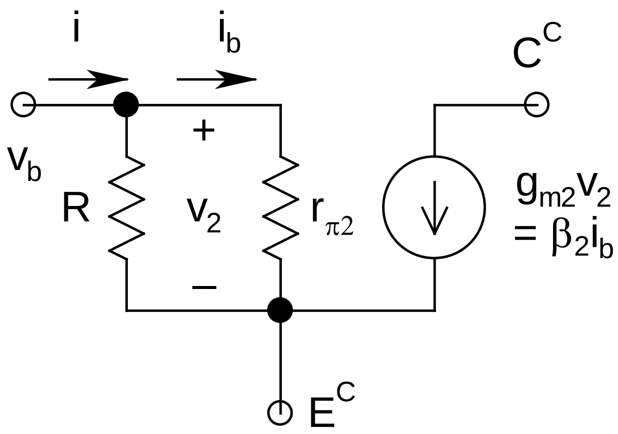
  $\Rightarrow$ ***β_1 would drop significantly from its nominal value*** $\Rightarrow$ ***Full advantage of the circuit can't be exploited***

➢ ***Need to jack up β_1***

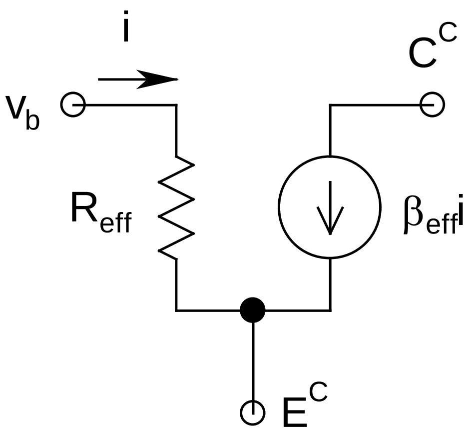
❖ ***How about using a keep-alive resistor***?



Darlington with Keep-Alive Resistor R



ac Midband Equivalent of Q_2-R Combination



Simplified Equivalent of Q_2-R Combination

- ***R drains a constant DC current of ~ 0.7/R***
- ***This current is supplied by Q_1, along with I_{B2}***

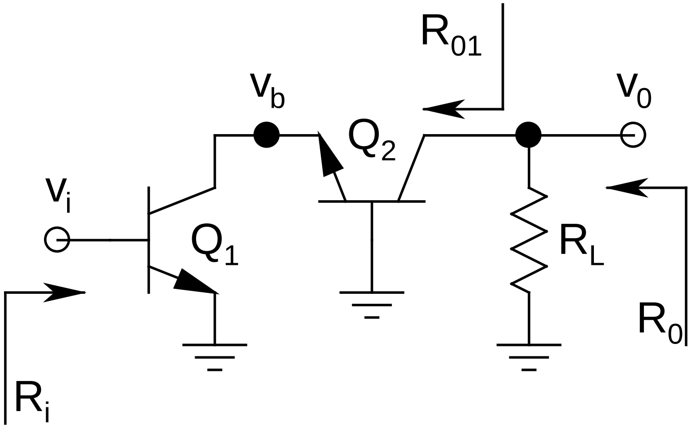
  $\Rightarrow I_{C1}\uparrow \Rightarrow \beta_1\uparrow$
- ***However, this technique also changes β_2***
- ***Analysis***:

  $i_b = iR/(R + r_{\pi2})$

  $\Rightarrow i_c = \beta_2 i_b = \beta_2 iR/(R + r_{\pi2}) = g_{m2}r_{\pi2}iR/(R + r_{\pi2}) = g_{m2}(R\|r_{\pi2})i = g_{m2}R_{eff}i = \beta_{eff}i$

  $\beta_{eff} = g_{m2}R_{eff} < \beta_2 \qquad (R_{eff} = R\|r_{\pi2})$
- As if $r_{\pi2,eff} = R_{eff}$

- ***npn Cascode***:
  - ***CE***, followed by ***CB***
  - Known as ***Wideband Amplifier***, due to its ***superior frequency response characteristic***



ac Schematic

  - ***Generally, both Q_1 and Q_2 are biased with the same I_C***
  - ***Assuming Q_1-Q_2 have same β***:

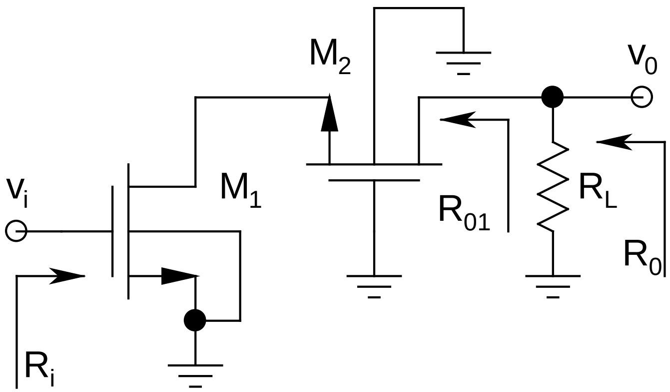
    $r_{E1} = r_{E2} = r_E$ and $r_{\pi 1} = r_{\pi 2} = r_\pi$

- ***This circuit can be analyzed by inspection***
- $R_i = r_{\pi 1}$
- $v_0/v_b = +g_{m2}R_L = R_L/r_{E2}$ (***CB Stage***)
- $v_b/v_i = -\,r_{E2}/r_{E1} = -1$
  - ***CE Stage with R_i of Q_2 (= r_{E2}) as its load***
- Thus, $A_v = v_0/v_i = -\,R_L/r_{E2}$
- ***Note that A_v is same as that for a CE stage, however, the bandwidth of this circuit is far superior than a CE stage***

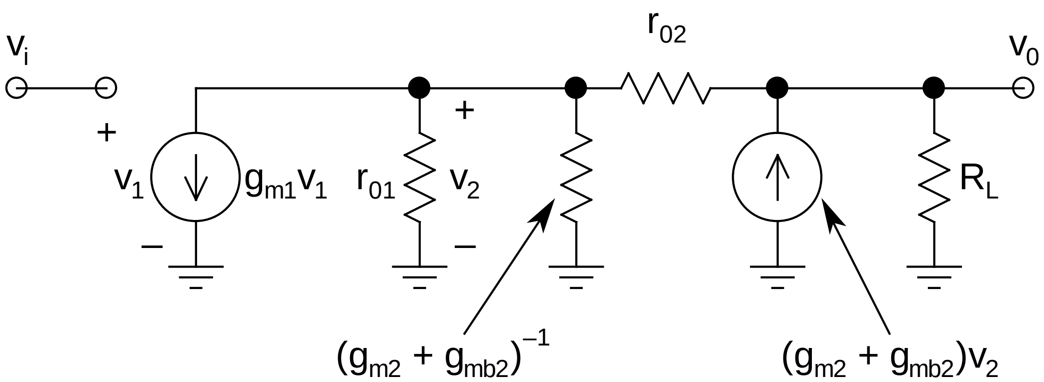
- $R_0 = R_L || R_{01}$
- ***If r_0 is neglected***, then $R_{01} \rightarrow \infty$ (***why?***)
- ***If r_0 is included***, then $R_{01} = \beta r_{02}$ (***very high***)
- However, ***it comes in parallel with R_L***

  $\Rightarrow$ ***Overall R_0 is still ~ R_L***
- ***Summary***:
  - ***Moderate voltage gain***
  - ***Moderate input resistance***
  - ***Potential of having very large output resistance***
  - ***Extremely large bandwidth***
  - ***Preferred over a simple CE stage***

• ***NMOS Cascode***:



ac Schematic



ac Midand Equivalent

- ***CS***, followed by ***CG***
- ***Generally, both M_1 and M_2 are biased with the same I_D***
- ***M_1 does not have body effect, but M_2 has***

- ***By inspection***, $R_i \rightarrow \infty$ and $R_0 = R_L||R_{01}$
- ***With r_{02} present***, ***the analysis becomes a little complicated*** $\Rightarrow$ ***neglect r_{02}*** $\Rightarrow R_0 = R_L$
- ***Neglecting r_{02}***:

$$v_0 = (g_{m2} + g_{mb2})v_2R_L$$

$$v_2 = -\,g_{m1}v_1/(g_{m2} + g_{mb2} + g_{01})\ (g_{01} = 1/r_{01})$$

$$\approx -\,g_{m1}v_1/(g_{m2} + g_{mb2})$$

[since, in general, $g_{01} << (g_{m2} + g_{mb2})$]

$$\Rightarrow A_v = v_0/v_i = -\,g_{m1}R_L\ (\text{since } v_1 = v_i)$$

- ***This is same as the CS stage, however, here broad-banding is happening***!

- ***A_v gets affected a little if r_{01} and r_{02} were included***
- ***Since r_{01} comes in parallel with $(g_{m2} + g_{mb2})^{-1}$, its effect on A_v is less pronounced than that of r_{02}***
- ***By inspection***:

  $R_{01} \approx (g_{m2} + g_{mb2})r_{01}r_{02}$ (***Show***!)
- ***Note that if either of r_{01} or $r_{02} \to \infty$, $R_{01} \to \infty$*** (***Why***?)