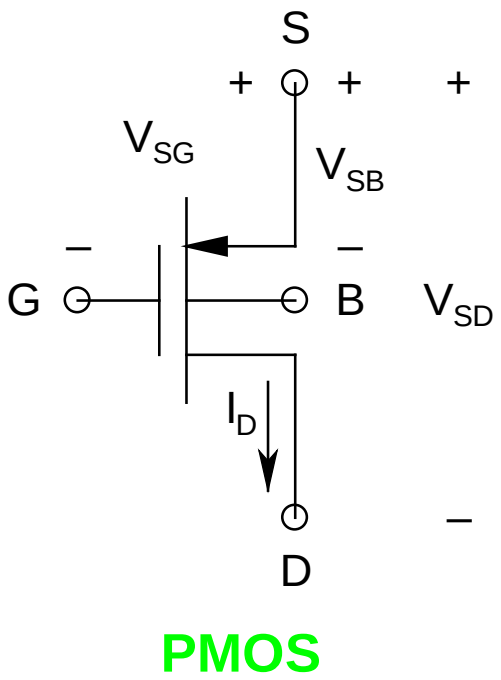
p-channel MOSFET (PMOS)

- Before moving to ***NMOS stages with active load***, it will be prudent to visit some details regarding ***PMOS***
- ***Substrate***: ***n-type*** (N_D)
  - ***Bulk Potential***:

    $\phi_F = V_T \ln(N_D/n_i)$
- ***Source/Drain***: p^+
- ***Channel Carriers***: ***Holes***



- ***Threshold Voltage***:

$$V_{TP} = V_{TP0} - \gamma\left(\sqrt{2\phi_F + V_{BS}} - \sqrt{2\phi_F}\right)$$

V_{TP0}: ***Zero back-bias threshold voltage*** (***negative***)

- ***Body effect coefficient***:

$$\gamma = \frac{\sqrt{2q\varepsilon_s N_D}}{C'_{ox}}$$

  - $V_{BS} \geq 0$ (***to prevent forward biasing of SB junction***)

- ***With back bias***, V_{TP} ***becomes more negative***
- V_{GS} ***has to be less than*** V_{TP} ***to turn device on***

- ***Current-Voltage Relation***:
  - ***Both V_{GS} and V_{DS} negative***
  - ***I_D flows from source to drain*** (the ***same direction of flow as holes***)
  - ***In saturation*** [$|V_{DSp}| > (|V_{GSp}| - |V_{TP}|)$]:

$$I_D = \frac{k'_P}{2}\frac{W}{L}\left(|V_{GSp}| - |V_{TP}|\right)^2\left(1+\lambda_p|V_{DSp}|\right)$$

  - ***In non-saturation*** [$|V_{DSp}| < (|V_{GSp}| - |V_{TP}|)$]:

$$I_D = k'_P\frac{W}{L}\left[\left(|V_{GSp}| - |V_{TP}|\right)|V_{DSp}| - |V_{DSp}|^2/2\right]$$

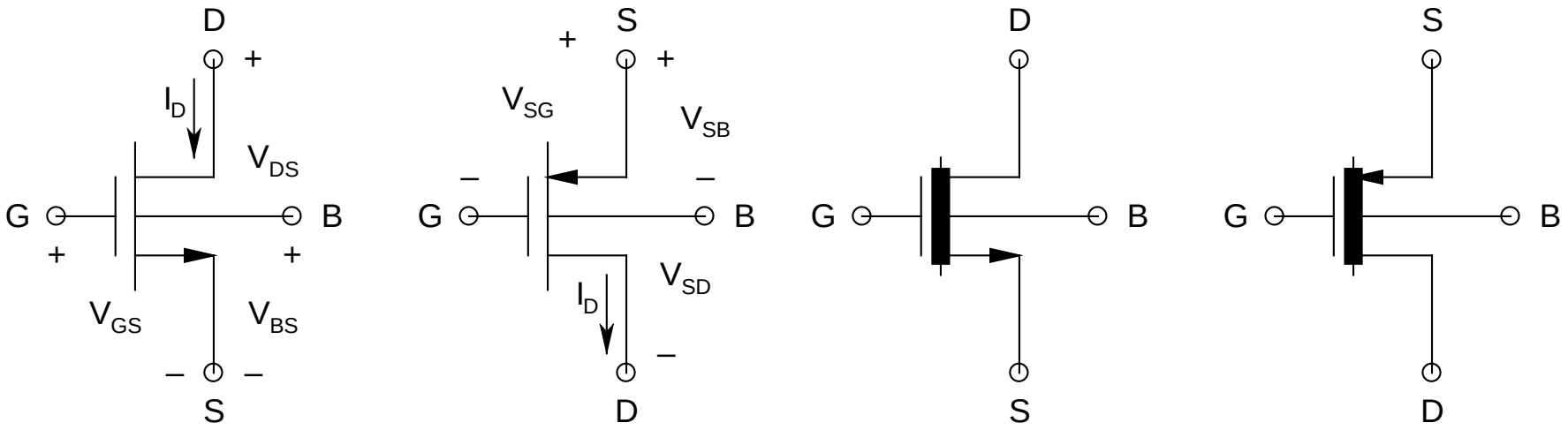
$$k'_P = \mu_p C'_{ox}$$

$$= \textbf{\textit{Process transconductance parameter}}$$

μ_p = ***Channel hole mobility***

- ***Based on the value of V_{TN0} and V_{TP0}***, there are ***two classifications***:
  - ***Enhancement Mode***: ***Normally Off*** (***with $V_{GS} = 0$***)
    - ***V_{TN0} positive*** and ***V_{TP0} negative***
  - ***Depletion Mode***: ***Normally On*** (***with $V_{GS} = 0$***)
    - ***V_{TN0} negative*** and ***V_{TP0} positive***

Symbols

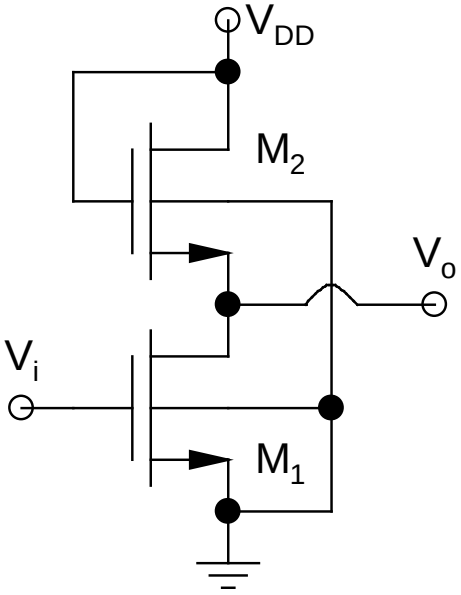


Enhancement Mode NMOS | **Enhancement Mode PMOS** | **Depletion Mode NMOS** | **Depletion Mode PMOS**

- Note the ***thick band*** in the ***channel region*** for ***depletion mode devices***, which implies that ***channel is present*** even ***with $V_{GS} = 0$***

- ***Variants of Actively Loaded CS Stage***:
  - ***Saturated Enhancement Load***
  - ***Depletion Load***
  - ***Complementary PMOS Load***
    - Also known as the ***CMOS Gain Stage***
- ***The last one is the most popular***

- ***Saturated Enhancement Load*:**
  - ***Both bodies tied to ground***
    - ***For M_1: $V_{SB1} = 0$***
    - ***For M_2: $V_{SB2} = V_o$***
  - ***M_2 is enhancement mode***
    - ***V_{TN02} positive***
  - ***M_2 is also diode-connected***
    - ***Always operates in saturation***
  - ***M_2 has a floating body effect problem*: V_o *is a variable* and V_{TN2} *will continuously change with a change in* V_o**



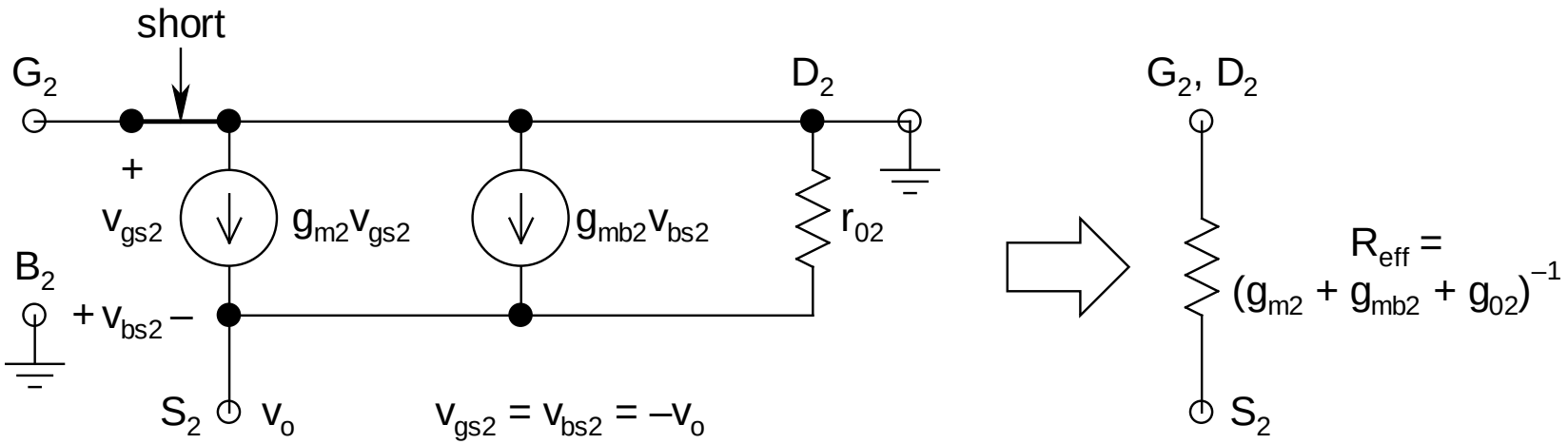
Circuit Schematic

- ***For M_2 to remain on, its V_{GS2} ($= V_{DD} - V_o$) must be > V_{TN2}***
- Thus, there is a ***maximum possible V_o***, beyond which ***it cannot rise*** (***M_2 would cut off***)
- To estimate this ***maximum V_o***, for the time being, ***neglect that $3V_T$ cushion***
- Then:

$$V_{DD} - V_{o,max} > V_{TN2} \text{ (with } V_{SB2} = V_{o,max})$$

$$V_{TN2} = V_{TN02} + \gamma\left(\sqrt{2\phi_F + V_{o,max}} - \sqrt{2\phi_F}\right)$$

- ***Solution of this equation would give $V_{o,max}$***
- ***Once $V_{o,max}$ is obtained***, the ***best bias point would be at $V_0 = V_{o,max}/2$***
- Before doing ***ac analysis***, ***let's investigate M_2***:



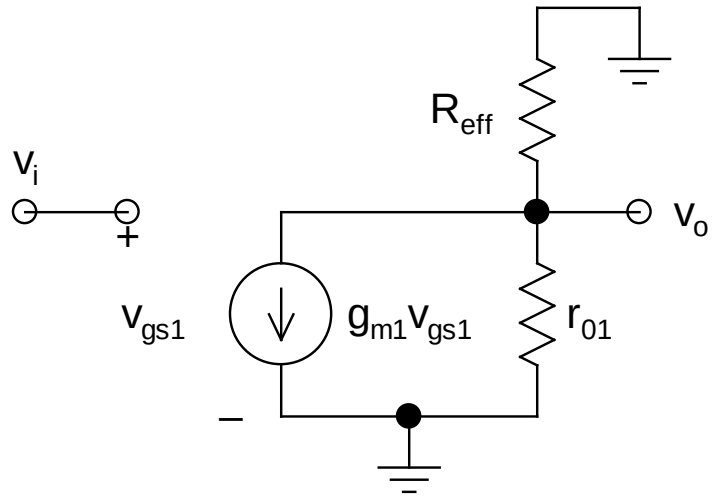
ac Midband Equivalent of M_2

Simplified Equivalent

- Thus, the ***complete equivalent***:
- ***By inspection***:

$$A_v = \frac{v_o}{v_i} = -g_{m1}\left(r_{01} \,||\, R_{eff}\right)$$

$$= -\frac{g_{m1}}{g_{m2} + g_{mb2} + g_{01} + g_{02}}$$



Complete Equivalent

- Now, in general,

$$(g_{m2} + g_{mb2}) >> (g_{01} + g_{02})$$

$$\Rightarrow A_v \approx -\frac{g_{m1}}{g_{m2} + g_{mb2}} = -\frac{g_{m1}}{g_{m2}(1+\chi_2)}$$

$$\chi_2 = \frac{\gamma}{2\sqrt{2\phi_F + V_{0Q}}}$$

V_{0Q} = ***Quiescent DC output voltage***

- Now, if M_2 can be put in its ***separate island***, then S_2 and B_2 can be ***connected together***

$$\Rightarrow v_{sb2} = 0 \Rightarrow g_{mb2}v_{sb2} = 0$$

$$\Rightarrow A_v \approx -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

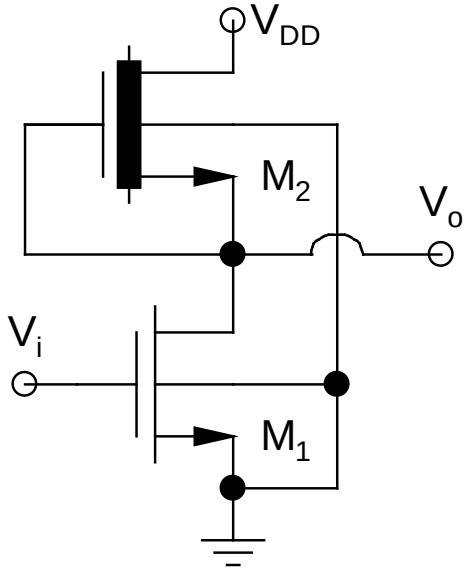
- $R_0 = (g_{m2} + g_{mb2} + g_{01} + g_{02})^{-1}$

- ***Insights***:
  - ***V_o doesn't go all the way to V_{DD}***

    $\Rightarrow$ Full rail-to-rail swing can't be achieved
  - ***When V_o falls below ΔV of M_1, it leaves the saturation region***, and ***enters non-saturation region***

    $\Rightarrow$ Distortion will set in at the output
  - Even for a ***moderate voltage gain of 10***, the ***ratio of the aspect ratios of M_1 and M_2 has to be 100***!
  - ***All these problems coupled together make this circuit highly unattractive for practical use***

- ***Depletion Load***:
  - M_2 is ***depletion mode***, having ***negative*** V_{TN0} (***denoted by*** V_{TD0})
  - ***Back bias of*** M_2: $V_{SB2} = V_o$
  - ***With*** V_o, V_{TD2} ***changes***
  - ***Maximum*** V_o ***desired*** $= V_{DD}$
  - ***This is also the maximum back bias of*** M_2



Circuit Schematic

- M_2 *has GS short* $\Rightarrow V_{GS2} = 0$
- *Even with* $V_o = V_{SB2}(max) = V_{DD}$, V_{TD2} *should remain negative with a cushion of at least 100 mV*

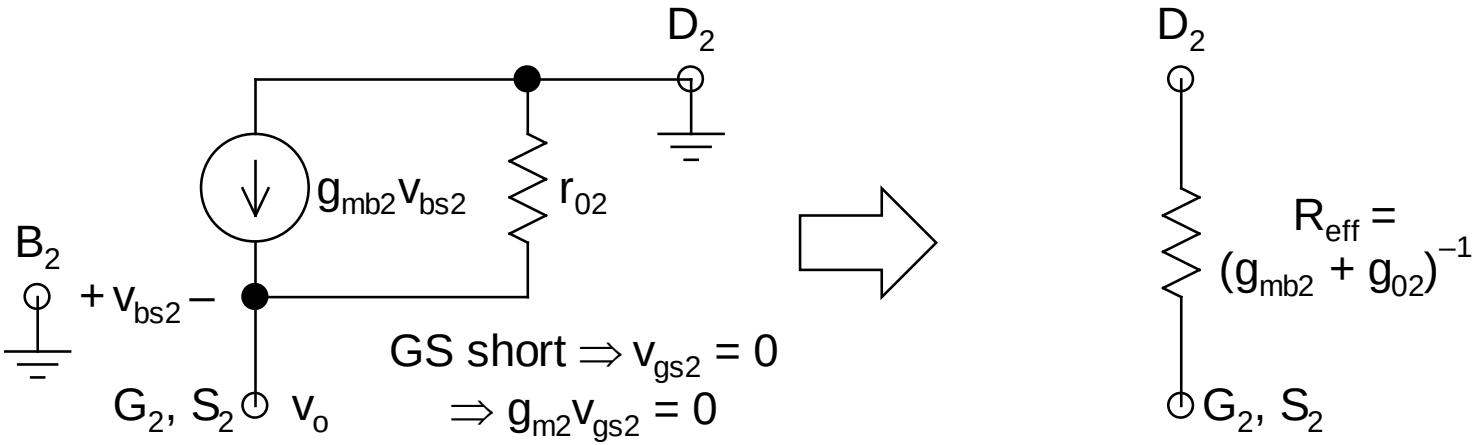
  $\Rightarrow V_{TD2}$ *with* $V_{SB2} = V_{DD}$ *should be –100 mV*

  $\Rightarrow V_{TD0}$ *should be chosen based on this*
- Now, $V_{DS2}(min) = V_{DD} - V_o(max) = 0$
- Under this condition, $V_{GS2} - V_{TD2} = \Delta V_2 = 100$ *mV*

  $\Rightarrow M_2$ *is in the linear region* (*since* $V_{DS2} < \Delta V_2$)

- ***This has to be lived with***, and ***slight distortion would appear at the output as*** $V_o \rightarrow V_{DD}$
- For ***best biasing***, $V_{0Q} = V_{DD}/2$

  $\Rightarrow$ ***Fixes the DC operating point***
- Before doing ***ac analysis***, ***let's investigate*** M_2:



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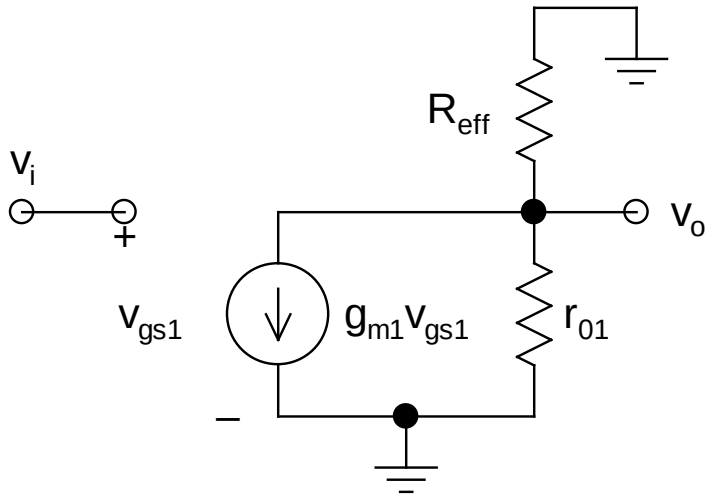

Complete Equivalent

- Now, in general,

$g_{mb2} >> (g_{01} + g_{02})$

$$\Rightarrow A_v \approx -\frac{g_{m1}}{g_{mb2}} = -\frac{g_{m1}}{\chi_2 g_{m2}} = -\frac{1}{\chi_2}\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$