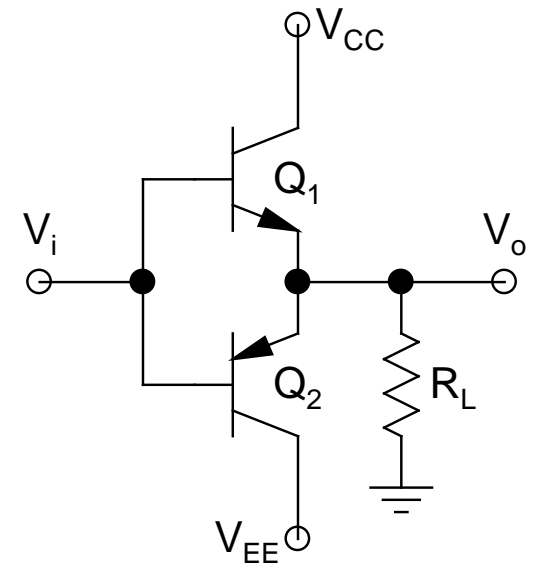- *Class B Push-Pull Output Stage*:
  BJT Implementation:
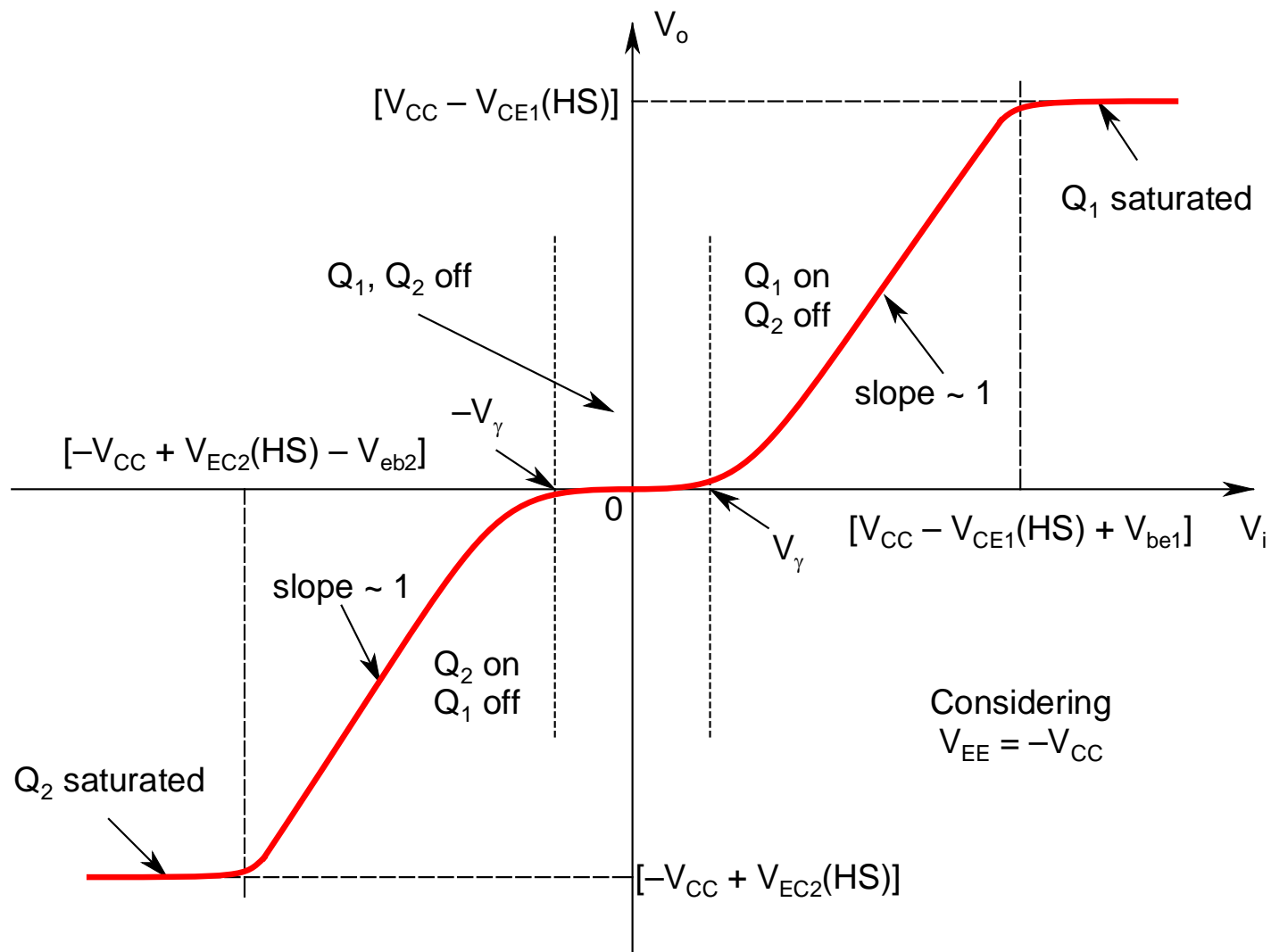 - ➤ Also known as *Comple-mentary Output Stage*
  - ➤ *Uses dual symmetric power supplies*
  - ➤ *Typical values used*:
    ±3 V, *±5 V*, *±12 V*, *±15 V*
  - ➤ *Q-point*: $V_i = V_o = 0$
    $\Rightarrow V_{be1} = V_{eb2} = 0$

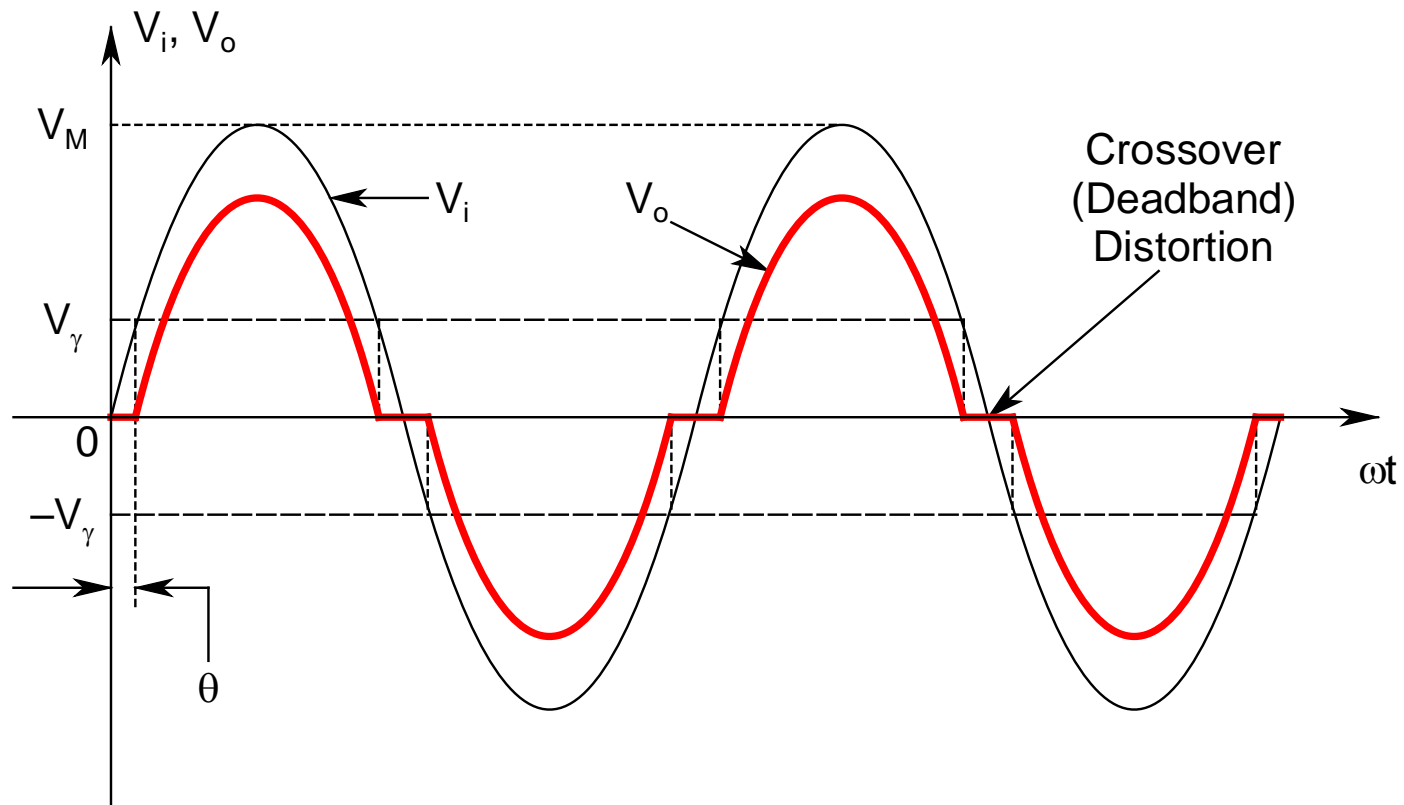**Circuit Schematic**

- *Both Q_1 and Q_2 cutoff*

  $\Rightarrow$ *Zero standby power*

- *Note*: $V_{be1} + V_{eb2} = 0$ (*always*)

- *As $V_i \uparrow$ beyond zero*, $V_{be1} \uparrow$ *and* $V_{eb2} \downarrow$

  $\Rightarrow$ *Q_1 moves towards turning on* and *Q_2 is pushed deeper into cutoff*

- *V_i has to be at least equal to V_γ for Q_1 to conduct* - till then, *V_o remains zero*

- *Once V_i becomes greater than V_γ, Q_1 turns on*, *supplies current to the load* (R_L), and *V_o starts to increase*

➢ Similarly, *as V_i↓ below zero*, *V_{be1}↓ and V_{eb2}↑*

$\Rightarrow$ *Q_2 moves towards turning on* and *Q_1 is pushed deeper into cutoff*

➢ Again, *V_i has to be at least equal to $-V_\gamma$ for Q_2 to conduct* - till then, *V_o remains zero*

➢ *Once V_i becomes less than $-V_\gamma$*, *Q_2 turns on*, *pulls current away from the load* (R_L), and *V_o starts to decrease* (*remains negative*)

➢ Thus, the name *Push-Pull*

▪ *Each transistor remains on for little less than half a cycle*

The Voltage Transfer Characteristic (VTC)

➢ Note the ***deadband*** ($V_o = 0$) ***between*** $\pm V_\gamma$

➢ Consider ***positive*** V_i :

- *For $V_i > V_\gamma$, V_o follows V_i with a **slope of almost unity** and **without any phase shift** (**CC stage**)*

- *As $V_o \nearrow$, $V_{ce1} \searrow$, and Q_1 starts to move towards saturation*

  $\Rightarrow$ ***Positive*** $V_{o,max} = V_{CC} - V_{CE1}(HS)$

- However, for this to happen, V_i ***has to be greater than*** V_{CC} (since there is an ***extra drop of*** V_{be1})

  $\Rightarrow$ ***This point can never be reached***

➢ ***The characteristic for negative*** V_i ***can be similarly understood***

Crossover Distortion

➢ *Crossover Distortion*:

- *Quantified by* θ (refer to the diagram)
- *Expressed as*:

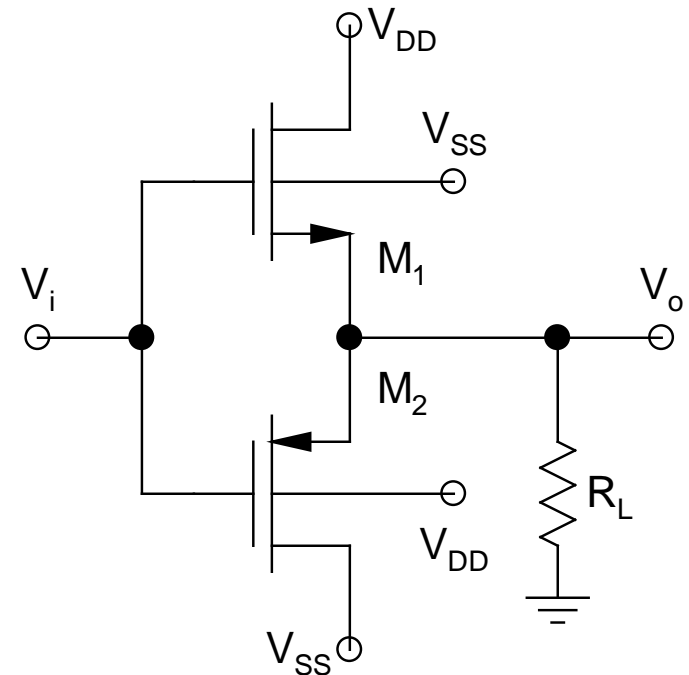 $\theta = sin^{-1}(V_\gamma / V_M)$

  V_M: *Amplitude of the input signal*
- *Appears four times over a complete cycle*
- *Parameterized* by a term known as the *Total Crossover Distortion* (*TCD*), *expressed in percent*:

  $TCD = (2\theta / \pi) \times 100\%$
- *This distortion becomes more acute as* $V_M \downarrow$
- *For* $V_M \leq V_\gamma$, *no output* ($V_o = 0$ *always*)

- *MOS Implementation*:
  - ➢ *Working principle absolutely similar to BJT implementation*
  - ➢ *Only exception that V_γ replaced by V_{TN} and V_{TP}*
  - ➢ *Q-point*: $V_i = V_o = 0$
  - ➢ *Both devices suffer from body effect issue*

Circuit Schematic

➢ **V_{TN} and V_{TP} function of V_o**

$\Rightarrow$ *VTC significantly nonlinear*

$\Rightarrow$ *Output shows more distortion*

➢ **V_i can't be more than V_{DD} or less than V_{SS}**

$\Rightarrow$ *V_o can't have rail-to-rail swing*

➢ Also, *MOS devices* are *inherently much poorer* than their *BJT counterparts* in terms of *current carrying capability*

$\Rightarrow$ *Makes this stage quite a poor choice* (*needs extremely large W/L ratios*)

- *Class AB Push-Pull Output Stage*:

  ➢ In a *Class B* stage, *Crossover Distortion* arises because the transistors are *absolutely cold* in the *standby state*, i.e., *dead off*

  ➢ If instead, these are *prebiased* at the *verge of conduction*, *but not quite turned on*, then a *slight swing* of the *input either way* can make *one of these transistors turn on* and *either supply current to the load* or *pull current away from the load*

  ➢ *This is the whole idea behind a Class AB stage*

- *Either of the output transistors remain on for complete half cycles*

- Thus, it's a *mixture of Class A and Class B operation*

- Hence, it's called *Class AB Push-Pull Stage*

- *Eliminates Crossover Distortion completely*

- *Obvious fallout*:
  - *Dissipation of standby power*

- *Extremely popular topology and widely used*

- *Efficiency drops slightly as compared to a pure Class B stage*

- **BJT Implementation**:
  - ➤ *Needs additional circuitry* (I_Q-Q_3-Q_4)
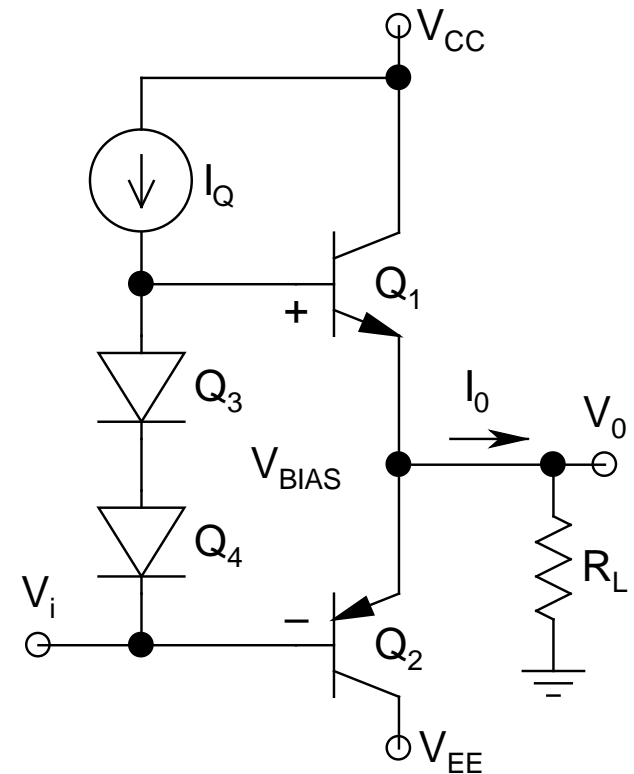 - ➤ Q_3-Q_4 *diode-connected* transistors and both are *biased by the same current* I_Q
  - ➤ This produces a *DC bias* V_{BIAS} between the *bases* of Q_1-Q_2

Circuit Schematic

➢ Consider *idling condition* with R_L *open-circuited* ($I_0 = 0$)

➢ *Neglecting base currents* of Q_1-Q_2, I_Q *flows through Q_3-Q_4* and *develops a voltage drop*:

$$V_{BIAS} = V_{BE3} + V_{BE4} = V_T \ln\left(\frac{I_Q^2}{I_{S3}I_{S4}}\right)$$

➢ *I_Q, I_{S3}, and I_{S4} chosen such that $V_{BIAS} \approx 2V_\gamma$*

➢ *Note*: *V_{BIAS} is also equal to ($V_{BE1} + V_{EB2}$)*

$\Rightarrow$ *Q_1-Q_2 remain at the verge of conduction*, *carrying a standby (or idling) current $I_{Standby}$*

➤ This ***extra current*** of $(I_Q + I_{standby})$ causes *standby* (or *idling*) power dissipation

➤ Noting that:

$$V_{BIAS} = V_{BE1} + V_{BE2} = V_T \ln\left(\frac{I^2_{Standby}}{I_{S1}I_{S2}}\right)$$

$$\Rightarrow I_{standby} = I_Q\sqrt{\frac{I_{S1}I_{S2}}{I_{S3}I_{S4}}}$$

➤ Now, ***Q_1-Q_2 has to supply/sink large amount of current to/from load*** $\Rightarrow$ *Their BE junction areas are made large* $\Rightarrow$ *Large I_{S1}-I_{S2}*

➢ *I_{S1}-I_{S2} typically 10 times or more than I_{S3}-I_{S4}*

$\Rightarrow$ *$I_{standby} \geq 10 I_Q$*

$\Rightarrow$ *Adds to the power*

overhead of the circuit

➢ *Another option of*

prebias circuit:

- ■ *V_{BE}-Multiplier*
- ■ *$V_{BIAS} = V_{BE3}(1 + R_2/R_1)$*
- ■ *Values of R_1 and R_2*

chosen to give

$V_{BIAS} = 2V_\gamma$