EE 381: DIGITAL CIRCUITS AND MICROPROCESSORS
2025-2026/II

EXPERIMENT 2
PRBS & SEQUENCE GENERATORS USING SHIFT REGISTERS

1. 74194: 4-BIT UNIVERSAL SHIFT REGISTER

Familiarize yourself with the Function Table of the 74LS194 Shift Register.

2. PRBS GENERATOR (Length=15) WITH SELF-STARTING

PRBS (Psuedo Random Bit Sequences, also called as Maximal Length sequences or ML sequences) are very commonly used as a test signal for evaluating digital communication links. They are very easily generated and at the receiving end the original sequence can be regenerated by loading one word from the received sequence. PRBS sequences are generated using shift registers and EX-OR gates. An N-bit shift register can generate a sequence of length 2^N-1. The total number of '1s' and '0s' in these sequences differ by just 1. For example, a sequence of length 15 will have either 8 ones and 7 zeros or 8 zeros and 7 ones. Hence for large N the number of ones and zeros are nearly the same. PRBS/ML sequences have several interesting properties. PRBS with N=15 is the most commonly used test sequence for link evaluation.

Questions: (i) These sequences are difficult to trigger and see on a CRO, for large N. Why? Suggest a solution to this problem.

(ii) From what is written above suggest how you would use such a sequence to measure the BER (bit error rate) of a digital communication system.

Lab Preparation and Experiment

(a) Design a PRBS generator of length of 15, using 74LS194. Choose the shift-right mode and make $D_{SR} = Q_2 \oplus Q_3$. Make a provision to automatically parallel load a non-zero state, whenever the output state is '0000'. You will be given 7486 and 7432 ICs in addition to the 74LS194.

(b) Write the sequence of states of your PRBS design before coming to the laboratory. Using manual clock and four LEDs verify that the circuit is giving the designed sequence and all the 15 states. Load '0000' and test the self-start capability of your design.

(c) Use the TTL output of the Function Generator (FG) and use a clock frequency in the range 50-500 kHz. Observe the PRBS outputs and sketch one of the outputs with respect to the clock.

3. PRBS GENERATOR (Length=7) WITH SELF-STARTING

Make a simple modification to the previous circuit such that $D_{SR} = Q_1 \oplus Q_2$. As in the previous case, make a provision to auto-load a non-zero state in case of a '000' state. Observe the outputs using manual clock. Using a TTL clock from the FG, observe and sketch one of the output waveforms.

4. SEQUENCES OF DIFFERENT LENGTHS

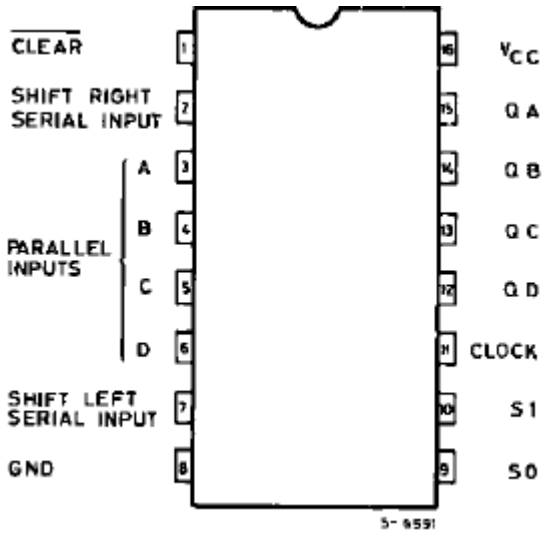
It is possible to alter the length of a PRBS sequence by some additional logic. This is generally done by decoding a state and inverting the D_{SR} bit whenever that state occurs.

Lab Preparation and Experiment

Make suitable modifications to the circuit in Part-2, so that the bit D_{SR} is inverted whenever a given state appears. For each of the following three cases, design a circuit which will decode the indicated state and invert the D_{SR} bit of your design (in Part-2) whenever that state occurs. For each of these cases, write the modified sequence of states. Use 7420 Dual 4-input NAND and 7486 Quad 2-input EX-OR ICs for implementing the decoder and inversion.

States to be decoded '$Q_0Q_1Q_2Q_3$': (i) 1000 (ii) 1100 (iii) 0101

4 BIT UNIVERSAL SHIFT REGISTER IC 74LS194



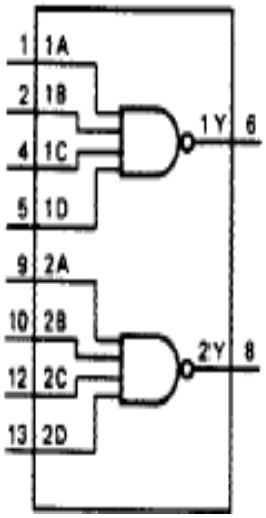
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{CLEAR}$	Asynchronous Reset Input (Active LOW)
2	SR	Serial Data Input (Shift Right)
3, 4, 5, 6	A to D	Parallel Data Input
7	SL	Serial Data Input (Shift Left)
9, 10	S0, S1	Mode Control Inputs
11	CLOCK	Clock Input (LOW to HIGH Edge-triggered)
15, 14, 13, 12	QA to QD	Paralle Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

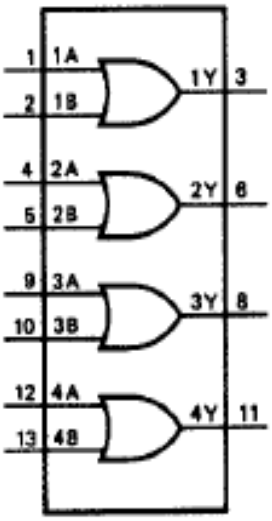
TRUTH TABLE

INPUTS										OUTPUS			
$\overline{CLEAR}$	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	⎣	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	⎍	X	X	a	b	c	d	a	b	c	d
H	L	H	⎍	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	⎍	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	⎍	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	⎍	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

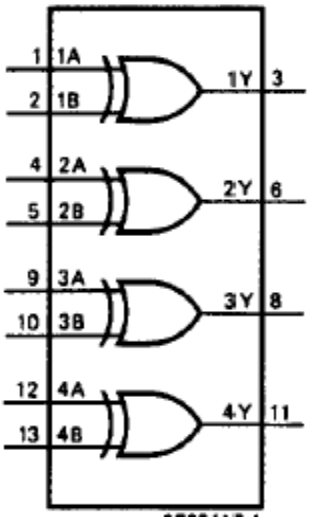
X: Don't Care : Don't Care
a ~ d : The level of steady state input voltage at input A ~ D respactively
QA0 ~ QD0 : No charge
QAn ~ QDn : The level of QA, QB, QC, respectively, before the mst recent positive transition of the clock.



7420 Dual 4-i/p NAND IC



7432 Quad 2-i/p OR IC



7486 Quad 2-i/p EX-OR IC

Note: For the above ICs (IC 7420, IC 7432 , and IC 7486) Pin 14 is Vcc and Pin 7 is GND