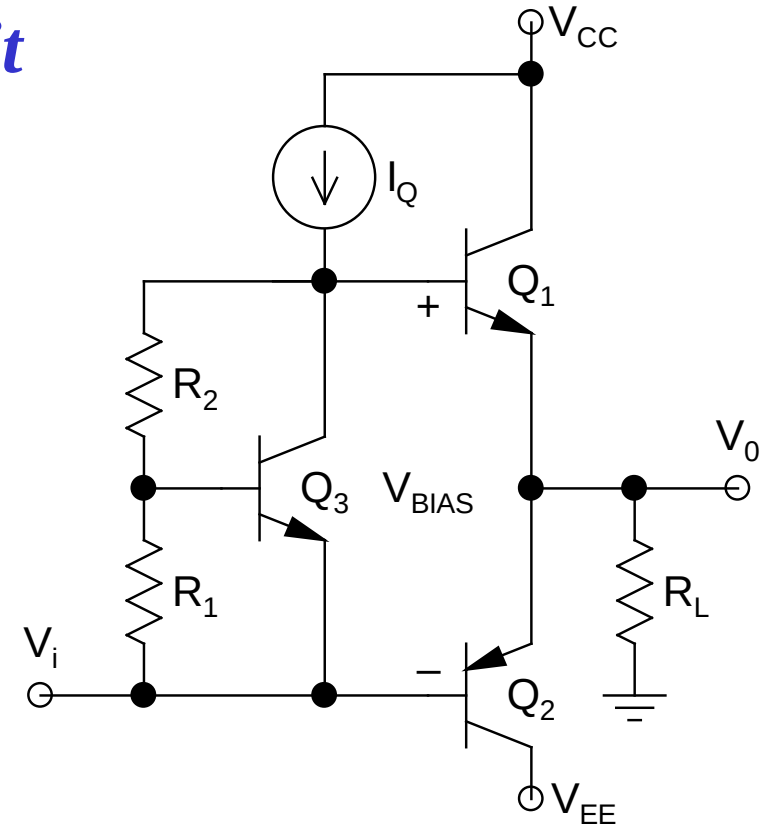
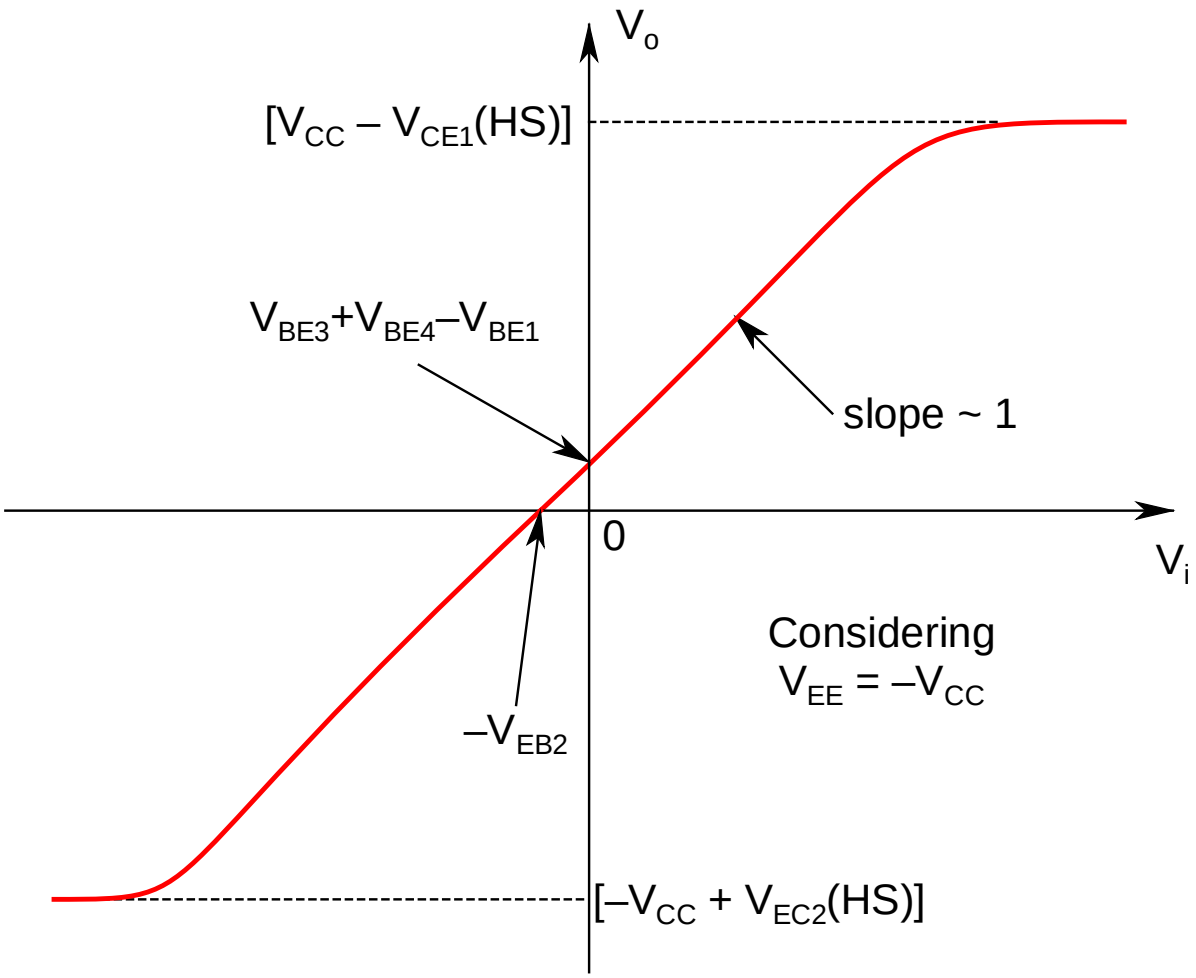
- I_{S1}-I_{S2} typically 10 times or more than I_{S3}-I_{S4}

  $\Rightarrow I_{standby} \geq 10I_Q$

  $\Rightarrow$ Adds to the power overhead of the circuit

- Another option of prebias circuit:
  - V_{BE}-Multiplier
  - $V_{BIAS} = V_{BE3}(1 + R_2/R_1)$
  - Values of R_1 and R_2 chosen to give $V_{BIAS} = 2V_\gamma$





The Voltage Transfer Characteristic (VTC)

- ***The VTC does not pass through origin***
- ***Intercepts*** (known as ***input-output offset***):
  - $V_i = 0$, $V_o = V_{BE3}+V_{BE4}-V_{BE1}$
  - $V_o = 0$, $V_i = -V_{EB2}$
- ***For $V_i > -V_{EB2}$, $V_{be1}\uparrow$ and $V_{eb2}\downarrow$, with their sum remaining constant at V_{BIAS}***

  $\Rightarrow$ ***Q_1 starts to conduct and supply current to the load*** (R_L), while ***Q_2 starts to go deeper into cutoff***

  $\Rightarrow$ ***V_o starts to follow V_i with a slope ~1*** (***CC stage***)

- ***V_o can rise all the way up to $[V_{CC} - V_{CE1}(HS)]$, provided that V_i can drive it that far***
- Similarly, ***for $V_i < -V_{EB2}$, V_{eb2} ↑ and V_{be1} ↓, with their sum again remaining constant at V_{BIAS}***

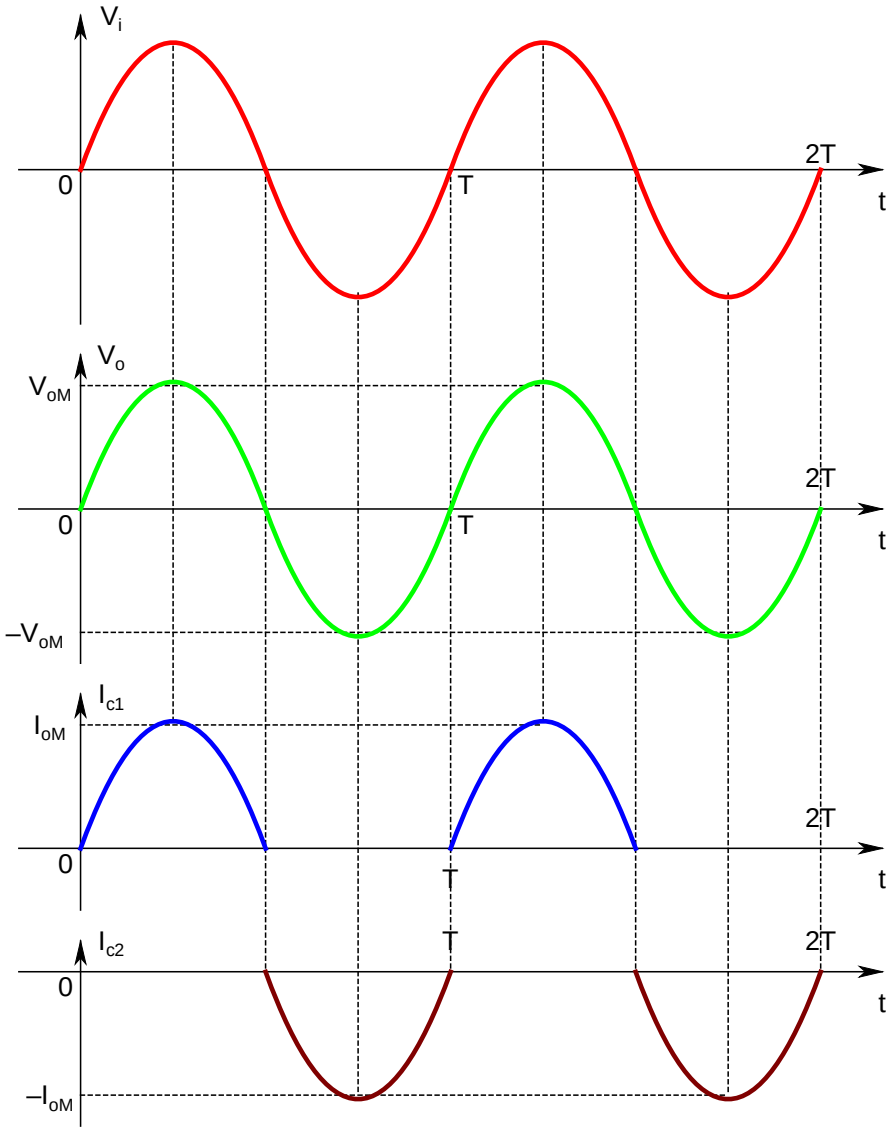
  $\Rightarrow$ ***Q_2 starts to conduct and pull current away from the load*** (R_L), while ***Q_1 starts to go deeper into cutoff***

  $\Rightarrow$ ***V_o again starts to follow V_i with a slope ~1***, and ***can go down all the way to $[V_{EE} + V_{EC2}(HS)]$***

➢ *Power Output and Efficiency*:

- Refer to the figure in the next slide
  - ❖ *The constant offset of $|V_{EB2}|$ is neglected*
- ***Both transistors are not ON over the entire cycle***
  - ❖ ***Q_1 takes care of the positive half cycle***
  - ❖ ***Q_2 takes care of the negative half cycle***
- V_{oM}: ***Maximum value of V_o***
  - ❖ ***Maximum possible swing between $[V_{CC} - V_{CE1}(HS)]$ and $[V_{EE} + V_{EC2}(HS)]$***
- I_{oM}: ***Maximum value of load current*** $(= V_{oM}/R_L)$
- ***Average rms power P_L delivered to load***:

$$P_L = \frac{V_{oM}}{\sqrt{2}} \times \frac{I_{oM}}{\sqrt{2}} = \frac{V_{oM}^2}{2R_L}$$


V_i
0
T
2T
t
V_o
V_{oM}
$-V_{oM}$
I_{c1}
I_{oM}
I_{c2}
$-I_{oM}$

- Now, we need to calculate the ***power supplied to the stage by the power supplies***
- The ***average current I_{supply} drawn by Q_1 from V_{CC}*** (***happens only during the positive half cycle***):

$$I_{supply} = \frac{1}{T}\int_0^T I_{c1}(t)dt = \frac{1}{2\pi}\int_0^{\pi} I_{oM}\sin\theta d\theta = \frac{I_{oM}}{\pi} = \frac{V_{oM}}{\pi R_L}$$

- ***The same current will also be pushed by Q_2 to V_{EE} ($= -V_{CC}$) during the negative half cycle***
- ***Thus, over a complete cycle, the average supply power P_{supply} drawn from the power supplies***:

$$P_{supply} = 2V_{CC}I_{supply} = 2V_{CC}V_{oM}/(\pi R_L)$$

- Thus, the ***power conversion efficiency*** (η):

$$\eta = \frac{P_L}{P_{supply}} = \frac{V_{oM}^2 / (2R_L)}{2V_{CC}V_{oM} / (\pi R_L)} = \frac{\pi V_{oM}}{4V_{CC}}$$

- ***η directly proportional to V_{oM}***, and ***independent of R_L***

  $\Rightarrow$ ***Significant advantage***

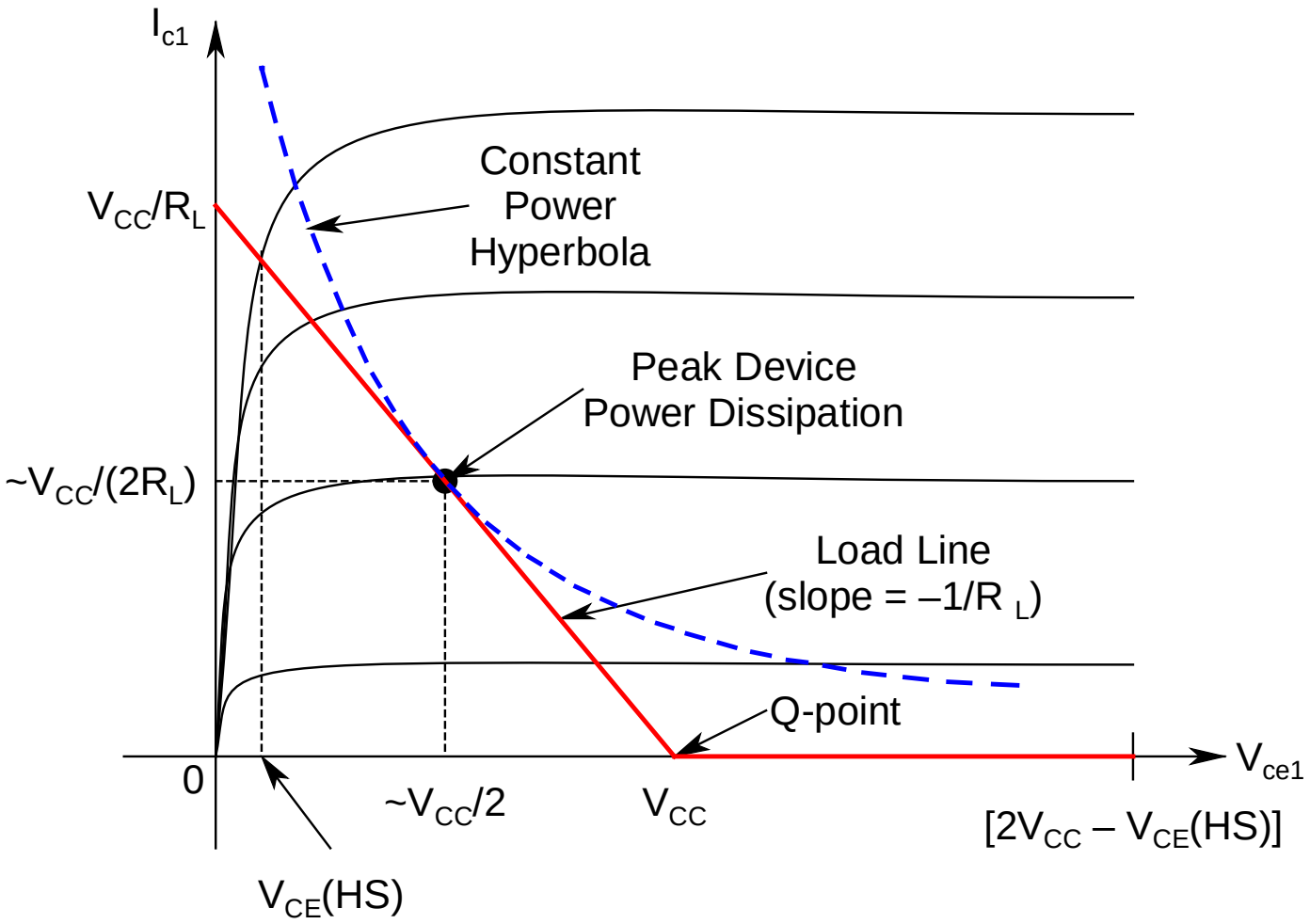
- Also, ***$V_{oM}(max) \approx V_{CC}$***

  $\Rightarrow$ ***$\eta_{max} = \pi/4 = 0.785$ (or 78.5%)***

- ***This value may not be attainable in practice***
  - ***For $V_{oM} = -V_{CC}$, V_i has to be less than $-V_{CC}$***, which ***may not be practically achievable***
  - This analysis ***neglects the standby power*** (***quite small though***) $\Rightarrow$ ***Inclusion of this term will reduce η_{max}***

➢ *Transistor Ratings*:

- Specified by *two parameters*:
  - ❖ ***Breakdown Voltage***
  - ❖ ***Maximum Power Rating***
- ***Breakdown Voltage***:
  - ❖ ***Maximum positive/negative V_{CE} that can be applied to an npn/pnp BJT***
    - o Known as the ***Collector-to-Emitter Breakdown Voltage with Base Open*** (BV_{CE0})
  - ❖ ***Focus on Q_1*** (***Q_2 will be similar***)
  - ❖ Refer to the diagram in the next slide (***Output characteristic of Q_1 along with the load line***)
  - ❖ In the analysis, the ***offset in the VTC***, the ***small standby current***, and ***V_{CE1}(HS)*** are ***neglected***



The Output Characteristics of Q_1 along with the Load Line

- ***At Q-point***: $V_o = 0 \Rightarrow V_{ce1} = V_{CC}$
- ***During positive half cycle***:

  $V_o(max) \approx V_{CC} \Rightarrow V_{ce1} \approx 0$

  $\Rightarrow$ ***V_{ce1} ranges between 0 and V_{CC} during the positive half cycle***
- The ***slope of the load line*** in this part of the characteristic = $-1/R_L$
- ***For negative half cycle***, ***Q_1 cuts off*** (***Q_2 conducts during this period***)

  $\Rightarrow$ ***$I_{c1} = 0$ for V_o ranging between 0 and $-V_{CC}$***

  $\Rightarrow$ ***$V_{ce1}(max) = 2V_{CC}$***

  $\Rightarrow$ ***$BV_{CE0} = 4V_{CC}$*** [using a ***Safety Factor*** (or ***Factor of Safety***) of 2] (***same for Q_2***)

- ***Maximum Power Rating***:
  - ***Same for both Q_1 and Q_2***
  - ***Average power P_L delivered by Q_1 to R_L during the positive half cycle*** = ***area covered under the load line***

$$\Rightarrow P_L = \frac{1}{2} \times V_{CC} \times \frac{V_{CC}}{R_L} = \frac{V_{CC}^2}{2R_L}$$

  - Refer to the ***constant power hyperbola*** ($V_{ce1} \times I_{c1}$) shown in the figure
  - ***Maximum power dissipation of Q_1 happens when this hyperbola becomes tangent to the load line***, ***which is right at the middle of the load line***
  - ***Proof***:

Constant power hyperbola (P_1):

$$P_1 = V_{ce1} \times I_{c1} = \left(V_{CC} - I_{c1}R_L\right) \times I_{c1} = V_{CC}I_{c1} - I_{c1}^2 R_L$$

Plug $dP_1/dI_{c1} = 0$ to get $I_{c1} = V_{CC}/(2R_L)$

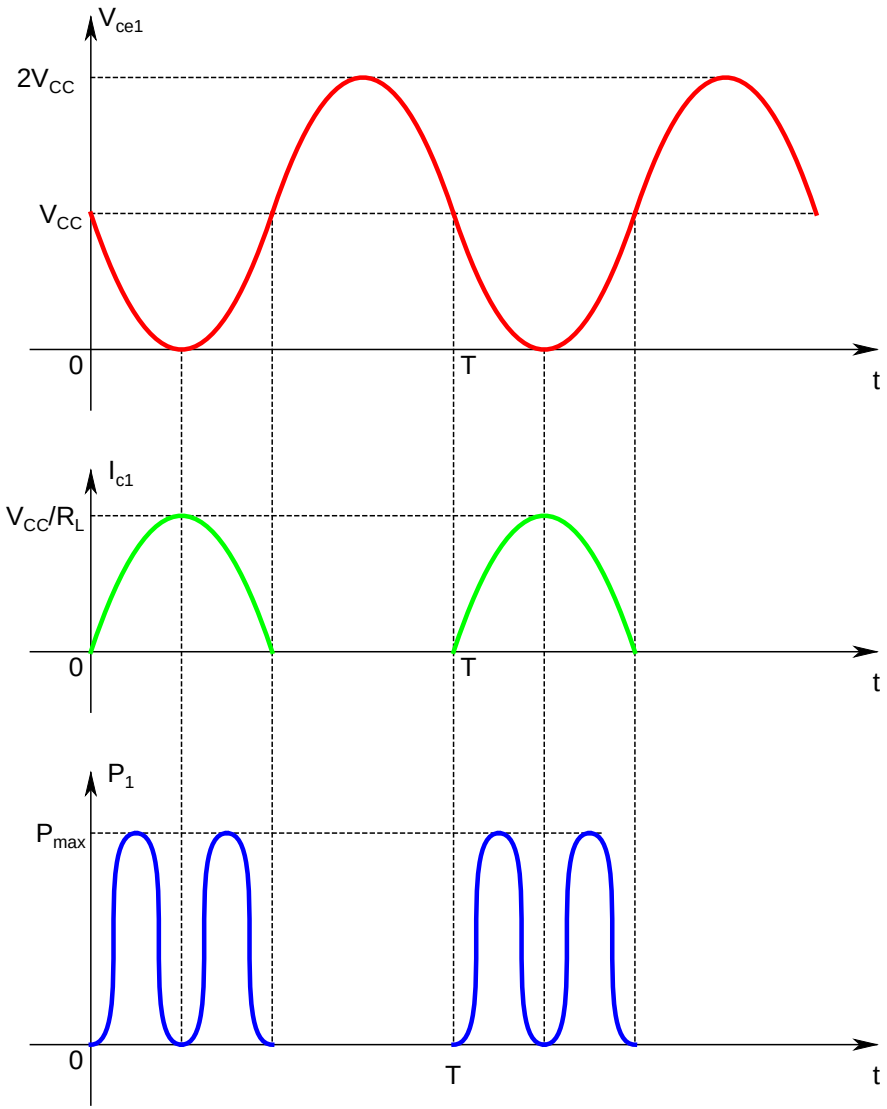
This is the ***mid-point of the load line***, with ***coordinates*** $[V_{CC}/2, V_{CC}/(2R_L)]$

$$\Rightarrow P_{max} = \frac{V_{CC}^2}{2R_L} \quad (\textbf{\textit{using a Safety Factor of 2}})$$

- There is also ***idling power***:

  $P_{idling} = 2V_{CC}I_{standby} + (V_{CC} - V_I)I_Q$

- In general, $P_{max} >> P_{idling}$
- Refer to the figure in the next slide
  - V_{ce1} ***oscillates between 0 and*** $2V_{CC}$
  - I_{c1} ***appears only during the positive half cycle***, ***with peak value of*** V_{CC}/R_L (***when*** $V_{ce1} = 0$)
  - P_1 $(= V_{ce1} \times I_{c1})$ ***oscillates*** between 0 and $V_{CC}^2/(4R_L)$ at ***twice the frequency*** only during the ***positive half cycle***


V_{ce1}
$2V_{CC}$
V_{CC}
0
T
t
I_{c1}
V_{CC}/R_L
0
T
t
P_1
P_{max}
0
T
t

- ***Two Special Cases***:
  - $R_L \rightarrow \infty$ (***open-circuit***):

    Load line becomes horizontal with $I_{c1} = 0$

    $\Rightarrow P_1 = 0 \Rightarrow$ ***no issue***
  - $R_L = 0$ (***short-circuit***):

    Load line becomes vertical with $I_{c1} \rightarrow \infty$

    Potentially dangerous situation

    Resulting power dissipation and consequent heat generation can completely damage the device
- ***In actual situation***, ***I_{c1} won't reach infinite value due to***:
  - ***Limited current driving capability of the driver stage***
  - ***Fall of β at high current levels*** due to ***High-Level Injection*** or ***Kirk Effect***
- These two are ***in-built self-protection mechanisms***
- Nevertheless, ***practical output stages need short-circuit protection***

➢ *Linearity and Output Resistance*:

- *While supplying/sinking current to/from load*, *Q_1/Q_2 operate in CC mode*

  $\Rightarrow A_v = R_L/(R_L + r_{Ei})$ $(i = 1,2)$ $(r_{Ei} = V_T/I_{ci})$

- Thus, if ***$R_L >> r_{Ei}$***, then ***$A_v \rightarrow 1$***, and ***very high linearity in the VTC can be achieved***
- However, ***r_{Ei} is not constant*** - rather ***it changes with the load current***
- Thus, ***A_v can depart significantly from unity***, when the ***load current is very small*** (***large r_{Ei}***)
- Referring to the ***VTC***, the ***slope of the characteristic near $\pm V_\gamma$*** will be ***significantly less than unity***