EE-380 EC Lab-07
Compensation in Multi-Stage Amplifiers

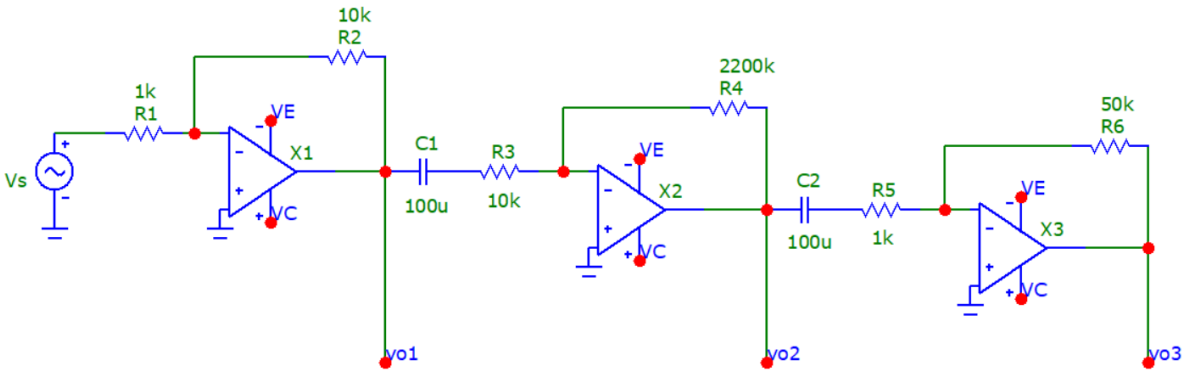
28th Oct 2025

Name: Ronit Kumar
Roll No.: 230875
Lab Partner: Rushabh Pandya (230732)
Section: C

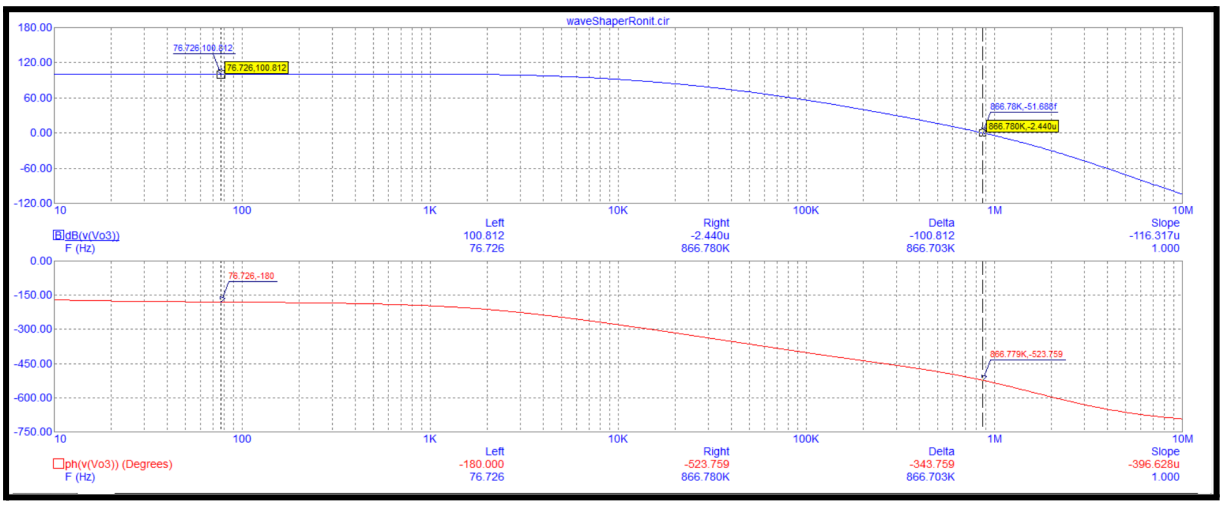
---

1 Study gain and phase margin for final output Vo3 using simulation and experimental measurements

1.1 Pre Lab



Frequency response of the above amplifier:



At a first glance it can be seen that the phase margin is negative and negative phase margin implies instability.

Phase margin PM is given by:

$PM = \phi(\omega_{gc})$; *where* ω_{gc} *is the gain crossover frequency*

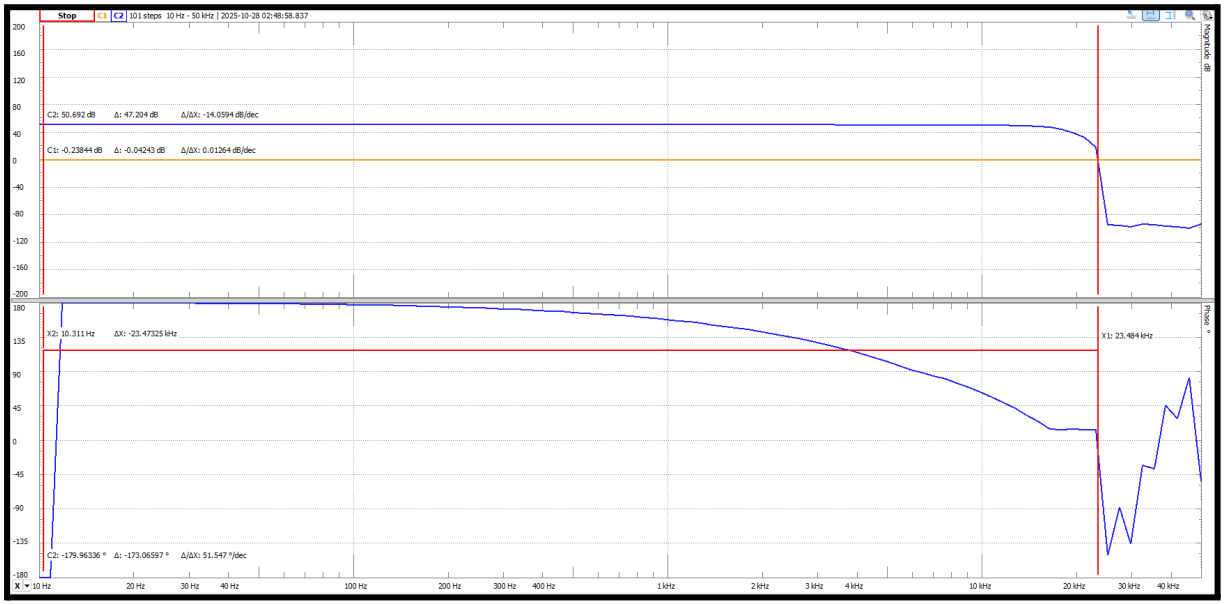
$\Rightarrow PM = -523.759 \; or \; -523.756 + 360$

$\Rightarrow PM = -163.759^{o}$

Gain margin is the gain where phase crosses -180 degrees

$\Rightarrow GM = 100.812\text{dB}$

1.2 In Lab



PM = -180 - (-173) = -7 $\Rightarrow PM \simeq -7^{o}$ and $GM = 50.7dB$

Both PM and GM are not satisfying the conditions for stability, hence this is an unstable system.

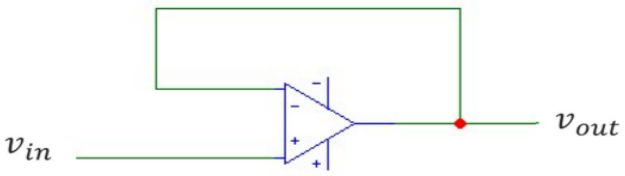
1.3 Post Lab

Note :

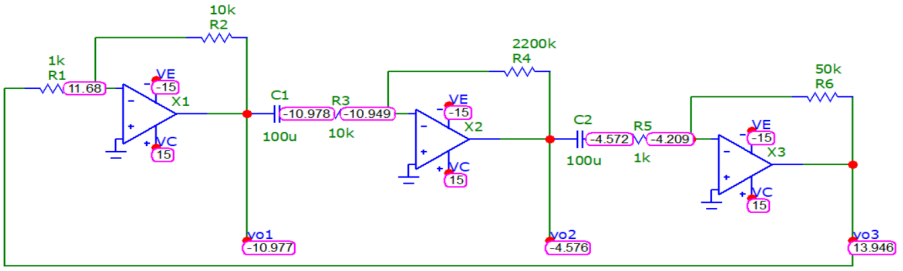
For unconditionally stable system **GM must be negative,** and **PM must be positive**

Hence this system is very unstable and goes into oscillation even when no input is applied.

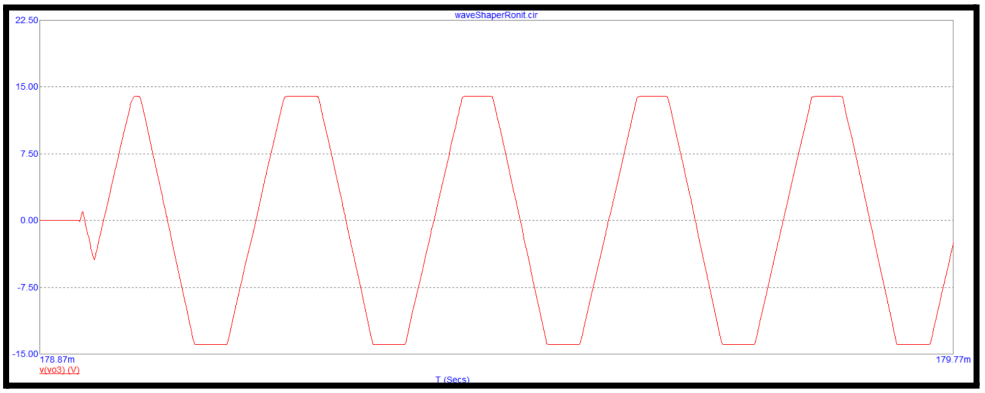
2 Make a unity gain buffer and study the oscillation for zero input voltage



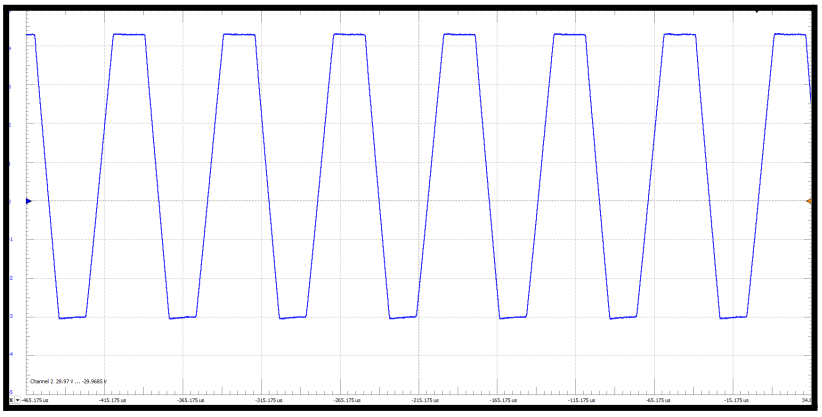
2.1 Pre Lab



V_{in}=0V or ground



2.2 In Lab

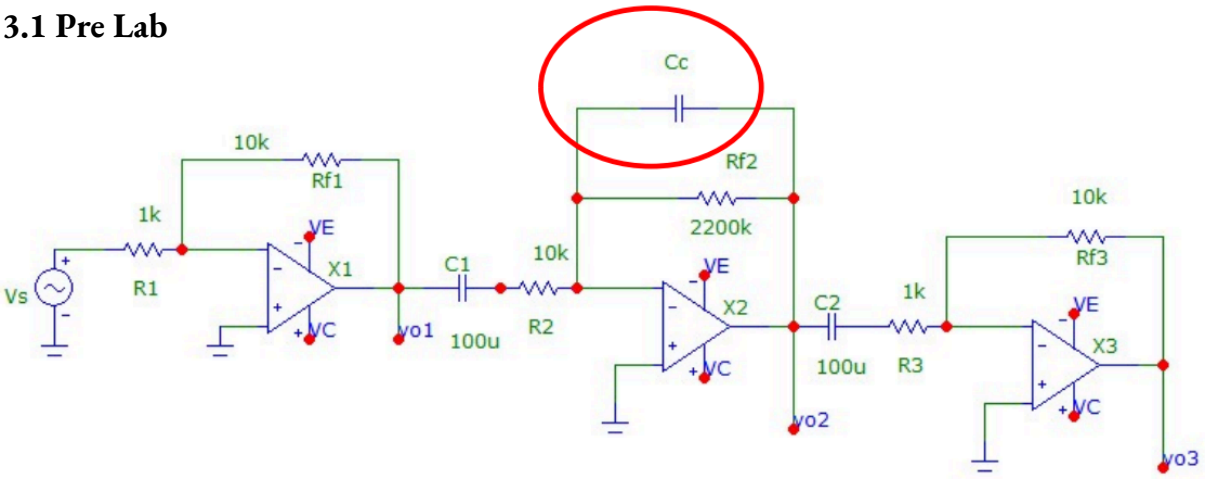


2.3 Post Lab

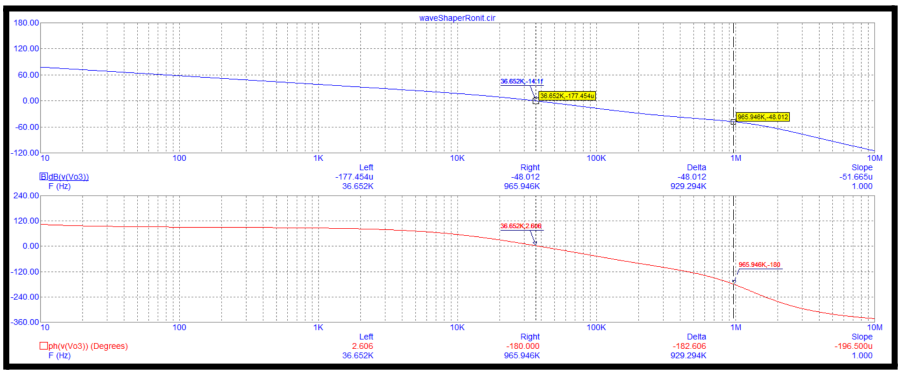
The output oscillates across the full supply range of the op-amp, from +5 V to −5 V, even with no input applied. This indicates that the system is unstable.

3 Add suitable compensation capacitor to the circuit and study new Gain/Phase margins

3.1 Pre Lab



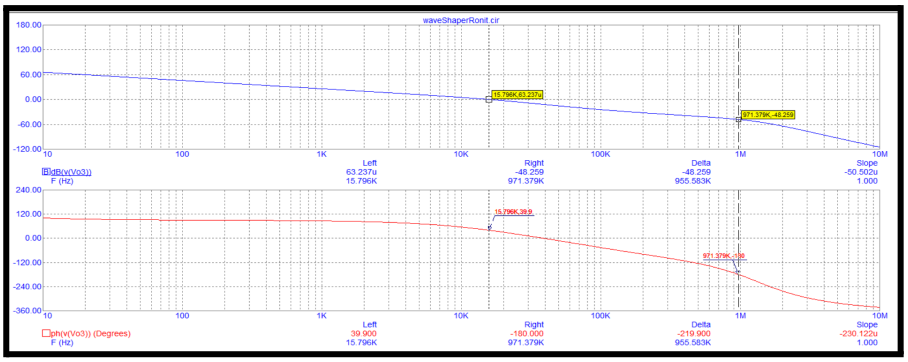
$C_C = 0.1\mu F$



$\Rightarrow PM = 2.60^o$

$\Rightarrow GM = -48.012$

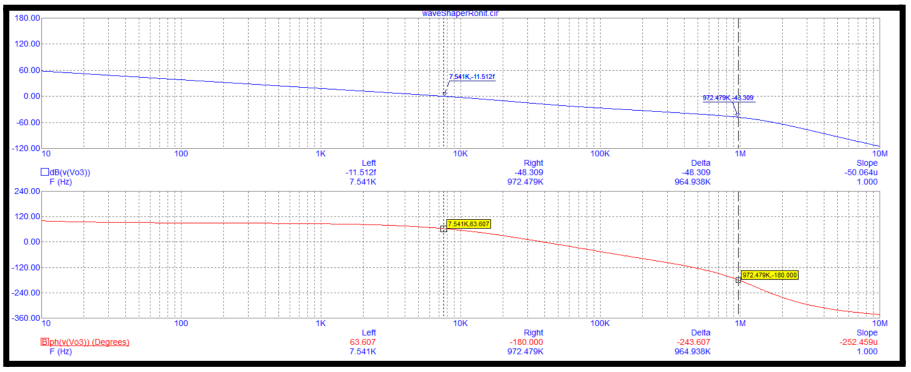
$C_C = 0.4\mu F$



$\Rightarrow PM = 39.9^o$

$\Rightarrow GM = -48.259$

$C_C = 1\mu F$



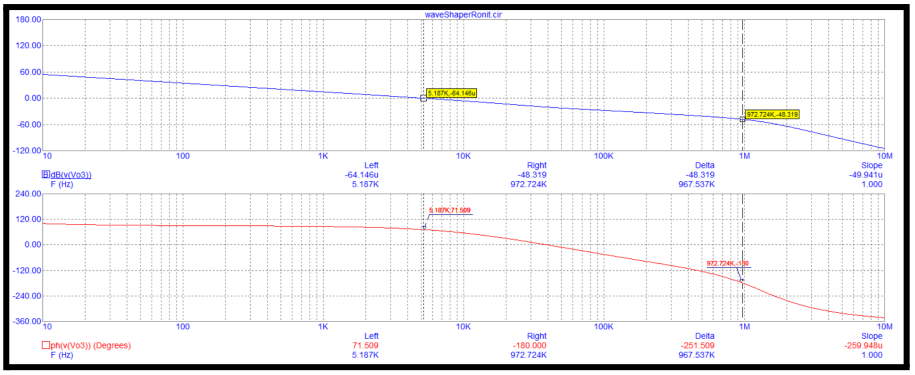
$\Rightarrow PM = 63.607^o$

$\Rightarrow GM = -48.309$

C_C=1.5μF

$\Rightarrow PM = 71.509^o$

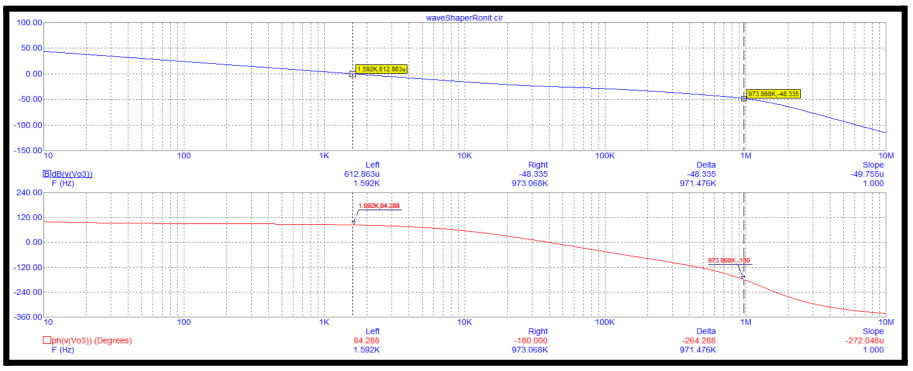
$\Rightarrow GM = -48.319$



C_C= 5μF

$\Rightarrow PM = 84.288^o$

$\Rightarrow GM = -48.335$

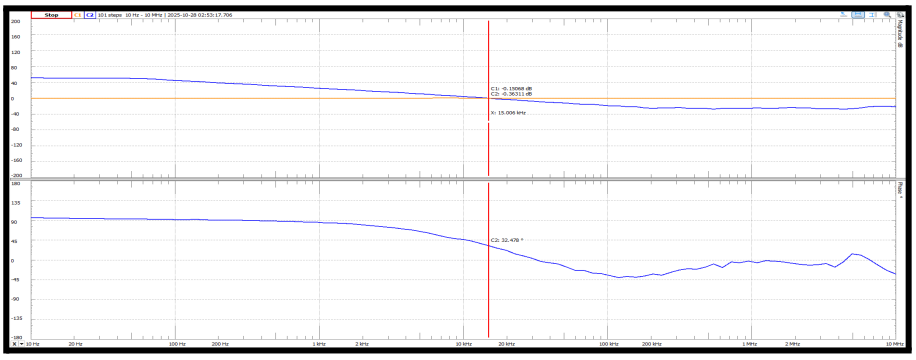


3.2 In Lab

C_C = 0.5μF

$\Rightarrow PM = 32.5^o$

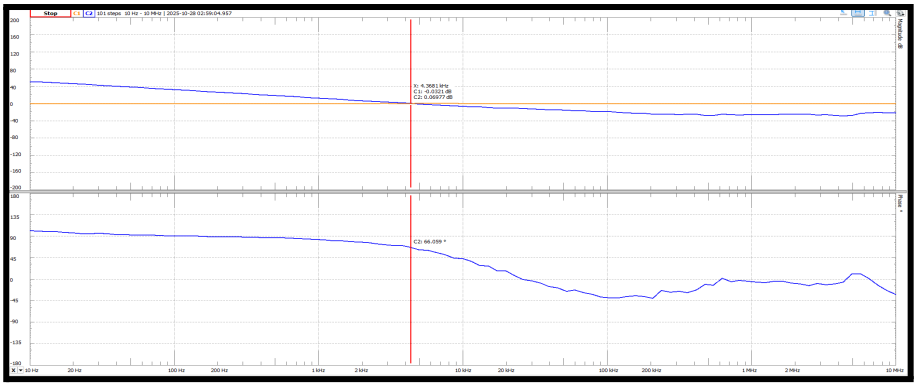
$\Rightarrow GM = NA$



C_C = 1μF

$\Rightarrow PM = 66.1^o$

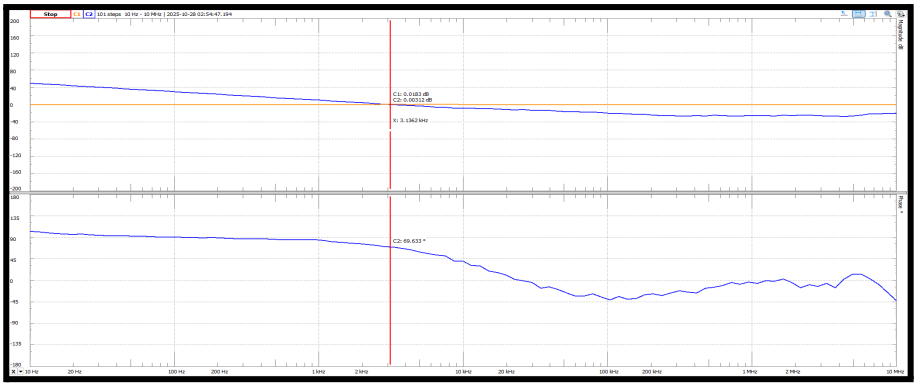
$\Rightarrow GM = NA$



$C_C = 1.72\mu F$

$\Rightarrow PM = 69.6^o$

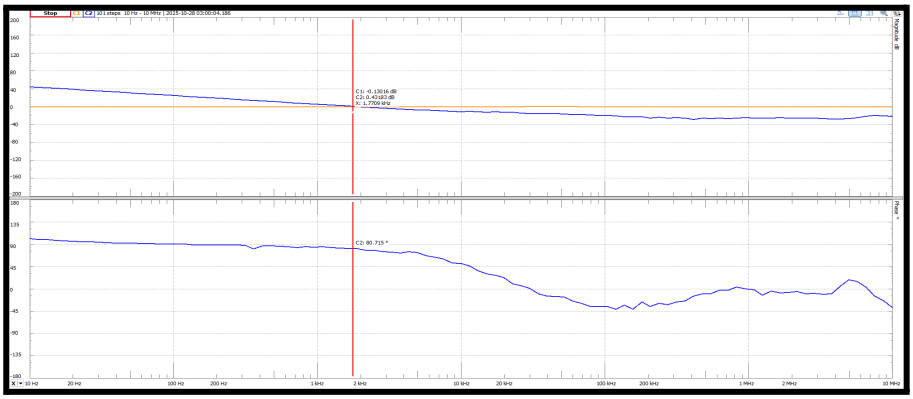
$\Rightarrow GM = NA$



$C_C = 5\mu F$

$\Rightarrow PM = 80.7^o$

$\Rightarrow GM = NA$



***Note:** *"NA"* in GM implies that the Bode Phase plot doesn't appear to cross -180° in the stable/operating ranges of frequency.

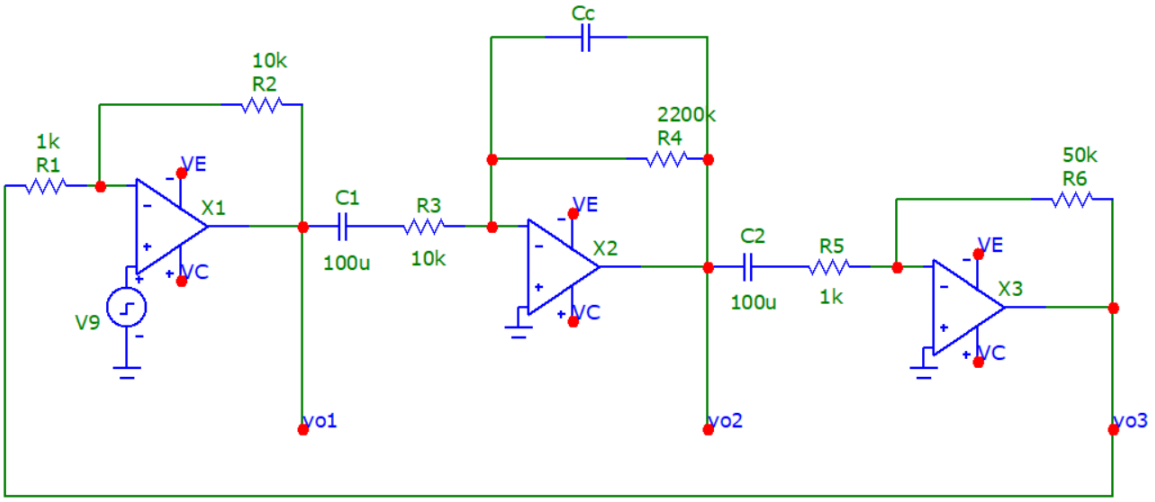
3.3 Post Lab

From the prelab analysis, phase margins of approximately 60°–70° appeared to give the best performance. Therefore, we tested several capacitor combinations in the lab. Among them, these four cases were recorded, as the fourth part of the lab was carried out first to identify which capacitor values produced the desirable response. The selected four results illustrate the full range of system behavior :-

from damped oscillations, to slight overshoot, to an ideal response with no overshoot and short settling time, and finally to the extreme case of very slow settling.

4 Correlate phase margin with overshoot and settling time of unity gain buffer obtained by connecting output vo6 to input and driving it with 1V square wave

4.1 Pre Lab



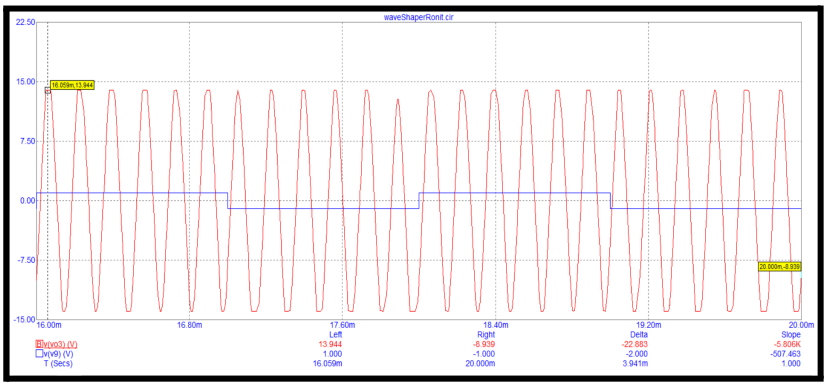
C_C=0.1μF

$\Rightarrow PM = 2.606^o$

$\Rightarrow GM = -48.012$

$\Rightarrow Overshoot = 1294\%$ from 1V

$\Rightarrow Settling\ time = doesn't$ settle for 0.5kHz square wave



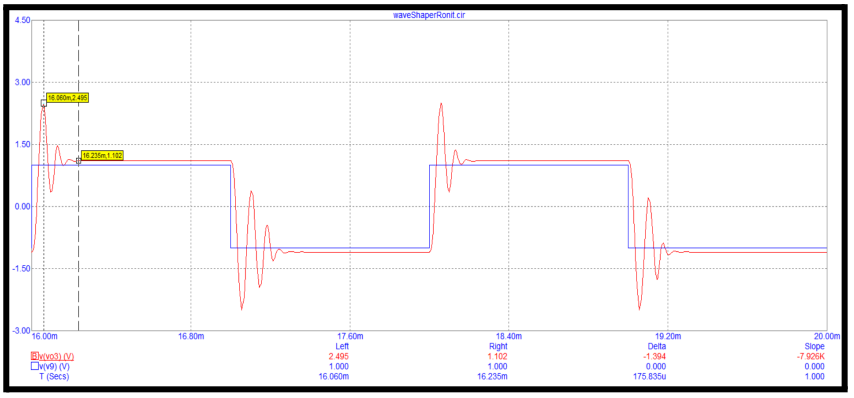
C_C=0.4μF

$\Rightarrow PM = 39.9^o$

$\Rightarrow GM = -48.259$

$\Rightarrow Overshoot = 139.3\%$

$\Rightarrow Settling\ time = 0.235ms$



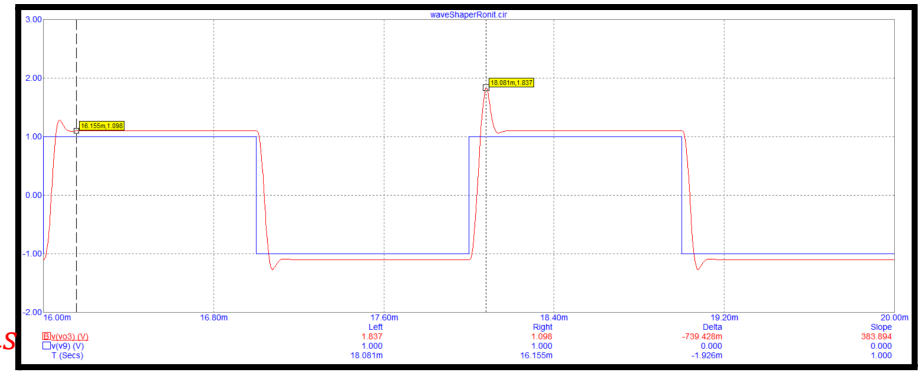
C_C=1μF

$\Rightarrow PM = 63.607^o$

$\Rightarrow GM = -48.309$

$\Rightarrow Overshoot = 73.9\%$

$\Rightarrow Settling\ time = 0.155ms$



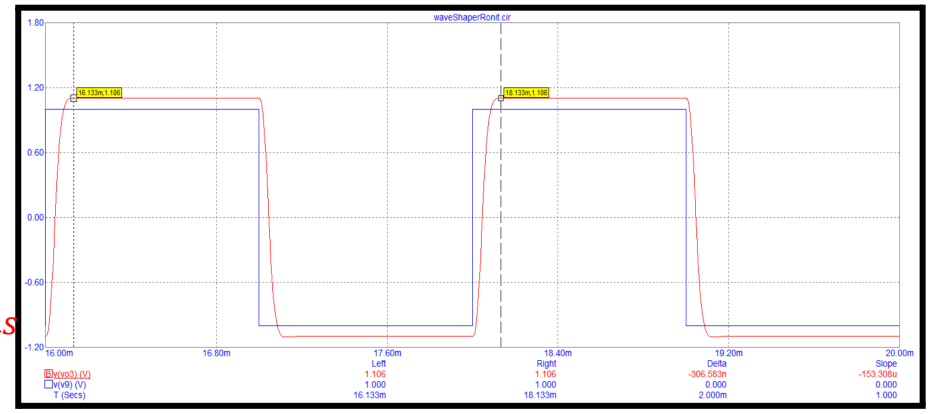
C_C=1.5μF

$\Rightarrow PM = 71.509^o$

$\Rightarrow GM = -48.319$

$\Rightarrow Overshoot = 0\%$

$\Rightarrow Settling\ time = 0.133ms$



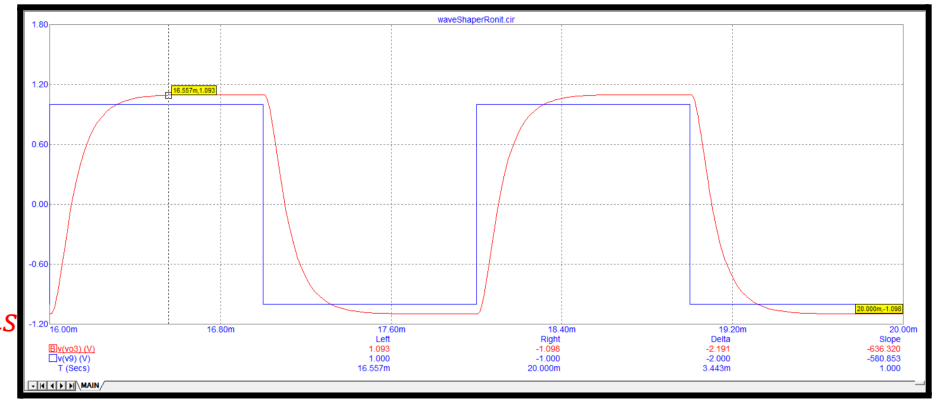
C_C=5μF

$\Rightarrow PM = 84.288^o$

$\Rightarrow GM = -48.335$

$\Rightarrow Overshoot = 0\%$

$\Rightarrow Settling\ time = 0.557ms$



4.2 In Lab

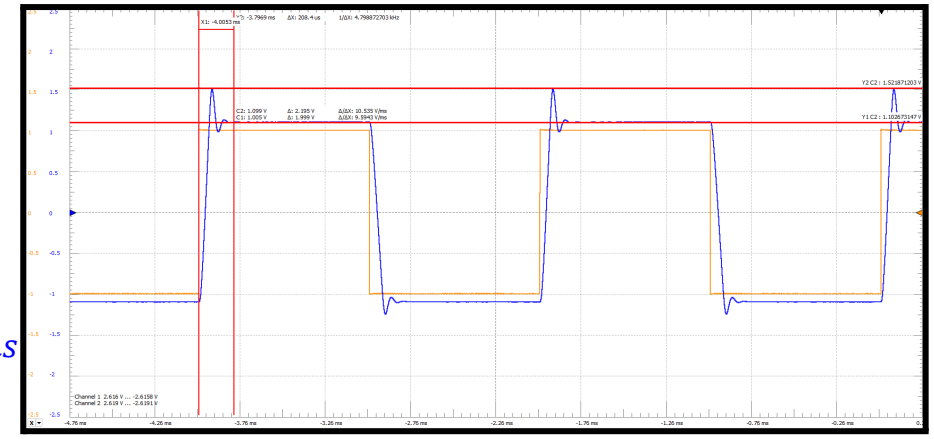
C_C=0.5μF

$\Rightarrow PM = 32.5^o$

$\Rightarrow GM = NA$

$\Rightarrow Overshoot = 38.2\%$

$\Rightarrow Settling\ time = 0.208ms$



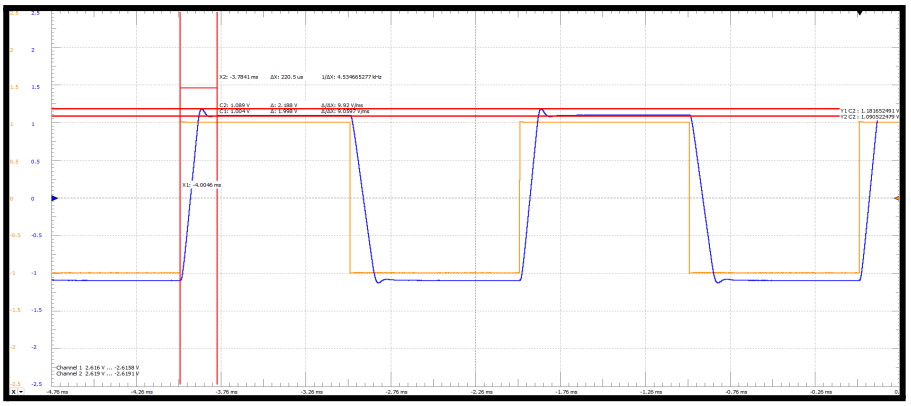
C_C=1μF

$\Rightarrow PM = 66.1^o$

$\Rightarrow GM = NA$

$\Rightarrow Overshoot = 7.27\%$

$\Rightarrow Settling\ time = 0.220ms$



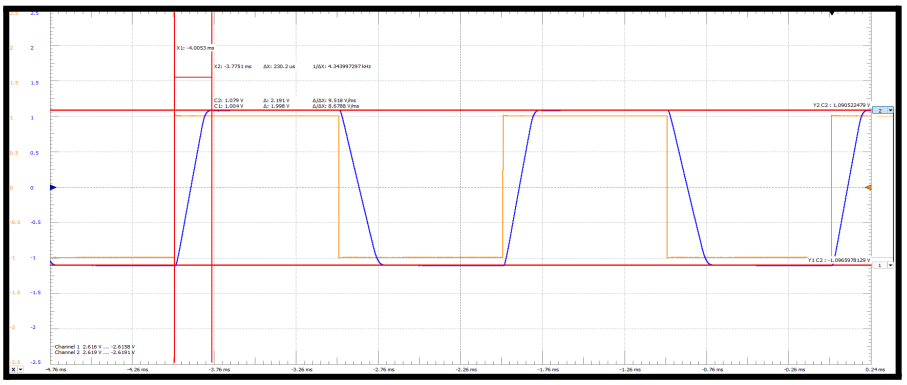
C_C=1.72μF

$\Rightarrow PM = 69.6^o$

$\Rightarrow GM = NA$

$\Rightarrow Overshoot = 0\%$

$\Rightarrow Settling\ time = 0.230ms$



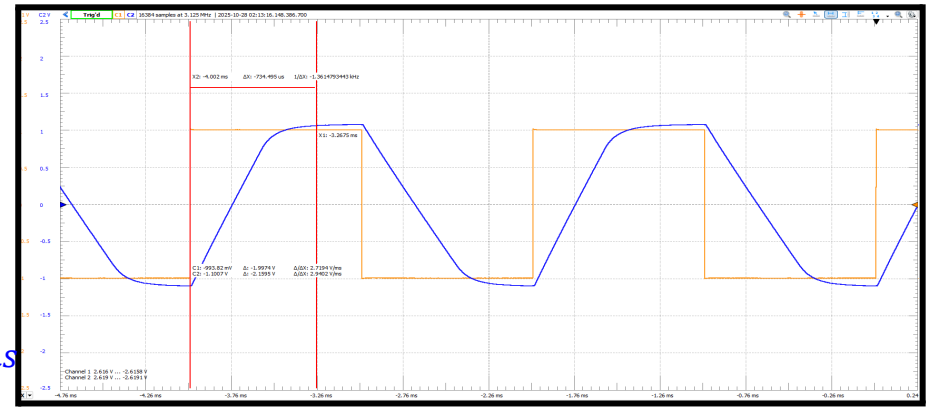
C_C=5μF

$\Rightarrow PM = 80.7^o$

$\Rightarrow GM = NA$

$\Rightarrow Overshoot = 0\%$

$\Rightarrow Settling\ time = 0.734ms$



4.3 Post Lab

From the simulation and lab experiment we come to the following conclusion

Phase Margin	**Overshoot**	**Settling time**
~ 0°-55°	Very large (can even be more than 100%) **Poorly damped**	It is large due to the oscillations (ringing) and it decreases as we increase the phase margin
~ 55°-70°	Very less or even 0%, this seems to be the optimum region. **Optimum damping**	Settling time reduces with increasing phase margin and reaches its optimum here. Low settling time and less overshoot can be seen in this region.
PM>70°	Now the capacitors take more time to charge and discharge, the overshoot is negligible, instead the response never reaches the target value if the phase margin is large. **Over damped**	Now the settling time starts to increase as we increase the phase margin, as the response becomes sluggish due to large capacitances being added.