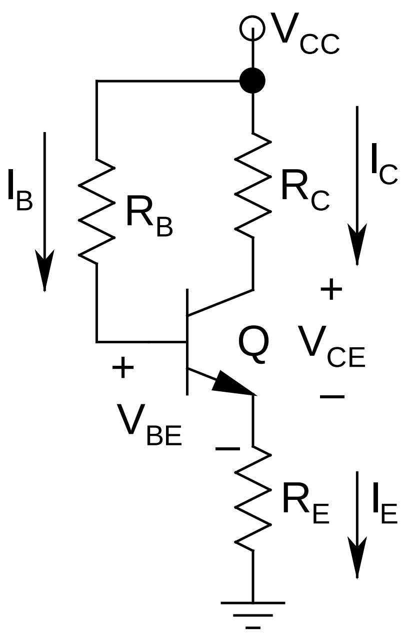
- ***Emitter Feedback Bias***:
  - ***While writing KVL, never take CE or BC loops, since V_{CE} and V_{BC} are not known***
  - ***Consider only BE loops with V_{BE} = 0.7 V***
  - $V_{CC} = I_B R_B + V_{BE} + I_E R_E$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$



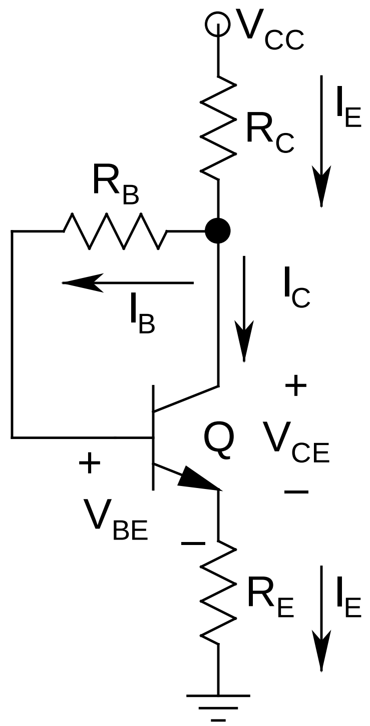
- $I_C = \beta I_B$
- $V_{CE} = V_{CC} - I_C R_C - I_E R_E \approx V_{CC} - I_C(R_C + R_E)$
- P_D (circuit) $= V_{CC} \times I_E$
- This is a ***3-element output branch***, with ***$V_{CE} = V_{CC}/3$ for BB***
- ***Rest $2V_{CC}/3$ drops across R_C and R_E, with the ratio typically chosen to be 2:1*** (reason later!)
- Circuit is ***very robust*** since R_E provides ***negative feedback***
- Also, has ***better β insensitivity***

- ***Collector Feedback Bias***:
   - $V_{CC} = I_E(R_C + R_E) + I_B R_B + V_{BE}$

     $$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)(R_C + R_E)}$$

   - $I_C = \beta I_B$
   - $V_{CE} = V_{CC} - I_E(R_C + R_E)$
   - P_D (circuit) $= V_{CC} \times I_E$
   - This circuit also provides

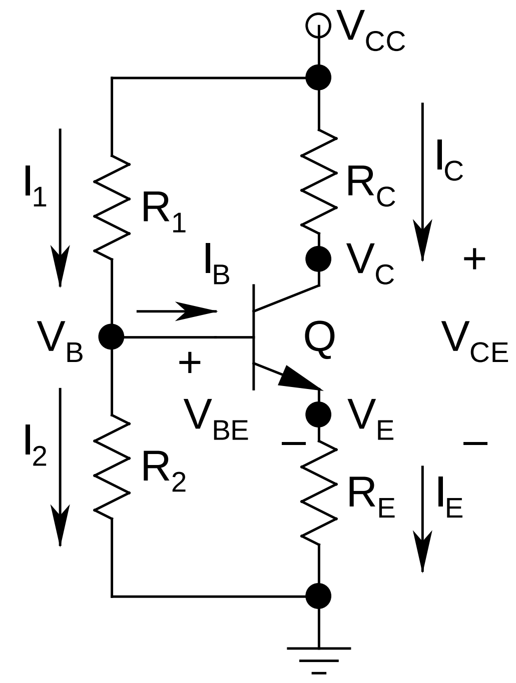
     better β insensitivity



- ***Voltage Divider (or 4-Resistor) Bias***:
  - ***The best***: ***Extremely robust and versatile***
  - If properly designed, ***almost β independent***
  - If $I_1 \geq 10 I_B$, $I_1 \approx I_2$

$$\Rightarrow V_B \simeq \frac{R_2}{R_1 + R_2} V_{CC}$$

$$\Rightarrow V_E = V_B - V_{BE} \text{ and } I_C \simeq I_E = V_E / R_E$$



- ***Example***: Let $V_{CC} = 5$ V, $R_1 = 40$ kΩ, $R_2 = 10$ kΩ, $R_C = 2$ kΩ, and $R_E = 300$ Ω
  - ***Quick estimate***: Assume $\beta \geq 100$

    $\Rightarrow V_B = 1$V, $V_E = 0.3$ V, $I_C \approx I_E = 1$ mA, $V_{CE} = 2.7$ V, and $P_D = 5.5$ mW

    $\Rightarrow$ Done! Piece of cake, isn't it?
  - $I_1 = 100$ μA and $I_B \leq 10$ μA (for $\beta \geq 100$): Assumption of $I_1 \geq 10I_B$ validated
  - Actually, ***as I_1 and β go down***, this ***analysis becomes more and more inaccurate***!

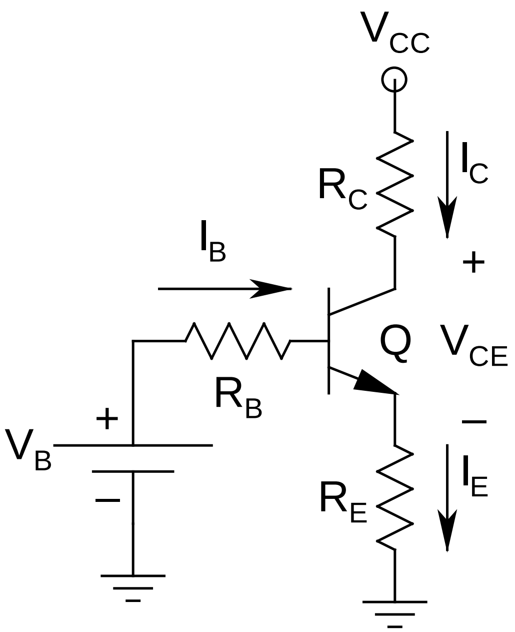
- ***Exact Analysis***:
  - ***Sufficiently more complicated***
  - ***Open the base lead*** and ***Thevenize the left branch***

$$\Rightarrow V_B = \frac{R_2}{R_1 + R_2} V_{CC} = 1\ \text{V}$$

$$R_B = R_1 \,||\, R_2 = 8\ \text{k}\Omega$$

  - Also, $V_B = I_B R_B + V_{BE} + I_E R_E$

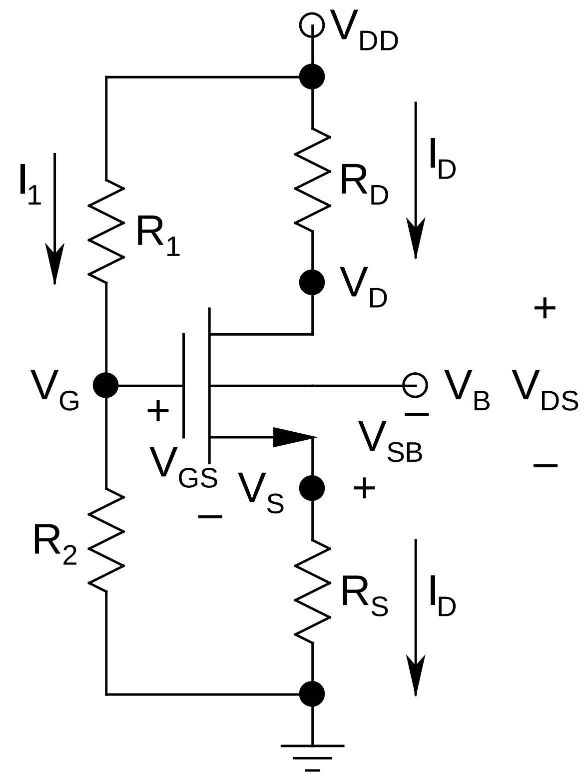
$$\Rightarrow I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1) R_E}$$



- Gives:
  - I_B = 7.83 μA, I_C = 0.78 mA, and V_{CE} = 3.2 V for β = 100 (***quite off from quick estimate***!)
  - I_B = 3.6 μA, I_C = 0.9 mA, and V_{CE} = 2.93 V for β = 250 (***within ±10% error band***)
- Thus, ***as β↑***, ***accuracy of quick estimate↑***
- Also, ***as R_B↓***, ***accuracy↑***
- ***R_B should not be too small***, ***since P_D↑↑***
- Thus, there are ***various design constraints***

Discrete Stage Biasing: MOSFET

- ***Almost universally biased using 4-Resistor Bias***
- ***Significantly more complicated than BJT biasing, since there is no quick estimate***
- ***Also, body effect and CLM complicate matters***



- ***No I_G*** $\Rightarrow$ ***R_1-R_2 combination provides a perfect voltage division***

$$\Rightarrow V_G \simeq \frac{R_2}{R_1 + R_2} V_{DD}$$

- $V_S = I_D R_S$ and $V_D = V_{DD} - I_D R_D$

$$\Rightarrow I_D = \frac{k_N}{2}\left(V_G - I_D R_S - V_{TN}\right)^2 \times \left(1 + \lambda\left[V_{DD} - I_D\left(R_S + R_D\right)\right]\right)$$

- Also:

$$V_{TN} = V_{TN0} + \gamma\left(\sqrt{2\phi_F + I_D R_S - V_B} - \sqrt{2\phi_F}\right)$$

- ***Extremely intimidating***!
- ***I_D equation becomes cubic***!
- ***Thus, bias calculation including all higher order effects is pretty tedious, and almost impossible for hand analysis***
- ***Need to make approximations***!

- Assume $\lambda V_{DS} < 0.1$:

$$\Rightarrow I_D = \frac{k_N}{2}\left(V_G - I_D R_S - V_{TN}\right)^2$$

- ***Even then it's quite complicated, since V_{TN} has a square root dependence on I_D***
- ***Tie B and S together*** $\Rightarrow V_{SB} = 0$ and $V_{TN} = V_{TN0}$
  - ***Note that it can't be done always***!

$$\Rightarrow I_D = \frac{k_N}{2}\left(V_G - I_D R_S - V_{TN0}\right)^2$$

- ***Even now, it's a quadratic equation in I_D***
- ***However, much easier to solve than earlier cases***
- ***No further simplification possible***!
- ***Solving, we will get 2 values of I_D***: ***one will be the correct one***, while ***the other one will be unphysical***
- ***2 values of I_D will give 2 different values of V_{GS}***: ***one > V_{TN0}*** and the ***other < V_{TN0}***

- ***Obviously, I_D for $V_{GS} < V_{TN0}$ is completely meaningless, since the device is off under that condition***
- Compute V_{DS} [$= V_{DD} - I_D(R_S + R_D)$]
  - ***Should be > V_{GT}*** (***saturation mode***)
  - ***For BB,*** $\mathbf{V_{DS} = V_{DD}/3}$
- $P_D = V_{DD} \times (I_D + I_1)$ [$I_1 = V_{DD}/(R_1 + R_2)$]
- ***Here, no constraints on R_1 and R_2, and they can be made as large as physically possible to reduce I_1, and thus P_D***