- ***The most important property of a DA is to be able to reject common-mode signals (noise), while amplifying the difference between the two signals applied at its two inputs***
- Characterized by a parameter known as the ***Common-Model Rejection Ratio*** (***CMRR***) (***always expressed in dB***):

  $CMRR = 20\log_{10}(|A_{dm}/A_{cm}|)$

- ***Ideal (Desirable) Properties***:
  - $|A_{dm}| \rightarrow \infty$ (~ 10^3-10^5)
  - $|A_{cm}| \rightarrow 0$ (<<< 1)
  - CMRR $\rightarrow \infty$ (~ 40-120 dB)

- ***The circuit has two inputs and two outputs***:

  $\Rightarrow$ ***Four possible configurations***:

  - ***Single-ended i/p***, ***single-ended o/p***
  - ***Single-ended i/p***, ***double-ended o/p***
  - ***Double-ended i/p***, ***single-ended o/p***
  - ***Double-ended i/p***, ***double-ended o/p***

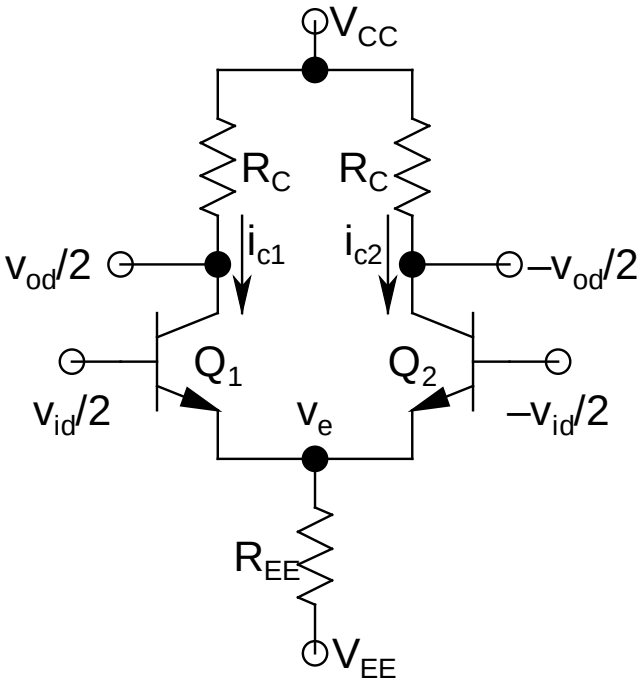
  $\Rightarrow$ ***Tremendous flexibility***

  - ***Double-ended o/p eliminates the common-mode signal completely***
  - ***However, at some point in the circuit, needs to be converted to a single-ended o/p***

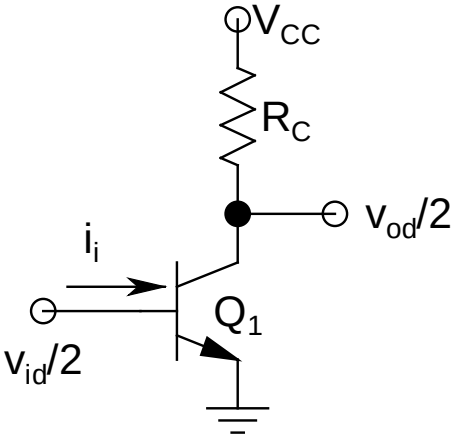
    $\Rightarrow$ ***High CMRR is an absolute must***!

➢ *Differential-Mode Half Circuit*:

Calculation of A_{dm}:



npn DA Under Pure Differential-Mode Input



Differential-Mode Half-Circuit

- ***Can be shown that $v_e = 0$ in three ways***:
  - ***From the symmetry of the circuit***:

    Equal and opposite voltages applied at the bases of Q_1 and Q_2 (perfectly matched)

    $\Rightarrow$ ***The emitter potential v_e got to be an average of the inputs, which is zero***
  - $i_{c1} = g_{m1}(v_{id}/2 - v_e)$ and $i_{c2} = g_{m2}(-v_{id}/2 - v_e)$

    Since $g_{m1} = g_{m2}$, i_{c1} must equal $-i_{c2}$ (***circulating current***)
    (***this is again from symmetry***)

    $\Rightarrow v_e = 0$
  - ***Drawing the complete ac low-frequency hybrid-π model, and summing currents at the common-emitter node***:

    Show that $v_e = 0$
- ***Caution***: ***$v_e = 0$ will hold true only for a balanced DA***

- ***Thus, the left and right parts of the circuit become absolutely symmetrical***

  $\Rightarrow$ ***Either of the parts can be used***

  $\Rightarrow$ ***Leads to the differential-mode half-circuit***

- $g_{m1} = g_{m2} = g_m = I_{EE}/(2V_T)$, $r_{E1} = r_{E2} = r_E = 2V_T/I_{EE}$, and $r_{\pi 1} = r_{\pi 2} = r_\pi = \beta r_E$

- ***Can be easily identified to be a CE stage***

  $\Rightarrow A_{dm} = v_{od}/v_{id} = (v_{od}/2)/(v_{id}/2) = -R_C/r_E$

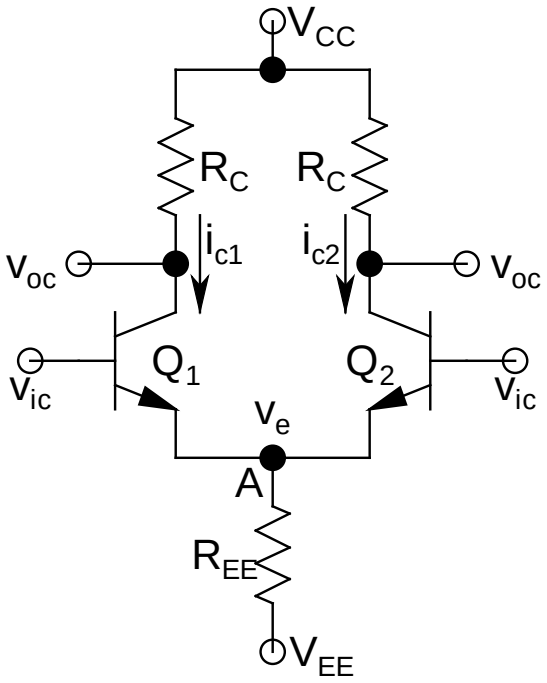
- ***Differential-mode input resistance***:

  $R_{id} = v_{id}/i_i = 2(v_{id}/2)/i_i = 2r_\pi$

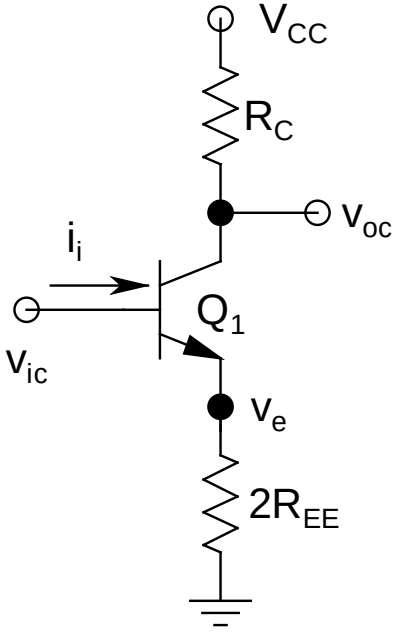
- ***The simplicity of the analysis is simply mind-boggling***!

➢ *Common-Mode Half-Circuit*:

Calculation of A_{cm}:



npn DA Under Pure Common-Mode Input



Common-Mode Half-Circuit

- $i_{c1} = i_{c2} = i_c = g_m(v_{ic} - v_e)$
- These two currents ***sum up at node A*** and ***flow through R_{EE}***, ***creating a voltage drop of $2i_cR_{EE}$ across it***
- Thus, ***R_{EE} can be split into two parts***, ***$2R_{EE}$ each***, and ***each part put in the emitter leads of Q_1 and Q_2***
- ***The lead connecting the two parts of R_{EE} would not carry any current, and can be removed***
- ***Thus, the circuit becomes perfectly symmetric along a vertical cut-line going through the middle of the circuit***, and we can ***consider either of them***

  $\Rightarrow$ ***Leads to the common-mode half-circuit***

- ***Can be easily identified to be a CE(D) stage***

  $\Rightarrow A_{cm} = v_{oc}/v_{ic} = -R_C/(r_E + 2R_{EE}) \approx -R_C/(2R_{EE})$

  (since, in general, $R_{EE} >> r_E$)

- ***Common-mode input resistance***:

  $R_{ic} = v_{ic}/i_i = r_\pi + (\beta + 1)2R_{EE} \approx 2\beta R_{EE}$

  (since, in general, $R_{EE} >> r_\pi$)

- ***Input resistance of the npn DA***:

  $R_i = R_{id} \| R_{ic} \approx R_{id} = 2r_\pi$ (***from superposition***)

  (since, in general, $R_{ic} >> R_{id}$)

- ***CMRR*** $= 20\log_{10}(|A_{dm}/A_{cm}|) \approx 20\log_{10}(2R_{EE}/r_E)$

- ***Some insights***:
  - A_{dm} *is independent of* R_{EE}, however, A_{cm} *is a strong function of* R_{EE}
  - *Goal is to make* A_{cm} *as close to zero as possible*

    $\Rightarrow$ *Make* R_{EE} *as large as possible*
  - *High value of* R_{EE} *will automatically ensure high value of CMRR* (*highly desirable*!)
  - *High CMRR can also be achieved by reducing* r_E

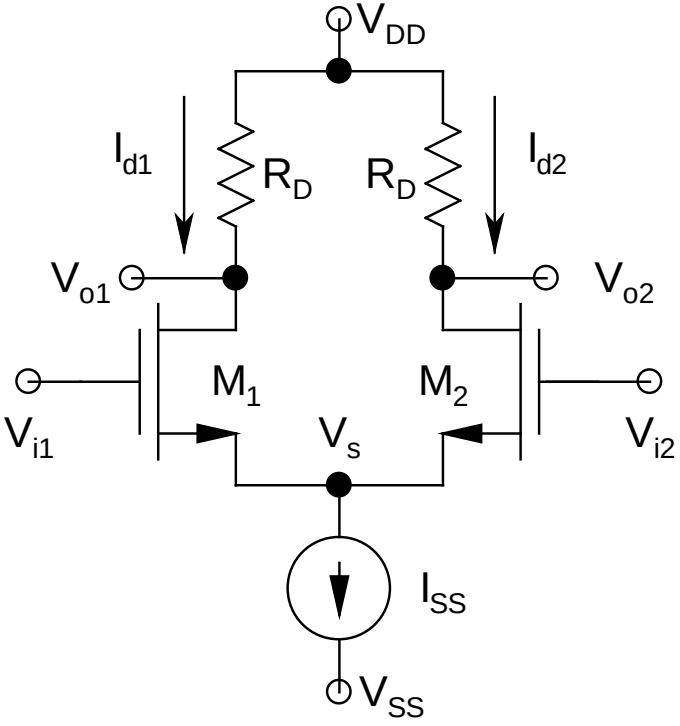
    $\Rightarrow$ *Can be obtained by increasing the DC bias current*

    $\Rightarrow$ *DC power dissipation of the circuit goes up*

    $\Rightarrow$ Also, *DC biasing may become suspect*!

- ***Increasing the Linear Range*:**
  - ***Linear Range*: $\pm 4V_T$ (~ ± 100 *mV at room temperature*)**
  - ***For some applications, this may not be enough***
  - ***Linear Range can be increased by attaching two identical resistors (R_E) in the emitter branches of Q_1 and Q_2***
  - ***Increases Linear Range by $I_{EE}R_E$ (Show!)***
  - ***This method decreases A_{dm} (differential-mode half-circuit becomes CE(D) topology)***
  - ***Has minimal effect on A_{cm}***
  - ***CMRR suffers! $\Rightarrow$ Not a good choice!***

- ***NMOS DA (SCP)***:
  - M_1-M_2 constitute a ***perfectly matched pair***, and have their ***sources connected together***, hence, the name
  - I_{SS}: ***DC bias current source***
  - ***All voltages and currents are instantaneous***



NMOS DA Topology

- $V_{gs1} = V_{i1} - V_s$, and $V_{gs2} = V_{i2} - V_s$
- ***KVL around M_1-M_2 GS loop***:

$$V_{i1} - V_{gs1} + V_{gs2} - V_{i2} = 0$$

$$\Rightarrow V_{gs1} - V_{gs2} = V_{i1} - V_{i2} = V_{id}$$

- ***Neglecting CLM Effect***:

$$I_{d1} = \frac{k'_N}{2}\left(\frac{W}{L}\right)\left(V_{gs1} - V_{TN1}\right)^2 \quad \text{and}$$

$$I_{d2} = \frac{k'_N}{2}\left(\frac{W}{L}\right)\left(V_{gs2} - V_{TN2}\right)^2$$

- Ran into a problem, since ***both M_1 and M_2 would have body effect present***
  - ***Both bodies connected to V_{SS}***, but the ***common source node is at a floating potential V_s***

    $\Rightarrow$ ***Analytical evaluation of I_{d1} and I_{d2} becomes pretty tedious***
- ***If the CLM effect is also included***, then ***the problem would need numerical solution***!
- To get a ***first-order estimate***, ***neglect body effect***

  $\Rightarrow V_{TN1} = V_{TN2} = V_{TN0}$

- Thus:

$$V_{id} = \frac{\sqrt{I_{d1}} - \sqrt{I_{d2}}}{\sqrt{\frac{k'_N}{2}\left(\frac{W}{L}\right)}} \qquad (1)$$

- Also:

$$I_{d1} + I_{d2} = I_{SS} \qquad (2)$$

- ***Solving Eqs.(1) and (2)***:

$$I_{d1} = I_{SS}/2 + \xi \quad \text{and}$$

$$I_{d2} = I_{SS}/2 - \xi$$