EE-380 EC Lab-02

Design, Prototype and Measure Simple Diode Circuits

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Section: C

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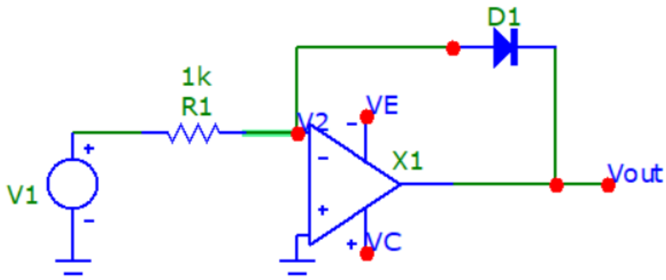
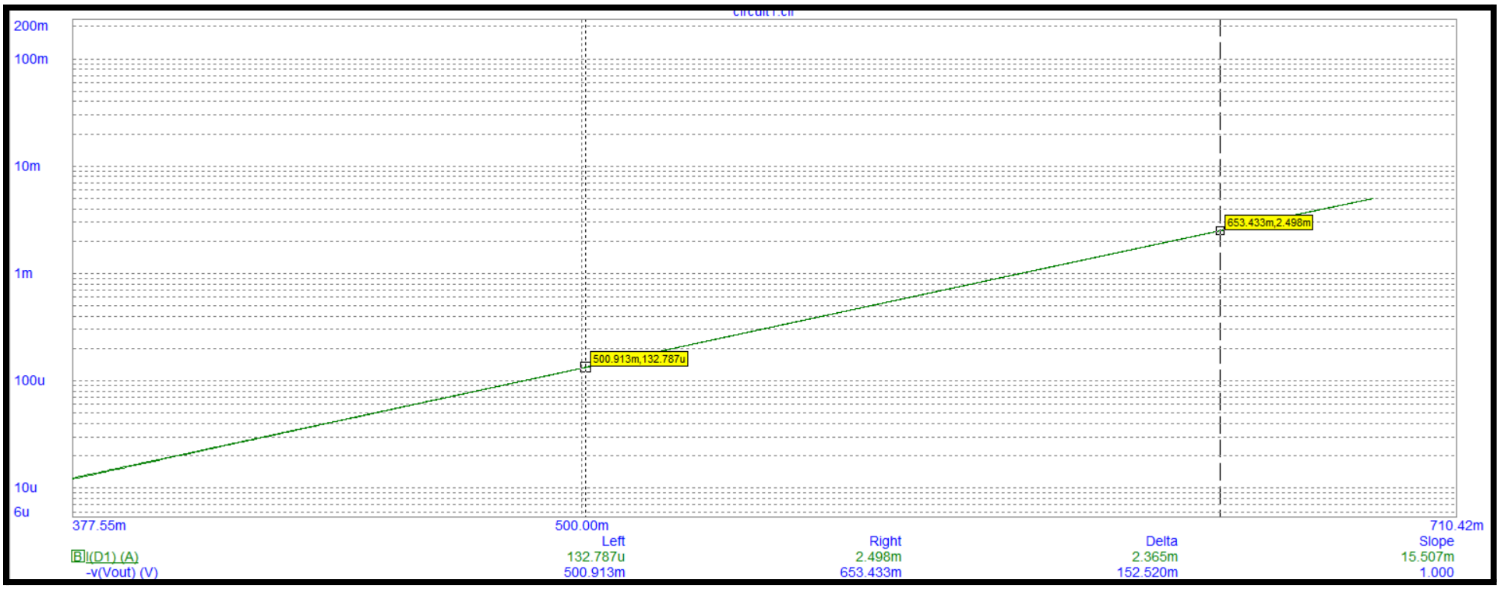
1 Measure diode current voltage characteristics and extract Saturation current I_s and ideality factor n



1.1 Pre Lab Simulation



$$slope = \frac{1}{nV_T} = \frac{ln(2.498)-ln(0.132787)}{653.433-500.913} mV^{-1} = 0.01924 mV^{-1}$$

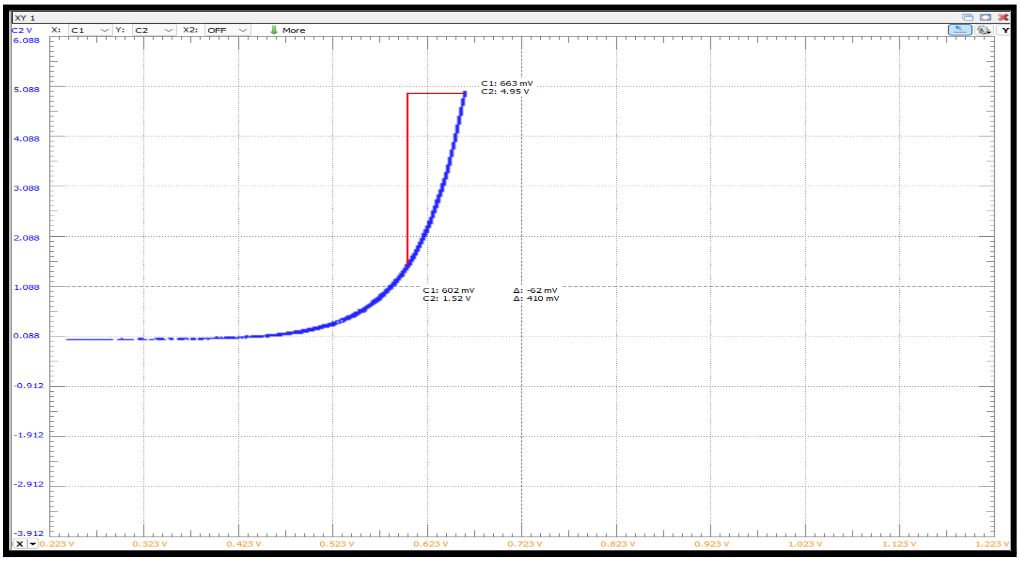
$$take\ V_T = 26mv ;\ \frac{1}{n} = 26 * 0.01924 = 0.50024$$

$n = 1.9990$ $From\ the\ equation\ ln(I_D) = ln(I_s) + \frac{V_D}{nV_T}\ ,\ we\ get\ ,\ I_s = e^{(ln(I_D) - \frac{V_D}{nV_T})}$

$putting\ V_D = 0.653433V,\ I_D = 0.002498mV,\ n = 1.999,\ V_T = 26mV, gives$

$I_s = 8.6nA$

1.2 In Lab Experimental Measurement



(Note : the plot is **NOT** in log scale and I_D=C2/1000, where C2 is the value corresponding to channel 2)

1.3 Post Lab Calculations and Result

$$(V_{D1}, I_{D1}) \equiv (663mV, 4.95mA)\ and\ (V_{D2}, I_{D2}) \equiv (602mv, 1.52mA)$$

$$so,\ n = \frac{1}{slope*V_T} = \frac{663-602}{(ln(4.95)-ln(1.52))*26}\quad (note:\ y_{axis}\ should\ be\ taken\ in\ log\ scale)$$

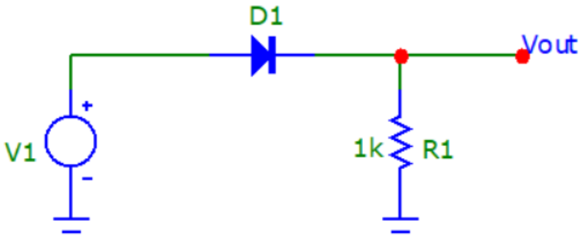
$n = 1.987$

$and\ using\ the\ equation\ I_s = e^{(ln(I_D) - \frac{V_D}{nV_T})}\ and\ point\ (663mV, 4.95mA)\ we\ get\ I_s = e^{(ln(0.00495) - \frac{663}{1.987*2}}$

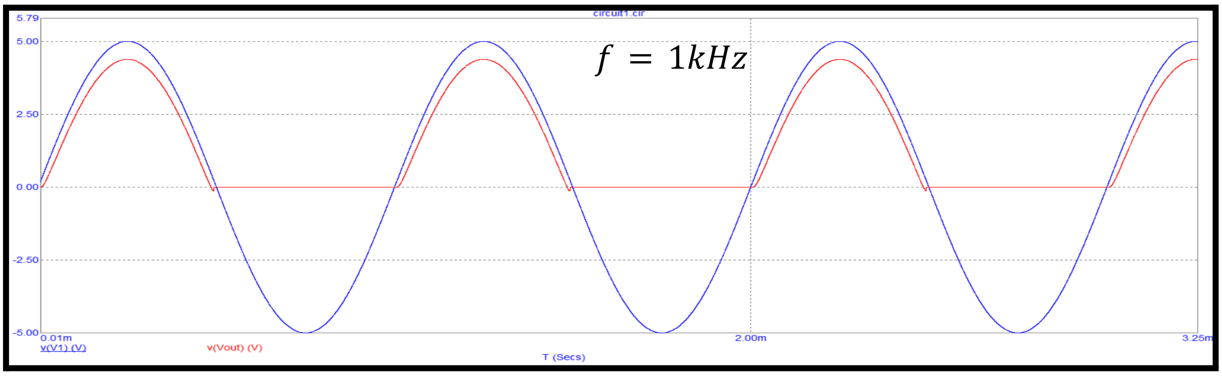
$I_s = 13.2nA$

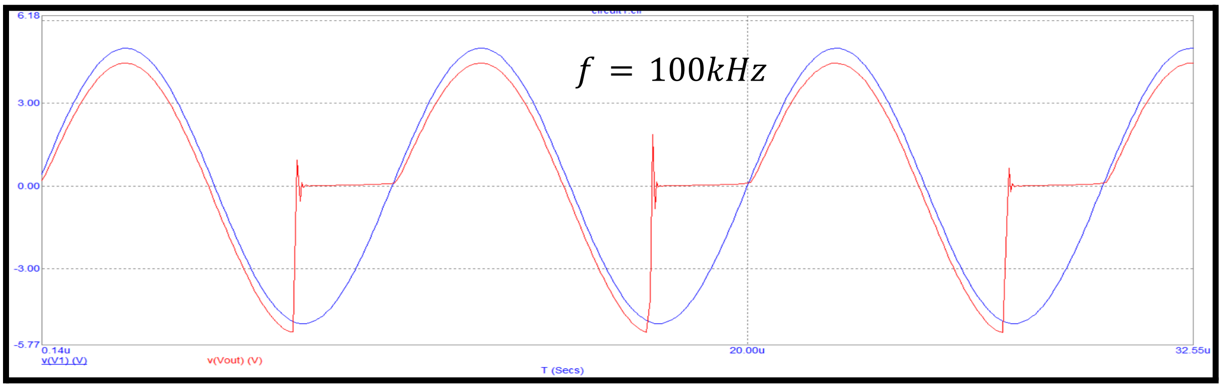
Value of n is almost same in simulation and in experiment, approximately equal to 2, the slight difference in I_s can be explained by practical factors such as resistor tolerances, parasitic effects in wiring and components, limitations in measurement equipment, temperature

2 Explore rectifier response at different input frequencies

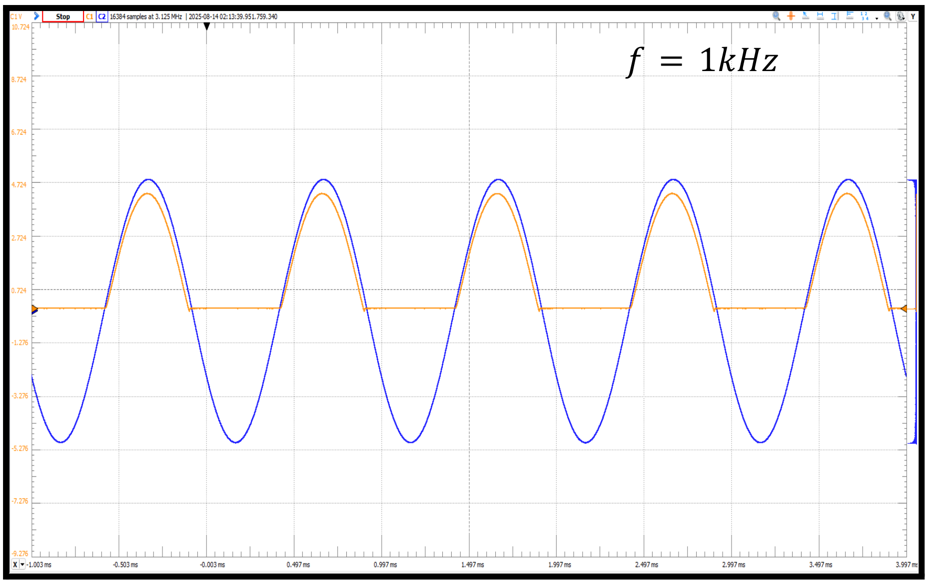


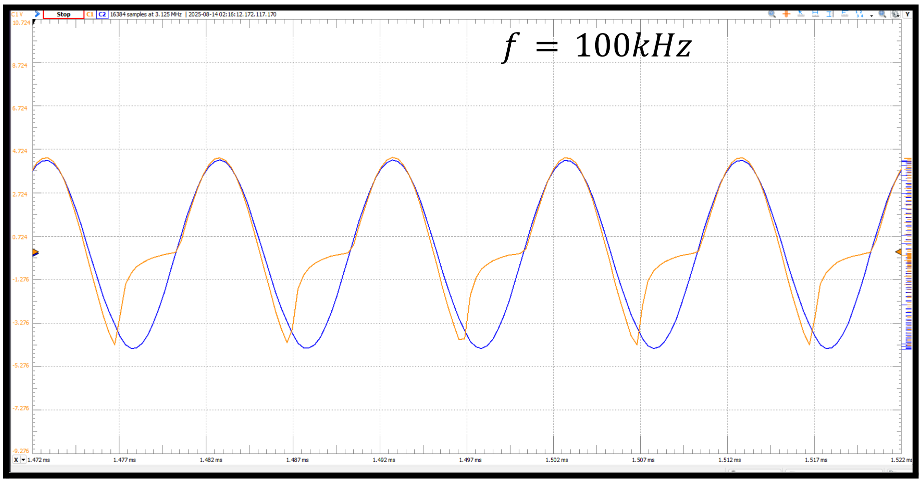
2.1 Pre Lab Simulations



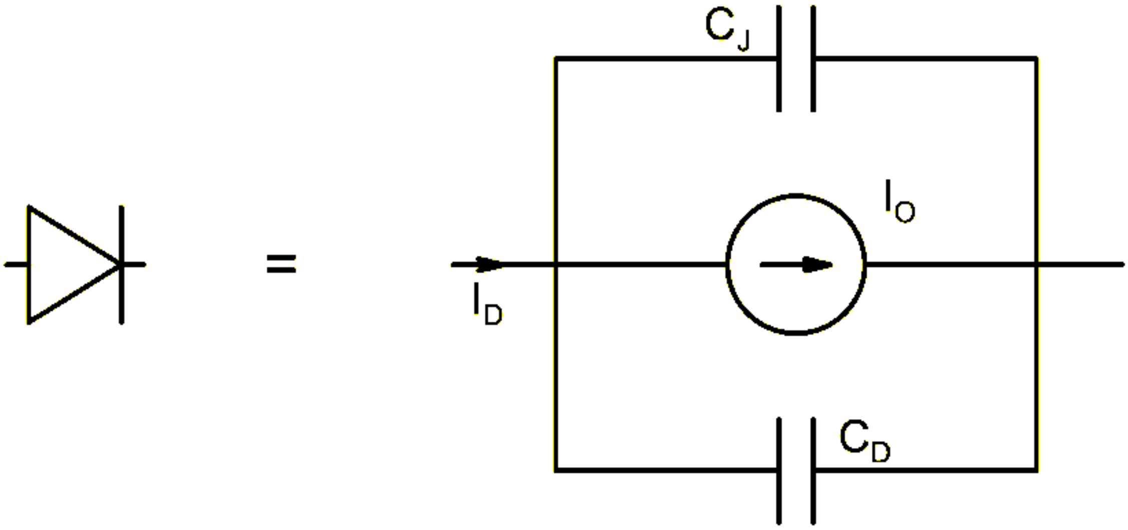


2.2 IN Lab Experiment



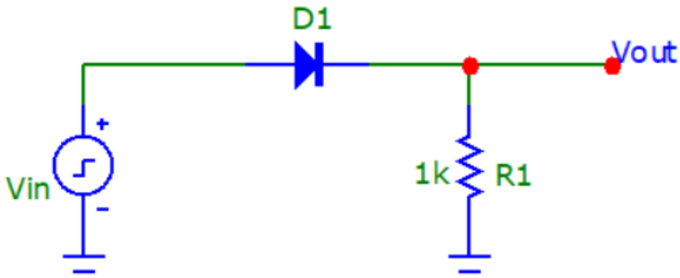


2.3 Post Lab Discussion

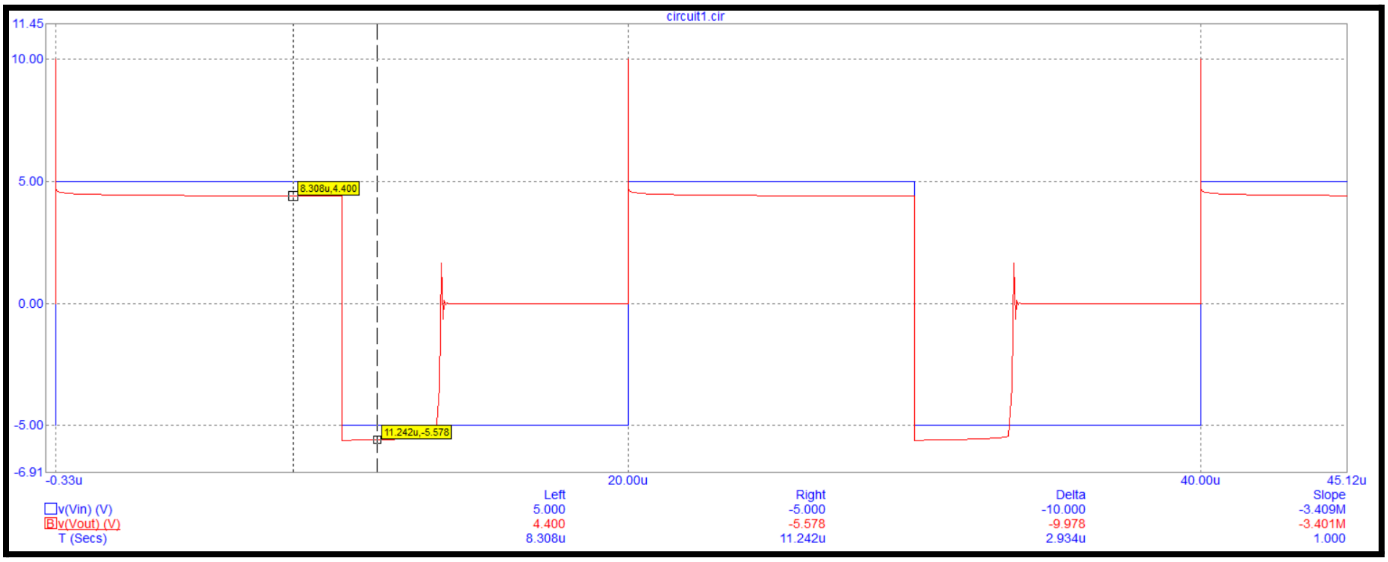


The simulated and experimental results are closely matched, with minor deviations. Experimentally, it is observed that the rectifying action of the diode weakens as the AC supply frequency increases. This is mainly due to the diode's finite switching speed and reverse recovery time, which prevent it from turning on and off instantaneously at higher frequencies. Additionally, the junction capacitances of the diode provide low-impedance paths at high frequencies, allowing a portion of the AC component to pass even under reverse bias. Together, these effects lead to reduced rectification efficiency, and distortion in the output waveform.

3 Measurement of Transit Time of diode using square wave input



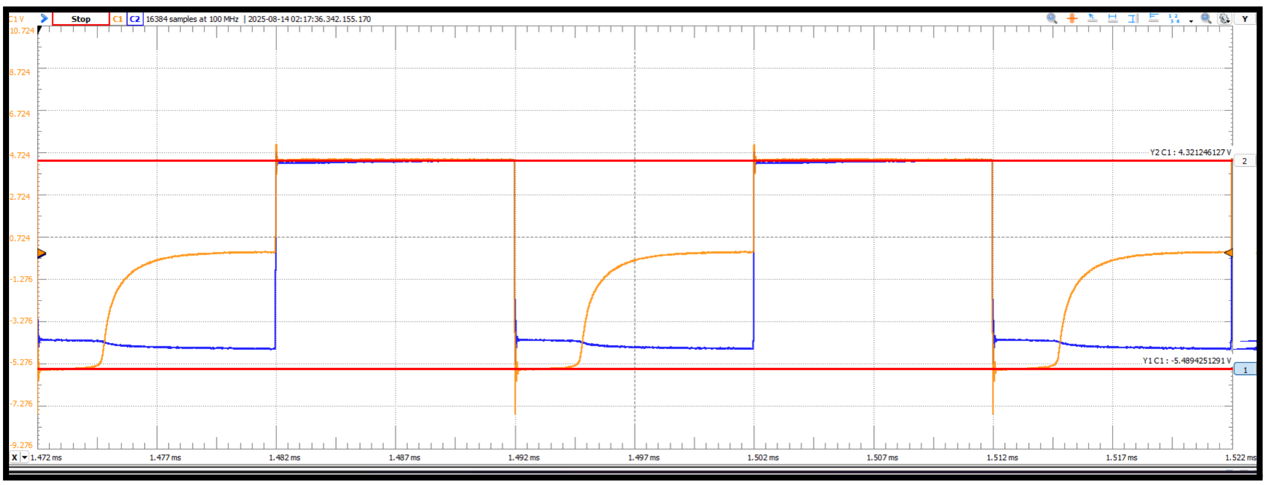
3.1 Pre Lab Simulation



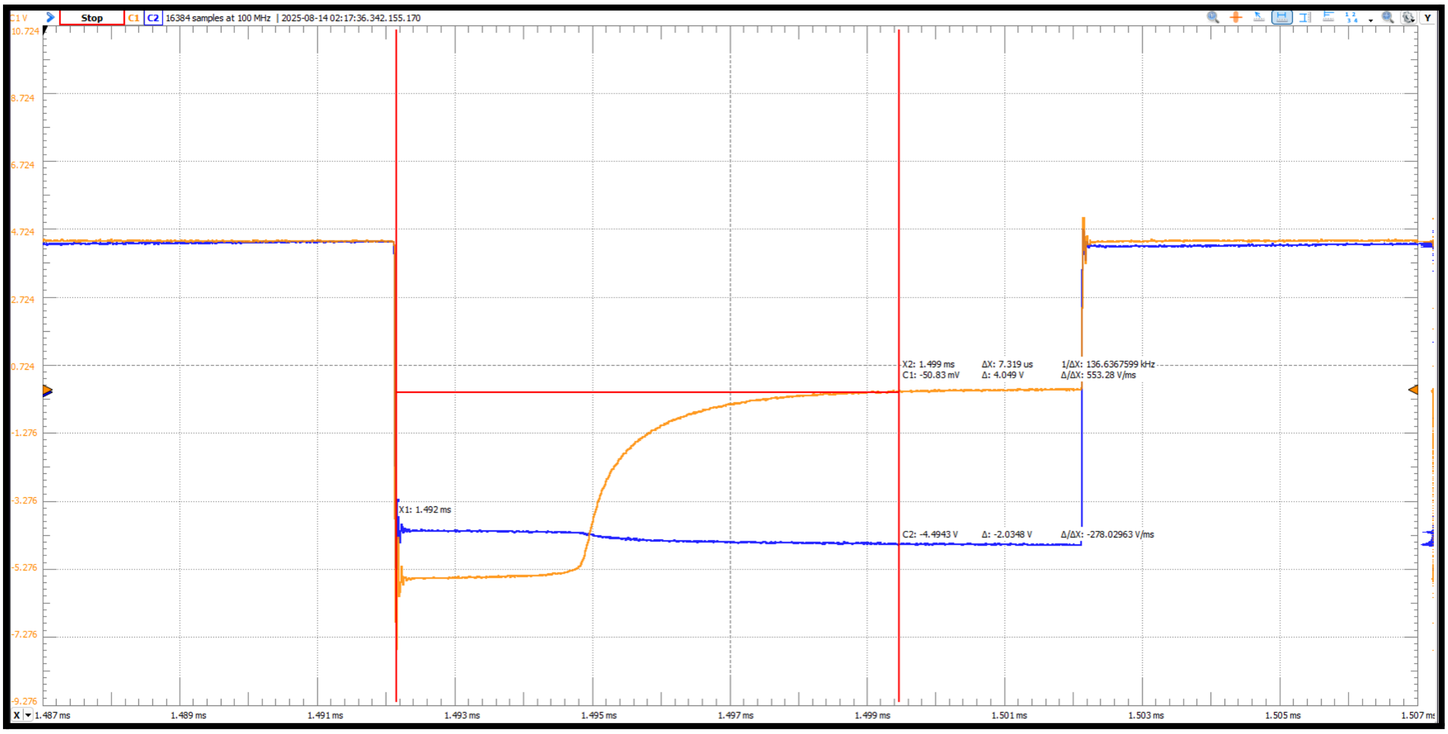
$\frac{I_F}{I_R} = \frac{4.4}{5.578} \simeq 0.789$ *and* $\tau_{RR} = 4.2\mu s$; *putting these in the equation* $\tau = \frac{\tau_{RR}}{ln(1+\frac{I_F}{I_R})}$ *we get*

$\tau = \frac{4.2}{ln(1.789)}\mu s \Rightarrow \tau = 7.22\mu s$

3.2 In Lab Experimental Measurement



$From\ the\ above\ plot\ we\ can\ see\ that\ I_F = 4.321\ V\ and\ I_R = 5.489\ V$



$This\ plot\ gives\ \tau_{RR} = 7.319\mu s$

3.3 Post Lab calculations and Result

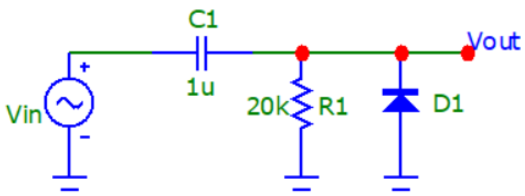
$\frac{I_F}{I_R} = \frac{4.321}{5.489} \simeq 0.787\ and\ \tau_{RR} = 7.319\mu s;\ putting\ these\ in\ the\ equation\ \tau = \frac{\tau_{RR}}{ln(1+\frac{I_F}{I_R})}\ we\ get$

$\tau = \frac{7.319}{ln(1.787)}\mu s \Rightarrow \tau = 12.6\mu s$

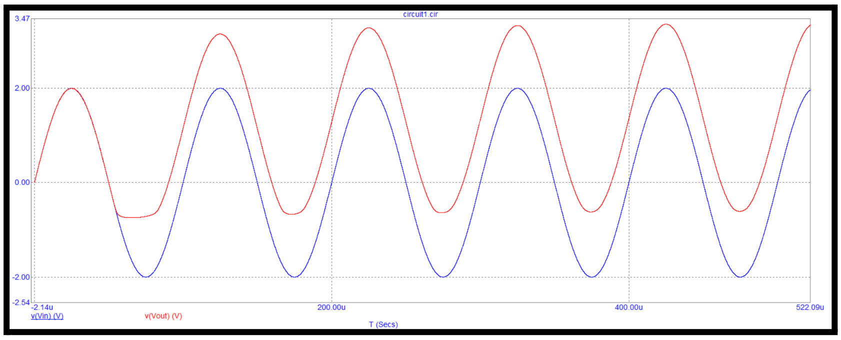
The minor differences between the simulation and experimental results can be attributed to factors such as resistor tolerances, parasitic effects in components and wiring, limitations of measurement equipment, and environmental conditions like temperature variations.

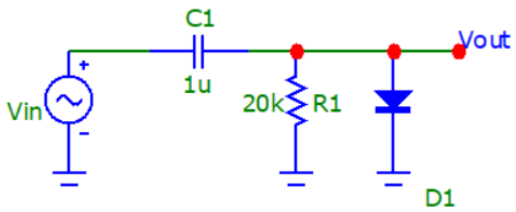
4 Explore Clamper operation and performance

4.1 Pre Lab Simulations

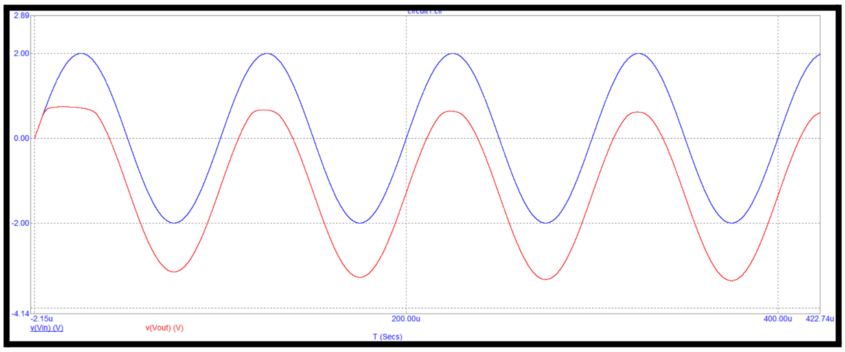


+ve clamper



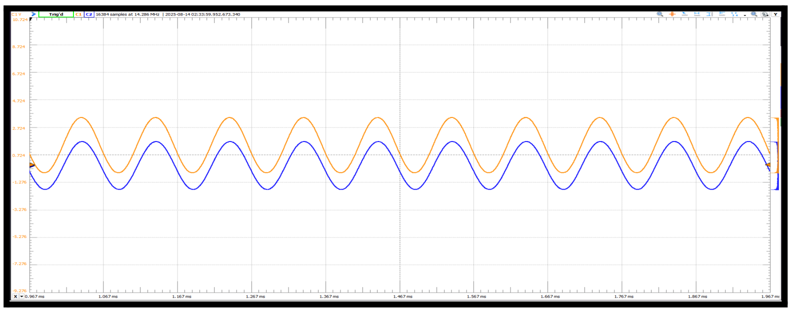


-ve clamper

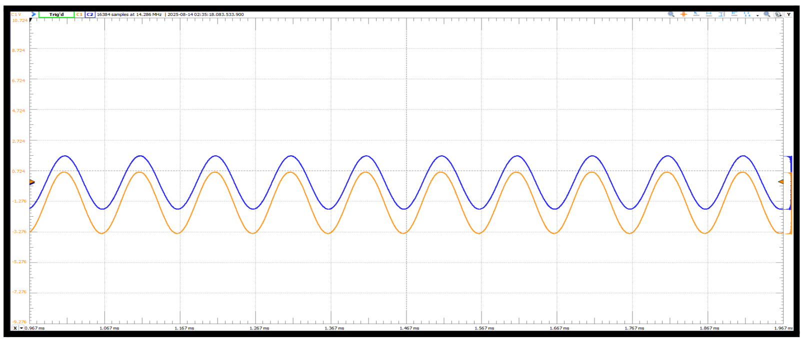


4.2 In Lab Measurements

+ve clamper



-ve clamper



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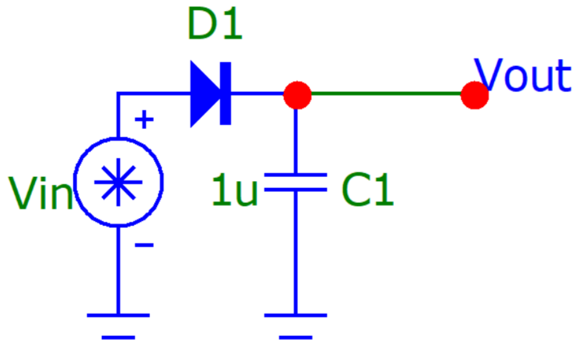
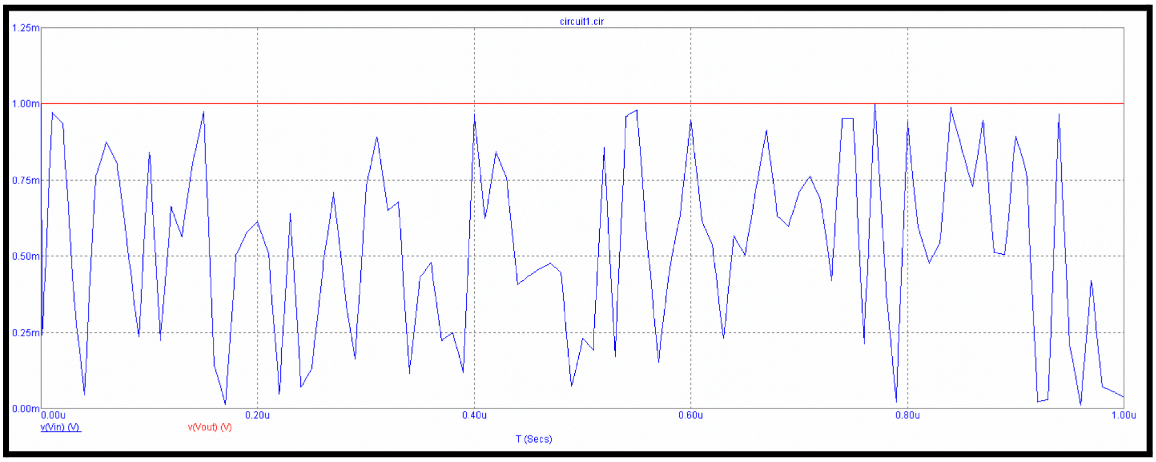
5 Explore Peak detector operation and performance



5.1 Pre Lab Simulation

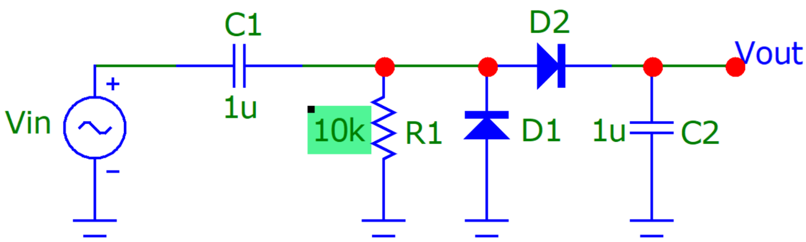


5.2 In Lab Measurement

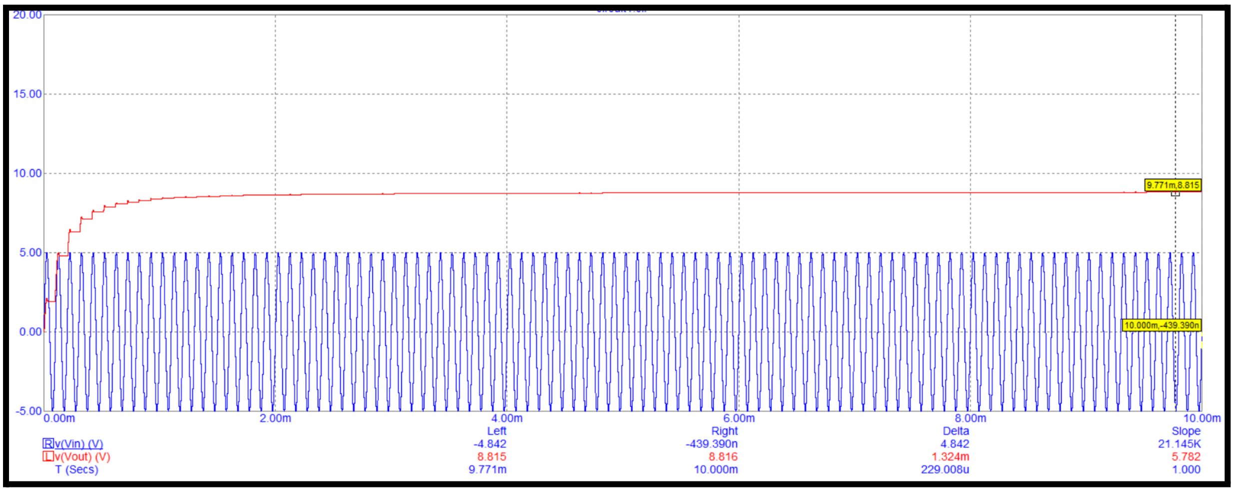
5.3 Post Lab Discussion

The peak of the noise detected is 1.524 V

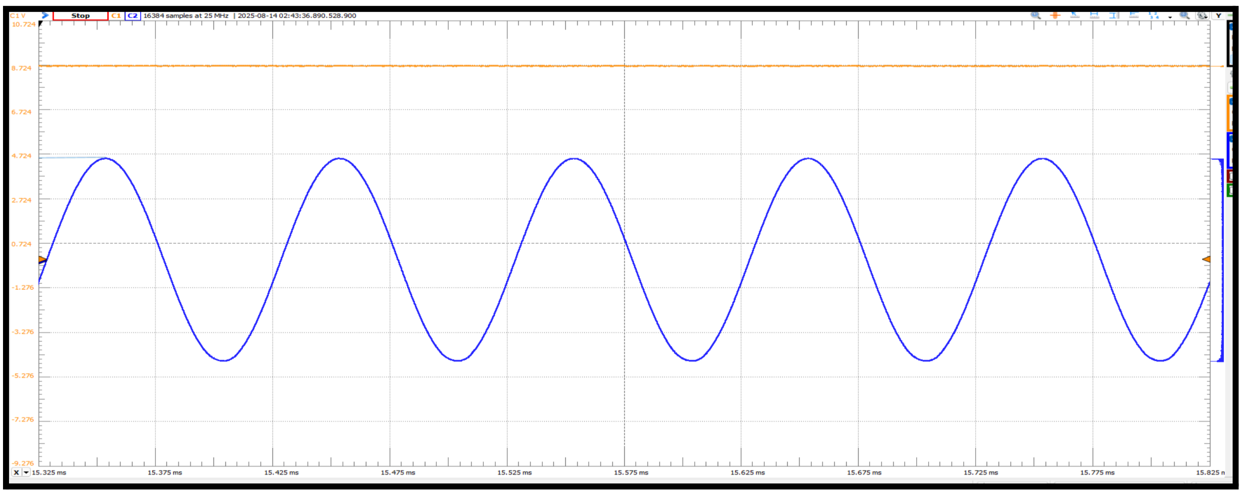
6 Explore Doubler operation and performance



6.1 Pre Lab Simulation



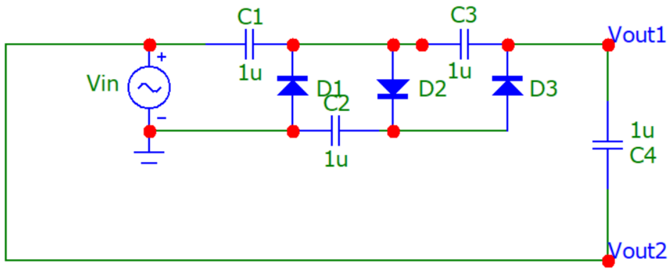
6.2 In Lab Measurement



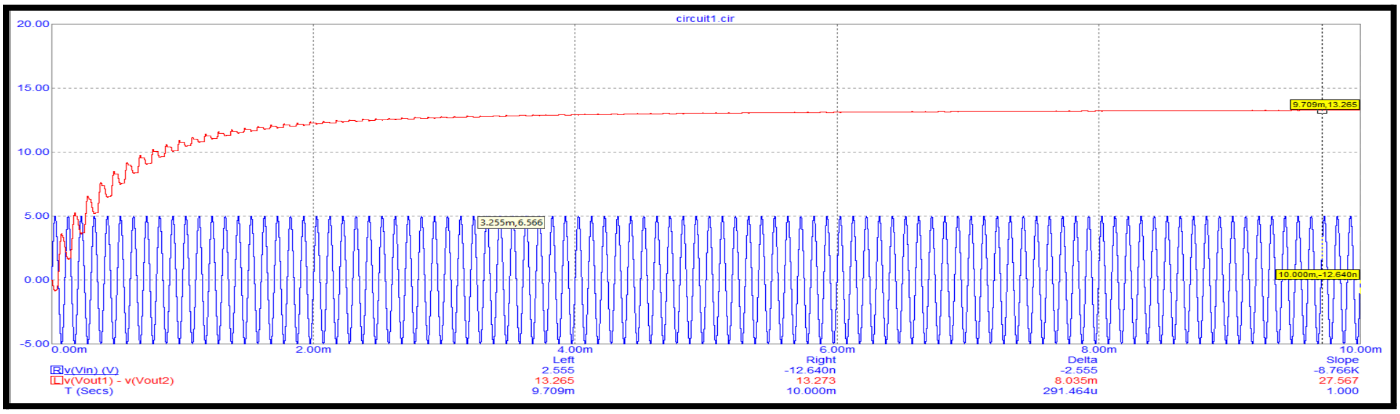
6.3 Post Lab Discussion

In the lab the peak voltage of the input signal (V_{peak}) was approximately 4.5 V, while the corresponding output DC voltage (V_{out}) was observed to be around 8.7 V. So $2V_{peak} \simeq V_{out}$. Hence, it can be concluded that the doubler circuit operates as expected.

7 (Bonus) Design a Tripler

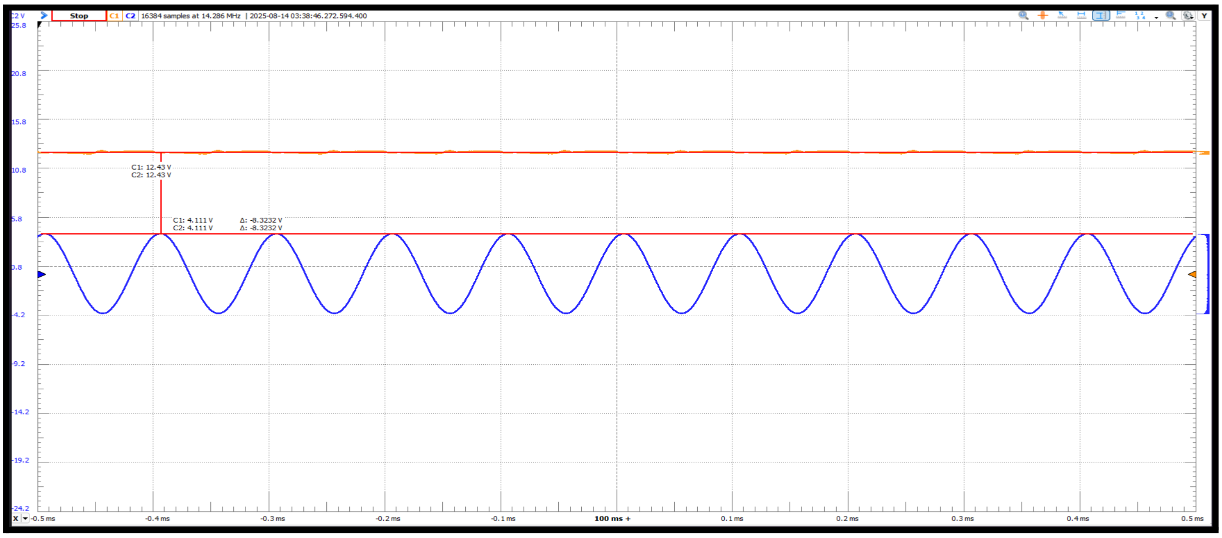


7.1 Pre Lab Simulation and Design



You get $3V_{in} = V_{out1} - V_{out2}$

7.2 In Lab Measurements



7.3 Post Lab Discussion

In the lab the peak voltage of the input signal (V_{peak}) was approximately 4.11 V, while the corresponding output DC voltage (V_{out}) was observed to be around 12.43 V. So $3V_{peak} \simeq V_{out}$ Hence, it can be concluded that the tripler circuit operates as expected.