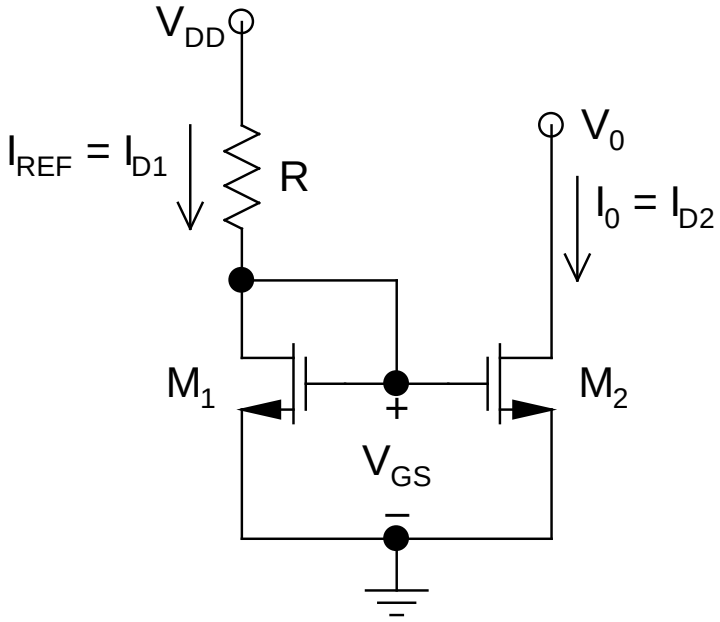
- ***Simple NMOS CM***:
  - $V_{GS1} = V_{GS2} = V_{GS}$
  - M_1 has its ***D and G shorted*** $\Rightarrow V_{GD1} = 0$
    $\Rightarrow$ ***always in saturation***, since $V_{DS1} > V_{GT1}$
    $\Rightarrow$ Known as ***diode-connected MOSFET***
  - Even though $I_G = 0$, the analysis is slightly more cumbersome than simple BJT CM



- ***In general, for NMOS (PMOS), the body terminal is always connected to the most negative (positive) potential available in the circuit to ensure that SB and DB junctions never get forward biased***
- ***Both M_1 and M_2 have their body terminals grounded*** $\Rightarrow V_{SB1} = V_{SB2} = 0$
  - $V_{TN1} = V_{TN01}$ and $V_{TN2} = V_{TN02}$
- Thus, neglecting CLM:

$$I_{REF} = I_{D1} = \frac{k'_{N1}}{2}\left(\frac{W}{L}\right)_1 \left(V_{GS} - V_{TN01}\right)^2$$

- For a ***given V_{DD} and R***, the equation has ***2 unknowns***: I_{D1} and V_{GS}
- Need ***another equation*** for ***unique solution***, which is the ***load line equation***:

  $I_{D1} = (V_{DD} - V_{GS})/R$
- ***Simultaneous solution*** of these ***two equations*** would give a ***unique solution*** for I_{D1} and V_{GS}
  - ***Caution***: ***2 roots, out of which, one will be unphysical***
- So far, we have ***neglected CLM***, which we would include soon!

- Now:

$$V_{GS} = V_{TN01} + \sqrt{\frac{2I_{REF}}{k'_{N1}\left(W/L\right)_1}} = V_{TN02} + \sqrt{\frac{2I_0}{k'_{N2}\left(W/L\right)_2}}$$

- Thus:

$$I_0 = \frac{k'_{N2}\left(W/L\right)_2}{2}\left[\left(V_{TN01} - V_{TN02}\right) + \sqrt{\frac{2I_{REF}}{k'_{N1}\left(W/L\right)_1}}\right]^2$$

- This is the ***exact expression*** of I_0, ***without making any assumptions/approximations whatsoever***

- Now, if $V_{TN01} = V_{TN02} = V_{TN0}$, and $k'_{N1} = k'_{N2} = k'_N$:

$$I_0 = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

- ***Very similar*** to BJT CM, but with a ***big difference***:
  - ***In BJT CM, this ratio could only be an integer***
  - ***In MOS CM, no such restriction exists***: ***$(W/L)_2$ can be > , = , or < $(W/L)_1$ $\Rightarrow$ any arbitrary current ratio can be obtained***

- Finally, if $(W/L)_2 = (W/L)_1$:

  $I_0 = I_{REF} \Rightarrow$ ***Current Mirror***!

- Two MOSFETs are deemed to constitute a ***matched pair***, if they have ***same*** V_{TN0}, γ, ϕ_F, λ, and k'_N
  - Note that all of these are ***process parameters***
  - ***(W/L) is NOT a process parameter***, since it's under ***designer's control***
  - ***If (W/L)s are also same, then the pair is known as perfectly matched***

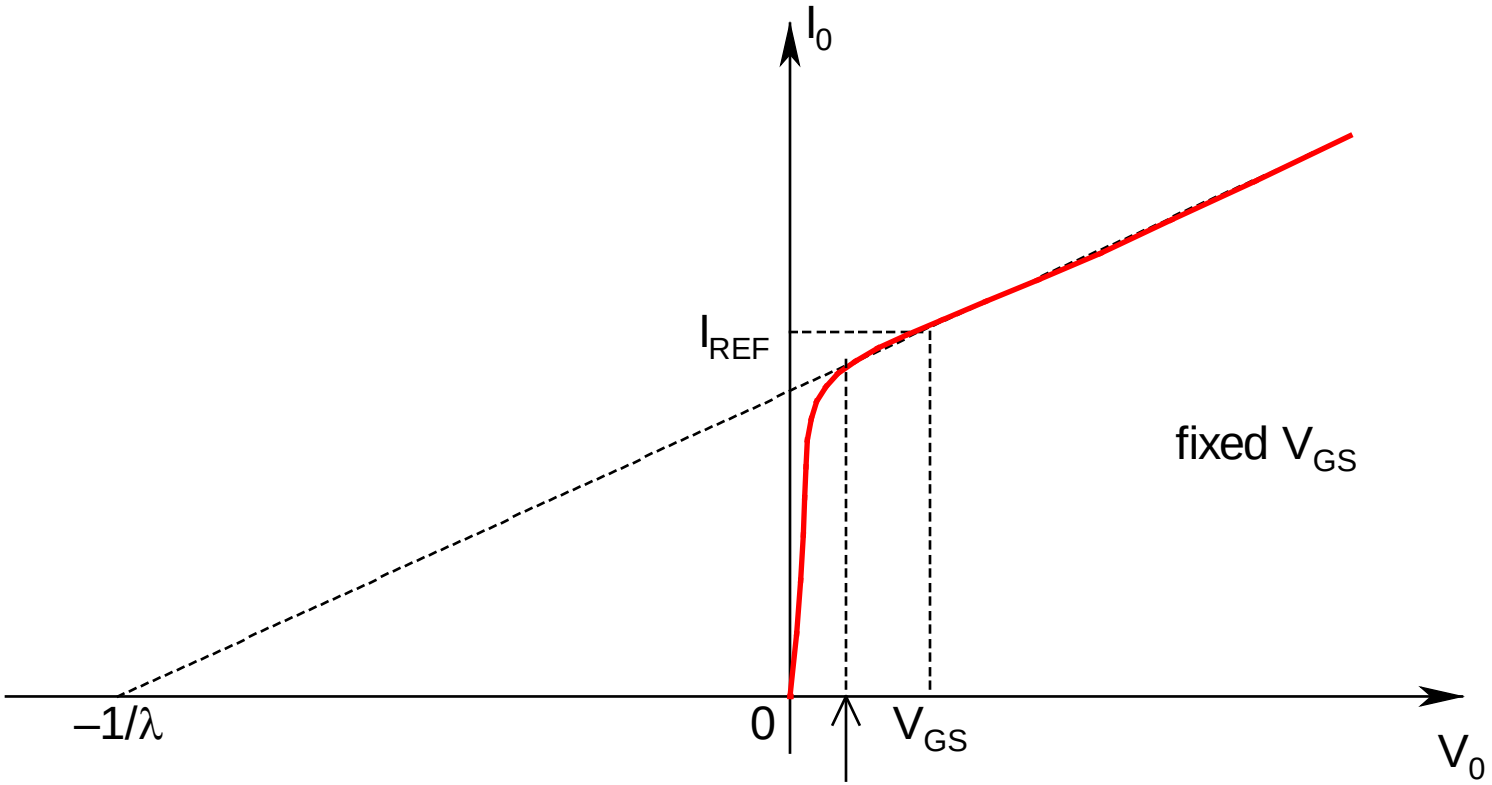
- ***Systematic Error***:
  - Even if M_1 and M_2 are ***perfectly matched***, still I_0 ***may not equal*** I_{REF}!
  - Recall:

$$I_D = \frac{k_N}{2} V_{GT}^2 \left(1 + \lambda V_{DS}\right)$$

  - Thus:

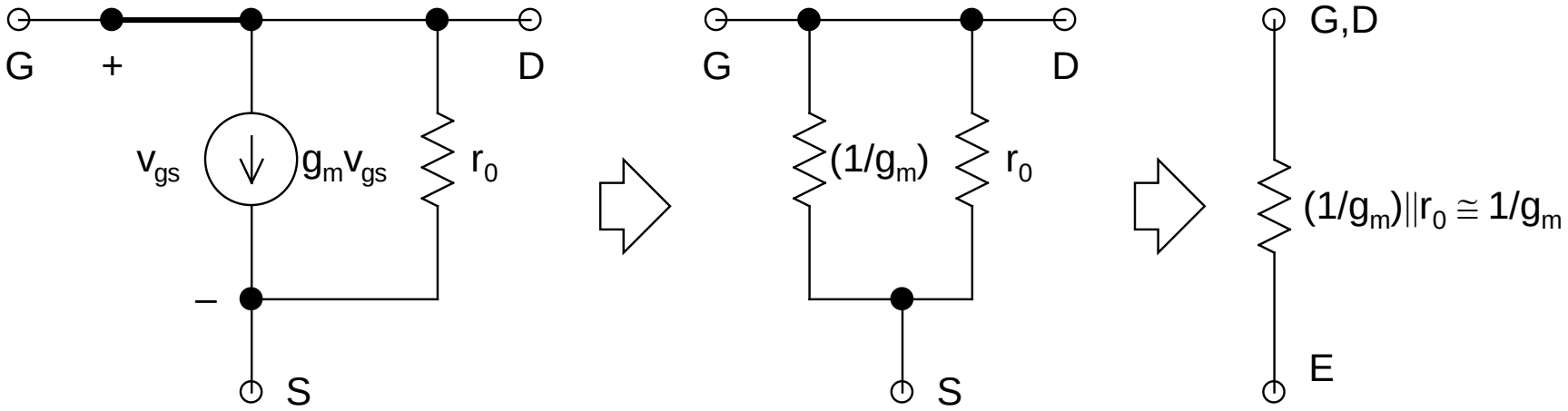
$$\frac{I_0}{I_{REF}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} = \frac{1 + \lambda V_0}{1 + \lambda V_{GS}}$$

  - Therefore, ***$I_0 = I_{REF}$ only when $V_0 = V_{GS}$***



$V_{0,min} = V_{DS2}(sat)$ (lowest allowed value $\approx 3V_T$)

- ***Output Resistance R_0***:
  - First, ***investigate M_1***

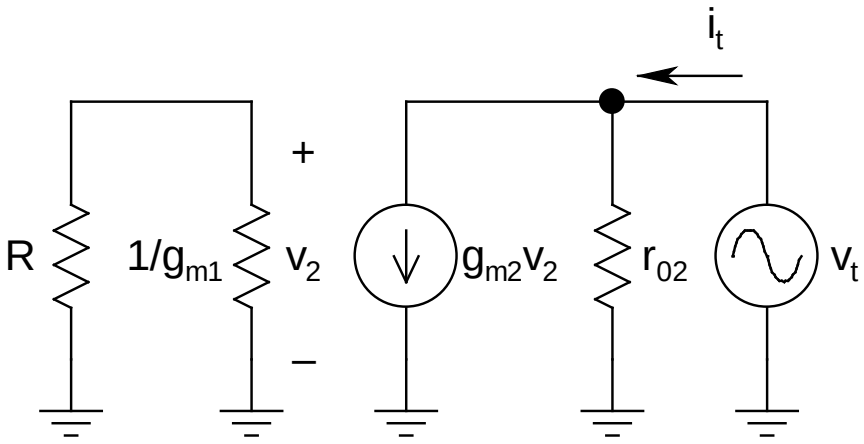


  - The ***small-signal equivalent*** consists simply of $1/g_m$, which is similar to r_D for ***diodes***
    - Hence the name ***diode-connected transistor***

- ***For the complete circuit***:
  - ***Left part of the circuit has no source***

    $\Rightarrow v_2 = 0$

    $\Rightarrow g_{m2}v_2 = 0$

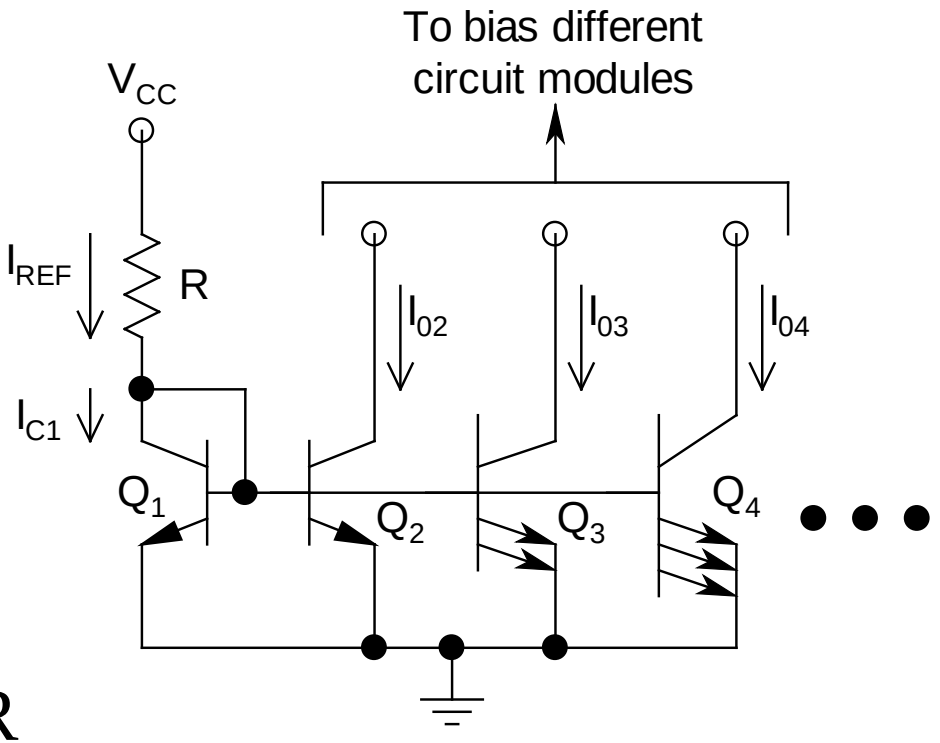


  - Thus, $R_0 = v_t/i_t = r_{02} = 1/(\lambda I_0)$
  - For a ***good current source***, ***R_0 should be as large as possible*** (***ideally infinite***)

    $\Rightarrow$ ***λ should be as small as possible*** and/or ***I_0 should be as small as possible***

- ***Golden Rule for Calculation of R_0***:
  - For a ***BJT*** (or ***MOSFET***):
    - With Emitter (or Source) ***grounded***
    - ***No electrical connection*** (***feedback***) between Collector (or Drain) and Base (or Gate)
    - ***Looking from*** the Collector (or Drain)
      - ***The only resistance seen will be the output resistance of the BJT (or MOSFET)***

- ***npn Current Repeater*:**
  - ***Uses multi-emitter BJTs***
  - ***Maximum number of emitters = 4***
  - ***All emitters tied together***
  - ***All Qs have same V_{BE}***
  - $I_{REF} = (V_{CC} - V_{BE})/R$

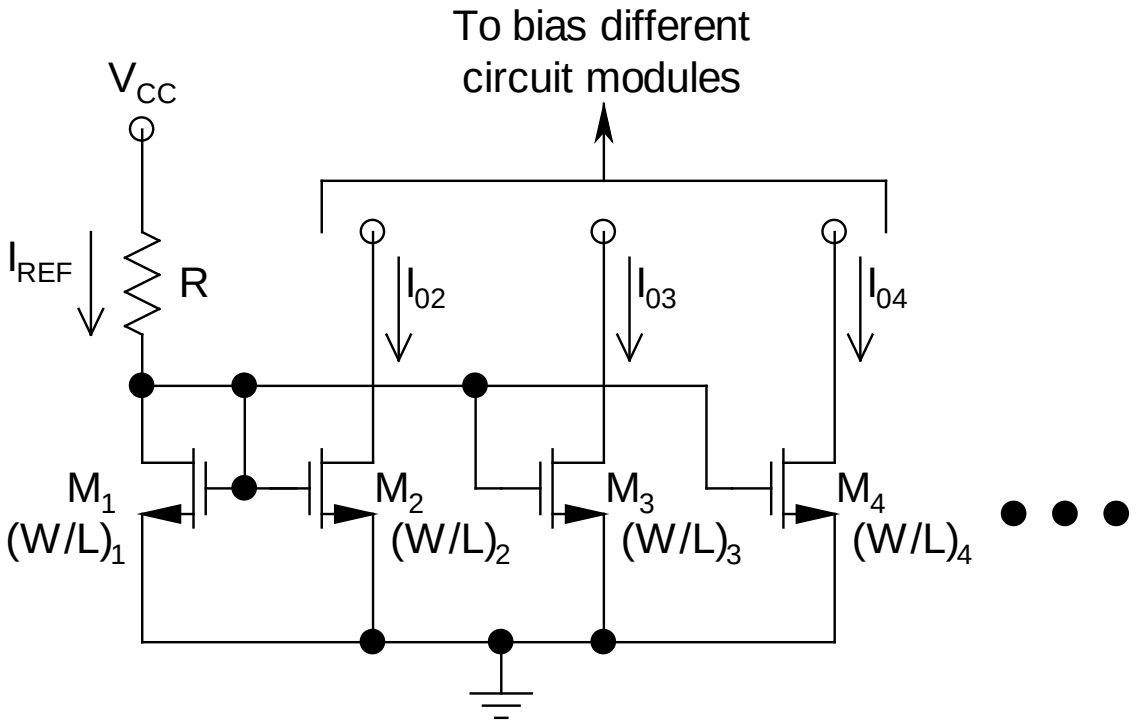


- ***Neglecting I_B***:

  $I_{02} = I_{REF}$, $I_{03} = 2I_{REF}$, $I_{04} = 3I_{REF}$, …

- ***Limitations***:
  - ***Output current can never be a non-integer ratio of I_{REF} $\Rightarrow$ no arbitrary scaling possible***
  - ***Loading Problem***:
    - ***I_{REF} not only supplies I_{C1}, but I_Bs of all the Qs***
    - ***As more Qs are added, I_Bs will keep on increasing***
    - ***I_{C1} starts to depart significantly from I_{REF}***
    - ***It's actually NOT I_{REF} that's mirrored, BUT it's I_{C1}***
    - ***A reduction in I_{C1} will affect all output currents***
    - ***Hence, this circuit is not very popular***

- ***NMOS Current Repeater***:



- $I_{REF} = I_{D1} = (V_{DD} - V_{GS})/R$

$$I_{D1} = \frac{k'_N}{2}\left(\frac{W}{L}\right)_1 V_{GT}^2 \quad \left(\textbf{\textit{assuming } } \lambda V_{DS} < 0.1\right)$$

- ***All Ms have same V_{GS} and are matched***

$$\Rightarrow I_{0i} = \frac{(W/L)_i}{(W/L)_1} I_{REF} \quad (i = 2, 3, 4, \ldots)$$

- ***Tremendous flexibility***
  - ***Any arbitrary current ratio can be obtained***
  - ***No loading effect***
  - ***Highly popular and universal choice***