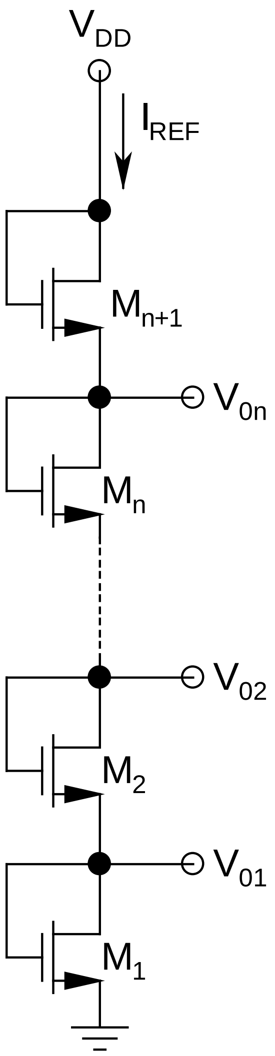
- ***NMOS Voltage Reference***:
  - ***Highly popular due to its simplicity and effectiveness***
  - ***Can generate n voltage references from (n + 1) MOSFETs***
  - ***All MOSFETs diode-connected*** $\Rightarrow$ ***Always saturated***
  - ***No resistors needed***
  - ***All bodies connected to ground***



- ***Only for M_1***, $V_{TN1} = V_{TN0}$
- ***All other MOSFETs will have body effect***, e.g., $V_{TN2} = V_{TN0} + \gamma\left(\sqrt{2\phi_F + V_{01}} - \sqrt{2\phi_F}\right)$
- Generally, ***all λs also same***, but ***aspect ratios are different***
- $V_{01}, V_{02}, \ldots, V_{0n}$ are the ***needed reference taps***
- $V_{GS1} = V_{DS1} = V_{01}$, $V_{GS2} = V_{DS2} = V_{02} - V_{01}$, $V_{GS3} = V_{DS3} = V_{03} - V_{02}, \ldots$
- $V_{SB1} = 0$, $V_{SB2} = V_{01}$, $V_{SB3} = V_{02}, \ldots$
- ***Same DC current I_{REF} flows through all MOSFETs***

- Assuming that ***all MOSFETs*** have ***same*** λ and ***same*** k'_N:

$$I_{REF} = \frac{k'_N}{2}\left(\frac{W}{L}\right)_1 \left(V_{01} - V_{TN1}\right)^2 \left(1 + \lambda V_{01}\right)$$

$$= \frac{k'_N}{2}\left(\frac{W}{L}\right)_2 \left(V_{02} - V_{01} - V_{TN2}\right)^2 \left[1 + \lambda\left(V_{02} - V_{01}\right)\right]$$

•••

- ***First I_{REF} needs to be found by ensuring that the circuit dissipates least DC power***
- ***Then, all (W/L)s can be calculated***

- ***Choice depends on several design paradigms***
- $P_D(\text{circuit}) = V_{DD} \times I_{REF}$

  $\Rightarrow$ ***For minimum P_D, I_{REF} should be minimum***
- ***Need to pick up a reference MOSFET to start the design process***
- ***Area of a MOSFET*** = W × L
- ***For minimum area***, W = L = MFS
  - ***MFS***: ***Minimum Feature Size*** (***that is allowed by the technology***)
- Pick the ***reference MOSFET*** by choosing its ***(W/L) = 1***, and having the ***least*** $V_{GT}^2(1+\lambda V_{DS})$

- ***This will yield minimum P_D***
- ***Once the reference MOSFET is chosen***, ***I_{REF} becomes known***, and ***(W/L)s of all other MOSFETs can be calculated***
- ***Total area taken up by the circuit***:

$$\sum_n (W \times L)_n$$

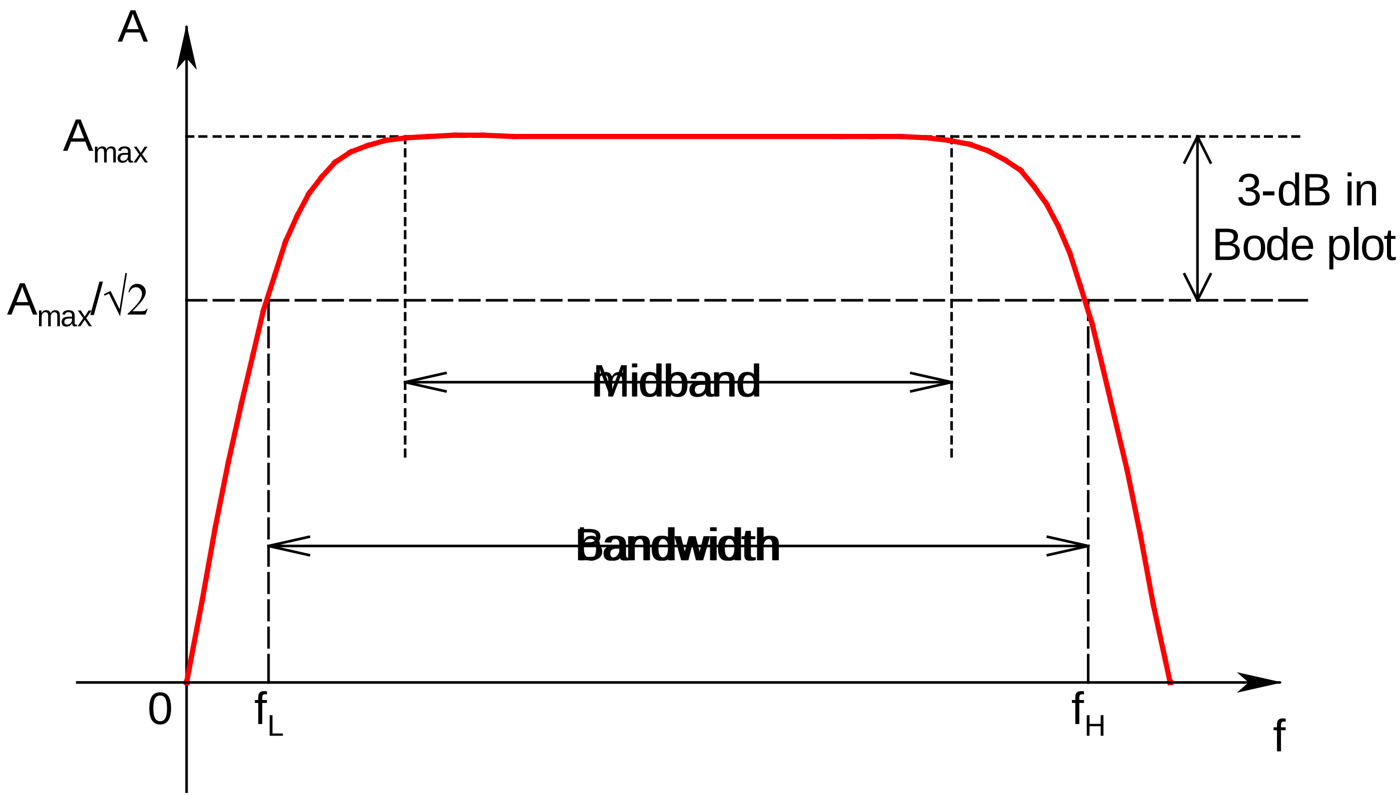
- ***Care***: ***No dimension can be < MFS***
- ***Then what to do if (W/L) < 1***?

AMPLIFIERS

Outline

- ***Amplification*** of ***ac signals*** (***voltage***, ***current***)
- ***Discrete*** and ***IC***
- ***Single-Stage*** and ***Multi-Stage***
- ***Modular approach***
- Interested in:
  - ➢ ***Voltage/Current Gain*** (A_v/A_i)
  - ➢ ***Input/Output Resistance*** (R_i/R_0)

Midband Analysis



f_L: Lower Cutoff Frequency

f_H: Upper Cutoff Frequency

Bandwidth = $f_H - f_L$

Single-Stage Topologies

- ***BJT***:
  - ***Common-Emitter*** (CE)
    - ***i/p to B***, ***o/p from C***, ***E common to both i/p and o/p***
  - ***Common-Base*** (CB)
    - ***i/p to E***, ***o/p from C***, ***B common to both i/p and o/p***
  - ***Common-Collector*** (CC)
    - ***i/p to B***, ***o/p from E***, ***C common to both i/p and o/p***
  - ***Common-Emitter (Degeneration)*** [CE(D)]
    - ***Same as CE***, but now with an ***emitter resistance attached***

- ***MOSFET***:
  - ***Common-Source*** (CS)
    - ***i/p to G***, ***o/p from D***, ***S common to both i/p and o/p***
  - ***Common-Gate*** (CG)
    - ***i/p to S***, ***o/p from D***, ***G common to both i/p and o/p***
  - ***Common-Drain*** (CD)
    - ***i/p to G***, ***o/p from S***, ***D common to both i/p and o/p***
  - ***Common-Source (Degeneration)*** [CS(D)]
    - ***Same as CS***, but now with a ***source resistance attached***

- For ***MOSFETs***, an ***additional topology*** possible: ***i/p to Body***, ***o/p from S/D***
  - Known as ***body-driven*** or ***bulk-driven*** stage
- Each of the ***topologies*** has ***specific characteristics*** in terms of ***voltage/current gain*** and ***input/output resistance***
- Each of these will be treated as a ***module***, and will do a ***complete analysis*** for each of these stages

Multi-Stage Topologies

- Also known as ***Compound Connections***
- ***Combination of 2 or more stages***
  - ***A module by itself***
- ***Some widely used topologies***:
  - ***Darlington***
  - ***Cascode***
  - ***Differential Amplifier/Differential Pair*** (***DA***/***DP***)

Basic Structure

- Consists of a ***driver*** and a ***load***
- ***Driver***: Universally ***active devices***, e.g., ***BJTs*** or ***MOSFETs***
- ***Load***: Can either be ***resistors*** (***passive***) or ***transistors*** (***active***)
- Generally, ***discrete stages*** have ***passive loads***, while ***IC stages*** have ***active loads***

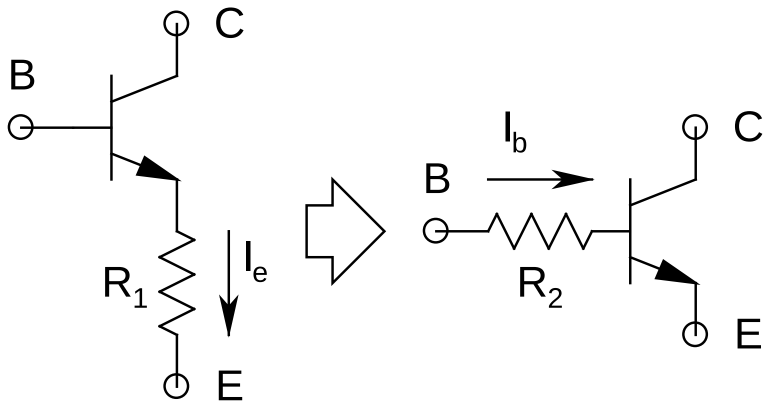
Resistance Transformation (Only for BJTs)

- ***A very useful technique***
- For ***equivalence***:

  $I_b R_2 = I_e R_1$

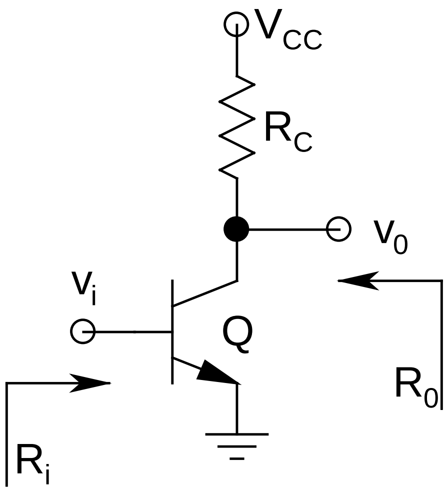
  $\Rightarrow R_2 = (\beta + 1) R_1$

  or $R_1 = R_2/(\beta + 1)$
- ***Apply it freely***!

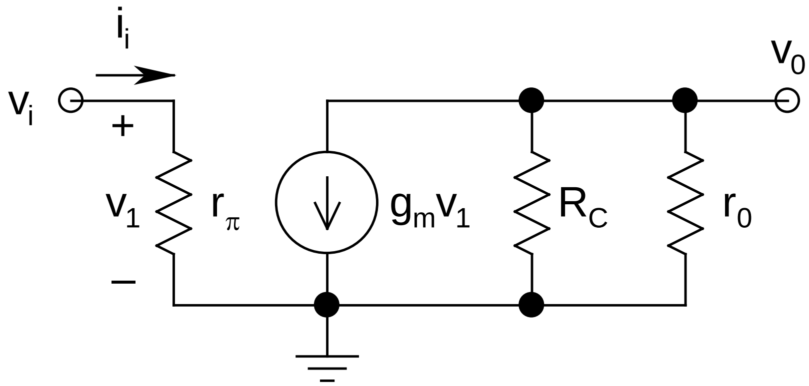


Single-Stage Amplifiers

- ***Common-Emitter*** (CE):



ac Schematic



ac Low-Frequency Equivalent

➢ ***Biasing circuit not shown***