- Thus:

$$V_{id} = \frac{\sqrt{I_{d1}} - \sqrt{I_{d2}}}{\sqrt{\frac{k'_N}{2}\left(\frac{W}{L}\right)}} \qquad (1)$$

- Also:

$$I_{d1} + I_{d2} = I_{SS} \qquad (2)$$

- ***Solving Eqs.(1) and (2)***:

$$I_{d1} = I_{SS}/2 + \xi \quad \text{and}$$

$$I_{d2} = I_{SS}/2 - \xi$$

$$\xi = \frac{k'_N}{4}\left(\frac{W}{L}\right)V_{id}\sqrt{\frac{4I_{SS}}{k'_N(W/L)} - V_{id}^2}$$

- For $V_{id} = 0$, $\xi = 0$, and $I_{d1} = I_{d2} = I_{SS}/2$
  - *Most preferred DC bias point of the circuit*
- *For $V_{id} > 0$, $I_{d1}\uparrow$ and $I_{d2}\downarrow$*
- *For $V_{id} < 0$, $I_{d1}\downarrow$ and $I_{d2}\uparrow$*
- But *for both cases*, the *sum of I_{d1} and I_{d2} remains constant at I_{SS}*
- *Linear Range* of this circuit is *defined by the values of V_{id}*, which *turns either M_1 or M_2 off*

- To find the ***Linear Range***, ***use Eq.(1)*** and ***put either I_{d1} or I_{d2} equal to I_{SS}***:

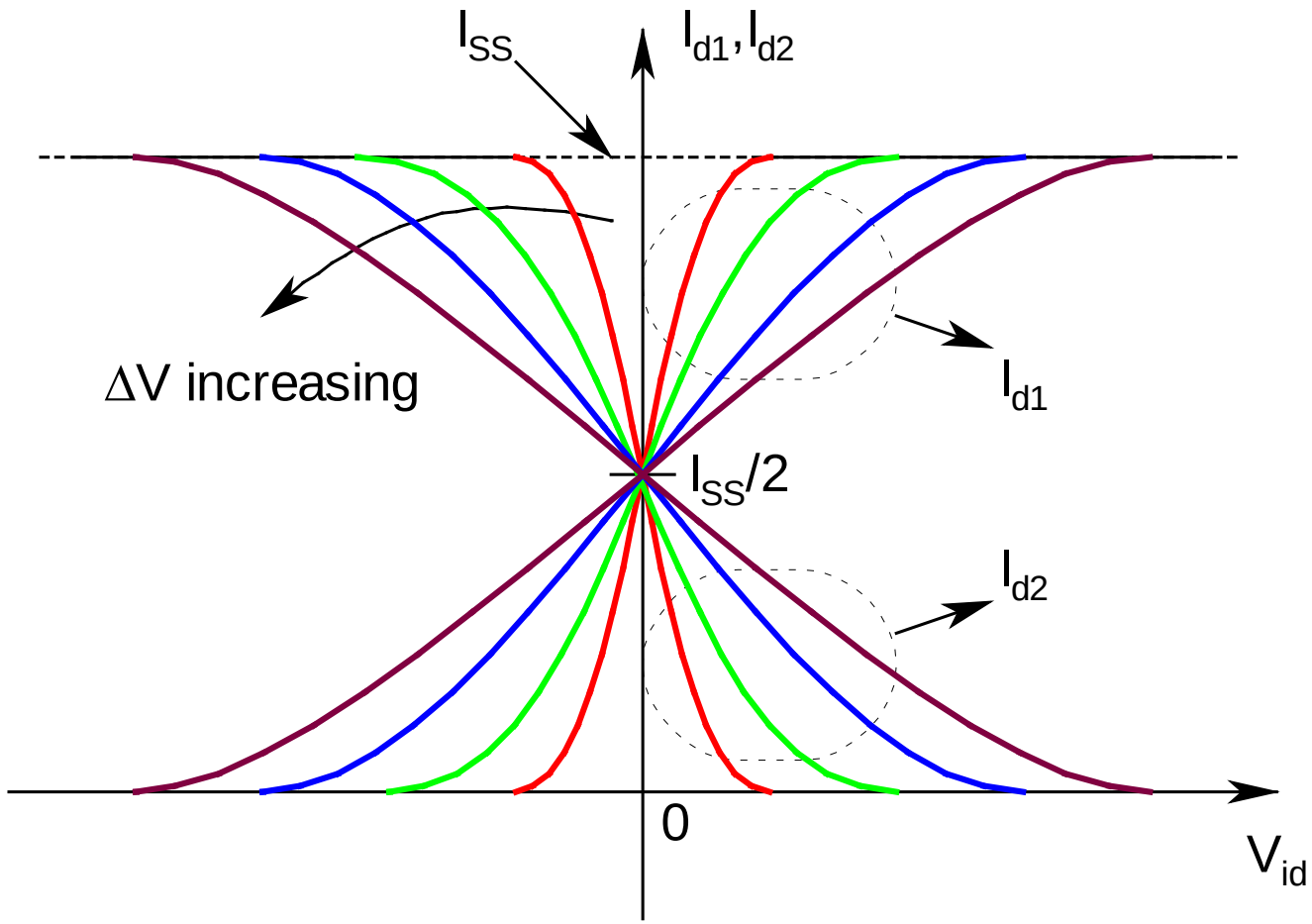
$$\Rightarrow V_{id} = \pm\sqrt{\frac{2I_{SS}}{k'_N\left(W/L\right)}} = \pm\sqrt{2}\left(\sqrt{\frac{2I_{d1}}{k'_N\left(W/L\right)}}\right)\Bigg|_{V_{id}=0}$$

$$= \pm\sqrt{2}\left(\Delta V\right)\Big|_{V_{id}=0}$$

since for $V_{id} = 0$, $I_{SS} = 2I_{d1} = 2I_{d2}$

ΔV = ***Gate Overdrive for M_1/M_2 for $V_{id} = 0$***

- ***Thus, the Linear Range is a function of I_{SS} and (W/L)*** $\Rightarrow$ ***Tremendous flexibility***!
- ***Recall***: In ***npn DA***, this ***Linear Range*** was ***$\pm 4V_T$***, and ***depended only on temperature***



The Current Transfer Characteristics of an NMOS DA

- ***Differential Current***:

$$\partial I_d = I_{d1} - I_{d2} = 2\xi$$

- ***Differential-Mode Output Voltage***:

$$V_{od} = V_{o1} - V_{o2} = (V_{DD} - I_{d1}R_D) - (V_{DD} - I_{d2}R_D)$$
$$= -(\partial I_d)R_D = -2\xi R_D$$

- ***Note***:
  - When $V_{id} = 0$, $\xi = 0$, $\partial I_d = 0$, and $V_{od} = 0$
  - ***This is the perfect DC bias point***
  - ***No need for interstage coupling capacitor***
  - $I_{D1} = I_{D2} = I_{SS}/2$
  - $V_{ID} = 0 \Rightarrow$ ***Tie both gates to ground*** and ***use a negative power supply***

- ***ac Analysis***:
  - ***The procedure adopted for npn DA can be lifted verbatim***
- ***Differential-Mode Half-Circuit***:

Calculation of A_{dm}:

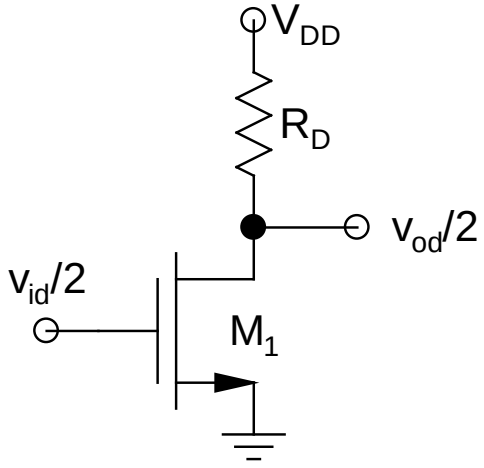
- ***The common-source node is at ac ground*** (***from symmetry***)
- ***Body is also at ac ground***

$\Rightarrow v_{bs} = 0 \Rightarrow g_{mb}v_{bs} = 0$

- ***Simple CS stage***:

$\Rightarrow A_{dm} = v_{od}/v_{id} = -g_m R_D$

$g_m = k_N \Delta V$



Differential-Mode Half-Circuit

- ***Common-Mode Half-Circuit***:

  Calculation of Acm:

  - ***CS(D) stage***, but now ***with body effect present***

    $\Rightarrow A_{cm} = v_{oc}/v_{ic}$

    $= -g_m R_D/[1 + (g_m + g_{mb})2R_{SS}]$

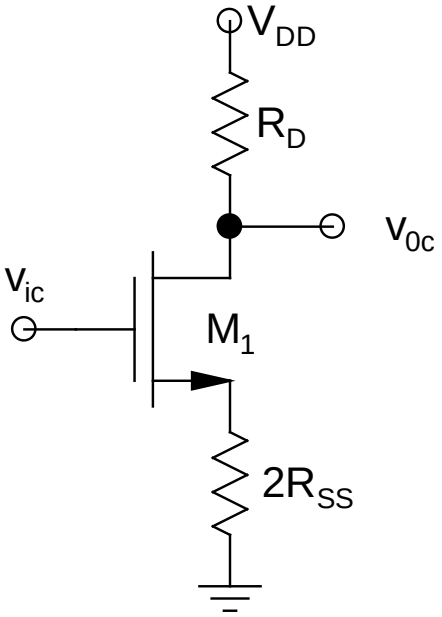
- Thus:

  $CMRR = 20\log_{10}(|A_{dm}/A_{cm}|)$

  $\approx 20\log_{10}[2(g_m + g_{mb})R_{SS}]$

- Again, ***R_{SS} plays no role in A_{dm}***, but ***determines A_{cm} and CMRR***

  $\Rightarrow$ ***A high value of R_{SS} highly desirable***



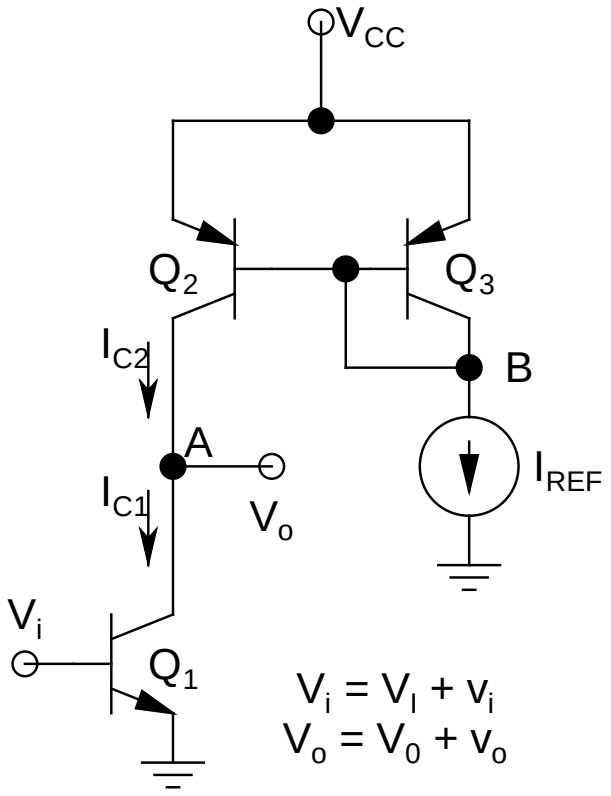
Common-Mode Half-Circuit

- ***Actual situation is not so rosy and hunky-dory***
- ***The DA can become unbalanced if there is a mismatch between the devices and/or the resistors, and our analysis would fail***!
- Gives rise to ***offset voltage*** (***for both npn and NMOS DA***) and ***offset current*** (***only for npn DA***)
- ***This mismatch is caused by technology and is totally random***
- ***Fortunately, the effect is not that severe, since there are technological innovations to match devices and/or resistors***

Actively Loaded Amplifier Stages

- ***Main Goal***: ***To reduce usage of resistors as much as possible*** and ***use transistors instead as active load***
- Interesting to note that ***transistors offer much higher resistance than physical resistors***, while ***occupying much smaller chip area***

- ***npn CE Stage With pnp Active Load***:
  - Q_1: ***Driver***, Q_2: ***Load***
  - Identify Q_2-Q_3 as a ***pnp current mirror***
  - Q_2-Q_3 constitute a ***matched pair***
  - ***Neglecting base currents***: $I_{C2} = I_{REF}$
  - ***Biasing of the circuit is tricky***



Circuit Diagram

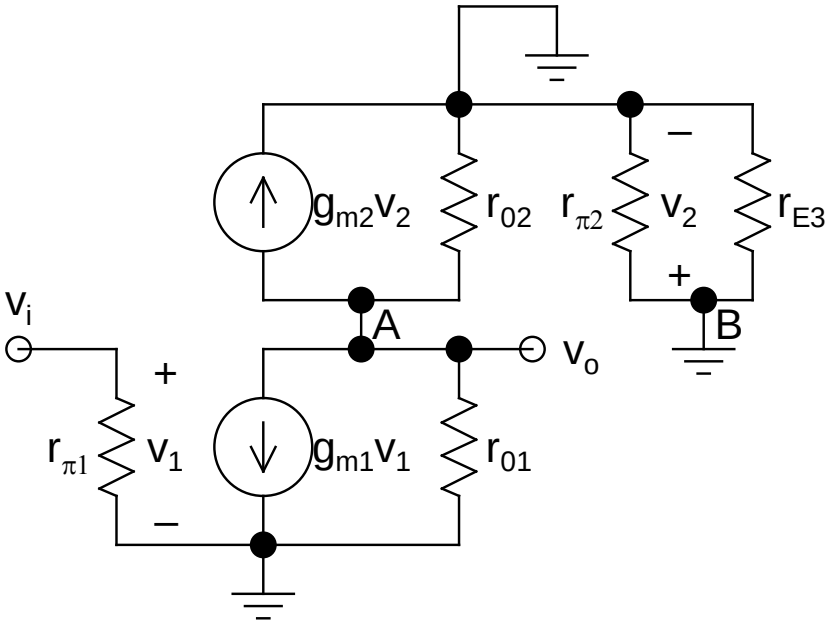
- There is a ***trivial solution*** of $I_{C1} = I_{C2} = 0$, and the ***biasing collapses***
- For ***proper biasing***, I_{C1} ***must equal*** I_{C2} $(= I_{REF})$
- Thus, V_I ***should be properly adjusted***, such that:

$$V_I = V_T \ln(I_{REF}/I_{S1})$$

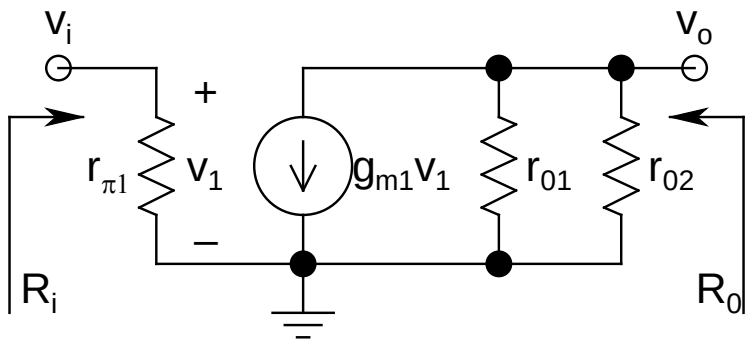
- ***Such a high precision in*** V_I ***may not be practically achievable***

$\Rightarrow$ ***Use a resistor in series with*** V_I ***and self-consistently solve for the bias point***

➢ *ac Analysis*:



ac Midband Equivalent



Simplified Equivalent

- First, note that Q_3 is ***diode-connected*** (***BC short***)

  $\Rightarrow$ The ***equivalent*** of Q_3 is simply a ***resistor*** r_{E3}
- ***Node B*** is a peculiar one, and can be considered ***both open and short***!
  - ***Open because the current source I_{REF} is ideal***
  - ***Short because the base of Q_2-Q_3 is at a fixed DC potential, and thus ac ground***
- In either case, ***$v_2 = 0 \Rightarrow g_{m2}v_2$ disappears***!

  $\Rightarrow$ Leads to the ***simplified equivalent***
- ***By inspection***: $R_i = r_{\pi 1}$ and $R_0 = r_{01} \| r_{02}$
- $A_v = v_o/v_i = -g_{m1}R_0 = -1/(\eta_n + \eta_p)$

  $\eta_n = V_T/V_{AN}$ and $\eta_p = V_T/V_{AP}$
- ***Enormously large gain possible***!