Department of Electrical Engineering
Indian Institute of Technology, Kanpur

EE 210 **Assignment #12** **Assigned: 4.4.25**

1. In a simple BJT Class-B push-pull output stage, as discussed in class, $V_{CC} = -V_{EE} = 12$ V, $R_L = 1$ kΩ, and $V_{CE}(sat) = 0.2$ V. Assume that there is sufficient sinusoidal input voltage available at V_i to drive V_0 to its limit of clipping. Calculate the maximum average power that can be delivered to R_L just before clipping occurs, the corresponding power conversion efficiency, and the maximum instantaneous device power dissipation. Neglect crossover distortion.

2. Consider the bipolar Class-AB push-pull output stage, as discussed in class, with $V_{CC} = -V_{EE} = 15$ V, $I_Q = 200$ μA, $\beta_F(pnp) = 50$, $\beta_F(npn) = 200$, and for all devices $V_{BE}(on) = 0.7$ V, $V_{CE}(sat) = 0.2$ V, and $I_S = 10^{-14}$ A.
   a) Calculate the maximum positive and negative limits of V_0 for $R_L = 10$ kΩ, 1 kΩ, and 200 Ω.
   b) Calculate the maximum average power that can be delivered to R_L (= 1 kΩ) before clipping occurs, and the corresponding power conversion efficiency (for the output devices only). Also, calculate the peak instantaneous power dissipation in each output device. Assume sinusoidal signals.

3. The CMOS Class-AB push-pull output stage, as shown in Fig.1, should be able to deliver a maximum undistorted peak-to-peak swing of the output voltage V_0 of ±3 V, with $R_L = 1$ kΩ, and $V_{DD} = -V_{SS} = 5$ V. Choose the value of the bias voltage V_B such that a bias current of 10 μA flows through M_3. The idling (i.e., standby) current flowing through M_1 and M_2 should be 100 μA. Set $(W/L)_3 = (W/L)_6 = 100$. Design the aspect ratios (i.e., W/L) of M_1, M_2, M_4, and M_5. Neglect body effect and channel length modulation effect. Device data: $V_{TN0} = 0.7$ V, $V_{TP0} = -1$ V, $k'_N = 60$ μA/V^2, and $k'_p = 30$ μA/V^2.

4. A simple RC-coupled amplifier is shown in Fig.2. The biasing circuit is omitted for simplicity, and it is assumed that the transistor is biased with some dc collector current I_C. Show that the low-frequency transfer function $A_v(s)$, taking both C_B and C_E into account, is given by

$$A_v(s) = \frac{v_0}{v_i}(s) = A_{v0}\frac{(s/\omega_B)(1+s/z_1)}{1+a_1 s + a_2 s^2}$$

   where $A_{v0} = -g_m R_C$, $\omega_B = 1/(r_\pi C_B)$, $z_1 = 1/(R_E C_E)$, $a_1 = [R_E C_E + \{R_S + r_\pi + (\beta + 1)R_E\}C_B]$, and $a_2 = R_E C_E(R_S + r_\pi)C_B$. Now, assume that $I_C = 1$ mA, $R_S = 1$ kΩ, $R_C = 2$ kΩ, $R_E = 500$ Ω, $C_B = 10$ μF, and $C_E = 100$ μF. Determine the locations of all the poles and zeros of the system. Also, for the given data, evaluate the lower cutoff frequency f_L of the circuit using the IVTC technique, and compare the result with that obtained from the exact analysis.

5. Consider Prob.8 (HA#9). Assuming $C_1 = C_3 = 10$ μF, $C_2 = C_4 = 100$ μF, and $C_5 = 20$ μF, determine the lower cutoff frequency f_L of the circuit. Hence, determine the lowest frequency square wave input that would show no more than 10% tilt at the output.

6. The transistor used in the circuit of Fig.3 has $\beta = 200$. For parts (c)-(e), use the IVTC technique.
   a) Determine the quiescent values of the dc collector current and the output voltage. Neglect the base current.
   b) Compute the midband voltage gain (v_0/v_s) of the circuit.
   c) Assuming that C_E can be made arbitrarily large, determine C_B so that the circuit has a lower cutoff frequency f_L of 20 Hz.
   d) Assuming that C_B can be made arbitrarily large, determine C_E to give $f_L = 20$ Hz.
   e) Calculate the values of C_B and C_E, such that the circuit has $f_L = 20$ Hz, and the total capacitance requirement is minimized.

7. Consider Prob.5 (HA#9). [The values of R_B and R_C have already been calculated in that problem.]
   a) Select the values of C_1, C_2, and C_3 such that the amplifier has a lower cutoff frequency f_L of 20 Hz, and the total capacitance used by the circuit is minimum.
   b) Given that i_s is a 200 Hz square wave, determine the percent tilt at the output.
   c) What is the lowest-frequency square wave that exhibits no more than 2% tilt at the output?

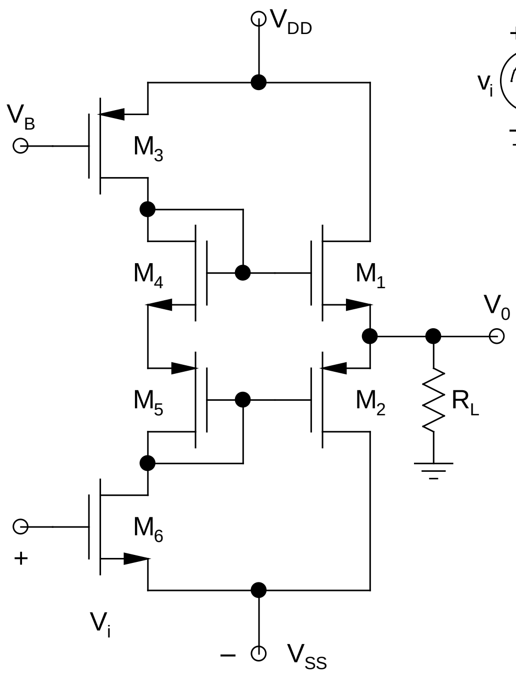

Fig.1

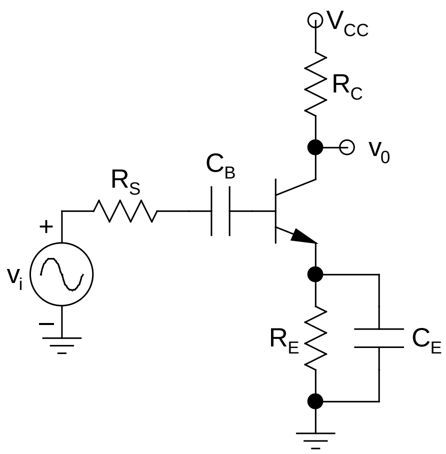

Fig.2

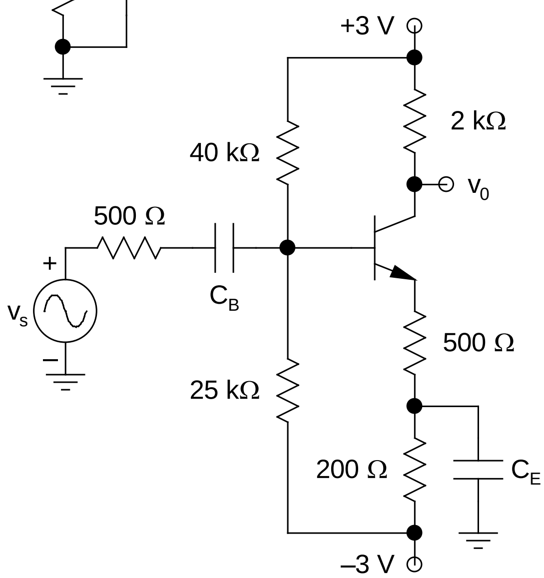

Fig.3