➢ *Linearity and Output Resistance*:

- *While supplying/sinking current to/from load*, *Q_1/Q_2 operate in CC mode*

  $\Rightarrow A_v = R_L/(R_L + r_{Ei})$ $(i = 1,2)$ $(r_{Ei} = V_T/I_{ci})$

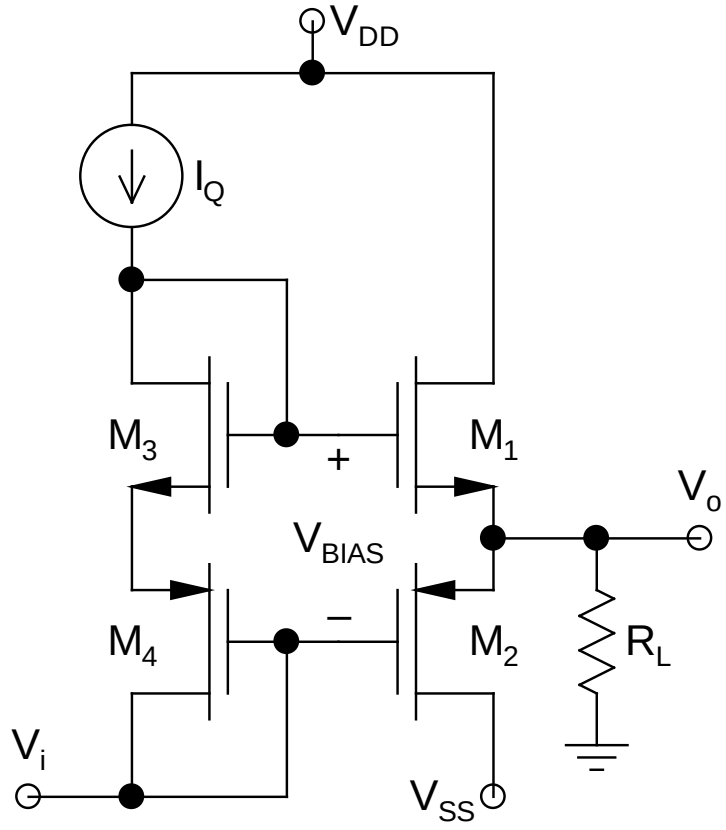
- Thus, if ***$R_L >> r_{Ei}$***, then ***$A_v \rightarrow 1$***, and ***very high linearity in the VTC can be achieved***
- However, ***r_{Ei} is not constant*** - rather ***it changes with the load current***
- Thus, ***A_v can depart significantly from unity***, when the ***load current is very small*** (***large r_{Ei}***)
- Referring to the ***VTC***, the ***slope of the characteristic near $\pm V_\gamma$*** will be ***significantly less than unity***

- However, ***as V_o ↑, load current ↑, r_{Ei} ↓***, and the ***VTC starts to attain its maximum slope of unity***
- Thus, ***for major part***, the ***VTC is highly linear*** and ***produces an almost distortionless output***
- ***Output Resistance***:
  - ***Open R_L*** and ***look back from the output***
  - ***$R_0 = r_{Ei}$*** (***by inpsection***), since ***bases of Q_1-Q_2*** can be considered to be at ***ac ground***
  - ***R_0 is variable***, but ***for major part***, ***extremely small***
- Generally, the ***linearity and output resistance*** are ***calculated*** at the ***region of maximum slope*** of the ***VTC***

- ***Summary***:
  - *Quite small standby power*
  - *Large current driving capability*
  - *Almost linear VTC*
  - *Very low distortion at the output*
  - $A_v \sim 1$
  - *No phase shift between input and output*
  - *Very low output resistance*

  Thus, this stage is a superb one and is highly popular!

- ***MOS Implementation***:
  - ***Biased using dual symmetric power supplies V_{DD}/V_{SS}***
  - ***M_1-M_2 in push-pull configuration***
    - ***M_1 supplying current to load (R_L) during the positive half cycle***
    - ***M_2 pulling current away from load during the negative half cycle***



Circuit Schematic

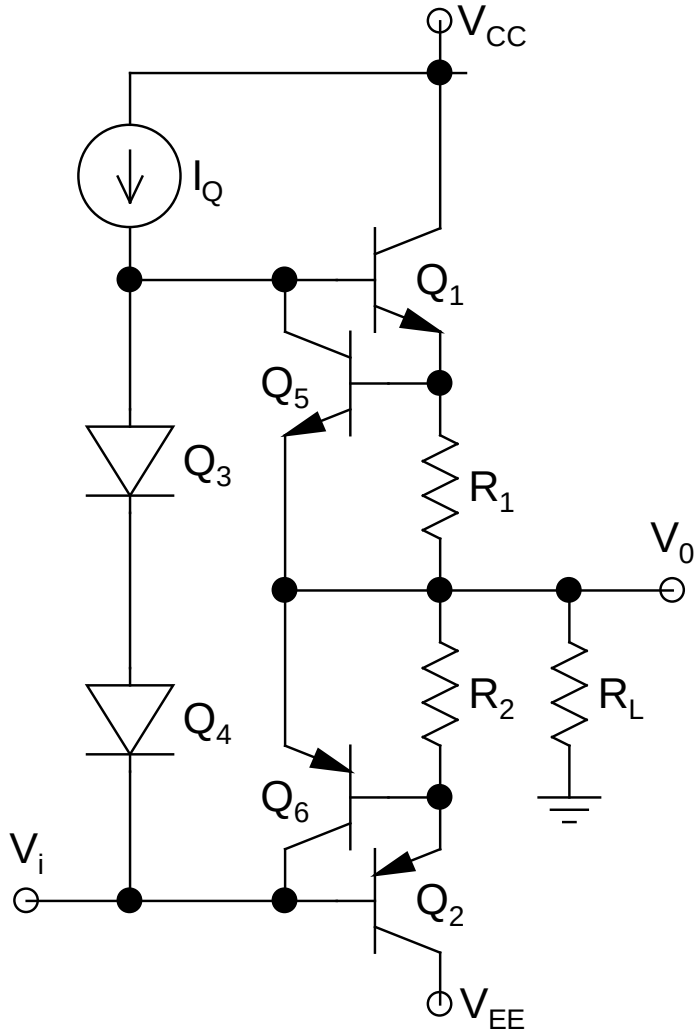
- M_1-M_2 ***prebiased*** by the ***series combination*** of M_3-M_4 (***both diode-connected***) ***biased with*** I_Q
- ***Develops*** V_{BIAS} ***across the gates of*** M_3-M_4, which is ***same as that between the gates of*** M_1-M_2
- V_{BIAS} ***chosen to be slightly less than*** $(V_{TN} + |V_{TP}|)$
- ***Crossover Distortion eliminated completely***, at the cost of ***introducing standby power*** into the system
- ***Rest of the operation of the circuit exactly similar to that of a BJT Class AB Push-Pull Output Stage***

- ***All transistors suffer from body effect problem***

  $\Rightarrow$ More distortion at the output
- ***The linearity of the VTC is not that good***
- ***Low current drive capability***
- ***Biasing itself becomes tricky***, due to the ***body effect of M_3-M_4***
- The ***output resistance not that low***, since ***MOSFETs have lower g_m than BJTs***
- Overall, the stage ***suffers from quite a few problems*** and is ***not used much***
- We will explore this through an assignment

- ***Overload Protection***:
  - ***Protects the output stage from accidental short-circuits***
  - ***Needs 4 more components***:
    - ***2 BJTs*** (Q_5,Q_6)
    - ***2 Resistors*** (R_1,R_2)

      R_1,R_2 ~ 25-50 Ω



Circuit Schematic

- During ***normal operation***, these ***extra circuits*** play absolutely ***no role***, and come ***into picture*** only under ***accidental short-circuit*** of the ***output terminal to ground***
- ***Numerical Example***:
  - Assume V_i at its ***positive peak***, the ***maximum drive current*** to the base of Q_1 = 1 mA, and $\beta_1 = 100$
  - Now output gets ***accidentally shorted to ground*** ($V_o = 0$)

    $\Rightarrow$ $I_{c1} = 100\ mA$ and $V_{ce1} = 5\ V$

    $\Rightarrow$ $P_1 = 500\ mW$
  - This may be ***way above*** the ***maximum power rating*** of the transistor (~ ***100-150 mW***) and the transistor would ***burn out*** $\Rightarrow$ ***potentially dangerous situation***!

➢ *Principle of Operation of the Protection Circuit*:

- Assume ***positive*** V_i with Q_1 ***supplying current to load***
- Q_2 ***is off during this time***
- As $R_L \downarrow$, $I_{c1} \uparrow$ (since $I_{c1} = V_o/R_L$)

  $\Rightarrow$ V_{be5} $(= I_{c1}R_1)$ ***also*** $\uparrow$
- As $V_{be5} \rightarrow V_\gamma$ of Q_5, it starts to ***turn on***

  $\Rightarrow$ A ***part of base drive current*** of Q_1 starts to get ***shunted away*** by Q_5, and ***appears at the output*** almost ***without any gain*** $(1/\alpha_5)$
- This acts as a ***limit of the rate*** at which the ***output current can increase***, and thus, ***protects the circuit***

- Thus, the ***current can't increase indefinitely***
- Assume $R_1 = 30\ \Omega$ and $V_\gamma = 0.6\ V$

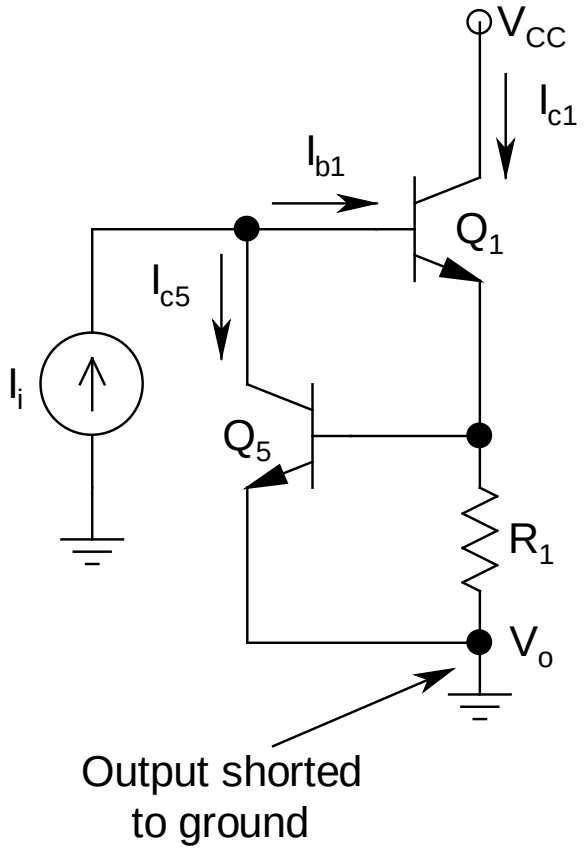
  $\Rightarrow$ As soon as I_{c1} ***reaches about 20 mA***, Q_5 ***cuts in***, ***shunts current away from the base of*** Q_1, and ***protects the circuit***
- Due to the ***exponential dependence*** of this ***shunted current*** on V_{be5}, the ***maximum output current*** will ***saturate near around 20 mA itself***
- Thus, under this case, if the output is ***accidentally shorted to ground***, then P_1***(max) will be around 100 mW***, which is ***well within limit***, and ***protection will be achieved***

- Similarly, for the ***negative half cycle***, this job of ***protection will be achieved by the Q_6-R_2 combination***
- The ***drop across R_2*** will depend on the ***amount of current*** being ***sunk by Q_2***
- Once this drop ***reaches the cut-in voltage*** of Q_6, it will ***turn on***, and ***bypass the drive current of Q_2***, thus ***protecting the circuit***
- This ***protection circuit*** is ***widely used*** due to its ***efficacy***, and the ***most popular analog building block***, the ***op-amp***, ***uses this protection scheme***

➢ *Quantitative Estimate of the Protection Mechanism*:

- Assume ***V_i positive*** and ***supplying drive current*** I_i to Q_1
- ***Output shorted to ground*** $\Rightarrow V_o = 0$
- $I_i = I_{b1} + I_{c5}$

  $I_{c5} = I_{S5}\exp(V_{be5}/V_T)$
- $V_{be5} = I_{c1}R_1$ (***assuming $\alpha_1 = 1$*** and ***neglecting I_{b5}***)



Protection Scheme

- For ***small values*** of I_{c1}, V_{be5} will be ***small***, and I_{c5} will be ***negligible***
- Also, $I_{c1} = \beta_1 I_{b1} = \beta_1 (I_i - I_{c5})$

  $\Rightarrow \beta_1 I_i = I_{c1} + \beta_1 I_{S5} \exp(I_{c1} R_1 / V_T)$
- This is the ***final protection expression***
- For ***small*** I_{c1}, the ***second term*** on the ***RHS*** will be ***negligible*** as compared to the ***first term***

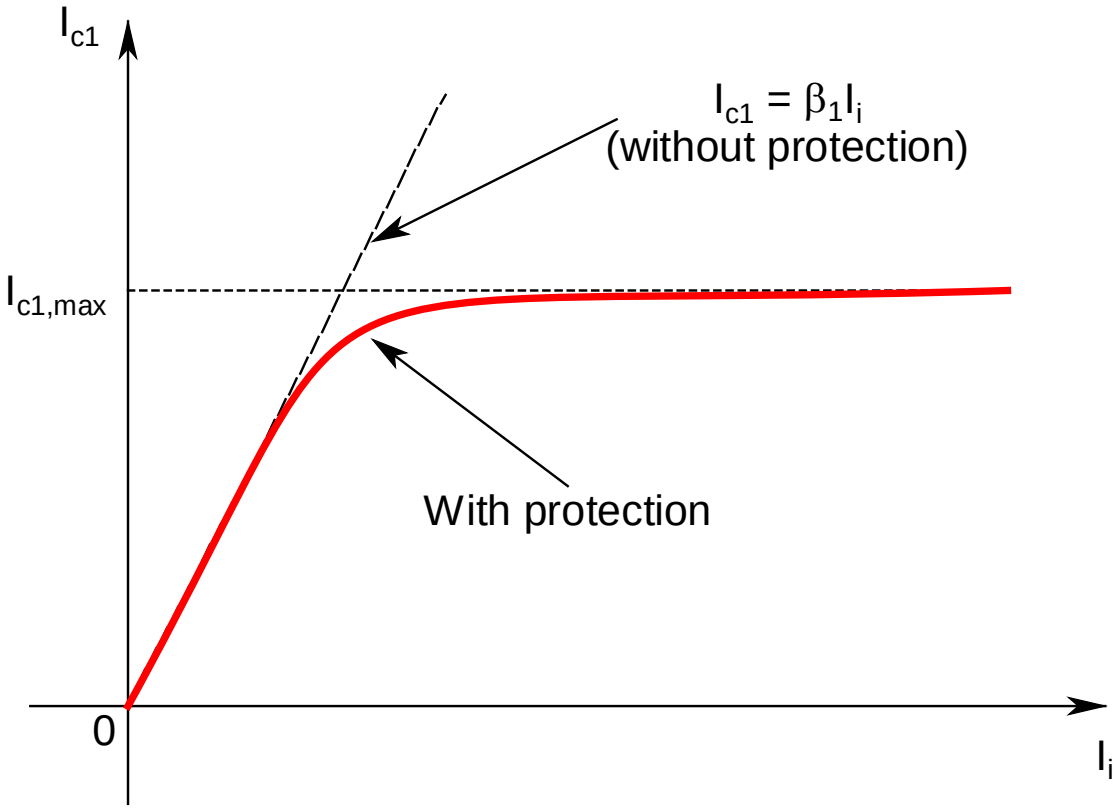
  $\Rightarrow$ ***I_{c1} would follow I_i linearly with proportionality constant β_1***
- As ***I_{c1}*** $\uparrow$, the ***second term*** on the RHS ***increases at a much more rapid rate*** than the ***first term***

- Once it starts to become ***comparable*** to the first term, a ***very little change*** in I_{c1} can ***counter a large change*** in I_i

  $\Rightarrow$ ***I_{c1} gets clamped to almost a constant value of $I_{c1,max}$***

- Note that the ***protection equation*** is ***transcendental***

  $\Rightarrow$ ***Needs numerical or iterative solution***



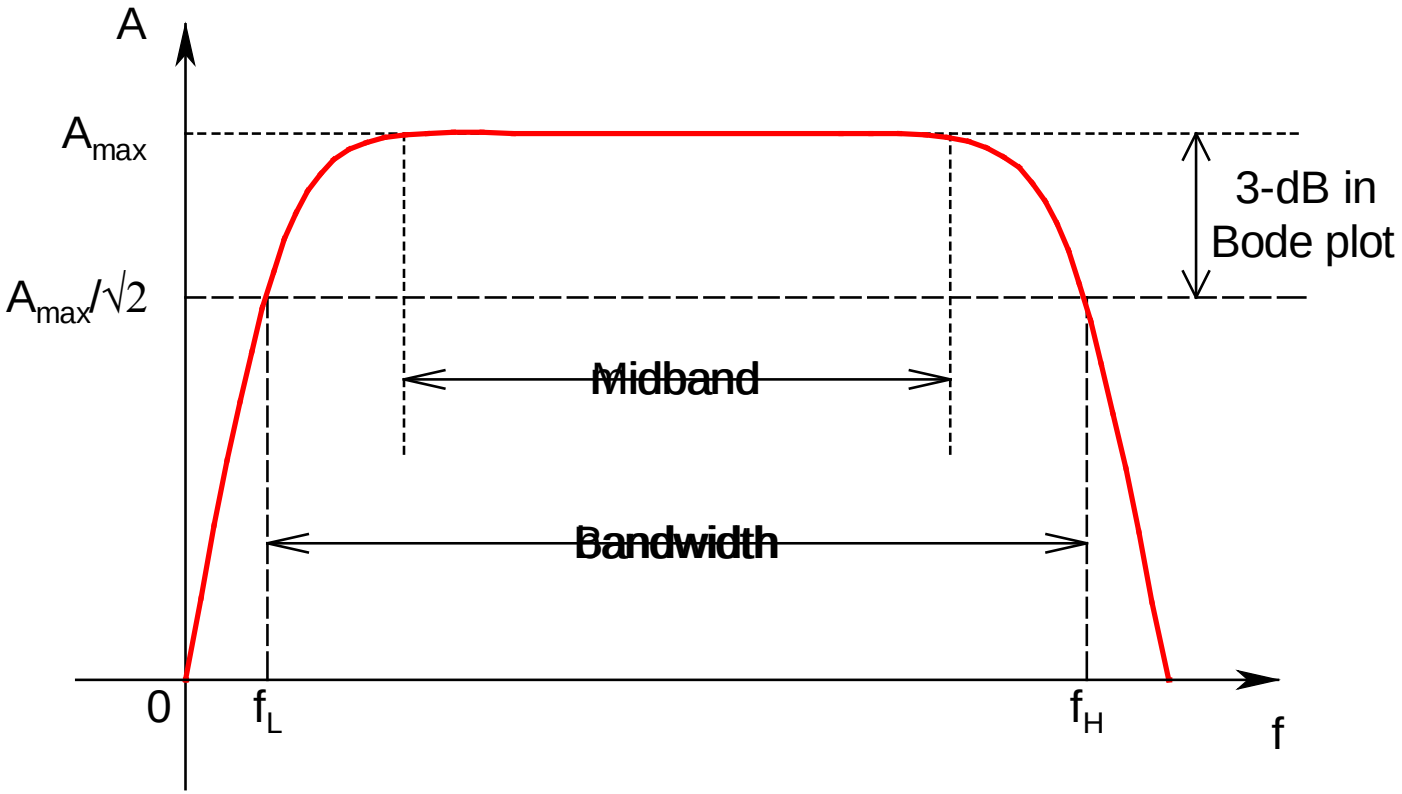
Protection Characteristic

FREQUENCY RESPONSE

- So far, considered ***midband analysis***, where ***all capacitive effects were neglected***
  - ***Voltage/current gain was independent of frequency***
- In ***practical amplifier circuits***, however, the ***gain would depend on frequency***
- ***Characterized by***:
  - ***Lower Cutoff Frequency*** (f_L)
    - ***Contributed by external capacitors*** (C_E, C_B, C_C)

- ***Upper Cutoff Frequency*** (f_H)
  - ***Contributed by device capacitances*** (***for BJTs***: C_π, C_μ; ***for MOSFETs***: C_{gs}, C_{gd}, C_{sb}, C_{db})

- These capacitors create ***charge storage effects***, and ***introduce time constants*** into the circuit
- ***Discrete circuits show both f_L and f_H***
- ***IC stages show only f_H***, since most of them are ***direct coupled*** without the need for any ***external capacitors***



f_L: Lower Cutoff Frequency

f_H: Upper Cutoff Frequency

Bandwidth = $f_H - f_L$

- ***Exact analysis extremely complicated***
  - Most often, results in ***very complicated expressions***, ***completely hiding the physical feel of the phenomenon***
  - ***Makes debugging extremely difficult***
    - For example, a circuit having ***4 capacitors***, will have a ***fourth-order transfer function***, which needs to be ***solved*** to get all the ***poles and zeros*** of the system
  - However, there are ***techniques***, which make these ***analyses*** extremely ***trivial***
    - ***Not accurate***, but ***extremely simple***, and makes ***debugging easy***

- ***Techniques***:
  - ***Infinite-Value Time Constant (IVTC) Method***
    - ***Used for obtaining f_L***
  - ***Zero-Value Time Constant (ZVTC) Method***
    - ***Used for obtaining f_H***
- These techniques are ***extremely easy to apply***, and the results are ***quite close to actuals***
- However, there is ***one limitation*** of these techniques

- They give information only regarding the ***Dominant Pole*** (DP) of the circuit
- ***Completely hides information*** about ***other poles and zeros*** of the circuit [known as ***Non-Dominant Poles*** (NDP) or ***Zeros*** (NDZ)]
- Anyway, information about ***NDP and NDZ*** are ***not*** that ***critically important*** from ***practical point of view***