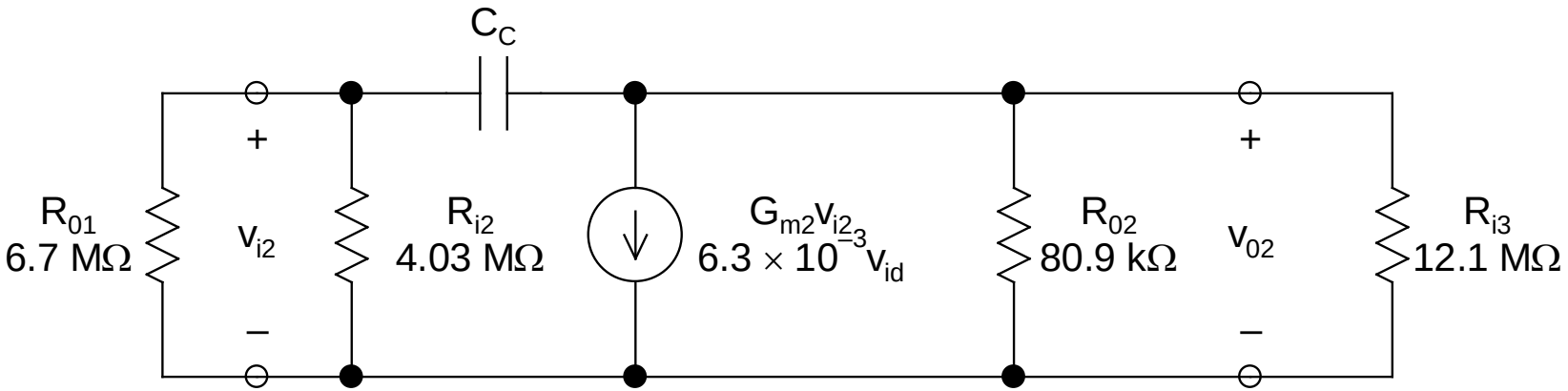
- ***Compensation***:
  - Actual evaluation of the ***frequency response*** characteristic of 741 is a ***huge task***, even with the ***ZVTC technique***
  - There will be ***numerous poles and zeros***, out of which, some will be ***important***, while others will be ***inconsequential***
  - However, there will of course be a ***Dominant Pole*** (DP), and rough calculation shows that it is ~ ***1 MHz***, which is the ***bandwidth*** of the ***uncompensated op-amp***

- Now, ~ ***100 dB open-loop gain*** with ***1 MHz bandwidth*** is a ***ready recipe for disaster*** as far as the ***stability of the system*** is concerned
- Hence, for ***unconditional stability*** under ***unity negative feedback***, e.g., ***voltage follower***, ***compensation is imperative***
- In 741, this task is accomplished by the technique of ***Dominant Pole Compensation*** (DPC) through the use of the ***compensation capacitor*** C_C, ***connected between the input and output of the gain stage***

- To obtain the ***required value*** of C_C, we use the cascade of the ***2-port networks***, as was done earlier to compute the ***overall voltage gain***



- Denote $R' = R_{01} \| R_{i2} = 2.5\ M\Omega$ and $R'' = R_{02} \| R_{i3} = 80.4\ k\Omega$

- The ***simplified circuit*** can be easily identified as the ***three-legged creature***, and using the ***ZVTC technique***:

$$R_C^0 = R' + R'' + G_{m2} R' R'' = 1.27\ \text{G}\Omega$$

- Now, to get an estimate of the ***DPF*** f_d, we assume that the ***open-loop gain*** is exactly 100 dB, and the ***first pole*** of the ***uncompensated op-amp*** is ***exactly 1 MHz***

$$\Rightarrow f_d = 10\ \text{Hz}$$

- Also, $f_d = \omega_d/(2\pi)$, with $\omega_d = 1/\tau$, and

$$\tau = R_C^0 C_C$$

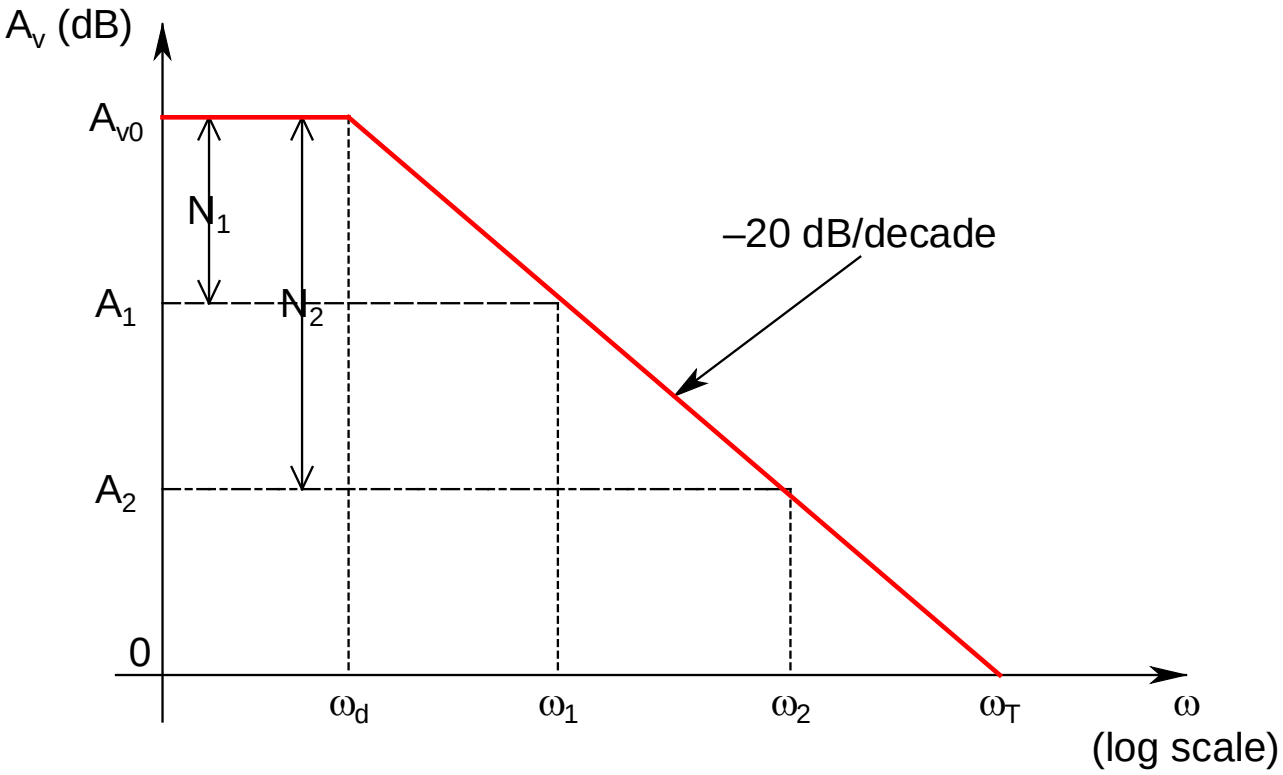
- Thus:

$$C_C = \tau / R_C^0 = 12.5 \text{ pF}$$

- Note that with this ***compensation scheme***, the ***open-loop bandwidth*** of the ***compensated op-amp*** drops all the way down to ***10 Hz*** from ***1 MHz***
- However, this is not really a ***limitation***, since the ***open-loop gain*** is ***so high***, that even with ***negative feedback***, ***sufficiently high values of gain can be achieved***

- ***Unity-Gain Bandwidth (f_T)***:
  - ***Product*** of the ***dominant pole frequency*** and the ***open-loop gain***
  - This is also the ***bandwidth*** of the system when the ***gain is unity*** (hence the name!)
  - Also known as the ***gain-bandwidth product*** (GBP)
  - It is ***1 MHz*** for this case
  - Note that under ***DPC***, it's also the ***first pole*** of ***uncompensated system***
  - With ***negative feedback***, the ***GBP remains constant***

    $\Rightarrow$ ***As gain $\downarrow$, bandwidth $\uparrow$, and vice-versa***



A_{v0}: Midband Gain, ω_d: Compensated Bandwidth, ω_T: Unity-Gain Bandwidth

N_1 and ω_1, N_2 and ω_2: Amount of Feedback and Corresponding Bandwidth

A_1, A_2: Gain With Feedback N_1, N_2

$$A_{v0}\omega_d = A_1\omega_1 = A_2\omega_2 = \omega_T$$

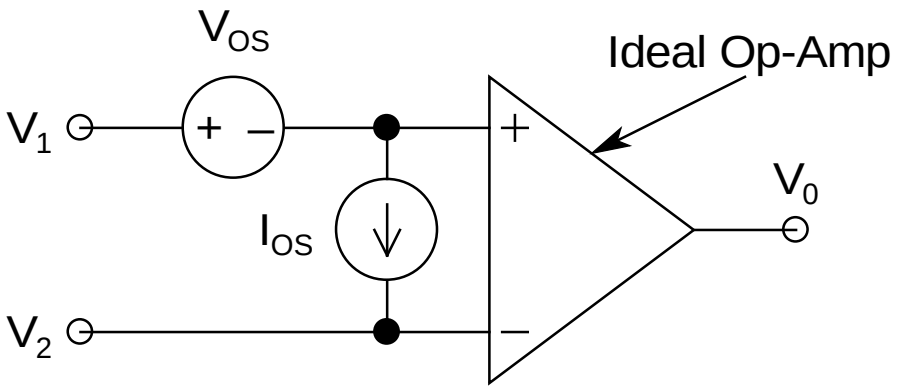
- ***Anomalies and Limitations***:
  - ***Input Offset Voltage/Input Offset Current***
  - ***Saturation Voltages***
  - ***Minimum Allowed Supply Voltage***
  - ***Slew Rate and Full-Power Bandwidth***

➢ *Input Offset Voltage/Input Offset Current*:

- Created due to a ***mismatch*** between the ***input transistors***
- For an ***op-amp*** with $A_{vOL} = 10^5$, operated with a ***power supply*** of ±10 V, V_{id} ***needed*** to cause V_0 to ***reach either of these two extremes*** = ±100 μV
- The ***mismatch*** between the ***input transistors*** typically create a ***voltage difference*** between the ***inputs***, known as the ***Input Offset Voltage*** (V_{OS})
- ***Typical value*** of V_{OS} for ***741 op-amp*** ~ 5-10 mV
- This would ***cause*** V_0 to ***saturate*** at either $+V_{CC}$ or $-V_{CC}$
- This is known as ***saturation*** or ***latch-up*** problem

- In ***741***, there is a ***provision*** to ***eliminate*** this ***problem***, known as ***offset nulling***
- Refer to the ***circuit*** of 741, and note ***pin numbers*** 1and 5 ***connected*** to the ***emitters*** of Q_5 and Q_6
- Between these ***two pins***, a ***potentiometer*** is connected, with its ***wiper*** connected to $-V_{CC}$
- This ***potentiometer*** is known as the ***offset null resistor***
- It ***eliminates*** the ***effect*** of V_{OS} by ***creating*** an ***unequal division*** of ***bias currents*** in the ***two branches*** of the ***input circuit***, just enough to ***balance*** the ***difference*** caused due to ***device mismatch***

- ***The Input Offset Current (I_{OS})***:
  - ***Difference*** between the ***base currents*** (known as ***Input Bias Currents*** I_1 and I_2) of Q_1 and Q_2
  - ***Extremely small*** (~ ***tens to hundreds of nA***)
- I_{OS} and V_{OS} are actually ***interrelated***, since both of them are created due to ***device mismatch***, and have almost ***identical manifestations***



Both V_{OS} and I_{OS} are not used
V_{OS} (I_{OS}) is used when the input is voltage (current)

Modeling of the Anomalies With Regard to V_{OS} and I_{OS}

➢ *Saturation Voltages*:

- An *ideal op-amp* should have *rail-to-rail swing* at the *output*
- The *actual output swing* of a *real op-amp* is *never between rail-to-rail*
- Also, the *positive* and *negative* peaks of V_0 are *not same*

  $\Rightarrow$ *Maximum possible output swing is asymmetric*
- These *two limits* of V_0 are known as *positive and negative saturation voltages* (V_{SAT}^+ and V_{SAT}^- respectively) *(~0.9 V below V_{CC} and ~1.6 V above V_{EE})*
- If the *input drive* to the *op-amp* and the *gain* are such that the *magnitude* of V_0 becomes *greater* than either V_{SAT}^+ or $|V_{SAT}^-|$, then V_0 would get *clipped* at either of these *two values*

➢ *Minimum Allowed Supply Voltage*:

- Circuit for 741 is ***extremely robust***, and can be ***operated*** with a ***very wide range*** of ***supply voltage***
- However, there is a ***lower limit*** of the ***supply voltage***, below which it ***can't be ensured*** that ***all transistors*** operate in the ***FA region***
- To find this, look for the ***branch*** containing the ***most number of transistors***, since ***that branch*** would obviously ***need the largest voltage*** across it to ***ensure*** that all its ***constituent transistors operate in the FA region***
- From the ***circuit schematic*** of 741, ***this branch*** can be very easily identified to be ***either of the two sections of the input stage***

- Considering the ***left branch***, neglecting the ***potential dropped*** across R_1, and not letting ***CE voltage*** of any of the ***transistors*** to ***drop below*** 0.7 V (***onset of saturation***), there would ***four diode drops*** (~ 2.8 V) ***along this branch***

  $\Rightarrow$ ***741 should work satisfactorily for power supply all the way down to about ± 3 V***

  $\Rightarrow$ ***Swing of +2.1 V and –1.4 V***

- Thus, there is a ***wide range*** of ***power supply***, ***starting from ± 3 V***, for which ***741 should work satisfactorily***

  $\Rightarrow$ ***Shows the robustness of the circuit***

➢ *Slew Rate and Full-Power Bandwidth*:

- This *limitation* is *observed* under *large-signal operation*, when the *input signal swing* is *greater* than the *linear range* of the *input differential pair*
- *Recall*: The *linear range* of a *bipolar differential pair* is $\sim \pm 4V_T$
- *Beyond this*, it basically *acts like a switch*, *transferring the bias current between the two branches*, *depending on the sign of the input voltage*
- Under such cases, the *compensation capacitor* C_C *limits* the *maximum possible rate of change* of V_0
- This is known as the *Slew Rate* (SR) of the op-amp:

  $SR = (dV_0/dt)_{max}$

- ***Two*** SRs are defined: SR^+ (***positive SR***) and SR^- (***negative SR***) for ***positive*** and ***negative*** excursions of V_0 respectively, generally expressed in ***V/μsec***
- Large negative signal applied to the base of Q_1

  $\Rightarrow$ It turns off

  $\Rightarrow$ Q_5-Q_6 turn off

  $\Rightarrow$ I_{C8} flows through Q_2-Q_4 and charges C_C

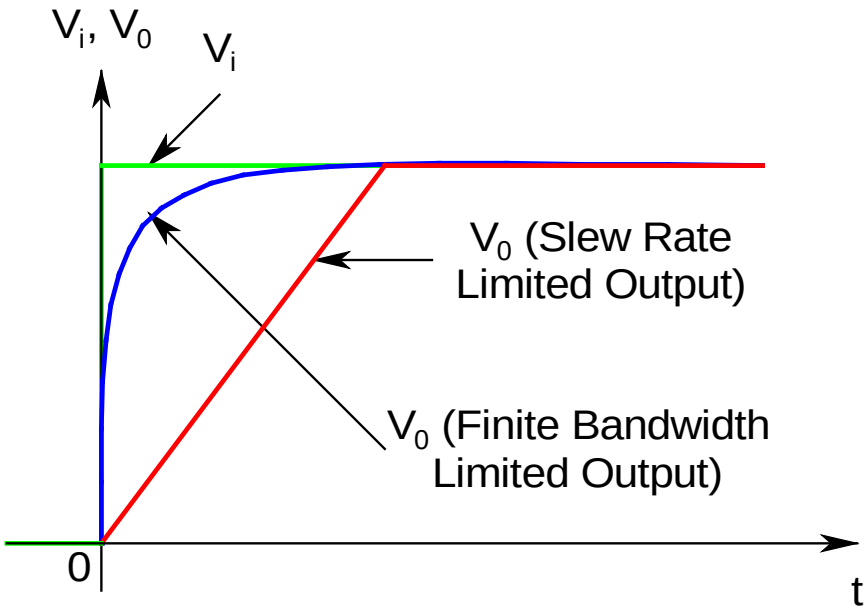
  $\Rightarrow$ Constant current charging

  $\Rightarrow$ V_0 starts to increase linearly with time

  $\Rightarrow$ $SR^+ = I_{C8}/C_C = (19\ \mu A)/12.5\ pF) = 1.52\ V/\mu sec$

- If the ***frequency*** of the ***input signal*** is such that the ***required time rate of change*** of V_0 is ***more*** than this, then V_0 ***won't be able to follow*** the input – rather, it will be ***dictated*** by the SR^+, and will ***change linearly with time***
- Similarly, when a large negative signal is applied to the base of Q_2, it turns off, Q_1-Q_5-Q_6 carry I_{C8}, with C_C discharging, and V_0 drooping linearly with time

  $\Rightarrow SR^+ = SR^- = 1.52$ V/μsec



Slew Rate Limitation of Op-Amps

- Situation becomes ***more dramatic*** if a ***sinusoidal signal*** is applied at the ***non-inverting input*** of the op-amp, connected in a ***voltage-follower*** configuration
- Let ***input signal*** $V_i = V_M \sin(\omega t)$, with ***large*** V_M

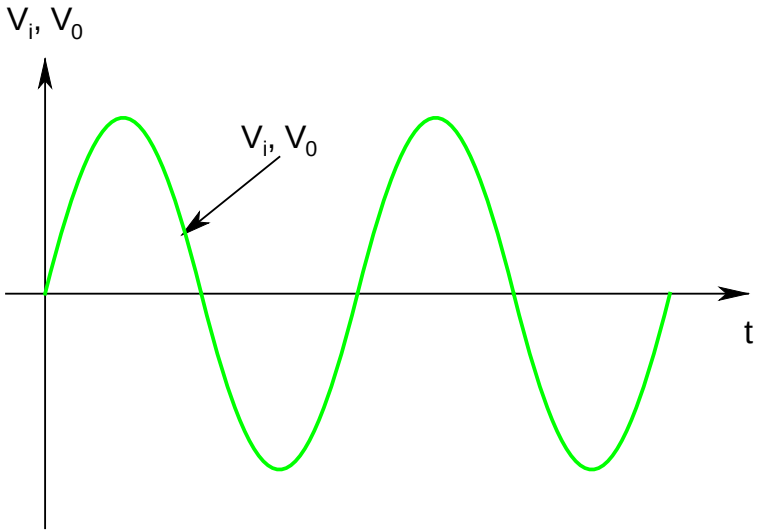
  $\Rightarrow$ ***Transistors*** in the ***differential input stage*** act as ***switches***
- Under ***unity feedback***, V_0 would ***follow*** V_i

  $\Rightarrow dV_0/dt = dV_i/dt = V_M \omega \cos(\omega t)$
- The ***maximum value*** of this ***derivative*** occurs when $\omega t = n\pi$ $(n = 0, 1, 2, \ldots)$

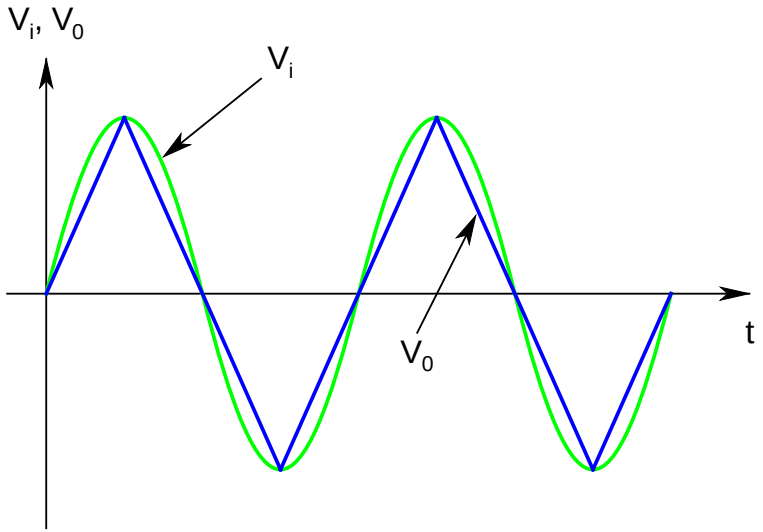
  $\Rightarrow$ It occurs when the ***signal crosses zero***
- So long as ***this rate*** remains ***smaller*** than SR, V_0 would ***follow*** V_i with ***fidelity***

- However, as soon as ***dV_0/dt becomes $\geq SR$***, V_0 ***won't be able to follow*** V_i anymore – rather, it would ***start to become triangular***
- ***Note***: $dV_0/dt\uparrow$ with an ***increase*** of ***either V_M or ω or both***

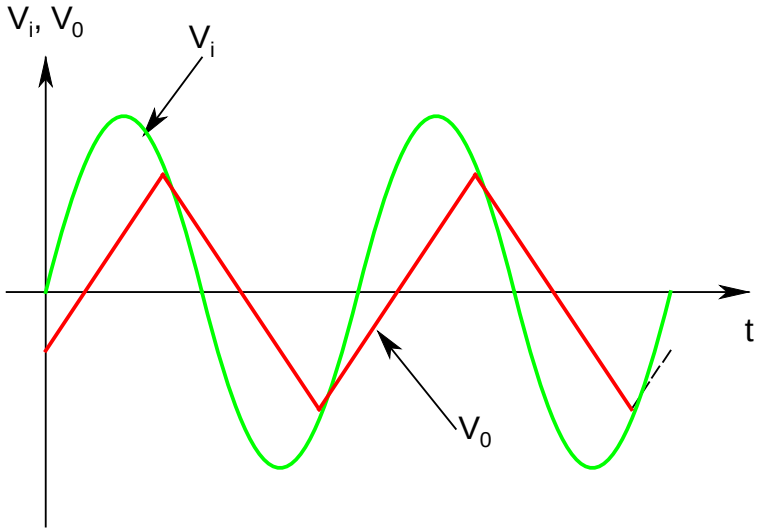
  $\Rightarrow$ ***What essentially matters is the product $V_M\omega$***
- If this ***product*** keeps on ***increasing*** beyond the SR, then V_0 remains ***triangular***, however, ***two major observations*** become apparent:
  - ❖ The ***zero crossings*** of V_0 ***do not quite coincide*** with those of V_i
  - ❖ The ***peak-to-peak swing*** of V_0 starts to become ***smaller*** than that of V_i due to V_0 ***not getting enough time*** to ***reach its maximum possible value***



Normal Behavior



Onset of Slew Rate Limitation



Severely Slew Rate Limited

- If $V_M\omega$ becomes ***very large***, then there ***may not be any output at all***

  $\Rightarrow V_0$ would ***become zero***, implying that the op-amp is ***not able to keep up with the variation*** of V_i at all!

- ***Mathematical Description***:
  - Let the ***gain*** of the op-amp = A

    $\Rightarrow (dV_0/dt)_{max} = AV_M\omega$
  - This must be ***less*** than the SR of the op-amp to get a ***distortion-free output***
  - ***Maximum possible value*** of $AV_M = V_{SAT}$

    $\Rightarrow$ The ***maximum allowed value*** of ω ($= \omega_M$) of V_i for V_0 to be ***without any distortion*** due to ***slew rate limitation***:

    $\omega_M = SR/V_{SAT}$

- This is an ***extremely important relation***, and ω_M is referred to as the ***full-power bandwidth***
- It is a ***constant*** for a given op-amp
- This ***derivation*** is for V_0 ***swinging*** between $\pm V_{SAT}$
- If the ***swing*** of V_0 is ***less*** than this, then ω can be ***increased*** beyond ω_M, following the ***relation***:

  $SR = \omega_M V_{SAT} = \omega_0 V_0 = \omega_0 A V_i$

  ω_0: ***Frequency till which V_0 won't have any slew rate limited distortion***

  $\Rightarrow$ ***Maximum amplitude*** of V_i (of ***frequency*** ω_0), beyond which ***slew rate limited distortion*** would ***set in at the output***:

  $V_{i,max} = \omega_M V_{SAT}/(\omega_0 A)$


"That's all Folks!"