EE-380 EC Lab-04
Multistage Amplifier

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Section: C

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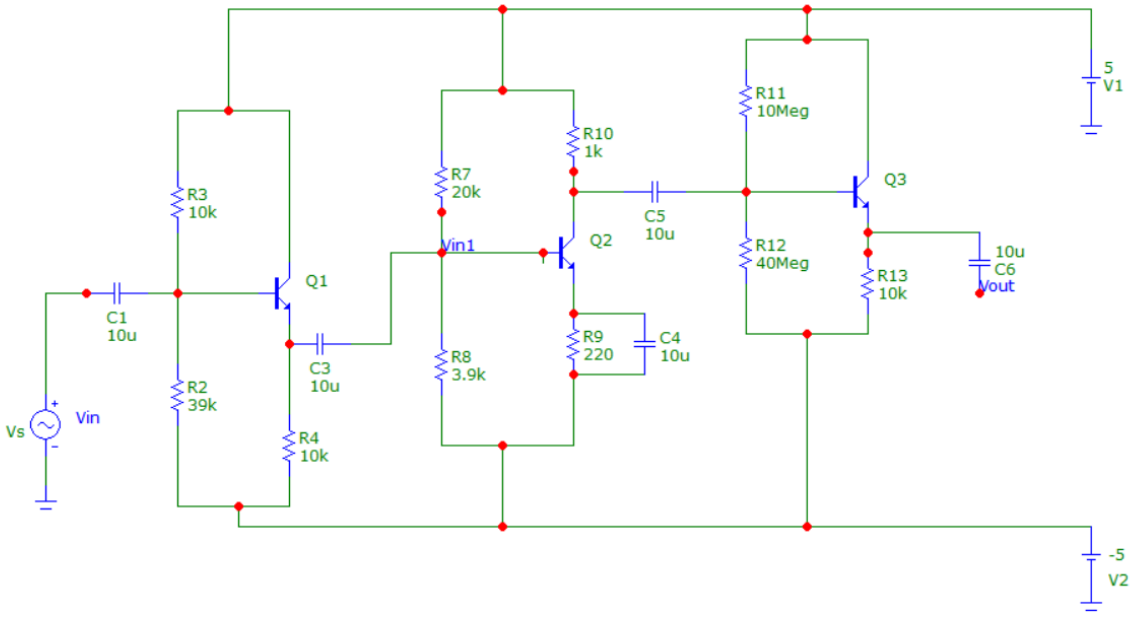
1 Design, prototype, and characterize three-stage amplifiers using three BC547 NPN BJTs, ensuring that the resulting circuits demonstrate characteristics with potential practical utility

Note: Since the values of β for different transistors were measured in the lab, the pre-lab simulations were repeated using β = 320 to allow a reasonable comparison.

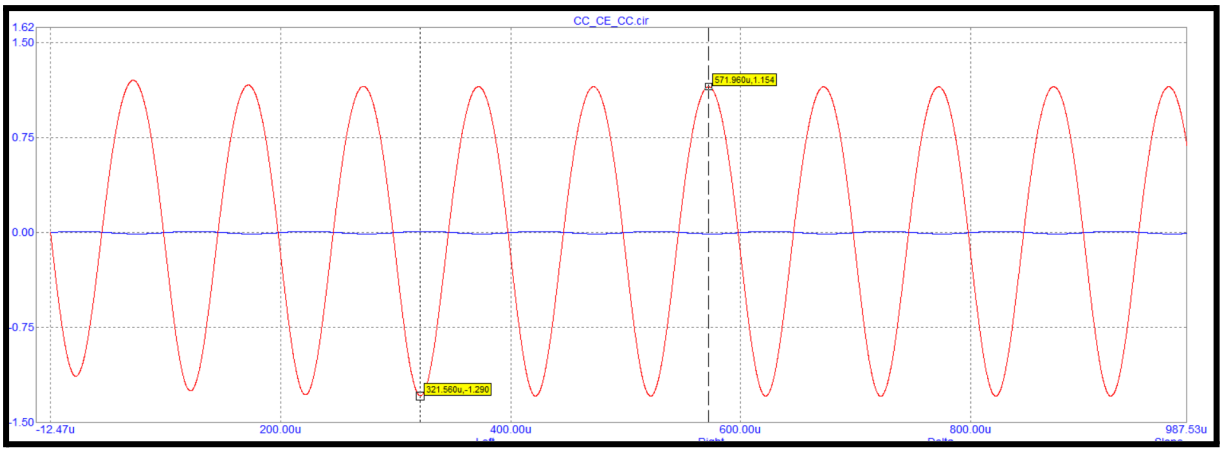
1.1 Pre Lab Simulation and Design

CC-CE-CC amplifier



1. β = 320 for all transistors

2. Overall Voltage Gain

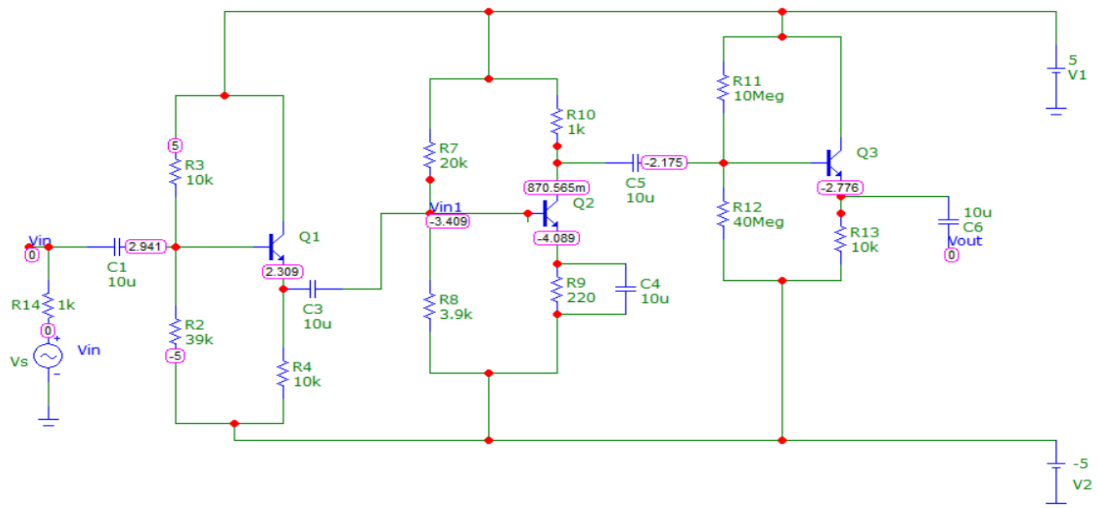


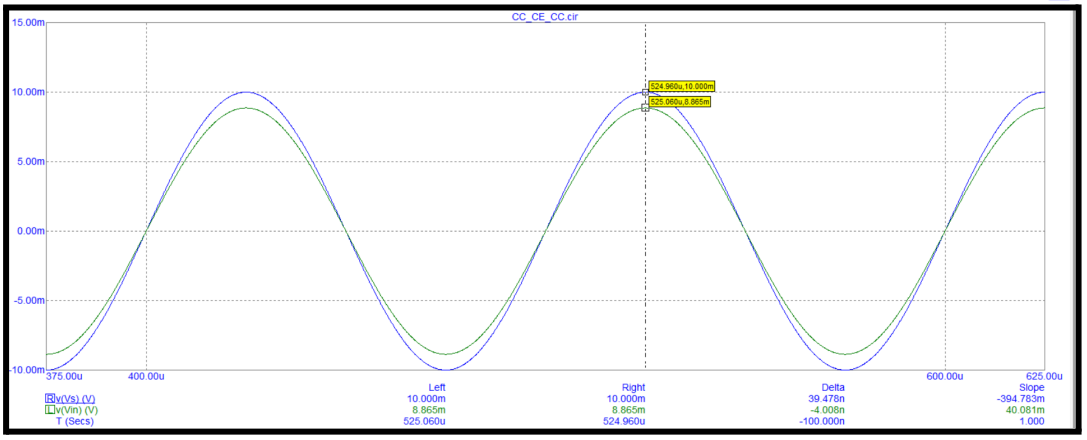
Input : $V_S = 10\sin(2\pi ft)$ mV , where f = 10kHz

Output Amplitude = $\frac{1.154-(-1.290)}{2} = 1.222V$

Voltage gain $A_v \simeq 122$

3. Input Resistance R_I

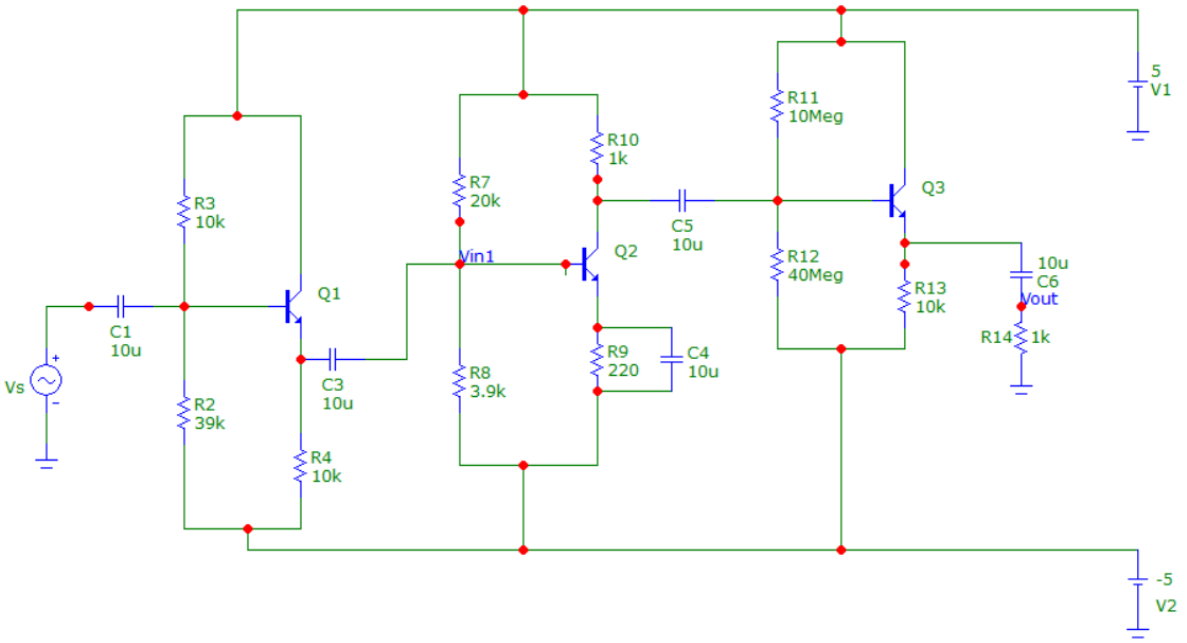


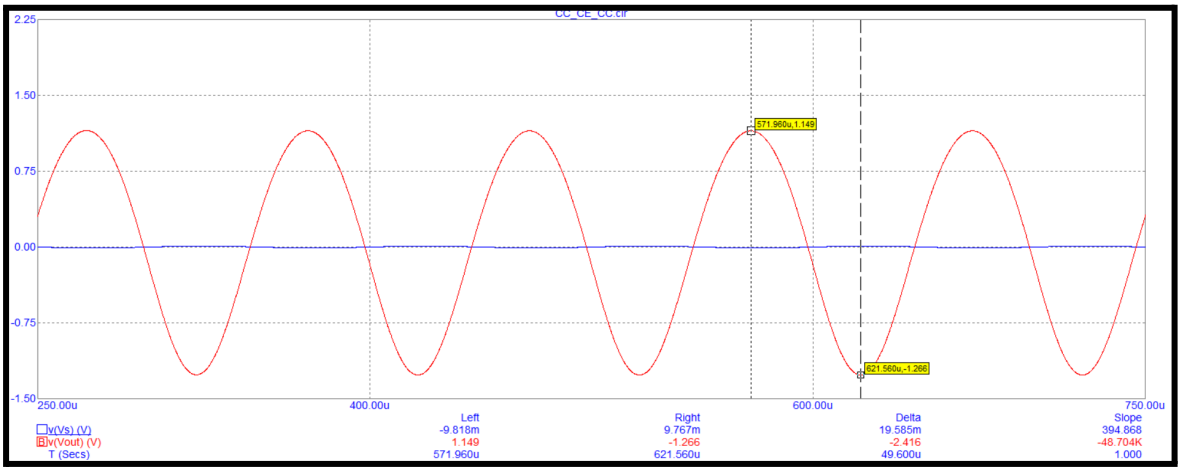


$$R_{in} = \frac{V_{in}}{V_S - V_{in}} R_s = \frac{8.865mV}{10mv - 8.862mv} (1k\Omega)$$

$$\Rightarrow R_{in} = 7.8k\Omega$$

4. Output Resistance R_O





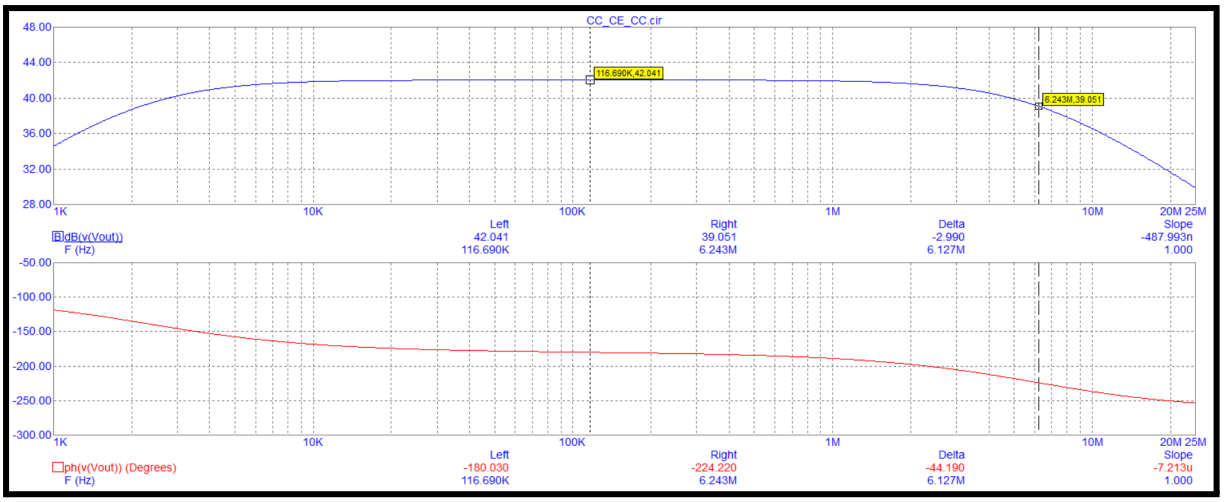
$$V_{out,\,without\,R_L} = 1.222V \text{ and } V_{out,\,with\,R_L} = 1.2075V$$

$$\text{we know that } \frac{V_{out,\,with\,R_L}}{V_{out,\,without\,R_L}} = \frac{R_L}{R_O + R_L}$$

$$0.98813 = \frac{20000}{R_O + 20000}$$

$$\Rightarrow R_O = 240.25\Omega$$

5. Measuring Frequency Response

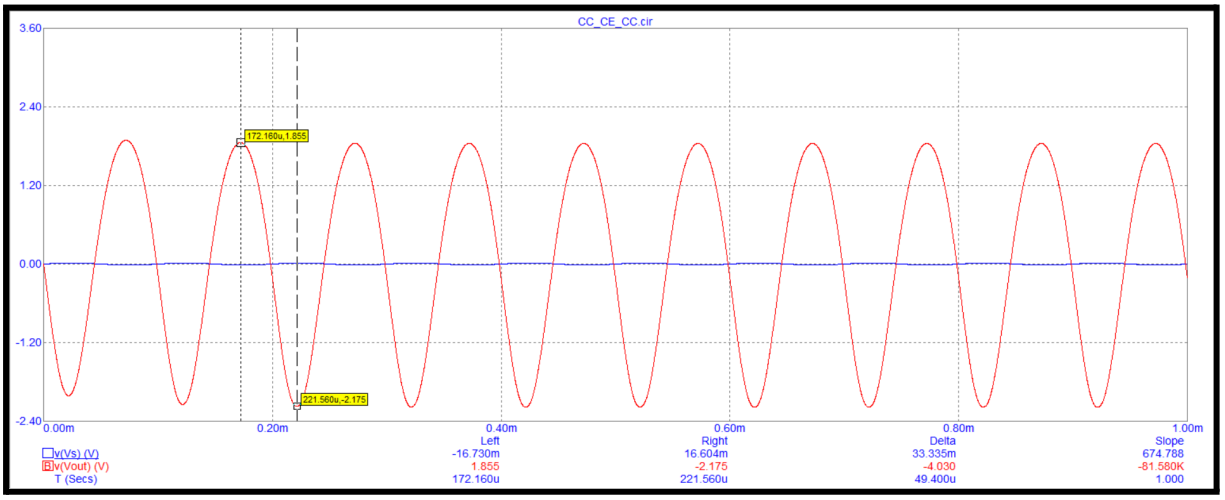


Cutoff/-3dB frequency is around 6.24MHz

6. Maximum Voltage Swing

   Increasing the input voltage above 17mv causes the output to distort

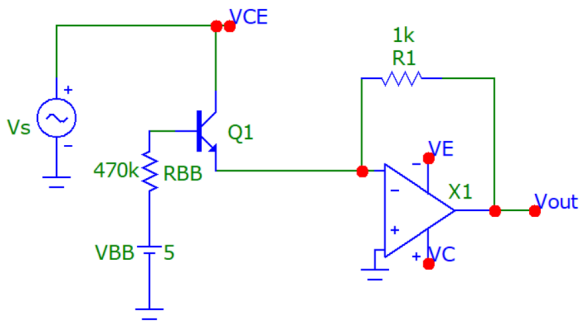
   Input : 18 mv sine wave



Therefore the maximum output swing is around 4.03V ~ 4V

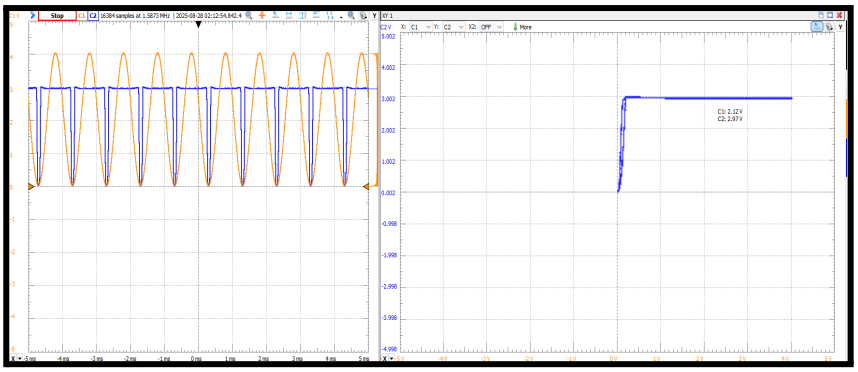
1.2 In Lab measurements and Post Lab calculations

1. Measuring β



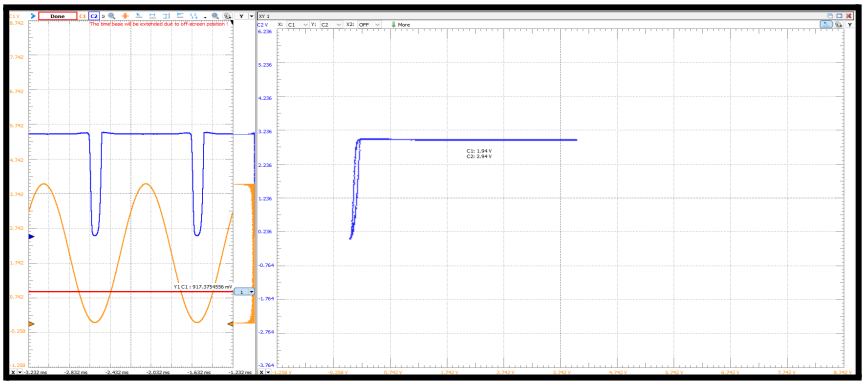
Transistor Q1:

$$I_B = \frac{V_{BB} - V_B}{R_{BB}} = \frac{5 - 0.66}{470} mA$$
$$= 0.00923mA \; or \; 9.23\mu A$$
$$\beta_{Q1} = \frac{I_C}{I_B} = \frac{2.97}{9.23} * 1000$$
$$\Rightarrow \beta_{Q1} = 321$$



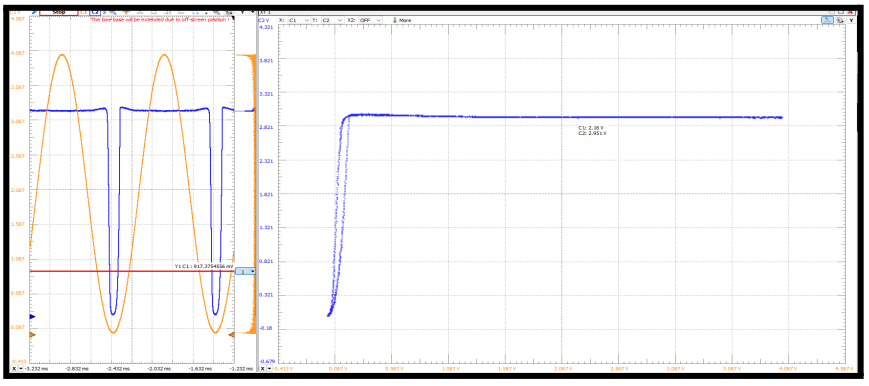
Transistor Q2:

$$I_B = \frac{V_{BB} - V_B}{R_{BB}} = \frac{5 - 0.66}{470} mA$$
$$= 0.00923mA \; or \; 9.23\mu A$$
$$\beta_{Q2} = \frac{I_C}{I_B} = \frac{2.94}{9.23} * 1000$$
$$\Rightarrow \beta_{Q2} = 319$$



Transistor Q3:

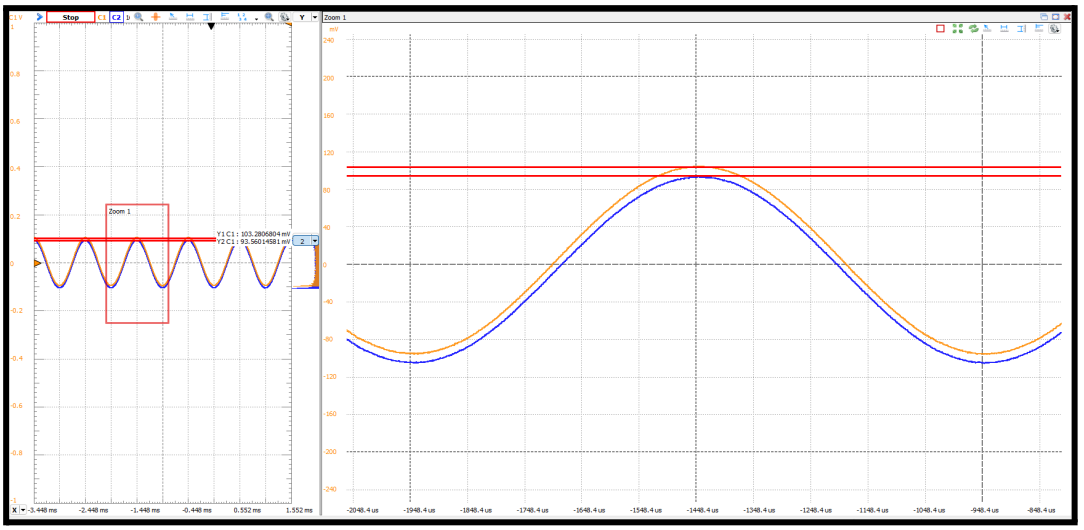
$$I_B = \frac{V_{BB} - V_B}{R_{BB}} = \frac{5 - 0.66}{470} mA$$
$$= 0.00923mA \; or \; 9.23\mu A$$
$$\beta_{Q3} = \frac{I_C}{I_B} = \frac{2.95}{9.23} * 1000$$
$$\Rightarrow \beta_{Q3} = 320$$



Approximately β comes around 320 for these transistors, and the same value was used in simulations.

2. Voltage Gains

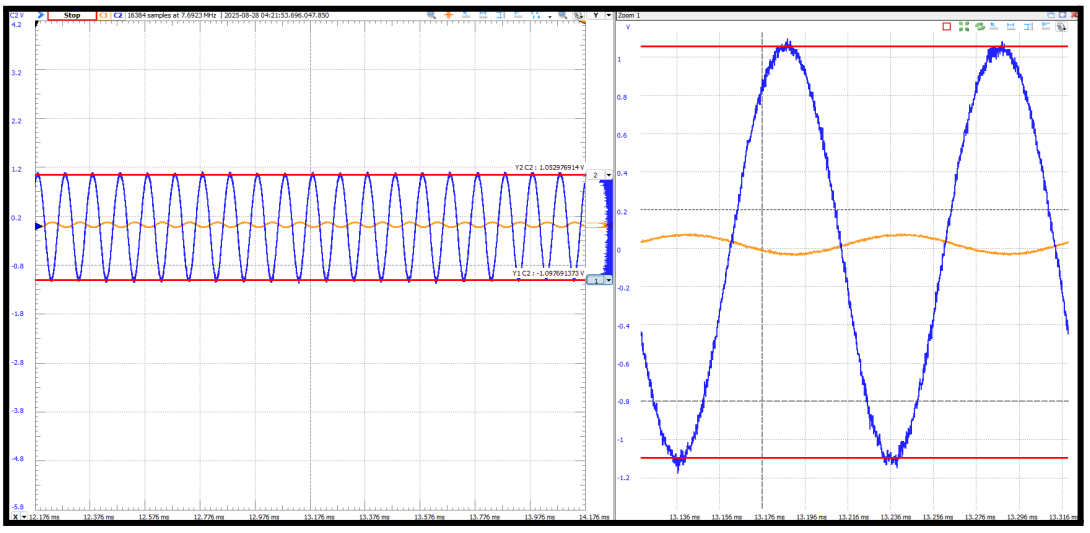
- CC stage



$Voltage\ gain\ of\ stage\ 1\ (CC_1),\ A_{v_{CC1}} \simeq \frac{0.936}{1.033}$

$\Rightarrow A_{v_{CC1}} \simeq 0.91$, which is expected as CC stage should have gain close to 1 and it is used as a buffer or impedance matcher

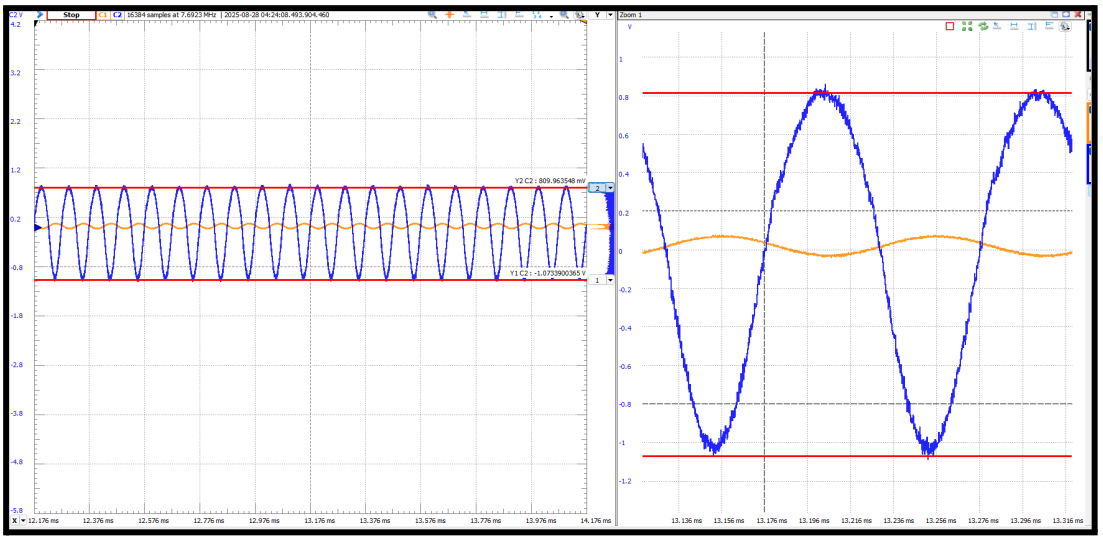
- CC-CE stage



$Voltage\ gain\ of\ stage\ 1\ +\ stage\ 2\ (CC\ -\ CE),\ A_{v_{CC1-CE}} \simeq \frac{(1.053+1.098)/2\ V}{0.01V}$

$\Rightarrow A_{v_{CC1-CE}} \simeq 107.55$, if we consider the stages to be non loading then the CE stage gain comes out to be $\frac{A_{v_{CC1-CE}}}{A_{v_{CC1}}} = \frac{107.55}{0.91}$, i.e $\Rightarrow A_{v_{CE}} \simeq 118$

- CC-CE-CC stage



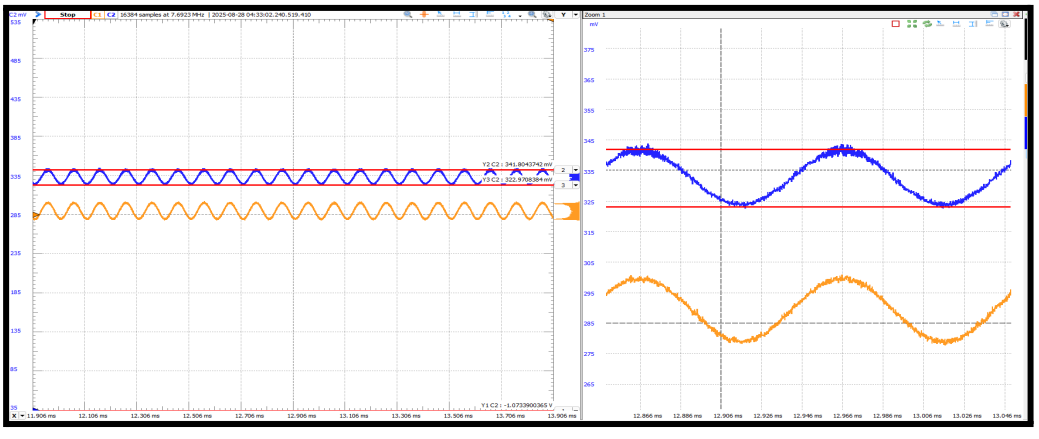
$$Voltage\ gain\ of\ CC-CE-CC,\ A_{v_{CC1-CE-CC}} \simeq \frac{(0.810+1.073)/2\ V}{0.01V}$$

$$\Rightarrow overall\ gain\ of\ the\ 3-stage\ amplifier\ A_v = A_{v_{CC1-CE-CC2}} \simeq 94.15$$

If we consider the stages to be non loading then the CC_2 stage gain comes out to be $\frac{A_{v_{CC1-CE-CC2}}}{A_{v_{CC1-CE}}} = \frac{94.15}{107.55}$, i.e $\Rightarrow A_{v_{CC2}} \simeq 0.875$, close to 1 as expected

In simulation the overall gain of the 3-stage amplifier came around 122 but in lab it was 94.15, which is fairly close, some differences are due to other parameters of the transistor apart from beta, which were not accounted for in the simulation and factors like resistance tolerances, parasitic effect etc.

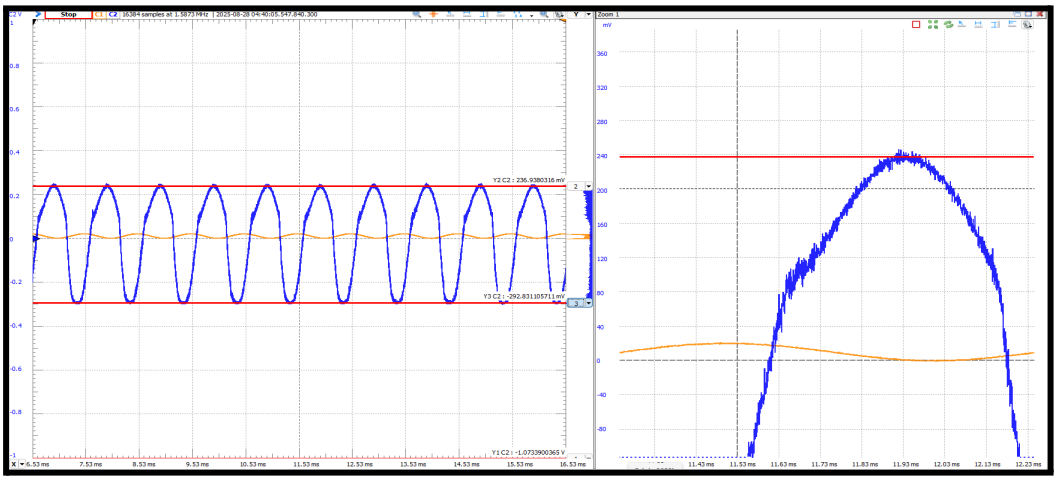
3. Input Resistance R_I



$$R_{in} = \frac{V_{in}}{V_S - V_{in}} R_s = \frac{9.415mV}{10mv - 9.415mv} (1k\Omega)$$

$$\Rightarrow R_{in} \simeq 16.1k\Omega$$

4. Output Resistance R_O



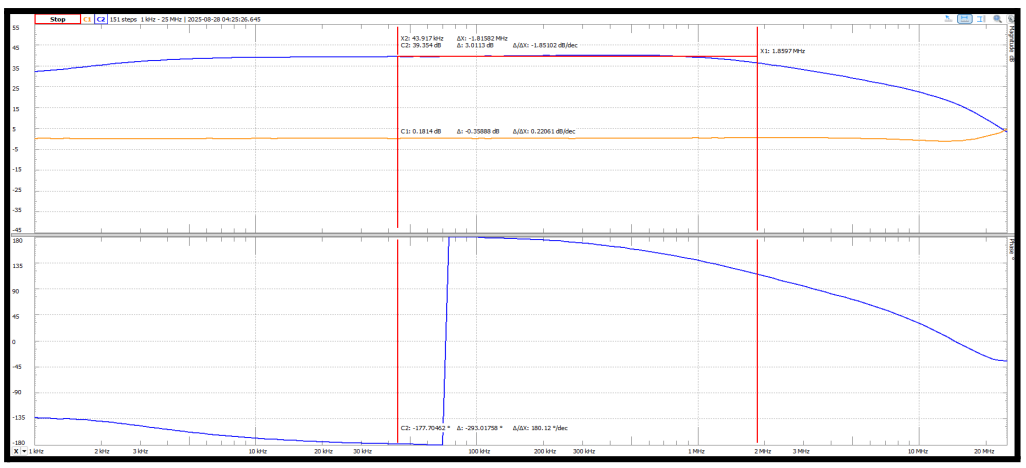
$$V_{out,\,without\,R_L} = 0.9415 \; and \; V_{out,\,with\,R_L} = 0.2649V$$

$$we\ know\ that \; \frac{V_{out,\,with\,R_L}}{V_{out,\,without\,R_L}} = \frac{R_L}{R_O + R_L}$$

$$0.2813 = \frac{300}{R_O + 300}$$

$$\Rightarrow R_O = 766\Omega$$

5. Measuring Frequency Response



Cutoff/-3dB frequency is around 1.8MHz

6. Maximum Voltage Swing