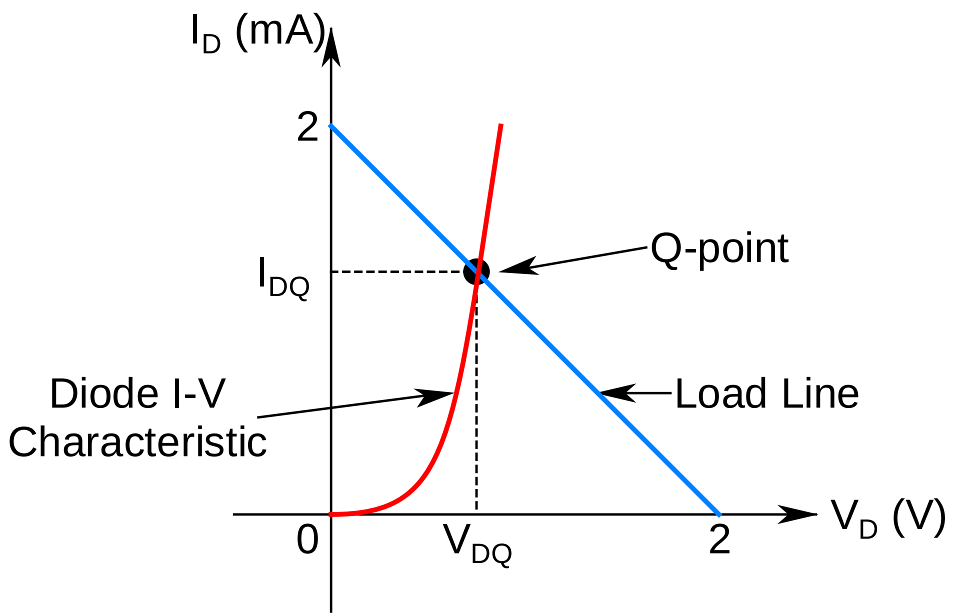
Finding the DC Operating Point

- Known as the ***Q-Point*** (***Quiescent Point***)
- ***Defined by (I_D, V_D)***
- ***Two solution techniques***:
  - ***Graphical Method*** (***Using Load Line***)
  - ***Iterative Method*** (***Self-Consistent***)
- ***Graphical Method***:
  - ***Use diode I-V relation***: $I_D = I_0 \exp(V_D/V_T)$
  - ***Use Load Line equation***: $I_D = (2 - V_D)/(1\ k\Omega)$
  - ***Intersection point is the operating point***



Graphical Method

V_{DQ}, I_{DQ}: Quiescent values of V_D, I_D = 0.7 V, 1.3 mA (obtained from iterative method using I_0 = 3 fA)

DC Quiescent Power Dissipation

$= V_{DQ} \times I_{DQ} = 0.9$ mW

The two ***end points*** of the ***load line***:

$$1.\ V_D = 0\text{: } I_D = 2/(1\text{ k}) = 2\text{ mA}$$

$$2.\ I_D = 0\text{: } V_D = 2\text{ V}$$

- ***Iterative Method***:
  - Also known as ***self-consistent analysis***
  - ***I-V relation*** and ***load line equation*** form a set of ***transcendental equations***
    - ***Analytical solution not possible***
    - Have to resort to ***numerical*** (***iterative***) analysis
  - ***Procedure***:
    - ***Choose*** $V_D = 0.7\ V$ and ***find*** I_D from ***load line equation***
    - ***Use this*** I_D to ***find*** V_D from ***I-V relation*** (***convert to ln form first***)
    - ***Repeat till convergence is achieved*** (pretty quick!)

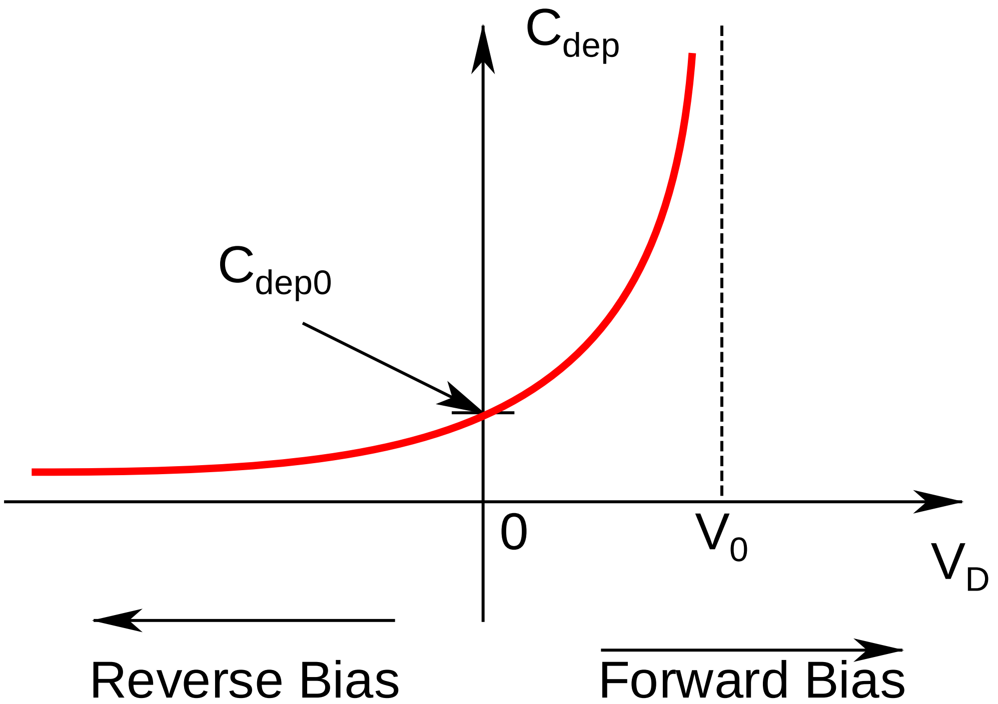
Series Resistance Effect

- The two ***quasi-neutral regions*** (p and n) have their own ***bulk resistances***
- ***Denoted as r_p and r_n***
- ***For small I_D***, their ***effects are negligible***
- However, ***for large I_D***, the ***potential dropped*** across them ***reduces*** the ***actual voltage*** appearing across the ***junction*** of the diode
- Known as the ***Series Resistance Effect***

- The ***actual voltage*** appearing across the ***junction***:
  - $V_{D,eff} = V_D - I_D(r_p + r_n)$
  - V_D: ***Diode terminal voltage***
- The ***new diode I-V relation***:
  - $I_D = I_0 \exp(V_{D,eff}/V_T)$
- ***Simultaneous solution*** of the above ***two equations*** would yield the ***Q-Point***
- ***In presence of*** r_p ***and*** r_n, V_D ***may exceed*** V_0, but $V_{D,eff}$ ***would always be less than*** V_0

Diode Capacitances

- ***Two components***:
  - ***Depletion Capacitance*** C_{dep}
  - ***Diffusion Capacitance*** C_{diff}
- ***Depletion Capacitance***:
  - Due to ***depletion charge dipole*** across the ***junction***
  - ***Expressed by***: $C_{dep} = C_{dep0}/(1 - V_D/V_0)^{1/2}$
    - $C_{dep0} = C_{dep}$ for $V_D = 0$
  - ***Present under both forward and reverse bias***



* **C_{dep} diverges as $V_D \rightarrow V_0$**
* **C_{dep} in reverse bias < C_{dep} in forward bias**
* **Rule of Thumb**: **C_{dep} in forward bias $\approx 2C_{dep0}$**

- ***Diffusion Capacitance***:
  - Due to ***charge injection*** in ***both sides of the junction*** (in the ***quasi-neutral regions***)
  - ***Expressed by***: $C_{diff} = I_D\tau/V_T$
    - τ: ***Injected carrier lifetime***
  - ***Present only in forward bias***, ***negligible in reverse bias***
  - ***Much larger than C_{dep}***
- ***Total Diode Capacitance*** C_D:
  - $C_D = C_{dep} + C_{diff}$

Small-Signal Model

- ***Needed for ac analysis***
- ***Electrical equivalent*** at the ***DC bias point***
- Represented as a ***network***, having various ***circuit components*** (***resistors***, ***capacitors***, ***current sources***, etc.)
- Also known as ***incremental model***
- ***Evaluated at*** (I_{DQ}, V_{DQ})
- Appropriate for ***small variations*** of the ***ac signal*** around the ***Q-point***

Small-Signal Model Parameters

- ***Diode Resistance*** (r_D)/***Diode Conductance*** (g_D):

$$r_D = (g_D)^{-1} = \left(\frac{\partial I_D}{\partial V_D}\right)^{-1}\Bigg|_{I_D = I_{DQ}} = \frac{V_T}{I_{DQ}}$$

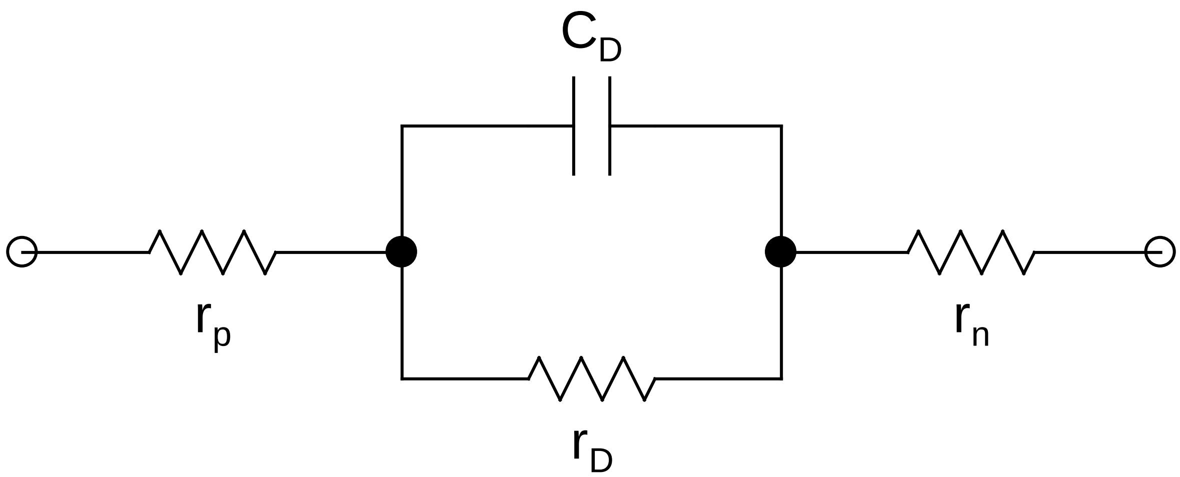
  - For I_{DQ} = 1 mA, r_D = 26 Ω
  - ***Under forward bias***, diode offers ***very small resistance***

- ***Diode Capacitance*** (C_D):
  - $C_D = C_{dep} + C_{diff}$

    $= C_{dep0}/(1 - V_D/V_0)^m + \tau/r_D$
    - m: ***Grading coefficient***

      (1/2 for ***abrupt step junction***, 1/3 for ***linearly graded junction)***
- ***Both r_D and C_D appear in parallel across the junction***
- ***The two quasi-neutral resistance r_p and r_n appear in series with this combination***

Small-Signal Equivalent



- ***In absence of r_p and r_n***, it's just a ***parallel RC circuit***, and ***shorts out*** at ***high frequency***
  - ***Diode time constant*** $\tau_D = r_D C_D = \tau$