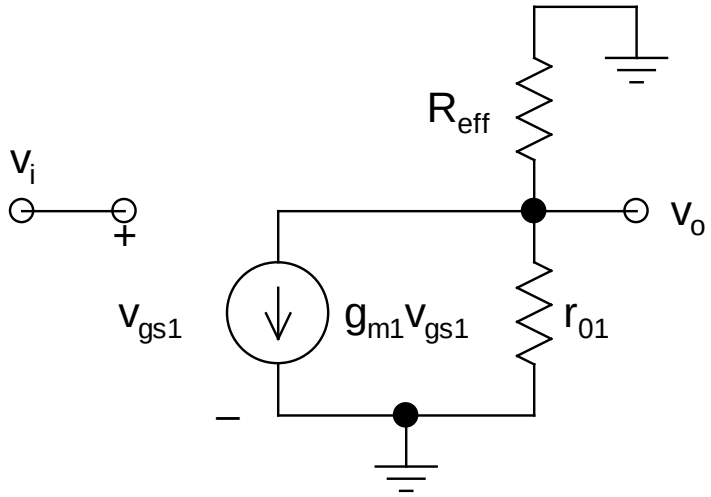
- Thus, the ***complete equivalent***:
- ***By inspection***:

$$A_v = \frac{v_o}{v_i} = -g_{m1}\left(r_{01} \,||\, R_{eff}\right)$$

$$= -\frac{g_{m1}}{g_{mb2} + g_{01} + g_{02}}$$



Complete Equivalent

- Now, in general,

$$g_{mb2} >> (g_{01} + g_{02})$$

$$\Rightarrow A_v \approx -\frac{g_{m1}}{g_{mb2}} = -\frac{g_{m1}}{\chi_2 g_{m2}} = -\frac{1}{\chi_2}\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

$$\chi_2 = \frac{\gamma}{2\sqrt{2\phi_F + V_{DD}/2}} < 1$$

$\Rightarrow$ ***Improvement*** as compared to previous stage

- Now, if M_2 can be put in its ***separate island***, then ***S_2 and B_2 can be connected together***

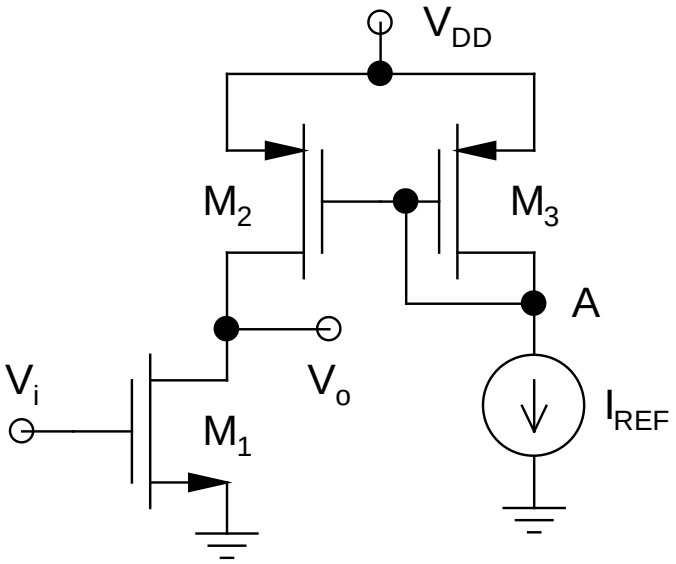
$\Rightarrow$ ***$v_{sb2} = 0$*** $\Rightarrow$ ***$g_{mb2}v_{sb2} = 0$***

$$\Rightarrow A_v = -\frac{g_{m1}}{g_{01} + g_{02}}$$

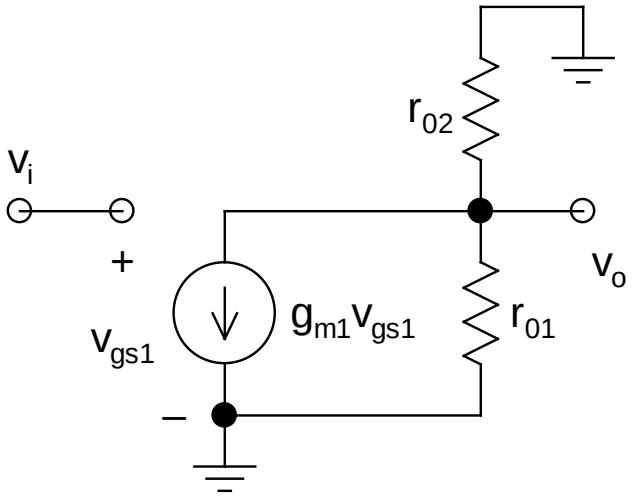
  - Can be ***very large*** (***a magnitude greater than 100 is possible***)

- $R_0 = (g_{mb2} + g_{01} + g_{02})^{-1}$ (***with body effect***)
- $R_0 = (g_{01} + g_{02})^{-1}$ (***without body effect***)
- The latter case produces ***very high R_0***
- Thus, this circuit produces ***much superior performance*** as compared to the ***saturated enhancement load***, in terms of:
  - ***Rail-to-rail swing***
  - ***With island technology***:
    - ***Very large A_v and R_0***
  - ***Without island technogy***:
    - ***Moderate A_v and R_0***

- ***Complementary PMOS Load***:
  - Also known as ***CMOS Gain Stage***
    - ***CMOS*** (***Complementary MOS***: ***Having both NMOS and PMOS*** in the circuit)
  - ***The Ultimate***: ***Much superior performance*** and ***outclasses all other gain stages***
  - ***Widely used***
  - ***High A_v and R_0***
  - ***Easy to bias and easy to operate***
  - ***Design also extremely simple***
  - ***Doesn't produce any anomalies***



Circuit Schematic



ac Midband Equivalent

- ***M_1 body connected to ground, M_2-M_3 bodies connected to V_{DD}***
  - ***No body effect problem for any of the devices (biggest advantage of this circuit)***

- Identify M_2-M_3 as a ***PMOS current mirror*** (***perfectly matched***)

  $\Rightarrow I_{D1} = I_{D2} = I_{D3} = I_{REF}$

- This gives the ***required value*** of V_I

  $\Rightarrow$ ***DC biasing*** of the circuit is ***pretty straightforward***

- For ***ac analysis***, we note that ***node A*** is ***both open and short*** at the same time (similar to ***npn gain stage*** with ***pnp active load***)

  $\Rightarrow A_v = v_o/v_i = -g_{m1}R_0$

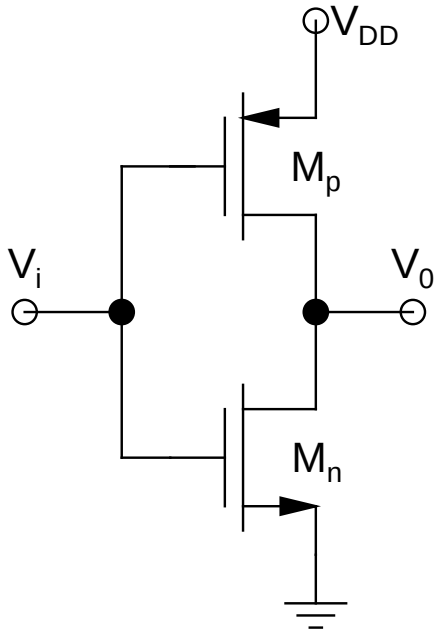
  R_0 ($= r_{01}||r_{02}$): ***Output resistance*** of the circuit

- ***Caution***: $r_{01} \neq r_{02}$, even though M_1 and M_2 carry the same ***DC bias current***, since $\lambda_n \neq \lambda_p$ (in general)
- This circuit is ***immensely useful*** since it gives ***extremely large voltage gain and output resistance***
- Only ***problem*** is that it needs a ***PMOS current mirror***, thus necessitating use of an ***extra PMOS***
- An ***even better design*** exists, which ***eliminates*** the need for this ***extra PMOS***

- ***A Better CMOS Gain Stage***:
  - ***No body effect issue***
  - However, there are ***some design issues***
  - M_1-M_2 have ***same magnitude*** of the ***threshold voltage***:

    $V_{TN0} = |V_{TP0}|$
  - ***Process transconductance parameters***:

    $k'_N = \mu_n C'_{ox}$ and $k'_P = \mu_p C'_{ox}$



Circuit Schematic

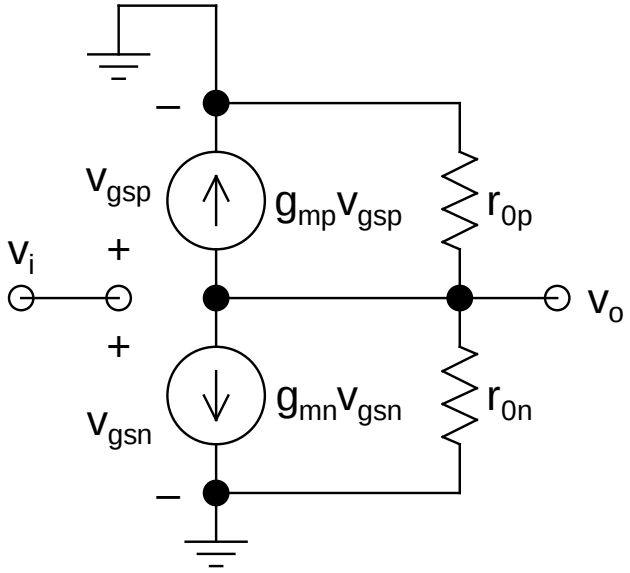
- ***Oxide capacitance per unit area*** $\left(C'_{ox} = \varepsilon_{ox} / t_{ox}\right)$ ***same for both devices***, since they have ***same*** t_{ox}
- However, $\mu_n \sim 2\mu_p$ (***for Si***)
- Thus, $k'_N = 2k'_P$
- ***Ideal DC bias point*** of the circuit is $V_I = V_0 = V_{DD}/2$ (yields $V_{GSn} = |V_{GSp}|$ and $V_{DSn} = |V_{DSp}|$)
- Can be achieved only if the stage is ***completely balanced*** (***same threshold voltage magnitude*** and ***same device transconductance parameter***)
- Thus, k_N ***and*** k_P ***need to be matched***

- ***Can be achieved by making $(W/L)_p = 2(W/L)_n$***
- If ***CLM effect*** is ***not that important***, or if $\lambda_n = \lambda_p$, then this procedure works out ***just fine***
- However, if $\lambda_n \neq \lambda_p$, then for ***balancing the circuit***, the following relation ***must hold*** (***show***!):

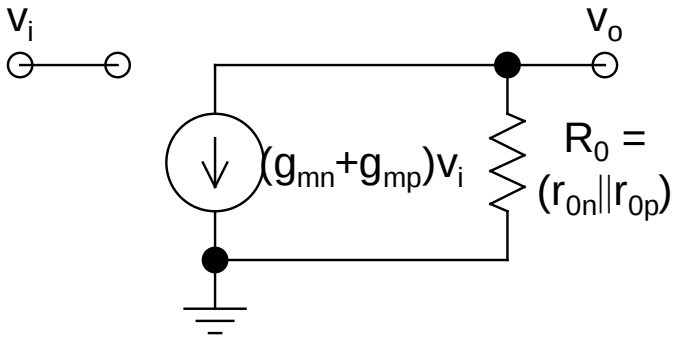
  $$(W/L)_p(1 + \lambda_p V_{DD}/2) = 2(W/L)_n(1 + \lambda_n V_{DD}/2)$$

- Under this condition, $k_N \neq k_P$, but the circuit will be ***perfectly matched and balanced***
- Known as: ***Stage unmatched by nature, but matched by performance***

➢ *ac Analysis*:



ac Midband Equivalent



Simplified Equivalent

- ***By inspection***:

$$A_v = -(g_{mn} + g_{mp})R_0$$

$$= -(g_{mn} + g_{mp})/(g_{0n} + g_{0p})$$

$$R_0 = r_{0n} \| r_{0p} = (g_{0n} + g_{0p})^{-1}$$

- ***Very high A_v and R_0***
- ***Extremely popular*** and ***widely used circuit***
- Sometimes, ***level shifters*** are used at the ***input*** for ***better ease*** of application