EE-380 EC Lab-03
BJT Parameters and Circuits

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Section: C

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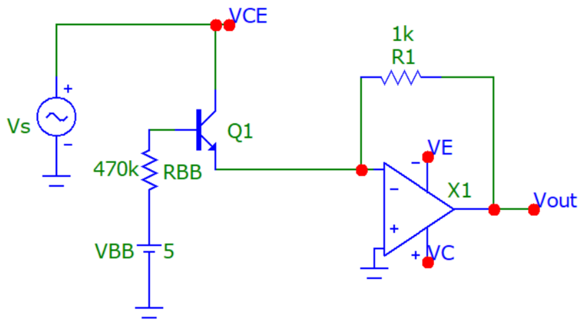
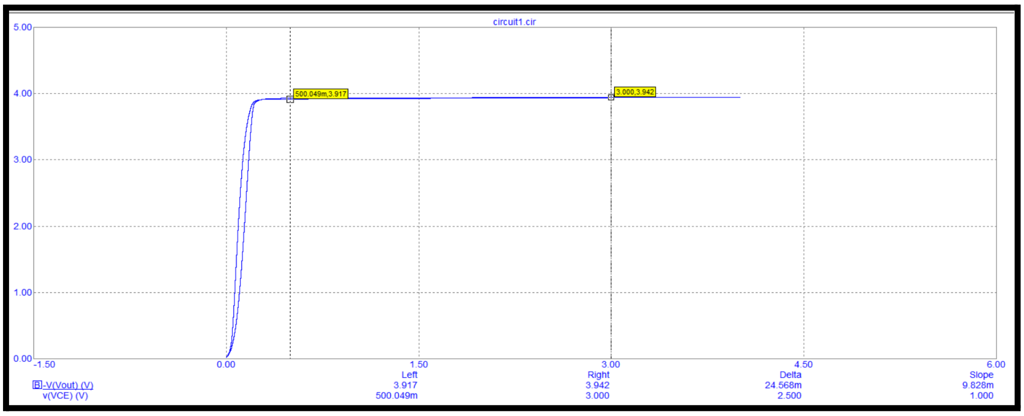
1 Measure IC vs VCE output characteristics and estimate current gain β and Early Voltage V_A



(note: here $V_S = 2 + 2sin(2\pi ft)$ $where$ $f = 1kHz$ and $I_E \simeq I_C = V_{out}/1000$)

1.1 Pre Lab Simulation and Calculations



1000^*I_C vs V_{CE}

$Assumption: V_B \simeq 0.65V \Rightarrow base\ current\ I_B = \frac{V_{BB}-V_B}{R_{BB}} = \frac{5-0.65}{470} mA = 0.0092mA\ or\ 9.2\mu A$

$Observing\ the\ forward\ active\ region\ of\ BJT\ we\ can\ say\ that\ collector\ current\ I_C \simeq 3.9mA$

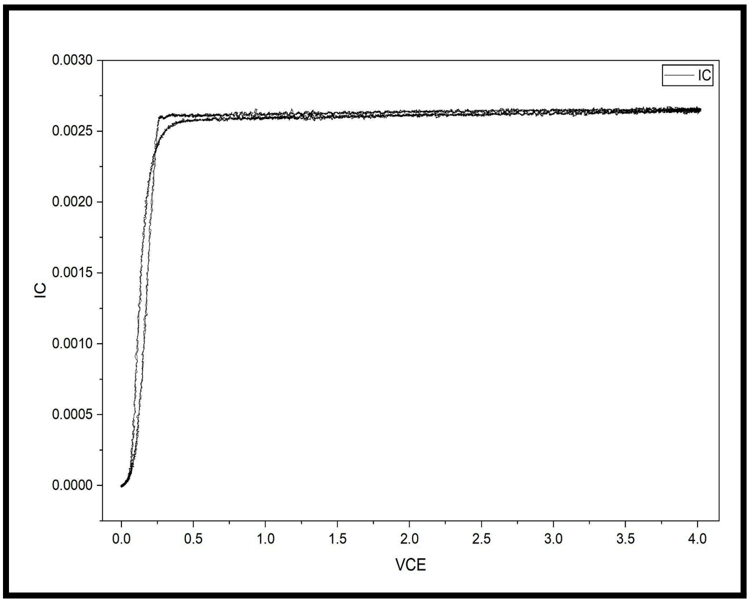
$\beta = \frac{I_C}{I_B} = \frac{3.9}{9.2} * 1000 \Rightarrow \beta = 423.91$

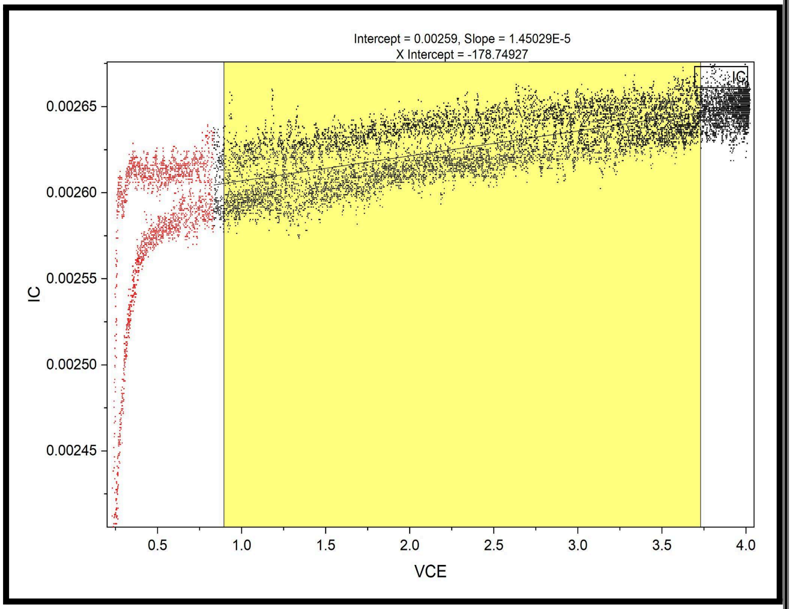
For the estimation of V_A we make use of the formula $I_C = \beta I_B(1 + \frac{V_{CE}}{V_A})$, From the above equation we can observe that the slope of I_C vs V_{CE} is $\frac{\beta I_B}{V_A}$

Calculating slope: $slope\ = \frac{(3.942-3.917)*10^{-3}}{3-0.5} = 0.01\ *\ 10^{-3}\ or\ 10^{-5}$

so , $V_A = \frac{\beta I_B}{slope} = \frac{423.91*9.2*10^{-6}}{10^{-5}} \Rightarrow V_A \simeq 390V$

1.2 In Lab Measurements





1.3 Post Lab Calculations and Conclusions

$Measured\ V_B \simeq 0.66V \Rightarrow base\ current\ I_B = \frac{V_{BB}-V_B}{R_{BB}} = \frac{5-0.66}{470}mA \simeq 0.0092mA\ or\ 9.2\mu A$

$Observing\ the\ forward\ active\ region\ of\ BJT\ we\ can\ say\ that\ collector\ current\ I_C \simeq 2.6mA$

$\beta = \frac{I_C}{I_B} = \frac{2.6}{9.2} * 1000 \Rightarrow \beta = 282.6$

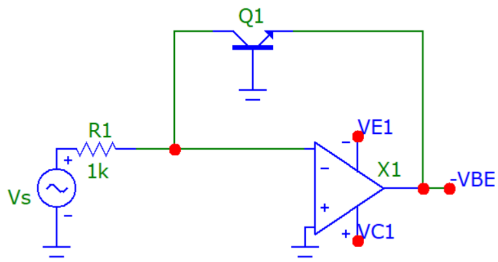
From the plot we can see that the slope of the best fit line is $1.45\ *\ 10^{-5}$

And using the equation we get $I_C = \beta I_B(1 + \frac{V_{CE}}{V_A})$,

$V_A = \frac{\beta I_B}{slope} = \frac{282.6*9.2*10^{-6}}{1.45*10^{-5}} \Rightarrow V_A \simeq 179.3V$

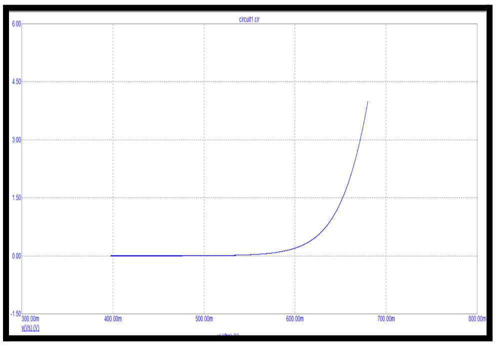
The differences between the simulation and experimental results are mainly due the fact that the transistor parameters in the simulation were different from those given in lab and real-world factors such as component tolerances, parasitic effects in wiring, and limitations of measurement instruments. Additionally, environmental conditions like temperature changes can influence BJT behavior, whereas simulations assume ideal or nominal component values, leading to minor discrepancies.

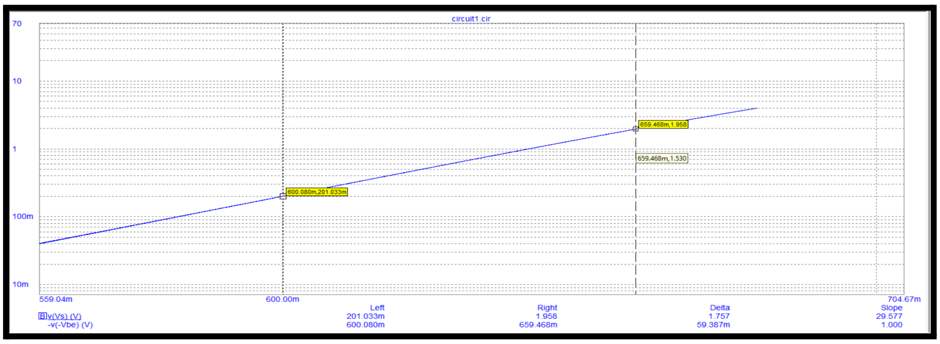
2 Measure transfer characteristics and extract saturation current and ideality factor.



(Note: here $I_C = V_S/1000$ and $V_S = 2 + 2sin(2\pi f t)$ *where* $f = 1kHz$)

2.1 Pre Lab Simulation and Calculations





(Current is in log scale)

we know that $I_C = I_S e^{\frac{V_{BE}}{nV_T}}$

$\Rightarrow ln(I_C) = ln(I_S) + \frac{V_{BE}}{nV_T}$

$\Rightarrow$slope for $ln(I_C)$ vs V_{BE} is $\frac{1}{nV_T}$

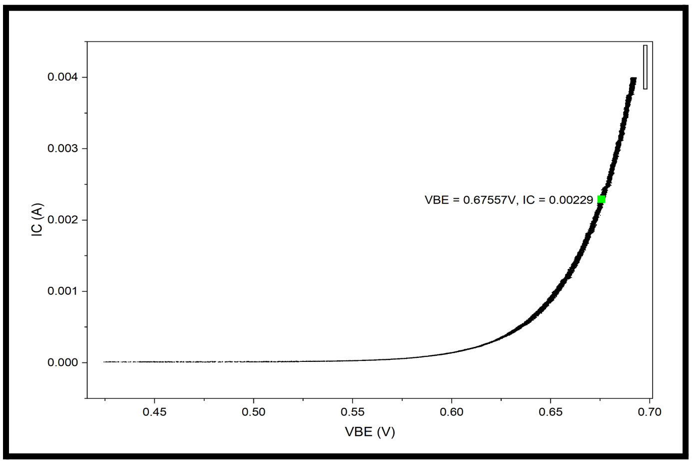
Form the plot, $slope = \frac{ln(1.958) - ln(0.201)}{659.468 - 600.08} mV^{-1} = 0.03833 mV^{-1}$

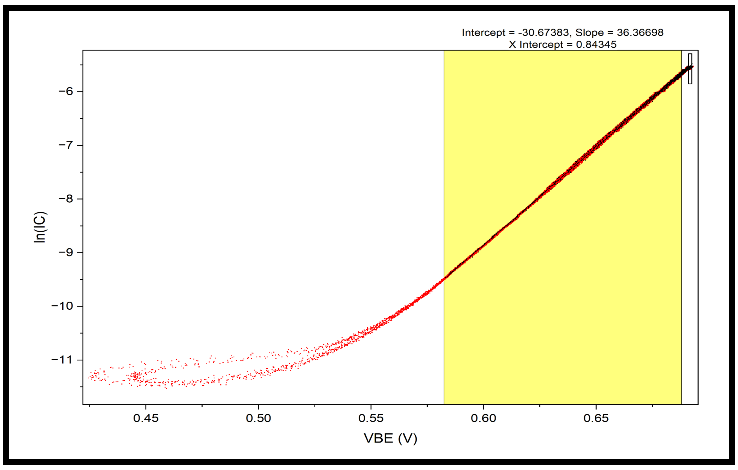
$\Rightarrow n = \frac{1}{slope * V_T}$, *by taking* $V_T = 26mV$ *we get* $n = 1.00$

Now, $I_S = I_C e^{-\frac{V_{BE}}{nV_T}}$, *take* $I_C = 0.001958A,\ V_{BE} = 0.659468,\ n = 1,\ V_T = 0.026V$

$I_S \simeq 18.9 fA$

2.1 In Lab Measurements





2.3 Post Lab Calculations and Conclusions

$I_C = I_S e^{\frac{V_{BE}}{nV_T}}$

$\Rightarrow ln(I_C) = ln(I_S) + \frac{V_{BE}}{nV_T}$

$\Rightarrow$slope for $ln(I_C)$ vs V_{BE} is $\frac{1}{nV_T}$

Form the plot, $slope = 36.37V^{-1}$

$\Rightarrow n = \frac{1}{slope*V_T}$, $by\ taking\ V_T = 0.026V\ we\ get$ $n = 1.02$

Now, $I_S = I_C e^{-\frac{V_{BE}}{nV_T}}$, $take\ I_C = 0.00229,\ V_{BE} = 0.67557,\ n = 1.02,\ V_T = 0.026V$

$I_S \simeq 19.7fA$

We can conclude that the simulated and experimental values are close, the slight differences may arise due to the reasons stated in 1st part.

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3 Design the inverter shown below to achieve approximately symmetrical characteristics. Then, measure the Vout vs Vin voltage transfer characteristics (VTC) and determine the inverter's voltage gain, threshold voltage, and noise margins.

3.1 Pre Lab Designing, Simulation and Calculations

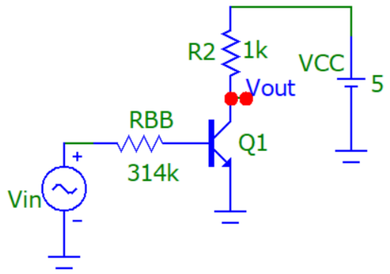
For symmetric characteristics, we should use the best biasing condition i.e $V_{out}=V_{CC}/2 = 2.5V$ and $\beta=423.91$

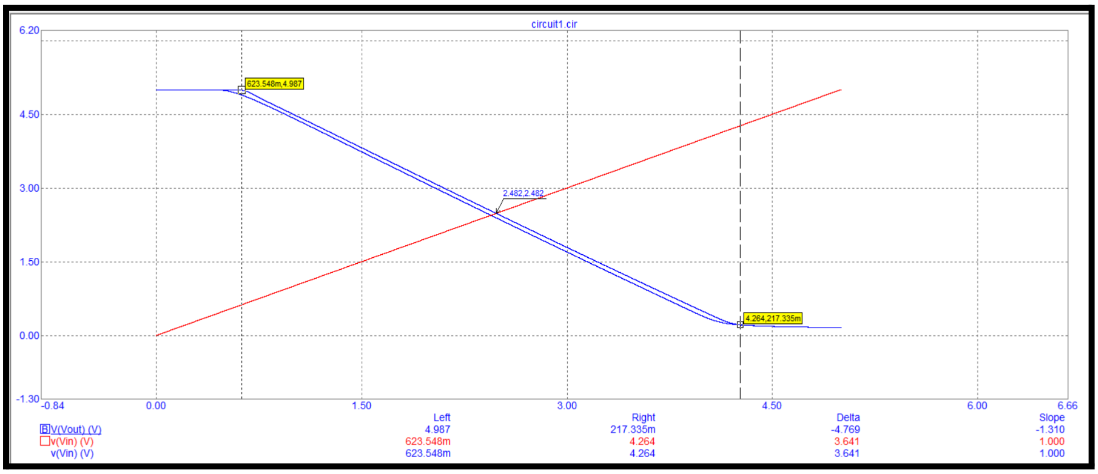
$I_c = \frac{5-2.5}{1000} A = 2.5mA$

$\Rightarrow I_B = \frac{I_c}{\beta} = \frac{2.5*10^{-3}}{423.91} \simeq 5.9\mu A$

$\Rightarrow R_{BB} = \frac{2.5-0.65}{5.9*10^{-6}} \Rightarrow$

$R_{BB} = 313.56k\Omega \sim 314k\Omega$





$(note:\ here\ V_{in} = 2.5 + 2.5sin(2\pi ft)\ where\ f = 1kHz)$

From the plot we can infer the following:

Thresh hold voltage $V_{th} = 2.482V$

Voltage gain (slope at threshold) $A_v = -1.31$

For noise margin:

$V_{OL} = 0.217V,\ V_{OH} = 4.987,\ V_{IL} = 0.624V,\ V_{IH} = 4.264$

$NM_L = V_{IL} - V_{OL} \Rightarrow NM_L = 0.407V$ and $NM_H = V_{OH} - V_{IH} \Rightarrow NM_H = 0.723V$

3.2 In Lab Calculations and Measurements

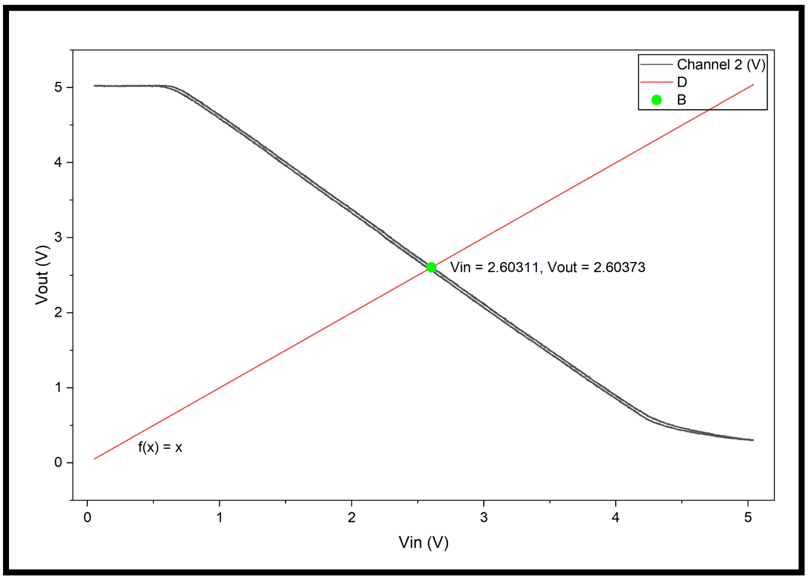
Using the best biasing condition i.e $V_{out}=V_{CC}/2 = 2.5V$ and $\beta=282.6$

$I_c = \frac{5-2.5}{1000} A = 2.5mA$

$\Rightarrow I_B = \frac{I_c}{\beta} = \frac{2.5*10^{-3}}{282.6} \simeq 8.8\mu A$

$\Rightarrow R_{BB} = \frac{2.5-0.66}{8.846*10^{-6}} \Rightarrow$

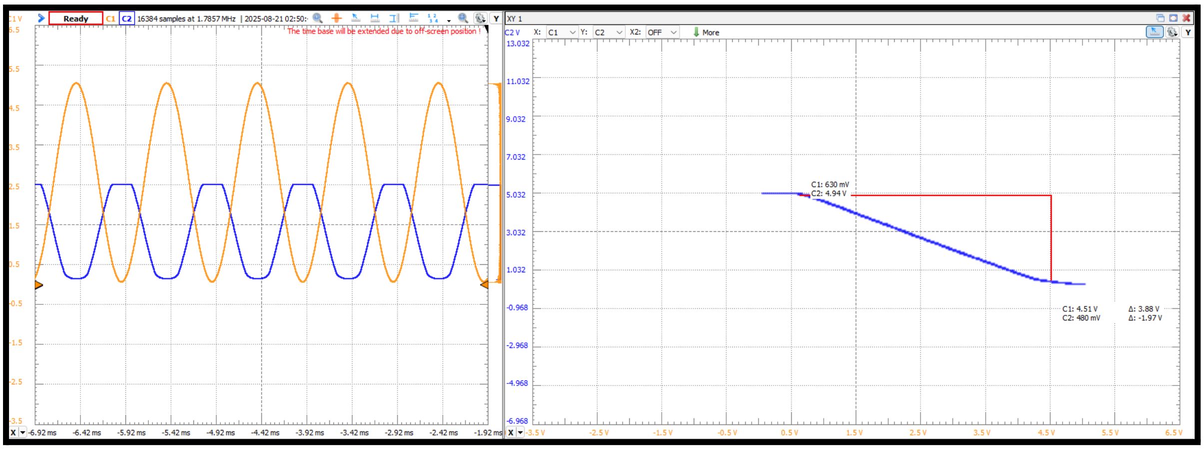
$R_{BB} = 210.2k\Omega$ **a 220kΩ resistor was used in the lab for convenience.*



3.3 Post Lab Calculations and Conclusions

From the plot we can infer the following:

Thresh hold voltage $V_{th} = 2.6V$



Voltage gain (slope at threshold) $A_v = -1.15$

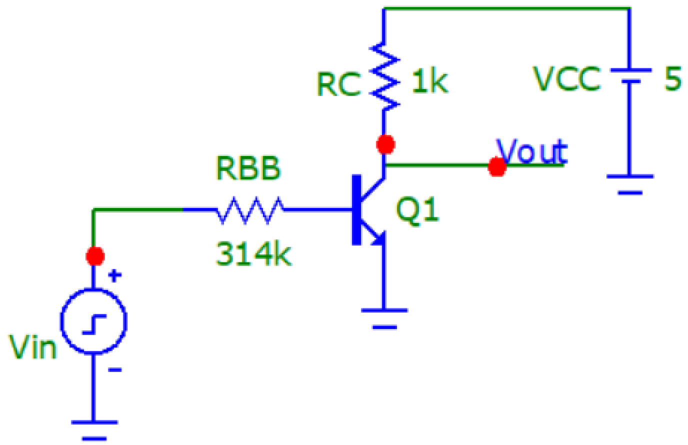
For noise margin:

$V_{OL} = 0.48V,\ V_{OH} = 4.94,\ V_{IL} = 0.630V,\ V_{IH} = 4.51$

$NM_L = V_{IL} - V_{OL} \Rightarrow NM_L = 0.15V$ and $NM_H = V_{OH} - V_{IH} \Rightarrow NM_H = 0.43V$

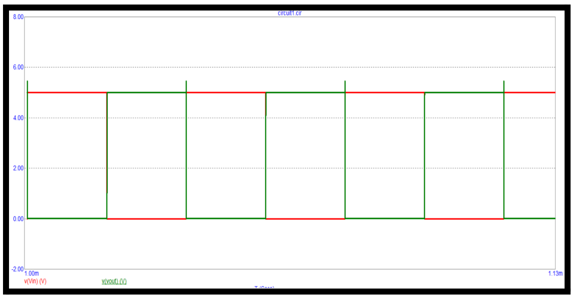
The deviations between the measurements and the simulation results are mainly due to the use of a transistor with different values of β and V_a in the simulation, along with unavoidable environmental influences.

4 Explore the transient response of the inverter for different values of R_{BB}.

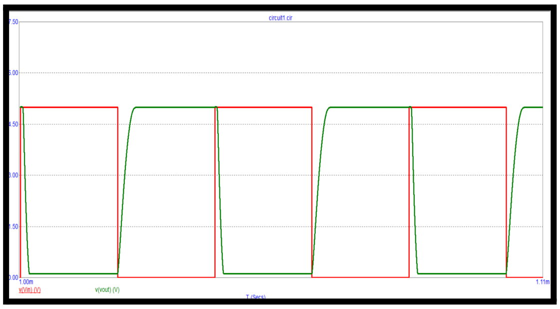


A square wave with a time period of 10µs was applied as input to the inverter

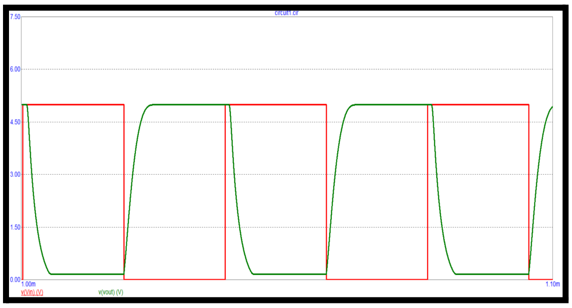
4.1 Pre Lab Simulations



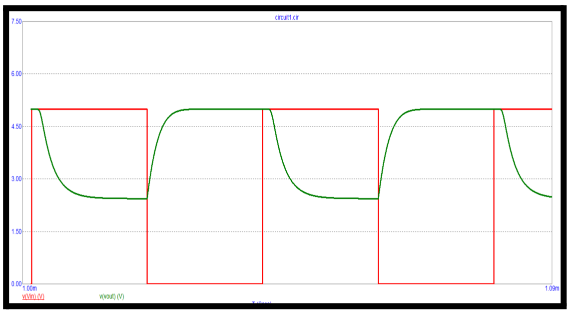
R_{BB}=500Ω



R_{BB}=150kΩ

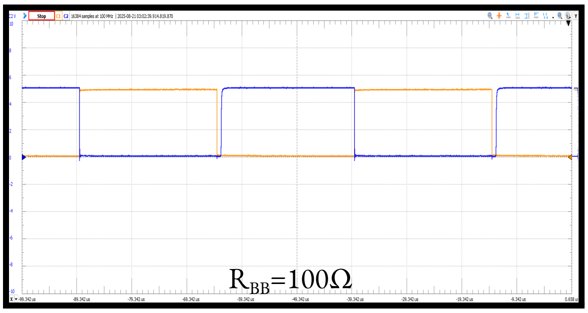


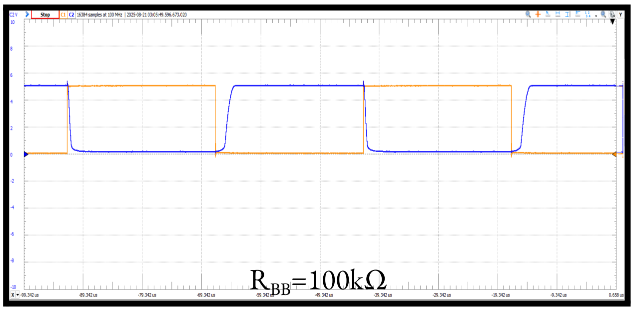
R_{BB}=314kΩ

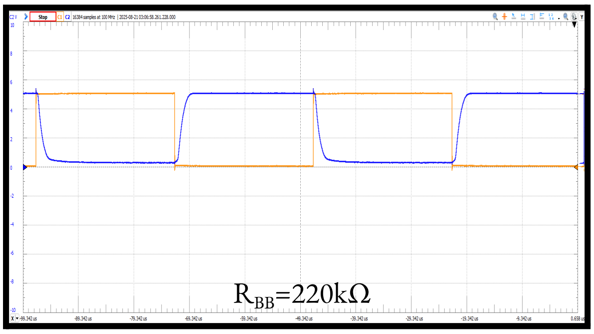


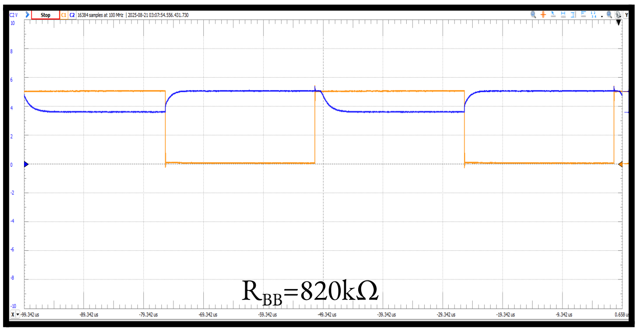
R_{BB}=750kΩ

4.2 In Lab Measurements









4.3 Post Lab Discussion

The variation in waveforms with different R_{BB} values is due to the change in base current and the RC time constant formed with the transistor's input capacitances. A low R_{BB} (e.g., 100Ω or 500 Ω) provides high base current, driving the transistor deep into saturation for sharp switching but with some storage delay on turn-off. As R_{BB} increases to around 200kΩ-300kΩ, the base current decreases, slowing charging and discharging of the base capacitances, which rounds the transitions and prevents full saturation, causing a little higher output low levels. At very high R_{BB} (e.g. more than 700kΩ-800kΩ), the transistor remains mostly in forward-active mode, and the output waveform no longer swings fully between logic levels.

5 For the given CE amplifier circuit, select R_{BB} to achieve a voltage gain of approximately 100. In the lab, measure the bias point, small-signal voltage gain, input resistance, output resistance, and frequency response of the amplifier.

5.1 Pre Lab Designing, Simulation and Calculations

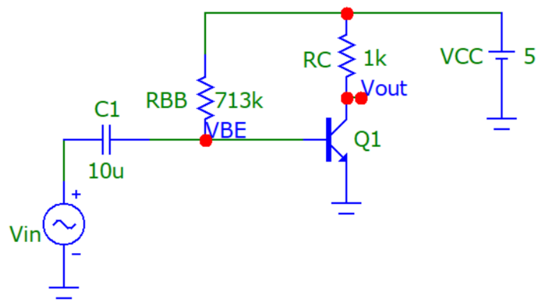
Small Signal analysis:

Since we need small signal voltage gain of 100,

i.e. $g_m R_C$=100, here R_C=1000Ω, so g_m=0.1S

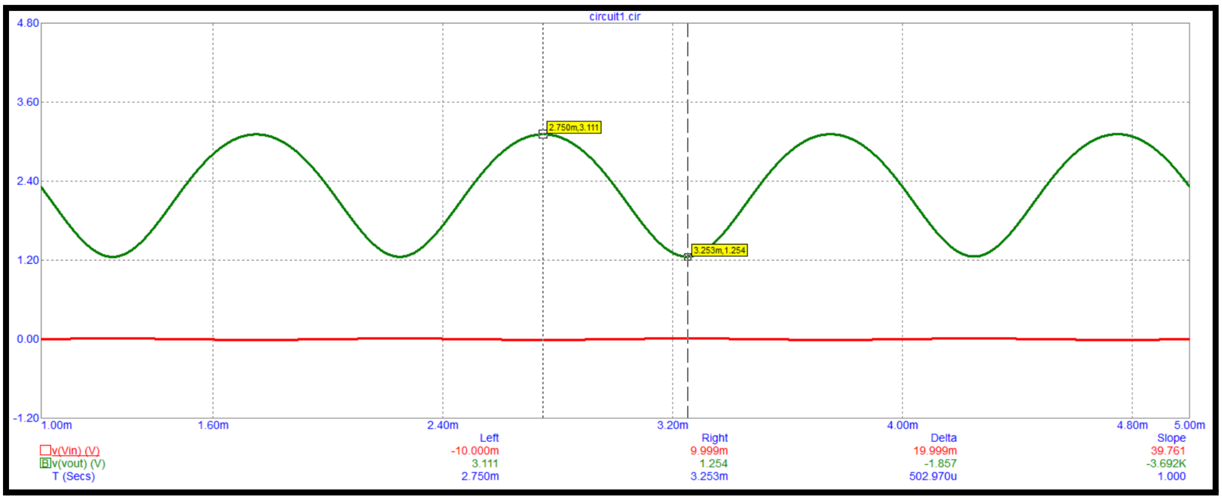
Now, $collector\ current\ I_C = g_m V_T$

$aking\ g_m = 0.1S\ and\ V_T = 0.026V \Rightarrow I_C = 0.0026A$



$Base\ current\ I_B = \frac{I_C}{\beta} = \frac{0.0026}{423.91} = 0.0000061334\ or\ 6.1\mu A$

$Assuming\ V_B \sim 0.65V,\ R_{BB} = \frac{V_{CC}-V_B}{I_B} = \frac{5-0.65}{6.1*10^{-6}} \Rightarrow R_{BB} = 713k\Omega$



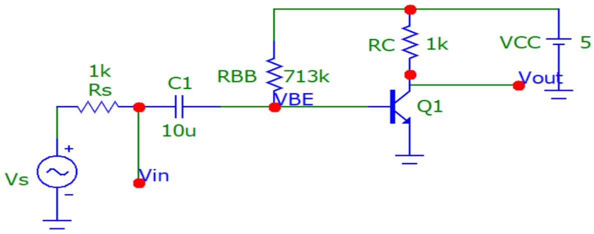
Let amplitude of V_{out} be , A_{out}

So, $A_{out} = \frac{3.111-1.254}{2} = 0.9285V\ or\ 928.5mV\ and\ the\ input\ amplitude,\ A_{in} = 10mV$

So the small signal voltage gain A_v=92.8, close to 100

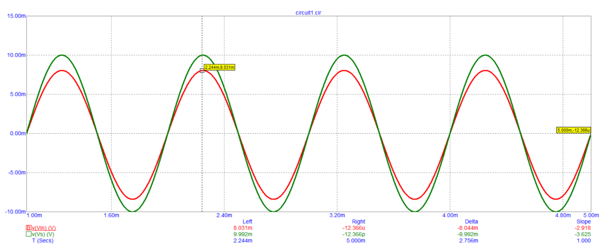
Bias point $V_{BE} = 0.667V\ (measured)$

> Measuring Input resistance:



$$R_{in} = \frac{V_{in}}{V_S - V_{in}} R_s = \frac{8mV}{10mv-8mv}(1k\Omega)$$

$\Rightarrow R_{in} = 4k\Omega$



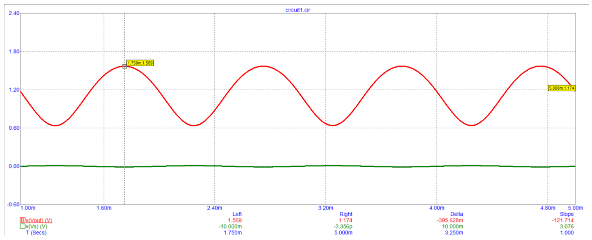
> Measuring Output resistance:

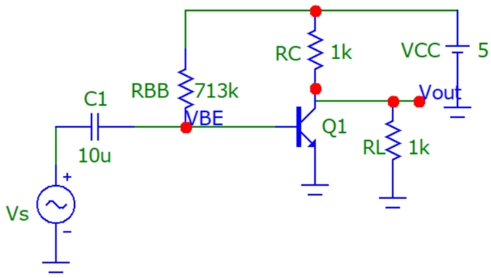
$V_{out,\, without\, R_L} = 3.111V\ and\ V_{out,\, with\, R_L} = 1.569V$

$we\ know\ that\ \frac{V_{out,\, with\, R_L}}{V_{out,\, without\, R_L}} = \frac{R_L}{R_O+R_L}$

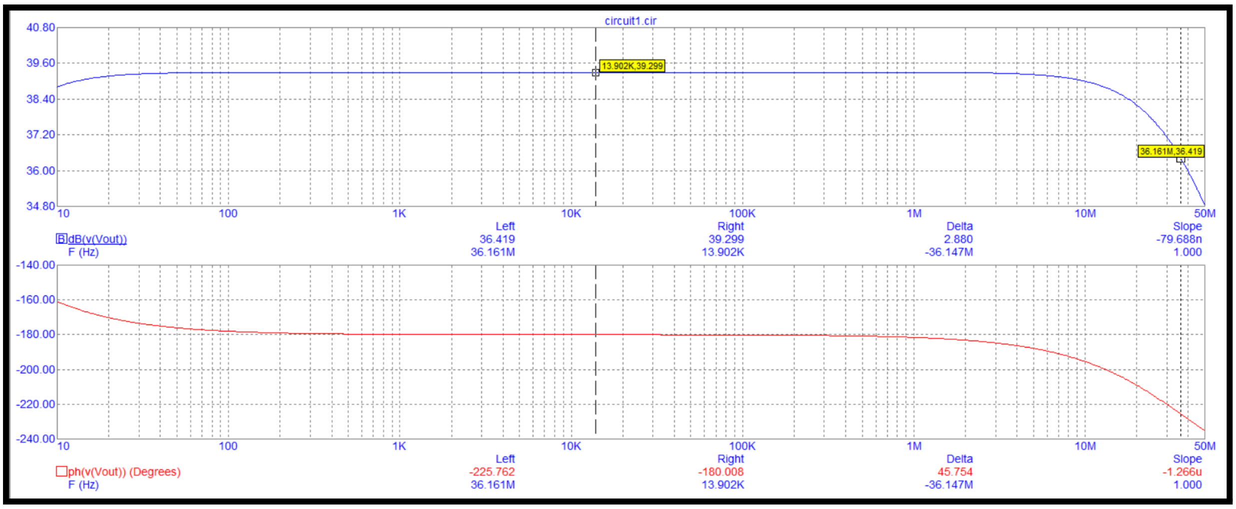
$0.5 = \frac{1000}{R_O+1000}$

$\Rightarrow R_O = 1k\Omega$





> Measuring frequency response of the amplifier:



Cutoff (-3dB frequency) is around 36.1MHz

5.2 In Lab Calculations and Measurements

Small Signal analysis:

voltage gain of 100 implies $g_m R_C$=100, here R_C=1000Ω, so g_m=0.1S

Now, $collector\ current\ I_C = g_m V_T$

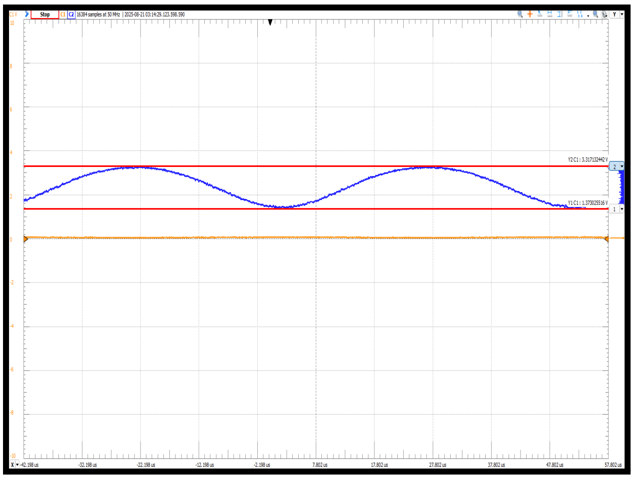
$aking\ g_m = 0.1S\ and\ V_T = 0.026V \Rightarrow I_C = 0.0026A$

$Base\ current\ I_B = \frac{I_C}{\beta} = \frac{0.0026}{282.6} = 0.0000092003\ or\ 9.2\mu A$

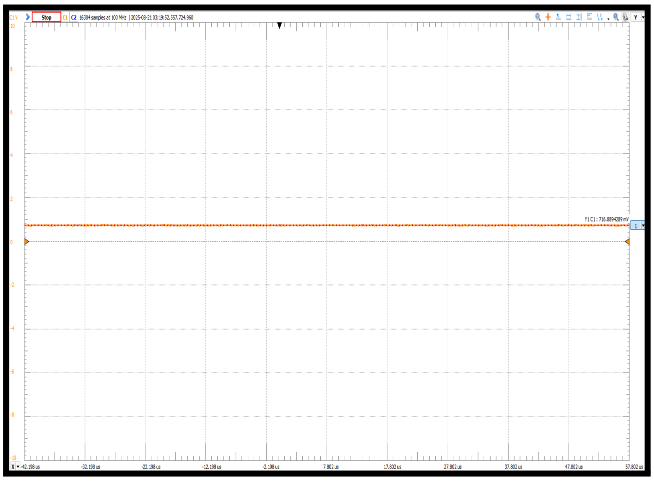
$Assuming\ V_B \sim 0.65V,\ R_{BB} = \frac{V_{CC}-V_B}{I_B} = \frac{5-0.65}{9.2*10^{-6}}$

$\Rightarrow R_{BB} = 472.8k\Omega$

**a 470kΩ resistor was used in the lab for convenience.*



Input and output wave forms



V_{BE}

Let amplitude of V_{out} be , A_{out}

So, $A_{out} = \frac{3.317-1.373}{2} = 0.972V\ or\ 972mV\ and\ the\ input\ amplitude,\ A_{in} = 10mV$

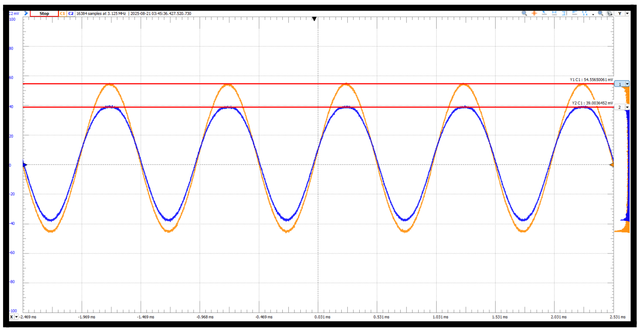
So the small signal voltage gain A_v=97.2, close to 100

Bias point $V_{BE} = 0.717\ (measured)$

1. Measuring Input resistance:

$$R_{in} = \frac{V_{in}}{V_S - V_{in}} R_s = \frac{39.003mV}{54.556mv - 39.003mv}(1k\Omega)$$

$$\Rightarrow R_{in} = 2.508k\Omega \sim 2.5k\Omega$$



2. Measuring Output resistance:

$V_{out,\ without\ R_L} = 3.317V\ (measured)\ and\ V_{out,\ with\ R_L} = 1.689V\ (measured)$

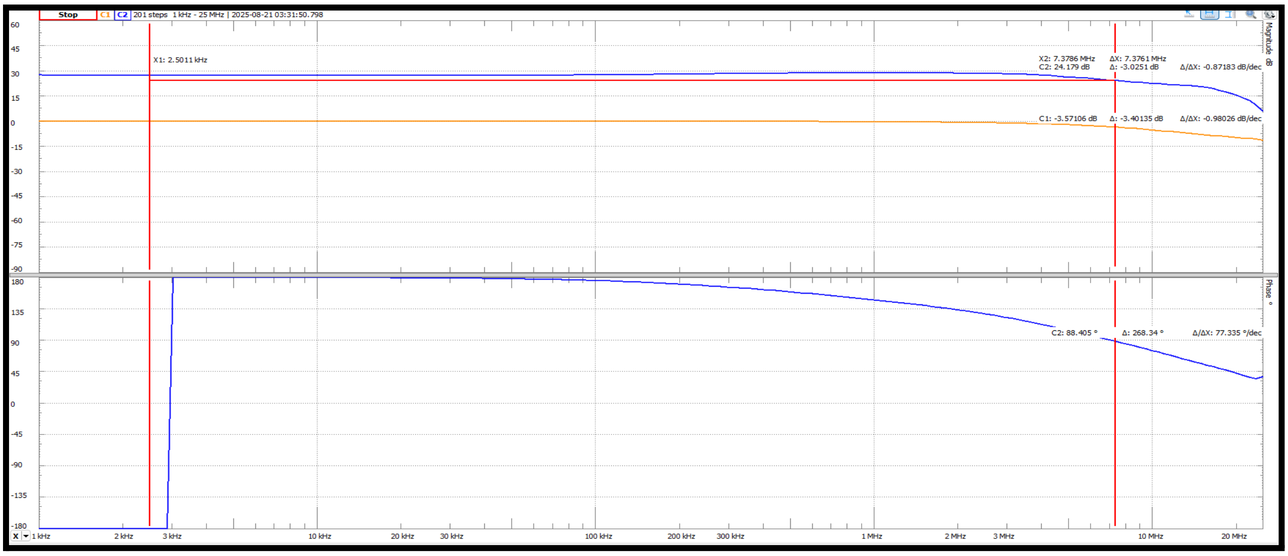
$$we\ know\ that\ \frac{V_{out,\ with\ R_L}}{V_{out,\ without\ R_L}} = \frac{R_L}{R_O + R_L}$$

$$\Rightarrow 0.51 = \frac{1000}{R_O + 1000}$$

$$\Rightarrow R_O = 960.784\Omega$$

3. Measuring frequency response of the amplifier:

Cutoff (-3dB frequency) is
around 7.3MHz



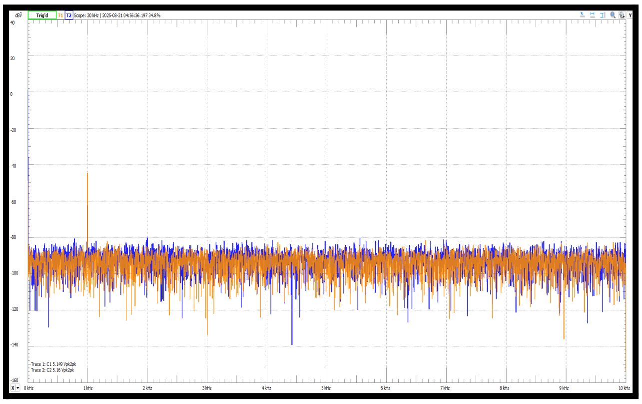
5.3 Post Lab Discussion

The simulation and experimental results show some differences, primarily due to variations in transistor parameters and environmental factors. The intended gain of 100 is nearly achieved, corresponding to a dB gain of ≃ 40 over a wide frequency range. The slight reduction in gain observed can be attributed to the internal emitter resistance of the transistor, which was not included in the calculations. Therefore, if the design target is a gain of 100, it would be advisable to design for a slightly higher gain, around 105–108, to account for these effects.

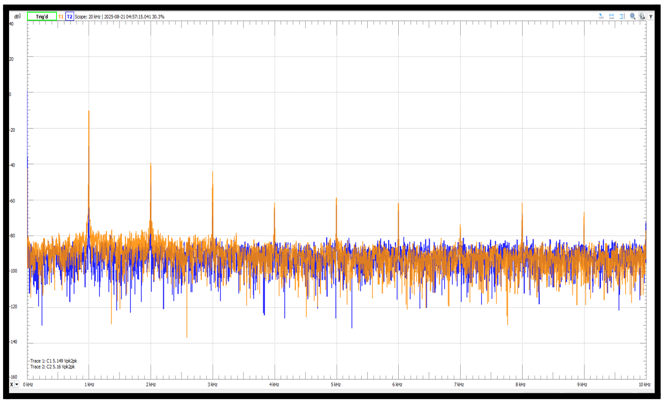
6 (Bonus) : Explore the relationship between output voltage swing and distortion

6.1 In Lab Designing, Simulation and Calculations

Input : 10sin(2π1t) mV , f=1kHz



Input: 500sin(2π1t) mV , f=1kHz



6.2 Post Lab Discussion

From the plots, we observe that as the input sine wave amplitude increases, the amplifier's nonlinearity becomes significant. The circuit no longer acts as a purely linear amplifier and introduces higher-order harmonics of the input frequency in the output spectrum. These distortion components reduce signal fidelity and effectively lower the amplifier's efficiency.

We can show this mathematically as follows:

Since, $I_C = I_S e^{\frac{V_{BE}}{nV_T}}$ and here, $V_{BE} = V_B = V_p sin(\omega t)\ and\ n \simeq 1$, so we get $I_C = I_S e^{\frac{V_p}{V_T} sin(\omega t)}$

Now, consider $e^{xsin(\omega t)} = 1 + \frac{xsin(\omega t)}{1!} + \frac{x^2 sin^2(\omega t)}{2!} + ...$ where $x = \frac{V_P}{V_T}$, thus for small signals (small V_p) we have small x and thus we can neglect the higher order terms in the taylor series expansion. Hence we get a linear relation between the input and I_C, and $V_{out}=5-1000I_C$, so the amplifier amplifies linearly.

Now as V_p increases x becomes significant and can no longer be neglected thus we get higher order terms in our output

$sin^2(\omega t) = \frac{1}{2}(1 - cos(2\omega t))\ and\ sin^3(\omega t) = \frac{3}{4}sin(\omega t) - \frac{1}{4}sin(3\omega t)\ and\ so\ on....$

We can see **harmonics** at 2ω, 3ω, etc., appearing in I_C as V_P/V_T gets larger, explaining why higher input amplitude in FFT shows harmonics.

So,

- Even harmonics (2f) appear due to squared terms
- Odd harmonics (3f, 5f) appear due to cubic and higher terms.