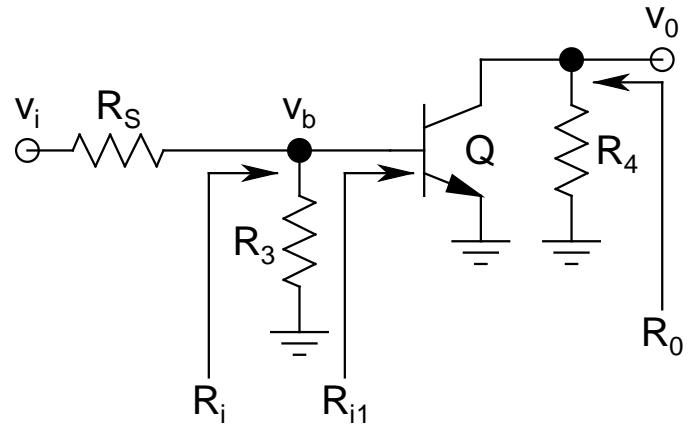


Complete Circuit



ac Schematic

C_B : Base Blocking Capacitor, C_C : Collector Coupling Capacitor

C_E : Emitter Bypass Capacitor, R_S : Source Resistance, R_L : Load Resistance

- C_B, C_C : Used for ***DC isolation*** of the ***bias circuit*** from ***the source and the load***
 - ***DC biasing becomes independent of source and load***
- C_E : ***Plays no role in DC (opens up)***, but ***shorts out R_E in ac*** (will see its effects later)
- These 3 capacitors dictate the ***lower cutoff frequency*** (f_L) of the circuit
- Typically have values in the order of ***μF to 100s of μF*** in order to give ***f_L as close to 0 (DC)*** as possible

➤ First need to do the ***DC analysis*** to find the ***operating point***

➤ ***All capacitors open up for DC analysis***

- ***R_S and R_L play no role***

➤ ***Neglecting base current:***

$$V_B = V_{CC}R_2/(R_1 + R_2) = 1.2 \text{ V}$$

$$\Rightarrow V_E = V_B - V_{BE} = 0.5 \text{ V}$$

$$\Rightarrow I_E \approx I_C = V_E/R_E = 2 \text{ mA}$$

$$V_C = V_{CC} - I_C R_C = 4 \text{ V}$$

$$V_{CE} = 3.5 \text{ V} \quad (\text{quite close to } V_{CC}/3)$$

➤ ***DC bias point analysis done!***

- Now we can move on to the *ac analysis*
- *All capacitors get shorted* due to their *high values*, assuming *frequency of operation* is *beyond f_L* and *less than f_H* , i.e., *midband range*
- *C_E bypasses R_E*
 - ⇒ *Emitter of Q goes to ground*
 - ⇒ *R_E plays no role in ac analysis*
- *Refer to the ac schematic*
 - $R_3 = R_1 \parallel R_2 = 9 \text{ k}\Omega$
 - $R_4 = R_C \parallel R_L = 2 \text{ k}\Omega$
- *Need β for ac analysis (choose 100)*

- $r_E = V_T/I_C = 13 \Omega$, and $r_\pi = \beta r_E = 1.3 \text{ k}\Omega$
- $R_{i1} = r_\pi = 1.3 \text{ k}\Omega$
- $R_i = R_{i1} \| R_3 = 1.14 \text{ k}\Omega$
- Total resistance *seen* by $v_i = R_S + R_i = 2.14 \text{ k}\Omega$
- For calculation of *voltage gain* A_v , apply *chain rule*:

$$A_v = v_0/v_i = (v_0/v_b) \times (v_b/v_i)$$

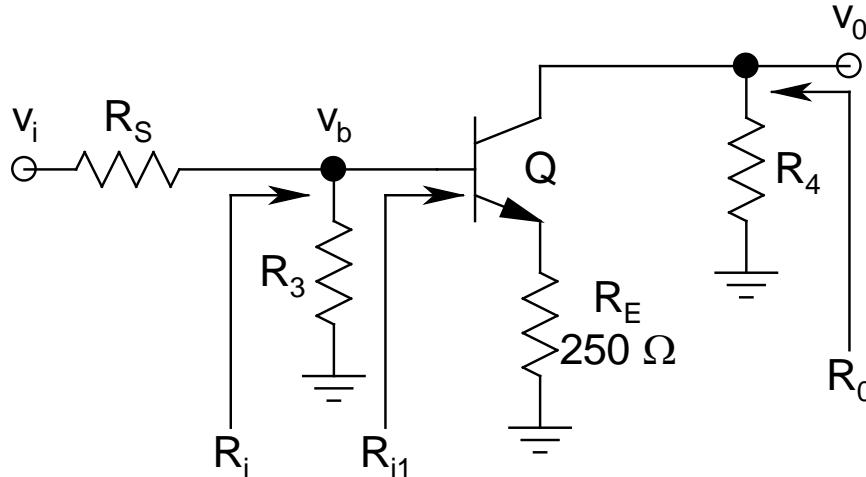
$$v_0/v_b = -R_4/r_E = -153.85 \text{ (*CE stage*)}$$

$$v_b/v_i = R_i/(R_i + R_S) = 0.533$$

$$\Rightarrow A_v = -82 \text{ (*Very Good Gain!*!)}$$

- Note that v_i and v_0 are *exactly out of phase*, which is expected from a *CE stage*
- $R_0 = r_0 \parallel R_4 \approx R_4 = 2 \text{ k}\Omega$
(since for *discrete circuits*, r_0 is generally *neglected*)
- *This completes the analysis of the stage*
- *Summary:*
 - $A_v = -82$
 - $R_i = 1.14 \text{ k}\Omega$
 - Resistance *seen* by $v_i = 2.14 \text{ k}\Omega$
 - $R_0 = 2 \text{ k}\Omega$

- Now let's explore what happens if C_E were absent, i.e., R_E unbypassed
- Redraw the *ac schematic*:

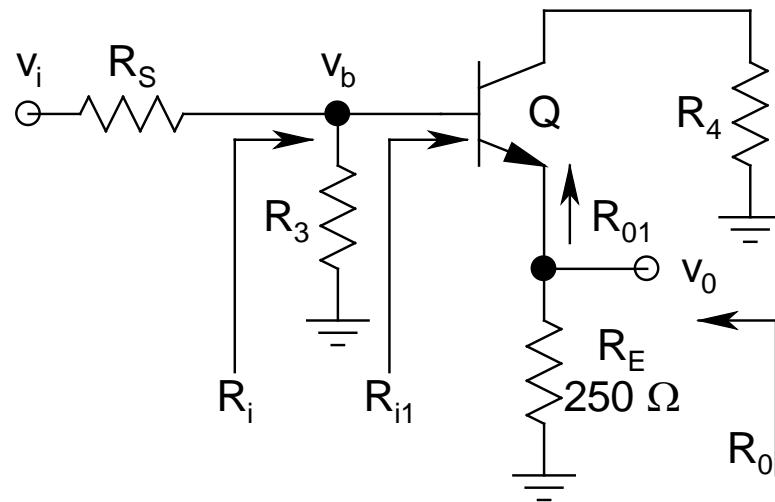


ac Schematic for R_E unbypassed

- **Note:** *Degeneration Factor* = $(1 + g_m R_E) \approx (1 + R_E/r_E) = 20.23$
- $R_{i1} = r_\pi + (\beta + 1)R_E = 26.55 \text{ k}\Omega$
 - *Exactly 20.23 times of the previous case* ($1.3 \text{ k}\Omega$)
- $R_i = R_{i1} \| R_3 = 6.72 \text{ k}\Omega$
- Total resistance *seen* by $v_i = R_S + R_i = 7.72 \text{ k}\Omega$
- $v_o/v_b = -R_4/(r_E + R_E) = -7.6$ [*CE(D) Stage*]
 - *Reduced by exactly 20.23 times of the previous case* (-153.85)
- $v_b/v_i = R_i/(R_i + R_S) = 0.87$
 - *Improvement as compared to previous case* (0.533)

- $A_v = - 6.6$
 - *Compare with -82 obtained in previous case (significant reduction)*
- $R_0 \approx R_4 = 2 \text{ k}\Omega$ (*if r_o is neglected*)
- *If r_o is considered, analysis becomes significantly complicated, since the Golden Rule can't be applied due to the presence of resistance (apart from r_π) in the base of Q*
- *Summary:*
 - $A_v = - 6.6$
 - $R_i = 6.72 \text{ k}\Omega$
 - Resistance *seen* by $v_i = 7.72 \text{ k}\Omega$
 - $R_0 = 2 \text{ k}\Omega$

- *What if the output is taken from emitter?*
- Redraw the *ac schematic*:



**ac Schematic for Output
Taken from Emitter**

- **R_4 actually redundant for this case (collector of Q could have been connected to V_{CC} directly)**
- $R_{i1} = 26.55 \text{ k}\Omega$, $R_i = 6.72 \text{ k}\Omega$, and resistance **seen** by $v_i = 7.72 \text{ k}\Omega$ (**same as before**)
- $v_o/v_b = R_E/(r_E + R_E) = 0.95$ (**CC Stage**)
- $v_b/v_i = R_i/(R_i + R_S) = 0.87$ (**same as before**)
- $A_v = 0.827 (<1$, as expected, but **could have been made closer to unity by better design!**)
- $R_0 = R_E \parallel R_{01}$
- **Computation of R_{01} is slightly more involved, but quite easy if the trick is understood!**

- First, short v_i to ground
 - ⇒ R_3 comes in parallel with R_S (call this combination R_5)
 - ⇒ $R_5 = R_3 \parallel R_S = 900 \Omega$
- R_5 comes in series with r_π (call this combination R_6)
 - ⇒ $R_6 = R_5 + r_\pi = 2.2 \text{ k}\Omega$
- Transform R_6 to emitter by dividing it by $(\beta + 1)$
 - ⇒ $R_{01} = R_6 / (\beta + 1) = 21.8 \Omega$

- Thus, $R_0 = 20 \Omega$ (*Easy?*)
- ***Summary:***
 - $A_v = 0.827$
 - $R_i = 6.72 \text{ k}\Omega$
 - Resistance *seen* by $v_i = 7.72 \text{ k}\Omega$
 - $R_o = 20 \Omega$
- Thus, this circuit has *voltage gain close to unity*, *ok input resistance*, and *very small output resistance*
 - *Ideal characteristics* needed for a *Buffer/Isolator/Impedance Matcher*

- *Loading Effect:*

➤ *Neglecting r_o :*

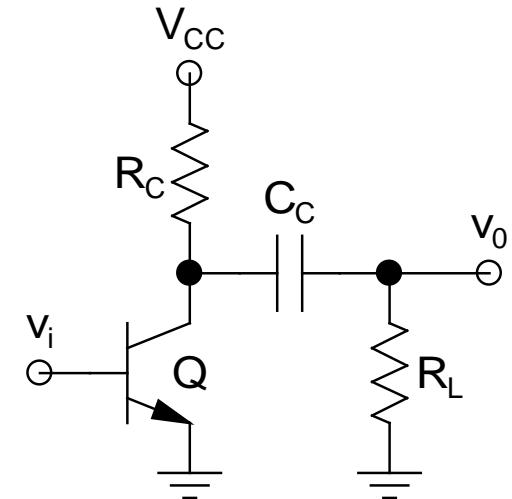
$$A_v = - g_m (R_C \parallel R_L)$$

➤ *R_L has no role in DC biasing, but comes into picture in ac calculations*

➤ As $R_L \downarrow \Rightarrow |A_v| \downarrow$

- Known as *Loading Effect*

➤ Similar situation happens when a *high output resistance driver* drives a *low input resistance load* (e.g., *CE stage driving a CB stage*)



- The *gain of the CE stage* will be *severely compromised* due to *low input resistance* of the *CB stage*
 - Known as *Impedance Mismatch* between *Driver and Load*
- Under such a situation, need an *Isolator/Buffer/Impedance Matcher* between the two stages
- A *CC stage perfectly fits the bill* due to its *high input resistance* and *low output resistance*, and *can be used to couple the CE stage to CB stage*
- *MOS circuits generally don't have this problem*