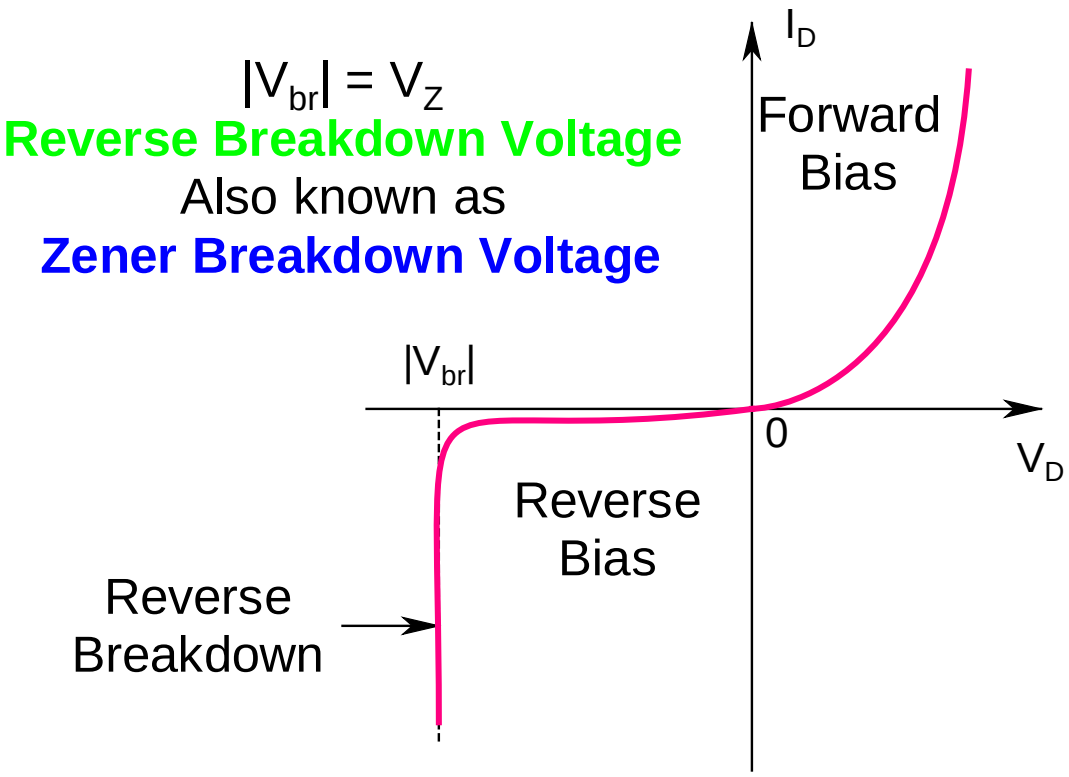
Complete I-V Characteristic



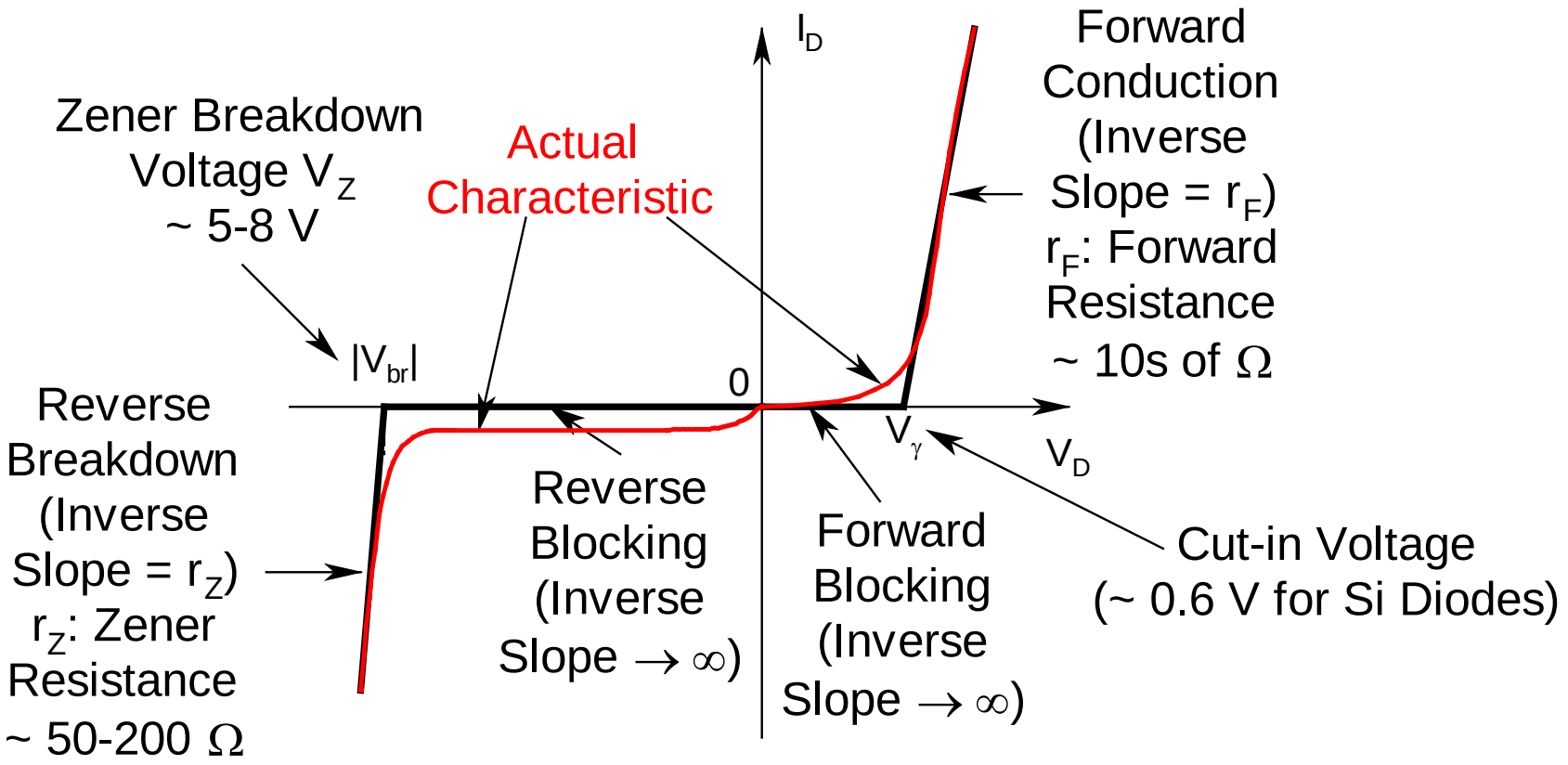
Note that the forward and reverse current scales are not same

Reverse Breakdown

- ***2 Mechanisms***:
  - ***Zener***
  - ***Avalanche***
- ***Zener***:
  - ***For junctions with both sides very heavily doped***
  - ***Thin depletion region***, through which carriers ***tunnel through*** (***quantum mechanical process***)
  - ***Typical $|V_{br}| < 3$ V***

- ***Avalanche***:
  - ***Classical breakdown process***
  - ***At least one side must be lightly doped***
  - ***Carrier multiplication*** due to ***impact ionization***
  - ***Typical $|V_{br}| > 5$ V***
- For diodes having $|V_{br}|$ ***in between 3 V and 5 V***, ***a combination of these two processes***
- ***Breakdowns*** are generally ***destructive***, unless the ***current*** is ***controlled*** by ***external means***, e.g., by a ***resistor***

Piece-Wise Linear (PWL) Model



Note: The forward and reverse current scales are not same

PWL Regions

- $0 \leq V_D \leq V_\gamma$: ***Forward Blocking***
  - V_γ: ***Cut-in Voltage*** (~ ***0.6 V for Si diodes***)
  - $I_D = 0$
- $V_D \geq V_\gamma$: ***Forward Conduction***
  - I_D ***increases linearly with*** V_D with an ***inverse slope of*** r_F
  - r_F: ***Diode Forward Resistance*** (~ 10s of Ω)

    $= [dI_D/dV_D]^{-1}$

- Diodes under ***forward bias*** and for $V_D \geq V_\gamma$, offer ***small resistance*** (results from the ***exponential*** I-V characteristic)
- V_D negative and $0 \leq |V_D| \leq |V_{br}|$: ***Reverse Blocking***
  - $I_D = 0$
- V_D negative and $|V_D| \geq |V_{br}|$: ***Reverse Breakdown***
  - $|I_D|$ ***increases linearly with*** $|V_D|$ with an ***inverse slope of*** r_Z

- r_Z: ***Zener Resistance*** (~ 50-200 Ω)

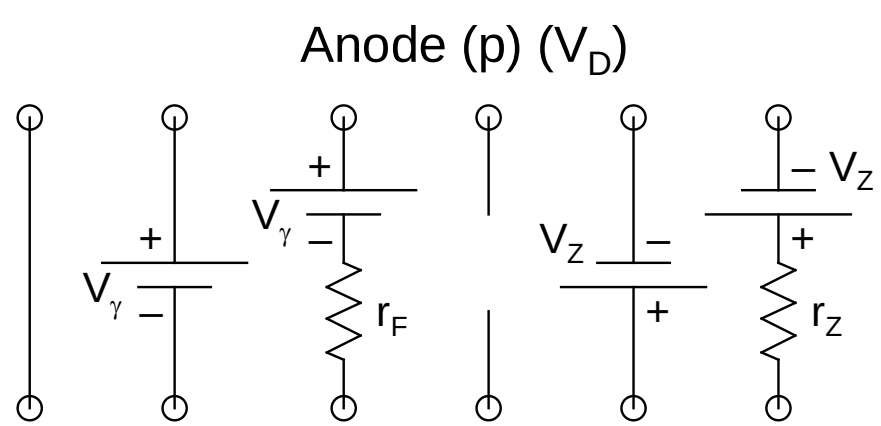
  $= [d|I_D|/d|V_D|]^{-1}$

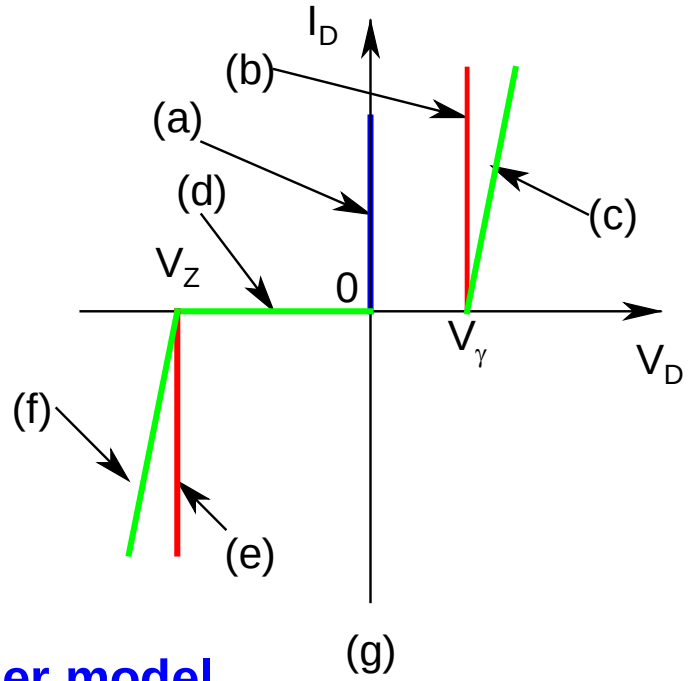
- Diodes under ***reverse bias*** and for $|V_D| \geq |V_{br}|$, offer ***small resistance***

  $\Rightarrow$ ***If current is not controlled by external means, then it may damage the device completely***

- Generally, diodes, unless they are to be operated in ***breakdown mode***, e.g., in a ***voltage regulator***, have ***very high*** $|V_{br}|$, typically of the order of ***100s of V or more***

PWL Circuit Models

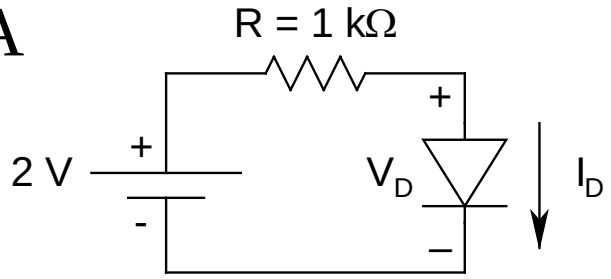




Forward Bias : **V_D positive**: (a) **0th order model**, (b) **1st order model**, (c) **2nd order model**,
Reverse Bias : **V_D negative**: (d) **0th order model**,
Breakdown : (e) **1st order model**, (f) **2nd order model**
(g) **Corresponding piecewise linear models**

0th-Order Model:
Ideal Diode

- Ex.: Find I_D and V_D, using: i) 0^{th} order, ii) 1^{st} order, and 2^{nd} order diode models. [V_γ = 0.6 V, $r_F = 50\ \Omega$]



i) ***0th order model***: $I_D = 2/(1\ \text{k}\Omega) = 2\ \text{mA}$

$V_D = 0\ \text{V}$

ii) ***1st order model***:

$I_D = (2-0.6)/(1\ \text{k}\Omega) = 1.4\ \text{mA}$ and $V_D = 0.6\ \text{V}$

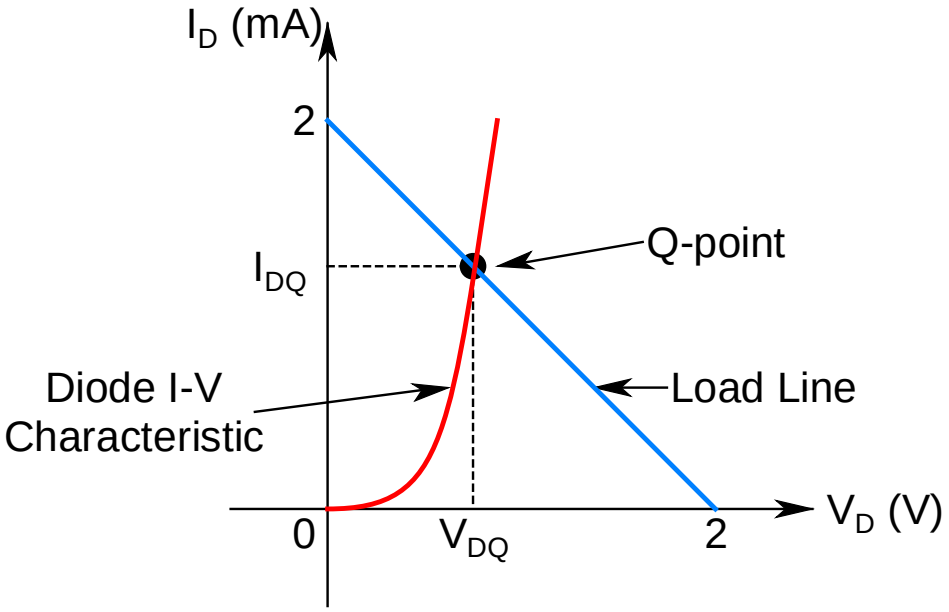
iii) ***2nd order model***:

$I_D = (2-0.6)/(1\ \text{k}\Omega + 50\ \Omega) = 1.33\ \text{mA}$

$V_D = V_\gamma + I_D r_F = 0.667\ \text{V}$

Finding the DC Operating Point

- Known as the ***Q-Point*** (***Quiescent Point***)
- ***Defined by (I_D, V_D)***
- ***Two solution techniques***:
  - ***Graphical Method*** (***Using Load Line***)
  - ***Iterative Method*** (***Self-Consistent***)
- ***Graphical Method***:
  - ***Use diode I-V relation***: $I_D = I_0 \exp(V_D/V_T)$
  - ***Use Load Line equation***: $I_D = (2 - V_D)/(1\ k\Omega)$
  - ***Intersection point is the operating point***



Graphical Method

V_{DQ}, I_{DQ}: Quiescent values of V_D, I_D = 0.7 V, 1.3 mA (obtained from iterative method using I_0 = 3 fA)

DC Quiescent Power Dissipation

= $V_{DQ} \times I_{DQ}$ = 0.9 mW

The two ***end points*** of the ***load line***:

1. $V_D = 0$: $I_D = 2/(1\text{ k}) = 2$ mA

2. $I_D = 0$: $V_D = 2$ V