- ***Actual measurement of f_T difficult* - *measured indirectly***
- ***Measurement done at $f_x >> f_\beta$*, where β *has dropped to about 5-10***
- Then, $f_T = \beta(f_x)f_x$
- Using $\alpha = \beta/(\beta + 1)$:

$$\alpha(j\omega) = \frac{\beta(j\omega)}{1+\beta(j\omega)} = \frac{\alpha_0}{1+ j\omega/\omega_\alpha}$$

α_0 [$= \beta_0/(\beta_0 + 1)$]: ***Low-frequency short-circuit common-base current gain***

$\omega_\alpha = (\beta_0 + 1)\omega_\beta$

- f_α [$= \omega_\alpha/(2\pi)$]: ***Alpha Cutoff Frequency***
- At $f = f_\alpha$, $\alpha = \alpha_0/\sqrt{2}$

- **Note**: ***f_α and f_T extremely close to each other***, with ***f_α marginally higher than f_T***, with ***both being much larger than f_β***
- ***Maximum Operable frequency***:

$$f_{max} = \frac{1}{2\pi\tau_F}$$

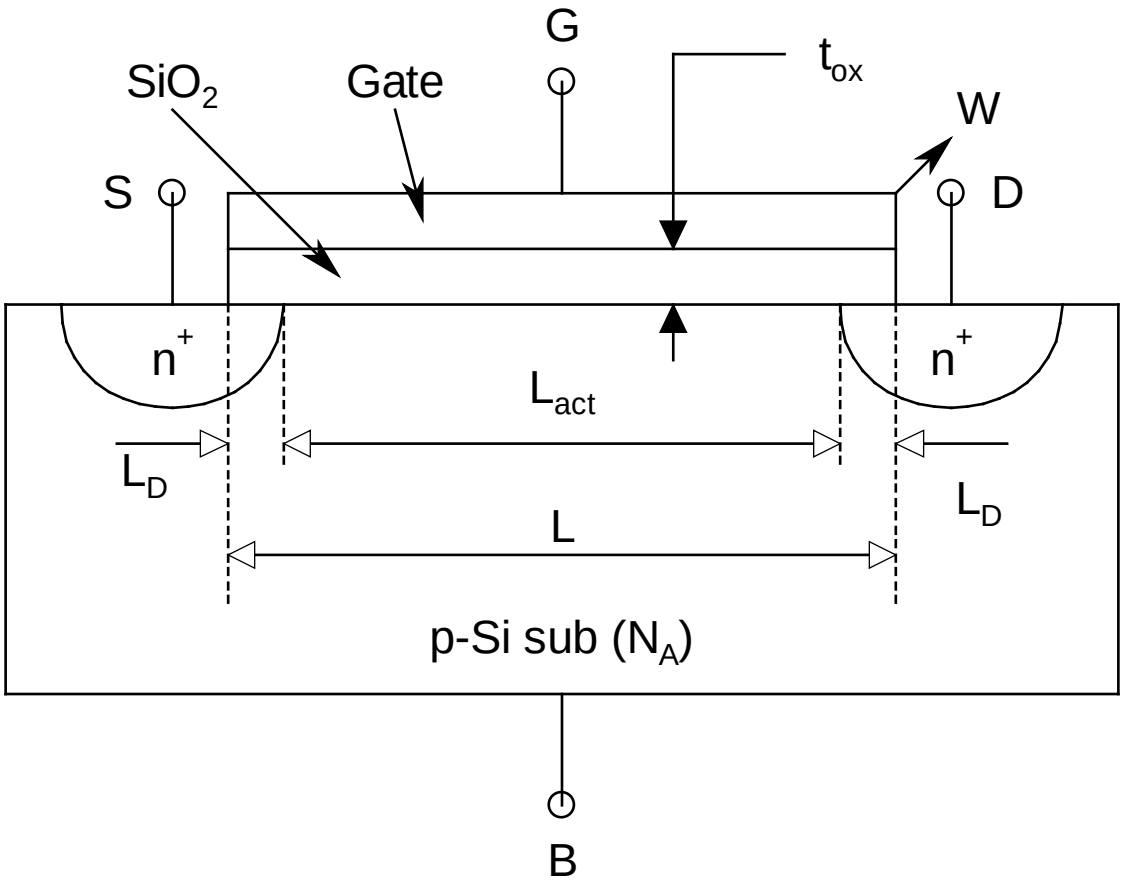
➢ Known as the ***Transit Time Model***

METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR (MOSFET)

- ***Extremely popular device*** - has almost pushed BJTs out of the market
- ***Three-Layer Device*** (***Metal***, ***Dielectric***, and ***Semiconductor***)
- ***Four-Terminal Device*** [***Drain*** (D), ***Source*** (S), ***Gate*** (G), and ***Body/Substrate*** (B)]
- ***Current*** through two terminals (D and S) can be ***controlled*** by the ***voltages*** applied at G and B
  - ***Voltage Controlled Device***

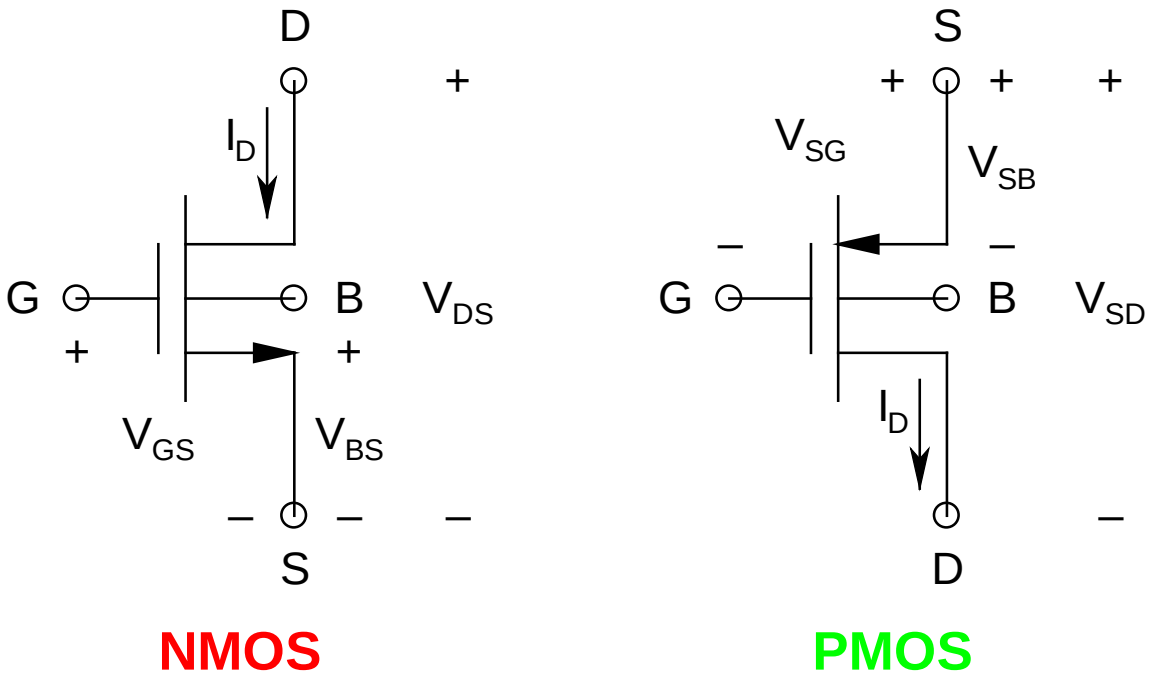
- ***Unipolar device***
  - Either ***electrons*** or ***holes*** participate in ***current conduction***
- ***Active device***
  - Capable of producing ***voltage/current/power gain***
- ***Two basic usage***:
  - **Amplification** (***Analog Circuits***)
  - **Switching** (***Digital Circuits***)
- ***Two Types*: *NMOS*** and ***PMOS***

NMOS Structure



- ***Technology Parameters***:
  - ***Channel Length*** (L)
  - ***Channel Width*** (W)
  - ***Oxide Thickness*** (t_{ox})
  - ***Substrate Doping*** (N_A)
- L_D: ***Lateral overlap*** between G and S/D
- ***Actual*** channel length: $L_{act} = L - 2L_D$
- For now, we will assume $L_D = 0$
  - $L_{act} = L$

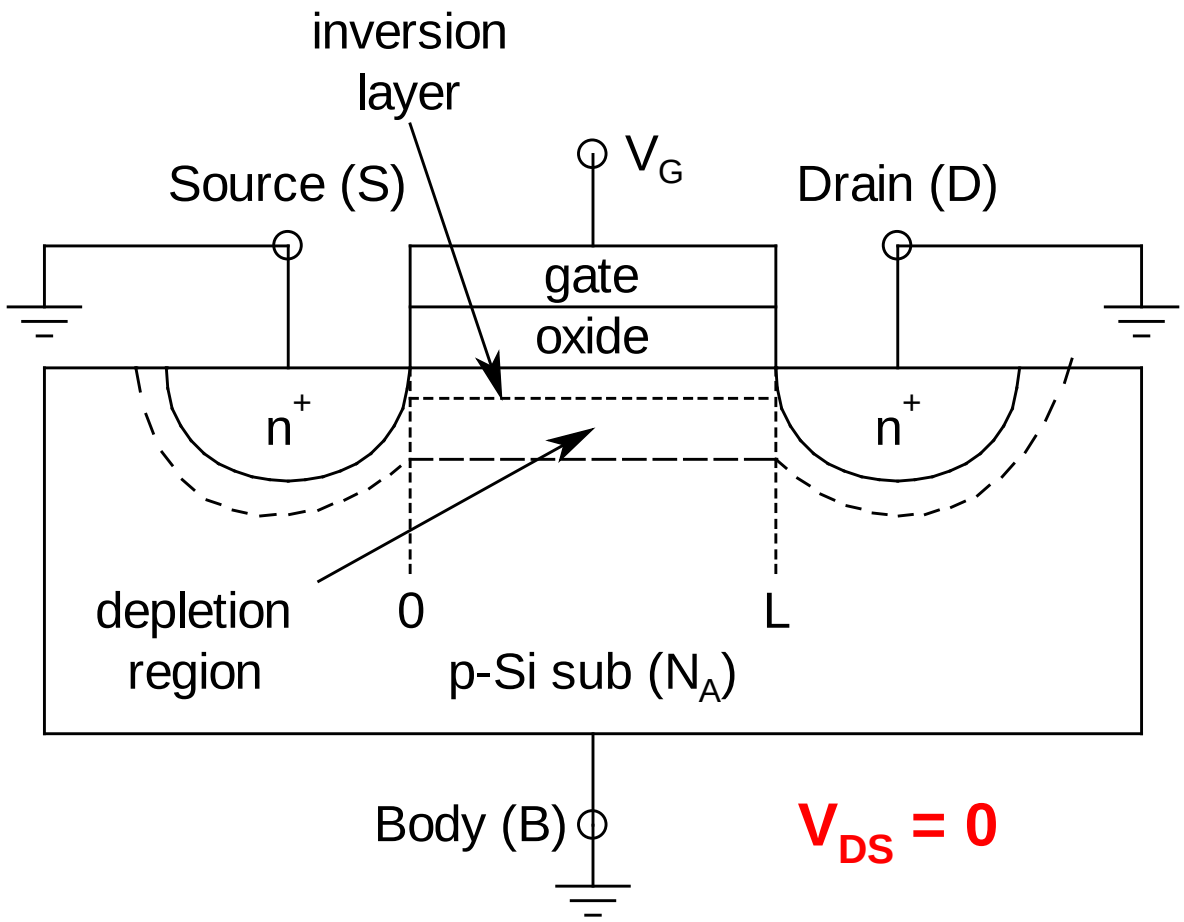
Symbols and Current-Voltage Conventions



- ***Voltage Convention***:
  - ***NMOS***: V_{GS} (***gate-source voltage***), V_{DS} (***drain-source voltage***), V_{BS} (***body-source voltage***)
  - ***PMOS***: V_{SG} (***source-gate voltage***), V_{SD} (***source-drain voltage***), V_{SB} (***source-body voltage***)
- ***Current Convention***:
  - ***NMOS***: I_D (***drain current***) flows into the ***drain terminal*** and exits from the ***source terminal***
  - ***PMOS***: I_D flows into the ***source terminal*** and exits from the ***drain terminal***

- ***Gate is DC isolated by the insulator***
  - ***Gate Current $I_G = 0$***
  - ***Tremendous advantage***!
- ***Same current I_D flows through the device***
- ***Extremely compact device***
  - ***Saves a lot of area***
- ***Reversible device***:
  - ***D and S terminals are determined by their bias states***

Operation


inversion
layer
Source (S)
V_G
Drain (D)
gate
oxide
n^+
n^+
depletion
region
0
L
p-Si sub (N_A)
Body (B)
$V_{DS} = 0$