AICTE Training and Learning (ATAL) Academy





Sponsored
Faculty Development Program
on

VLSI Design Concepts and its Application for Semiconductor industry with Hands on Training

01st -06th Sept, 2025

Organized by

Department of Electronics and Communication Engineering, SVIET Banur, Punjab, India



Coordinators

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Highlights of FDP

This FDP will cover the following:

- Introduction and Design of VLSI Circuits for Low Power Application
- Sub threshold Logic Design
- Memory devices and process integration
- Connecting Technocrats to the Semiconductor Industry
- Transistors Design for High- Frequency Applications
- Current Trend and Challenges in Semiconductor Industry
- Multi Gate Semiconductor Devices
- Semiconductor Memories for Low Power Appliances
- Industrial visit to Semiconductor Laboratory Mohali
- SOC Design & Verification
- Sand to System on Chip: VLSI Design
- Hands on Training on Cadance Virtuoso Layout Suite EXL

Eminent Speakers

Dr. Sudeb Das Gupta Professor, IIT Roorkee



Dr. Arun Kumar Singh, Professor, PEC Chandigarh



Ms. Ana Monga, Technical Leader, ST Microelectronics



Dr. Balwinder Raj Associate Professor NIT Jalandhar



Dr. Balwinder Singh Joint Director, CDAC Mohali



Mr. Abhinav Behl Sr. Design &Verification Engineer, Cadence



Mr. Rajat Kumar Singh CEO VLSI FOR ALL Pvt Ltd.



Mr. Anuj Sharma CEO Chip Web Technologies



Registration Fee

There is NO REGISTRATION FEE to attend this offline FDP. Participants are requested/willing to attend this offline FDP at host institute should be nominated by their respective Head of Institutions.

Eligibility of Participants

The faculty members from the Higher Education Institutions, research scholars, PG scholar within 100 km of the host Institute and 30% staff of host institutions are eligible to attend the program.

Registration Process

Interested participants who want to attend this online FDP need to make mandatory online registration on the ATAL portal (https://atalacademy.aicteindia.org/login). Note: Shortlisted candidates will be announced through email within 2-3 days of online registration.

Certification

Candidates would be eligible to receive a certificate up on achieving at least 70% cumulative weightage in the following aspects:

- 1. Attendance (20%): Minimum 80% attendance required
- 2. Assessment (10%): MCQs/short answers/reasoning
- 3. Article Summary (30%): 2-page summary per team
- 4. Practical Sessions (15%): Individual output
- 5. Industrial Visit Report (10%): Team report
- 6. Reflection Journal (15%): Individual journal at the last session

CHIEF PATRON

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Sh. Ashok Garg Honorable President, SVIET, Banur

PATRON

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Prof. (Dr.) Sanjeev Saini Director Academics SVIET Banur

> Dr. Pretik Garg Principal SVIET Banur

ORGANIZING COMMITTEE

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About the SVIET

Established in 2004 with Engineering as a flagship program, Swami Vivekanand Institute of Engineering and Technology, Banur (SVIET) has come a long way in its journey of delivering quality higher education. Swami Vivekanand Institute of Engineering and Technology exemplifies the excellence in technical education. Empowering it's Graduates with the skills to facilitate their transition into their professional life, the SVIET Banur strives to create a steadfast workforce for the nation



About the ECE Department

The Department of Electronics and Communication Engineering was established in 2004. All the programs of department of ECE are approved by AICTE. It aims to produce quality professionals in this field to compete globally and excel by carrying out research in emerging areas by forging strong industry- institute interaction.

For more details, please visit www.sviet.ac.in