

Feb 08, 2024 01:05 PM

0000 00

Ghidra - MC68705U3_35C.BIN

```
PORT B I/O Lines

PB0 = /WMM (clock signal to latch PA(7:0) data on chip 32B / ...
PB1 = /WRCLK (connected to MM58247 RTC pin 3 /WD)
PB2 = /ROCLK (connected to MM58247 RTC pin 2 /RD)
PB3 = /RMM (signal to somewhere(?) on the CPU board)
PB4 = STAT3
PB5 = STAT4
PB6 = READ (IDB:13)
PB7 = STAT7 => INVERTED TO PRES (IDB:15) <= PRESENT SIGNAL if...

PORTB
XREF[77]:  RESET:012c(W), RESET:0153(RW),
           RESET:0155(RW), RESET:0195(RW),
           Output_Current_Date_Port_A_Mayba.,
           Output_Current_Date_Port_A_Mayba.,
           Output_Current_Date_Port_A_Mayba.,
           Output_Current_Date_Port_A_Mayba.,
           Output_Current_Date_Port_A_Mayba.,
           Clock_PB3_RMM_Return_Port_A:09bd.,
           Clock_PB3_RMM_Return_Port_A:09c1.,
           Write_RegA_To_PortA_And_Latch_to.,
           Write_RegA_To_PortA_And_Latch_to.,
           WriteDateBytesToPortA_LatchToIDB.,
           WriteDateBytesToPortA_LatchToIDB.,
           WriteDateBytesToPortA_LatchToIDB.,
           WriteDateBytesToPortA_LatchToIDB.,
           WriteDateBytesToPortA_LatchToIDB.,
           WriteDateBytesToPortA_LatchToIDB.,
           WriteDateBytesToPortA_LatchToIDB.,
           [more]

0001 00      db      0h

PORT C I/O Lines

STAT 0-4 goew to IDB(8:11)

PC0 = STAT0
PC1 = STAT1
PC2 = STAT2

DISP1-5 is to control display ? Goes to bus /DP(5:1) via inve...

PC3 = DISP1
PC4 = DISP2
PC5 = DISP3
PC6 = DISP4
PC7 = DISP5

PORTC
XREF[13]:  RESET:0134(W),
           Read_Write_Port_C:04a7(R),
           Read_Write_Port_C:04b0(W),
           Read_Write_Port_C:04b2(W),
           Read_Write_Port_C:04b6(W),
           Read_Write_Port_C:04b8(RW),
           Read_Write_Port_C:04be(W),
           Read_Write_Port_C:04c0(RW),
           Read_Write_Port_C:04cc(W),
           Read_Write_Port_C:04cd(RW),
           Read_Write_Port_C:04d5(W),
           Output_Current_Date_Port_A_Mayba.,
           Output_Current_Date_Port_A_Mayba.

0002 00      db      0h
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PORT D *INPUT* lines
PIN PD6 can be /INT2

PD0 = PCR0
PD1 = PCR1
PD2 = PONI
PD3 = IONI
PD4 = LHIT
PD5 = LEV0 (Level 0. Meaning CPU inactive)
PD6 = HIGH (To avoid external interrupt to be triggered)
PD7 = /EMP
PORTD
XREF[5]: RESET:0158(R), RESET:01a2(R),
          Read_Port_D:09af(R),
          Read_Port_D:09b4(R),
          Read_Port_D_Update_CLR:09d4(R)
0003 00      db      0h

DDRA
XREF[8]: RESET:0128(W),
          Read_Bytes_from_Port_A:0643(W),
          Write_RegA_To_PortA_And_Latch_to...,
          Write_RegA_To_PortA_And_Latch_to...,
          WriteDateBytesToPortA_LatchToIDB...,
          WriteDateBytesToPortA_LatchToIDB...,
          RTC_Initialize_Maybe:0ac2(W),
          RTC_Initialize_Maybe:0bdh(W)
0004 00      db      0h

DDRB
XREF[2]: RESET:0130(W),
          Read_Bytes_from_Port_A:0645(W)
0005 00      db      0h

DDRC
XREF[2]: RESET:0138(W),
          Read_Bytes_from_Port_A:0647(W)
0006 00      db      0h

DDRD
XREF[1]: RESET:013a(W)
0007 00      db      0h

TDR_Timer_Data_Register
XREF[3]: RESET:0145(W), RESET:0197(R),
          TIMER_INTERRUPT:08ca(W)
0008 00      db      0h

Timer Control Register Bits

b7 - TIR - Timer Interrupt Request Status (Set to 1 when time...
b6 - TIM - Timer Interrupt MASK (1=Interrupt inhibited, 0=Int...
b5 - TIN - Timer Input Select (1=External clock, 0=Internal c...
b4 - TIE - Timer External Input Enable (1=Enable external tim...
b3- PSC - Prescaler Clear (Write only. Writing 1 resets the p...
b2 - PS2 - Prescaler select 2
b1 - PS1 - Prescaler select 1
b0 - PS0 - Prescaler select 0

PS2 PS1 PS0 - Divide by
0 0 0 1
0 0 1 2
0 1 0 4
0 1 1 8
1 0 0 16
1 0 1 32
1 1 0 64
1 1 1 128

TCR_Timer_Control_Register
XREF[3]: RESET:0141(W),
          Read_Bytes_from_Port_A:063d(W),
          TIMER_INTERRUPT:08cc(RW)
0009 00      db      0h

MR_Misc_register
XREF[2]: RESET:0149(W),
          Read_Bytes_from_Port_A:0639(W)
000a 00      db      0h

PCR_Program_Control_Register
XREF[1]: Read_Bytes_from_Port_A:0641(W)
000b 00      db      0h
NOT USED MEMORY 0x00C-0x00F

000c 00      db      0h
000d 00      db      0h
000e 00      db      0h
000f 00      db      0h

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0x010 RAM START (112 bytes)
0x07F RAM END
RAM_0010

0010 00      db      0h

RAM_0011

XREF[5]:  Intialize_Ram_52_59_From_0xD22_0h,
          Read_Bytes_from_Port_A:053d(W),
          Read_Bytes_from_Port_A:0603(W),
          Read_Bytes_from_Port_A:0618(W),
          Read_Port_D:09ad(W)

0011 00      db      0h

RAM_0012

XREF[6]:  Intialize_Ram_52_59_From_0xD22_0h,
          Read_Bytes_from_Port_A:0543(W),
          Read_Bytes_from_Port_A:0568(W),
          Read_Bytes_from_Port_A:05fd(W),
          Read_Bytes_from_Port_A:0613(W),
          Read_Port_D:099c(W)

0012 00      db      0h

RAM_0013

XREF[7]:  Intialize_Ram_52_59_From_0xD22_0h,
          Read_Bytes_from_Port_A:0558(W),
          Read_Bytes_from_Port_A:0561(W),
          Read_Bytes_from_Port_A:056d(W),
          Read_Bytes_from_Port_A:05b2(W),
          Read_Bytes_from_Port_A:05f1(W),
          Read_Bytes_from_Port_A:0622(W)

0013 00      db      0h

RAM_0014

XREF[7]:  Intialize_Ram_52_59_From_0xD22_0h,
          Read_Bytes_from_Port_A:0556(W),
          Read_Bytes_from_Port_A:055f(W),
          Read_Bytes_from_Port_A:0570(W),
          Read_Bytes_from_Port_A:05be(W),
          Read_Bytes_from_Port_A:05eb(W),
          Read_Bytes_from_Port_A:061d(W)

0014 00      db      0h

RAM_0015

XREF[6]:  Something_RAM_0052_0059:025f(R),
          Something_RAM_0052_0059:026d(R),
          Something_RAM_0052_0059:027h(R),
          Read_Bytes_from_Port_A:051e(W),
          Read_Bytes_from_Port_A:0589(W),
          Read_Bytes_from_Port_A:05d0(W)

0015 00      db      0h

RAM_0016

XREF[8]:  Something_RAM_0052_0059:0230(R),
          Something_RAM_0052_0059:0240(R),
          Something_RAM_0052_0059:024d(R),
          Something_RAM_0052_0059:025d(R),
          Something_RAM_0052_0059:02c8(R),
          Read_Bytes_from_Port_A:0528(W),
          Read_Bytes_from_Port_A:0587(W),
          Read_Bytes_from_Port_A:05ce(W)

0016 00      db      0h

RAM_0017

XREF[11]: Something_RAM_0052_0059:0213(R),
          Something_RAM_0052_0059:021f(R),
          Something_RAM_0052_0059:022e(R),
          Something_RAM_0052_0059:02ad(R),
          Something_PortC:03ff(R),
          Something_PortC:040d(R),
          Something_PortC:041b(R),
          Read_Bytes_from_Port_A:0523(W),
          Read_Bytes_from_Port_A:0582(W),
          Read_Bytes_from_Port_A:05cd(W),
          Something_Ram_17_18:0670(R)

0017 00      db      0h

XREF[13]: Something_PortC:03a9(R),
          Something_PortC:03b9(R),
          Something_PortC:03c6(R),
          Something_PortC:03d9(R),
          Something_PortC:03fd(R),
          Something_PortC:045a(R),
          Read_Bytes_from_Port_A:0532(W),
          Read_Bytes_from_Port_A:057d(W),
          Read_Bytes_from_Port_A:059d(W),
          Read_Bytes_from_Port_A:05da(W),
          Something_Ram_17_18:067h(W),
          Something_Ram_17_18:0687(W),
          Something_Ram_17_18:068e(W)
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	RAM_0018		XREF[12]:	Something_PortC:038c(R), Something_PortC:0398(R), Something_PortC:03a7(R), Something_PortC:043c(R), Read_Bytes_from_Port_A:052d(W), Read_Bytes_from_Port_A:0578(W), Read_Bytes_from_Port_A:0597(W), Read_Bytes_from_Port_A:05d5(W), Something_Ram_17_18:067d(RW), Something_Ram_17_18:0682(R), Something_Ram_17_18:0689(W), Something_Ram_17_18:068c(RW)
0018 00	db	0h		
	PortD_PONI_IONI_bit_4_5_Ring_3_0		XREF[7]:	Read_Bytes_from_Port_A:05ad(R), Read_Bytes_from_Port_A:05b4(R), PortD_Update_PONI_IONI_bits:06b7(W), PortD_Update_PONI_IONI_bits:06ba(W), Read_Port_D_Update_CLR:09dd(W), Read_Port_D_Update_CLR:09e9(R), Read_Port_D_Update_CLR:09eb(W)
0019 00	db	0h		
	RAM_001a		XREF[5]:	RESET:014c(W), Read_Bytes_from_Port_A:053e(R), Read_Bytes_from_Port_A:0545(R), Read_Bytes_from_Port_A:054d(R), Read_Bytes_from_Port_A:060h(W)
001a 00	db	0h		
	RAM_001b		XREF[22]:	Something_RAM_0052_0059:01ed(R), Something_RAM_0052_0059:01f0(R), Something_RAM_0052_0059:0202(R), Something_RAM_0052_0059:029h(R), Something_PortC:037b(R), Something_PortC:03d6(R), Read_Bytes_from_Port_A:0534(RW), Read_Bytes_from_Port_A:0536(RW), Read_Bytes_from_Port_A:0538(RW), Read_Bytes_from_Port_A:058h(RW), Read_Bytes_from_Port_A:058d(RW), Read_Bytes_from_Port_A:058f(RW), Read_Bytes_from_Port_A:059e(RW), Read_Bytes_from_Port_A:05a0(RW), Read_Bytes_from_Port_A:05a2(RW), Read_Bytes_from_Port_A:05c3(RW), Read_Bytes_from_Port_A:05c5(RW), Read_Bytes_from_Port_A:05c7(RW), Read_Bytes_from_Port_A:064d(RW), Read_Bytes_from_Port_A:0652(RW), [more]
001b 00	db	0h		
	RAM_001c		XREF[10]:	Read_Bytes_from_Port_A:04db(W), Read_Bytes_from_Port_A:04dd(R), Read_Bytes_from_Port_A:04e3(R), Output_Current_Date_Port_A_Mayba(W), Output_Current_Date_Port_A_Mayba(W), Output_Current_Date_Port_A_Mayba(W), Output_Current_Date_Port_A_Mayba(W), Output_Current_Date_Port_A_Mayba(W), Output_Current_Date_Port_A_Mayba(W), Output_Current_Date_Port_A_Mayba(W)
001c 00	db	0h		
	RAM_001d		XREF[10]:	Something_RAM_0052_0059:01f9(R), Something_PortC:037e(R), Read_Bytes_from_Port_A:04ed(R), Read_Bytes_from_Port_A:05a6(W), Read_Bytes_from_Port_A:062a(W), Read_Bytes_from_Port_A:0654(R), Read_Bytes_from_Port_A:0662(R), Read_Bytes_from_Port_A:0666(W), SomeLogic_From_RAM_001D_store_00(W), SomeLogic_From_RAM_001D_store_00(W)
001d 00	db	0h		

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	RAM_001e		XREF[7]:	Read_Bytes_from_Port_A:05aa(W), Read_Bytes_from_Port_A:062ff(W), Read_Bytes_from_Port_A:0657f(W), Read_Bytes_from_Port_A:065af(W), Read_Bytes_from_Port_A:065df(R), Read_Bytes_from_Port_A:0660f(W), Something_Ram_17_18:0674f(R)
001e 00	db	0h		
	counter_wait_pd7_signal_EMP_n		XREF[2]:	RESET:0150(W), RESET:015b(RW)
001f 00	db	0h		
	BYTE_0020		XREF[15]:	Something_RAM_0052_0059:0323(R), Something_RAM_0052_0059:0348(R), CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Something_RAM_20_25:093b(RW), WriteDateBytesToPortA_LatchToIDB. RTC_Initialize_Maybe:0ae8(W), RTC_Initialize_Maybe:0afff(R), RTC_Initialize_Maybe:0b01f(W)
0020 00	db	0h		
	BYTE_0021		XREF[14]:	Something_RAM_0052_0059:035d(R), Something_RAM_0052_0059:036h(R), CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Something_RAM_20_25:0917f(R), Something_RAM_20_25:0931f(RW), Something_RAM_20_25:0933f(R), Something_RAM_20_25:0939f(W), WriteDateBytesToPortA_LatchToIDB. RTC_Initialize_Maybe:0b0ff(W), RTC_Initialize_Maybe:0b26f(R), RTC_Initialize_Maybe:0b28f(W)
0021 00	db	0h		
	BYTE_0022		XREF[9]:	CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Something_RAM_20_25:0925f(RW), Something_RAM_20_25:0927f(R), Something_RAM_20_25:092df(W), WriteDateBytesToPortA_LatchToIDB. RTC_Initialize_Maybe:0b36f(W), RTC_Initialize_Maybe:0b4df(R), RTC_Initialize_Maybe:0b4ff(W)
0022 00	db	0h		
	BYTE_0023		XREF[10]:	CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Something_RAM_20_25:090ff(RW), Something_RAM_20_25:0911f(R), Something_RAM_20_25:0915f(W), WriteDateBytesToPortA_LatchToIDB. RTC_Initialize_Maybe:0b5df(W), RTC_Initialize_Maybe:0b74f(R), RTC_Initialize_Maybe:0b76f(W)
0023 00	db	0h		
	BYTE_0024		XREF[12]:	Something_RAM_0052_0059:02ef(R), Something_RAM_0052_0059:0302f(R), CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Something_RAM_20_25:0905f(RW), Something_RAM_20_25:0907f(R), Something_RAM_20_25:090bf(W), WriteDateBytesToPortA_LatchToIDB. RTC_Initialize_Maybe:0b84f(W), RTC_Initialize_Maybe:0b9bf(R), RTC_Initialize_Maybe:0b9df(W)
0024 00	db	0h		

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		BYTE_0025		XREF[13]:	Something_RAM_0052_0059:02e(R), Something_RAM_0052_0059:0302(R), CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Something_RAM_20_25:08f(R), Something_RAM_20_25:08fd(R), Something_RAM_20_25:0901(W), WriteDateBytesToPortA_LatchToIDB. WriteDateBytesToPortA_LatchToIDB. RTC_Initialize_Maybe:0bab(W), RTC_Initialize_Maybe:0bc2(R), RTC_Initialize_Maybe:0bc4(W)
0025	00	db	0h		
		BYTE_0026		XREF[16]:	CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Something_RAM_20_25:092(R), Something_RAM_20_25:093d(W), Something_RAM_20_25:093f(R), Something_RAM_20_25:0945(W), WriteDateBytesToPortA_LatchToIDB. RTC_Initialize_Maybe:0ada(W)
0026	00	db	0h		
0027	00	db	0h		
0028	00	db	0h		
0029	00	db	0h		
002a	00	db	0h		
002b	00	db	0h		
002c	00	db	0h		
002d	00	db	0h		
002e	00	db	0h		
002f	00	db	0h		
0030	00	db	0h		
0031	00	db	0h		
0032	00	db	0h		
0033	00	db	0h		
0034	00	db	0h		
0035	00	db	0h		
0036	00	db	0h		
0037	00	db	0h		
0038	00	db	0h		
0039	00	db	0h		
003a	00	db	0h		
003b	00	db	0h		
003c	00	db	0h		
003d	00	db	0h		
003e	00	db	0h		
003f	00	db	0h		
0040	00	db	0h		
0041	00	db	0h		
0042	00	db	0h		
		BYTE_0043		XREF[1]:	Read_Write_Port_C:04bd(R)
0043	00	db	0h		
		BYTE_0044		XREF[1]:	Read_Write_Port_C:04bd(R)
0044	00	db	0h		
		BYTE_0045		XREF[3]:	RESET:0166(W), Read_Write_Port_C:04b4(R), Read_Write_Port_C:04c8(R)
0045	00	db	0h		
		PortC_ValueToWrite		XREF[5]:	RESET:0166(W), Something_RAM_050_051:0496(R), Something_RAM_050_051:0498(W), Read_Write_Port_C:04ab(R), Read_Write_Port_C:04c8(R)
0046	00	db	0h		
		BYTE_0047		XREF[3]:	CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08.
0047	00	db	0h		

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	BYTE_0048		XREF[4]:	CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08.
0048 00	db	0h		
	BYTE_0049		XREF[2]:	CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08.
0049 00	db	0h		
	BYTE_004a		XREF[2]:	CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08.
004a 00	db	0h		
	BYTE_004b		XREF[17]:	RESET:0170(W), RESET:017e(W), RESET:018c(W), Something_RAM_050_051:048(R), CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08.
004b 00	db	0h		
	BYTE_004c		XREF[24]:	RESET:0174(W), RESET:0182(W), RESET:0190(W), Something_RAM_050_051:049(QR), CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. [more]
004c 00	db	0h		
	BYTE_004d		XREF[29]:	CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. [more]
004d 00	db	0h		

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004e 00	db	0h	XREF[31]:	CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. [more]
004f 00	db	0h	XREF[11]:	Something_RAM_0052_0059:02e9(W), Something_RAM_0052_0059:02fd(R), Something_RAM_0052_0059:030e(RW), Something_RAM_0052_0059:0310(R), Something_RAM_0052_0059:0314(RW), Something_RAM_050_051:047b(W), Something_RAM_050_051:0492(R), Something_RAM_050_051:0494(RW), Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08.
0050 00	db	0h	XREF[2]:	Something_RAM_050_051:0483(W), Something_RAM_050_051:049c(RW)
0051 00	db	0h	XREF[20]:	Something_RAM_0052_0059:02b0(W), Something_RAM_0052_0059:02bd(R), Something_RAM_0052_0059:02c4(RW), Something_RAM_0052_0059:02ce(W), Something_RAM_0052_0059:02da(R), Something_RAM_0052_0059:02e2(RW), Something_RAM_0052_0059:02ed(W), Something_RAM_0052_0059:0300(R), Something_RAM_0052_0059:0310(RW), Something_RAM_0052_0059:0318(R), Something_PortC:0442(W), Something_PortC:044e(R), Something_PortC:0456(RW), Something_PortC:0460(W), Something_PortC:046c(R), Something_PortC:0474(RW), Something_RAM_050_051:047a(W), Something_RAM_050_051:049a(R), Something_RAM_050_051:04a0(RW), Something_RAM_050_051:04a2(R)
0052 00	db	0h	XREF[37]:	Initialize_Ram_52_59_From_0xD22_0. Something_RAM_0052_0059:0289(W), Something_RAM_0052_0059:02a1(W), Something_RAM_0052_0059:032b(W), Something_RAM_0052_0059:0335(W), Something_PortC:03e9(W), Something_PortC:0429(W), CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. CopyData_In_Ram_Dest_0x46_0x4e:0. Calc_Something_Dest_0x48_0x4f:08. Calc_Something_Dest_0x48_0x4f:08. RTC_Initialize_Maybe:0afa(W), RTC_Initialize_Maybe:0afd(R), RTC_Initialize_Maybe:0b21(W), RTC_Initialize_Maybe:0b24(R), [more]

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0053 00	db	0h	BYTE_0053	XREF[15]:	Intialize_Ram_52_59_From_0xD22_0a. Something_RAM_0052_0059:0279(W), Something_RAM_0052_0059:02a5(W), Something_RAM_0052_0059:032f(W), Something_RAM_0052_0059:0339(W), Something_PortC:03e7(W), Something_PortC:0419(W), CopyData_In_Ram_Dest_0x46_0x4e:0a. CopyData_In_Ram_Dest_0x46_0x4e:0a. CopyData_In_Ram_Dest_0x46_0x4e:0a. CopyData_In_Ram_Dest_0x46_0x4e:0a. CopyData_In_Ram_Dest_0x46_0x4e:0a. CopyData_In_Ram_Dest_0x46_0x4e:0a. CopyData_In_Ram_Dest_0x46_0x4e:0a.
0054 00	db	0h	BYTE_0054	XREF[9]:	Intialize_Ram_52_59_From_0xD22_0a. Something_RAM_0052_0059:026b(W), Something_RAM_0052_0059:02dc(W), Something_RAM_0052_0059:0346(W), Something_PortC:03e5(W), Something_PortC:03ef(R), Something_PortC:03f3(W), Something_PortC:040b(W), Something_PortC:046e(W)
0055 00	db	0h	BYTE_0055	XREF[11]:	Intialize_Ram_52_59_From_0xD22_0a. Something_RAM_0052_0059:020e(W), Something_RAM_0052_0059:025b(W), Something_RAM_0052_0059:02a7(RW), Something_RAM_0052_0059:02dc(W), Something_RAM_0052_0059:032Q(RW), Something_RAM_0052_0059:0355(W), Something_PortC:03d4(W), Something_PortC:03ef(R), Something_PortC:046e(W), Something_RAM_050_051:048c(RW)
0056 00	db	0h	BYTE_0056	XREF[6]:	Intialize_Ram_52_59_From_0xD22_0a. Something_RAM_0052_0059:021Q(W), Something_RAM_0052_0059:024b(W), Something_RAM_0052_0059:0312(W), Something_RAM_0052_0059:0357(W), Something_PortC:03c4(W)
0057 00	db	0h	BYTE_0057	XREF[6]:	Intialize_Ram_52_59_From_0xD22_0a. Something_RAM_0052_0059:023e(W), Something_RAM_0052_0059:02fe(W), Something_RAM_0052_0059:031c(RW), Something_RAM_0052_0059:035b(W), Something_PortC:03b7(W)
0058 00	db	0h	BYTE_0058	XREF[9]:	Intialize_Ram_52_59_From_0xD22_0a. Something_RAM_0052_0059:0207(W), Something_RAM_0052_0059:022c(W), Something_RAM_0052_0059:02be(W), Something_RAM_0052_0059:0312(W), Something_RAM_0052_0059:0369(W), Something_PortC:03a5(W), Something_PortC:045Q(W), Something_RAM_050_051:048Q(RW)
0059 00	db	0h	BYTE_0059	XREF[10]:	Intialize_Ram_52_59_From_0xD22_0a. Something_RAM_0052_0059:0207(W), Something_RAM_0052_0059:021d(W), Something_RAM_0052_0059:02be(W), Something_RAM_0052_0059:02fe(W), Something_RAM_0052_0059:031c(RW), Something_RAM_0052_0059:0378(W), Something_PortC:0396(W), Something_PortC:045Q(W), Something_RAM_050_051:048Q(RW)

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	PortC_SavedValue			XREF[18]:	Something_RAM_0052_0059:02ac(W), Something_RAM_0052_0059:02b2(R), Something_RAM_0052_0059:02c0(RW), Something_RAM_0052_0059:02c2(RW), Something_RAM_0052_0059:02ca(W), Something_RAM_0052_0059:02d0(R), Something_RAM_0052_0059:02d2(RW), Something_RAM_0052_0059:02e0(RW), Something_PortC:043e(W), Something_PortC:0444(R), Something_PortC:0452(RW), Something_PortC:0454(RW), Something_PortC:045c(W), Something_PortC:0462(R), Something_PortC:0470(RW), Something_PortC:0472(RW), Read_Write_Port_C:04a9(W), Read_Write_Port_C:04d3(R)
005a 00	db	0h			
	RAM_005b			XREF[3]:	RESET:011a(W), TIMER_INTERRUPT:08da(RW), TIMER_INTERRUPT:08e3(W)
005b 00	db	0h			
	RAM_005c			XREF[3]:	RESET:011e(W), TIMER_INTERRUPT:08e5(RW), TIMER_INTERRUPT:08eb(W)
005c 00	db	0h			
	RAM_005d			XREF[3]:	RESET:0122(W), TIMER_INTERRUPT:08ed(RW), TIMER_INTERRUPT:08f3(W)
005d 00	db	0h			
	BYTE_005e			XREF[1]:	MoveDataBytes_061_06f:0980(R)
005e 00	db	0h			
	BYTE_005f			XREF[1]:	MoveDataBytes_061_06f:097d(R)
005f 00	db	0h			
	BYTE_0060			XREF[3]:	PortD_Update_PONI_IONI_bits:06b5, PortD_Update_PONI_IONI_bits:06b9, MoveDataBytes_061_06f:0978(R)
0060 00	db	0h			
	BYTE_0061			XREF[2]:	MoveDataBytes_061_06f:0974(R), MoveDataBytes_061_06f:0982(W)
0061 00	db	0h			
	BYTE_0062			XREF[2]:	MoveDataBytes_061_06f:0970(R), MoveDataBytes_061_06f:097e(W)
0062 00	db	0h			
	BYTE_0063			XREF[2]:	MoveDataBytes_061_06f:096c(R), MoveDataBytes_061_06f:097a(W)
0063 00	db	0h			
	BYTE_0064			XREF[2]:	MoveDataBytes_061_06f:0968(R), MoveDataBytes_061_06f:0976(W)
0064 00	db	0h			
	BYTE_0065			XREF[2]:	MoveDataBytes_061_06f:0964(R), MoveDataBytes_061_06f:0972(W)
0065 00	db	0h			
	BYTE_0066			XREF[2]:	MoveDataBytes_061_06f:0960(R), MoveDataBytes_061_06f:096e(W)
0066 00	db	0h			
	BYTE_0067			XREF[2]:	MoveDataBytes_061_06f:095c(R), MoveDataBytes_061_06f:096a(W)
0067 00	db	0h			
	BYTE_0068			XREF[2]:	MoveDataBytes_061_06f:0958(R), MoveDataBytes_061_06f:0966(W)
0068 00	db	0h			
	BYTE_0069			XREF[2]:	MoveDataBytes_061_06f:0954(R), MoveDataBytes_061_06f:0962(W)
0069 00	db	0h			

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	BYTE_006a		XREF[2]:	MoveDataBytes_061_06f:0950(R), MoveDataBytes_061_06f:095e(W)
006a 00	db	0h		
	BYTE_006b		XREF[2]:	MoveDataBytes_061_06f:094d(R), MoveDataBytes_061_06f:095a(W)
006b 00	db	0h		
	BYTE_006c		XREF[2]:	MoveDataBytes_061_06f:0948(R), MoveDataBytes_061_06f:0956(W)
006c 00	db	0h		
	BYTE_006d		XREF[1]:	MoveDataBytes_061_06f:0952(W)
006d 00	db	0h		
	BYTE_006e		XREF[1]:	MoveDataBytes_061_06f:094e(W)
006e 00	db	0h		
	BYTE_006f		XREF[2]:	PortD_Update_PONI_IONI_bits:06b2., MoveDataBytes_061_06f:094a(W)
006f 00	db	0h		
	PortD_SavedValue		XREF[3]:	Read_Port_D_Update_CLR:09d6(W), Read_Port_D_Update_CLR:09de(R), Read_Port_D_Update_CLR:09e1(R)
0070 00	db	0h		
	RAM_0071		XREF[3]:	RESET:0126(W), Read_Port_D:0985(RW), Read_Port_D:098b(W)
0071 00	db	0h		
	BYTE_0072		XREF[3]:	Read_Port_D:098d(R), Read_Port_D:0993(W), Read_Port_D:09b2(RW)
0072 00	db	0h		
	BYTE_0073		XREF[3]:	Read_Port_D:099e(R), Read_Port_D:09a4(W), Read_Port_D:09b7(RW)
0073 00	db	0h		
0074 00	db	0h		
0075 00	db	0h		
0076 00	db	0h		
0077 00	db	0h		
0078 00	db	0h		
0079 00	db	0h		
007a 00	db	0h		
007b 00	db	0h		
007c 00	db	0h		
007d 00	db	0h		
007e 00	db	0h		
007f 00	db	0h		
	RAM ENDS AT 0x007F ***** ROM START AT 0x0080 ENDS AT 0x0FFF BYTE_0080		XREF[2]:	CopyData_In_Ram_Dest_0x46_0x4e:0., Calc_Something_Dest_0x48_0x4f:08.
0080 02	db	2h		
	BYTE_0081		XREF[2]:	CopyData_In_Ram_Dest_0x46_0x4e:0., Calc_Something_Dest_0x48_0x4f:08.
0081 da	db	DAh		
	BYTE_0082		XREF[1]:	CopyData_In_Ram_Dest_0x46_0x4e:0.
0082 0e	db	Eh		
	BYTE_0083		XREF[1]:	CopyData_In_Ram_Dest_0x46_0x4e:0.
0083 10	db	10h		
0084 07	db	7h		
0085 bb	db	BBh		
0086 00	db	0h		
0087 10	db	10h		
0088 20	db	20h		
0089 30	db	30h		
008a 40	db	40h		
008b 50	db	50h		
008c 60	db	60h		
008d 70	db	70h		
	BYTE_008e		XREF[1]:	RESET:0113(W)
008e 00	db	0h		

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	BYTE_008f		XREF[1]:	RESET:0113(W)
008f 10	db	10h		
0090 20	db	20h		
0091 30	db	30h		
0092 40	db	40h		
0093 50	db	50h		
0094 60	db	60h		
0095 70	db	70h		
0096 00	db	0h		
0097 10	db	10h		
0098 20	db	20h		
0099 30	db	30h		
009a 40	db	40h		
009b 50	db	50h		
009c 60	db	60h		
009d 70	db	70h		
009e 00	db	0h		
009f 10	db	10h		
00a0 20	db	20h		
00a1 30	db	30h		
00a2 40	db	40h		
00a3 50	db	50h		
00a4 60	db	60h		
00a5 70	db	70h		
00a6 00	db	0h		
00a7 10	db	10h		
00a8 20	db	20h		
00a9 30	db	30h		
00aa 40	db	40h		
00ab 50	db	50h		
00ac 60	db	60h		
00ad 70	db	70h		
00ae 00	db	0h		
00af 10	db	10h		
00b0 20	db	20h		
00b1 30	db	30h		
00b2 40	db	40h		
00b3 50	db	50h		
00b4 60	db	60h		
00b5 70	db	70h		
00b6 00	db	0h		
00b7 10	db	10h		
00b8 20	db	20h		
00b9 30	db	30h		
00ba 40	db	40h		
00bb 50	db	50h		
00bc 60	db	60h		
00bd 70	db	70h		
00be 00	db	0h		
00bf 10	db	10h		
00c0 20	db	20h		
00c1 30	db	30h		
00c2 40	db	40h		
00c3 50	db	50h		
00c4 60	db	60h		
00c5 70	db	70h		
00c6 00	db	0h		
00c7 10	db	10h		
00c8 20	db	20h		
00c9 30	db	30h		
00ca 40	db	40h		
00cb 50	db	50h		
00cc 60	db	60h		
00cd 70	db	70h		
00ce 00	db	0h		
00cf 10	db	10h		
00d0 20	db	20h		
00d1 30	db	30h		
00d2 40	db	40h		
00d3 50	db	50h		
00d4 60	db	60h		
00d5 70	db	70h		
00d6 00	db	0h		
00d7 10	db	10h		
00d8 20	db	20h		
00d9 30	db	30h		
00da 40	db	40h		
00db 50	db	50h		
00dc 60	db	60h		
00dd 70	db	70h		
00de 00	db	0h		
00df 10	db	10h		
00e0 20	db	20h		
00e1 30	db	30h		

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```

00e2 40      db      40h
00e3 50      db      50h
00e4 60      db      60h
00e5 70      db      70h
00e6 00      db      0h
00e7 10      db      10h
00e8 20      db      20h
00e9 30      db      30h
00ea 40      db      40h
00eb 50      db      50h
00ec 60      db      60h
00ed 70      db      70h
00ee 00      db      0h
00ef 10      db      10h
00f0 20      db      20h
00f1 30      db      30h
00f2 40      db      40h
00f3 50      db      50h
00f4 60      db      60h
00f5 70      db      70h
00f6 00      db      0h
00f7 10      db      10h
00f8 20      db      20h
00f9 30      db      30h
00fa 40      db      40h
00fb 50      db      50h
00fc 60      db      60h
00fd 70      db      70h

RAM_00fe                                         XREF[9]:      RESET:013c(W), RESET:0161(W),
                                                    RESET:016b(W), RESET:0176(W),
                                                    RESET:0179(W), RESET:0184(W),
                                                    RESET:0187(W), RESET:0192(W),
                                                    RESET:019e(W)

00fe 00      db      0h
00ff 10      db      10h
0100 20      db      20h
0101 30      db      30h
0102 40      db      40h
0103 50      db      50h
0104 60      db      60h
0105 70      db      70h
0106 00      db      0h
0107 00      db      0h
0108 00      db      0h
0109 00      db      0h
010a 00      db      0h
010b 00      db      0h
010c 00      db      0h
010d 00      db      0h
010e 00      db      0h
010f 00      db      0h

*****
*                               *
*                               *
*****
undefined RESET()
undefined      A:1      <RETURN>
byte          X:1      bVar2                      XREF[2]:      01a5(W), 01a8(W)
byte          X:1      bVar3                      XREF[1]:      01a8(W)

Initial analysis of the code seems to show that this CPU is o...
And this chip will respond if the output line /WMM line is lo...

I am guessing that this CPU combined with the RTC (Chip 34A, ...

In addition there is some statistics that are output (STAT[...

* DISPLAY/DP signals goes to A-BUS which is "Console and Pane...
* STAT signals goes to IDB[11:8] and also the STAT[4:3] goes ...
It somehow impacts the logic together with LCS_n on the out...
PRQ_n goes to DGA_POW module (where it somehow impacts IDB0...
VAL goes to ??

RESET                                         XREF[2]:      Read_Bytes_from_Port_A:0649(c),
                                                    Offe(*)

0110 9c      RSP
0111 ae 7f   LDX      #0x7f

LAB_0113                                         XREF[1]:      0116(j)
                                                    = 10h
0113 6f 10   CLR      0x10,X=>BYTE 008f
0115 5a      DECX
0116 2a fb   BPL      LAB_0113
0118 a6 10   LDA      #0x10
011a b7 5b   STA      RAM_005b
011c a6 c8   LDA      #0xc8

```

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```

011e b7 5c      STA      RAM_005c
0120 a6 02      LDA      #0x2
0122 b7 5d      STA      RAM_005D
0124 a6 80      LDA      #0x80
0126 b7 71      STA      RAM_0071
0128 3f 04      CLR      DDRA
012a a6 2f      LDA      #0x2f
012c b7 01      STA      PORTB
012e a6 ff      LDA      #0xff
0130 b7 05      STA      DDRB
0132 a6 f8      LDA      #0xf8
0134 b7 02      STA      PORTC
0136 a6 ff      LDA      #0xff
0138 b7 06      STA      DDRC
013a 3f 07      CLR      DDRD
013c cd 0a c0    JSR      RTC_Initialize_Maybe      undefinedRTC_Initialize_Maybe()

Set Timer Control register value 0x35

TIM=0 => Timer Interrupt Enable
TIN=1 => Timer Input Select External Clock
TIE=1 => Timer External Input Enable
PS=101 => Prescaler divide by 32.

--- DESIGN INFO --- (might be wrong, but based on schemas)
PANOSC will only oscillate (as a function of RTOSC) when CLOSC...
PANOSC = RTOSC / 4.
RTOSC = 153.6Khz
PANOSC = RTOSC/4 = 38400 HZ

With prescale divider on 32, the timer interrupt should be 12...

68705 CPU is running on 4MHZ, so that means an Timer interrupt...

013f a6 35      LDA      #0x35
0141 b7 09      STA      TCR_Timer_Control_Register
0143 a6 03      LDA      #0x3
0145 b7 08      STA      TDR_Timer_Data_Register
0147 a6 7f      LDA      #0x7f
0149 b7 0a      STA      MR_Misc_register
014b 9a        CLI
014c 3f 1a      CLR      RAM_001a

LAB_014e
014e a6 ff      LDA      #0xff
0150 b7 1f      STA      counter_wait_pd7_signal_EMP_n
0152 9b        SEI
0153 18 01      BSET     0x4,PORTB
0155 19 01      BCLR     0x4,PORTB
0157 9a        CLI

Wait for signal "/EMP" to go HIGH on port D pin 7.
LAB_0158
0158 0e 03 06   BRSET     0x7,PORTD,LAB_0161      XREF[1]: 015f(j), 01b1(j)
015b 3a 1f      DEC      counter_wait_pd7_signal_EMP_n
015d 26 f9      BNE      LAB_0158
015f 20 ed      BRA      LAB_014e

LAB_0161
0161 cd 04 d8   JSR      Read_Bytes_from_Port_A      XREF[2]: 0158(j), 01a2(j)
0164 ae 1f      LD      #0x1f      undefinedRead_Bytes_from_Port_A()

LAB_0166
0166 6f 27      CLR      0x27,X=>PortC_ValueToWrite      XREF[1]: 0169(j)
0168 5a        DECC
0169 2a fb      BPL      LAB_0166
016b cd 01 b4   JSR      Intialize_Ram_52_59_From_0xD22_area      undefinedIntialize_Ram_52_59_Fr...
016e a6 40      LDA      #0x40
0170 b7 4b      STA      BYTE_004b
0172 a6 04      LDA      #0x4
0174 b7 4c      STA      BYTE_004c
0176 cd 04 79   JSR      Something_RAM_050_051      undefinedSomething_RAM_050_051()
0179 cd 01 ed   JSR      Something_RAM_0052_0059      undefinedSomething_RAM_0052_005...
017c a6 20      LDA      #0x20
017e b7 4b      STA      BYTE_004b
0180 a6 02      LDA      #0x2
0182 b7 4c      STA      BYTE_004c
0184 cd 04 79   JSR      Something_RAM_050_051      undefinedSomething_RAM_050_051()
0187 cd 03 7b   JSR      Something_PortC      undefinedSomething_PortC()
018a a6 10      LDA      #0x10
018c b7 4b      STA      BYTE_004b
018e a6 01      LDA      #0x1
0190 b7 4c      STA      BYTE_004c
0192 cd 04 79   JSR      Something_RAM_050_051      undefinedSomething_RAM_050_051()
0195 1b 01      BCLR     0x5,PORTB

```

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```

LAB_0197
0197 b6 08 LDA TDR_Timer_Data_Register XREF[1]: 019b(j)
0199 a1 03 CMP #0x3
019b 26 fa BNE LAB_0197
019d 9b SEI
019e cd 04 a7 JSR Read_Write_Port_C voidRead_Write_Port_C(void)
01a1 9a CLI
01a2 0e 03 bc BRSET 0x7,PORTD,LAB_0161
Wait for 320 Clock Ticks.
01a5 ae 20 LDX #0x20

LAB_01a7
01a7 9f TXA XREF[1]: 01af(j)
01a8 ae 0a LDX #0xa

LAB_01aa
01aa 5a DECX XREF[1]: 01ab(j)
01ab 26 fd BNE LAB_01aa
01ad 97 TAX
01ae 5a DECX
01af 26 f6 BNE LAB_01a7
01b1 cc 01 4e JMP LAB_014e

*****
* FUNCTION *
*****
undefined Intialize_Ram_52_59_From_0xD22_area)
A:1 <RETURN>
Intialize_Ram_52_59_From_0xD22_area XREF[1]: RESET:016b(c)
01b4 be 13 LDX RAM_0013
01b6 58 ASLX
01b7 d6 0d 22 LDA DAT_0d22,X
01ba b7 59 STA BYTE_0059
01bc 5c INCX
01bd d6 0d 22 LDA DAT_0d22,X
01c0 b7 58 STA BYTE_0058
01c2 be 12 LDX RAM_0012
01c4 58 ASLX
01c5 d6 0d 22 LDA DAT_0d22,X
01c8 b7 57 STA BYTE_0057
01ca 5c INCX
01cb d6 0d 22 LDA DAT_0d22,X
01ce b7 56 STA BYTE_0056
01d0 be 11 LDX RAM_0011
01d2 58 ASLX
01d3 d6 0d 22 LDA DAT_0d22,X
01d6 b7 55 STA BYTE_0055
01d8 5c INCX
01d9 d6 0d 22 LDA DAT_0d22,X
01dc b7 54 STA BYTE_0054
01de be 10 LDX RAM_0010
01e0 58 ASLX
01e1 d6 0d 22 LDA DAT_0d22,X
01e4 b7 53 STA BYTE_0053
01e6 5c INCX
01e7 d6 0d 22 LDA DAT_0d22,X
01ea b7 52 STA BYTE_0052
01ec 81 RTS

*****
* FUNCTION *
*****
undefined Something_RAM_0052_0059()
A:1 <RETURN>
Something_RAM_0052_0059 XREF[1]: RESET:0179(c)
01ed 03 1b 09 BRCLR 0x1,RAM_001b,LAB_01f9
01f0 04 1b 03 BRSET 0x2,RAM_001b,LAB_01f6
01f3 cc 02 e7 JMP LAB_02e7

LAB_01f6
01f6 cc 03 23 JMP LAB_0323

LAB_01f9
01f9 b6 1d LDA RAM_001d
01fb a4 03 AND #0x3
01fd 27 03 BEQ LAB_0202
01ff cc 02 aa JMP LAB_02aa

LAB_0202
0202 07 1b 0e BRCLR 0x3,RAM_001b,LAB_0213
0205 ae 07 LDX #0x7

LAB_0207
0207 6f 52 CLR 0x52,X=>BYTE_0059 XREF[1]: 020a(j)

```


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0209	5a	DECX	
020a	2a fb	BPL	LAB_0207
020c	a6 08	LDA	#0x8
020e	b7 55	STA	BYTE_0055
0210	b7 56	STA	BYTE_0056
0212	81	RTS	
	LAB_0213		XREF[1]: 0202(j)
0213	b6 16	LDA	RAM_0016
0215	a4 07	AND	#0x7
0217	ab 10	ADD	#0x10
0219	97	TAX	
021a	d6 0c f8	LDA	DAT_0cf8,X
021d	b7 59	STA	BYTE_0059
021f	b6 16	LDA	RAM_0016
0221	44	LSRA	
0222	44	LSRA	
0223	44	LSRA	
0224	a4 07	AND	#0x7
0226	ab 10	ADD	#0x10
0228	97	TAX	
0229	d6 0c f8	LDA	DAT_0cf8,X
022c	b7 58	STA	BYTE_0058
022e	be 16	LDX	RAM_0016
0230	b6 15	LDA	RAM_0015
0232	58	ASLX	
0233	49	ROLA	
0234	58	ASLX	
0235	49	ROLA	
0236	a4 07	AND	#0x7
0238	ab 10	ADD	#0x10
023a	97	TAX	
023b	d6 0c f8	LDA	DAT_0cf8,X
023e	b7 57	STA	BYTE_0057
0240	b6 15	LDA	RAM_0015
0242	44	LSRA	
0243	a4 07	AND	#0x7
0245	ab 10	ADD	#0x10
0247	97	TAX	
0248	d6 0c f8	LDA	DAT_0cf8,X
024b	b7 56	STA	BYTE_0056
024d	b6 15	LDA	RAM_0015
024f	44	LSRA	
0250	44	LSRA	
0251	44	LSRA	
0252	44	LSRA	
0253	a4 07	AND	#0x7
0255	ab 10	ADD	#0x10
0257	97	TAX	
0258	d6 0c f8	LDA	DAT_0cf8,X
025b	b7 55	STA	BYTE_0055
025d	be 15	LDX	RAM_0015
025f	b6 14	LDA	RAM_0014
0261	58	ASLX	
0262	49	ROLA	
0263	a4 07	AND	#0x7
0265	ab 10	ADD	#0x10
0267	97	TAX	
0268	d6 0c f8	LDA	DAT_0cf8,X
026b	b7 54	STA	BYTE_0054
026d	b6 14	LDA	RAM_0014
026f	44	LSRA	
0270	44	LSRA	
0271	a4 07	AND	#0x7
0273	ab 10	ADD	#0x10
0275	97	TAX	
0276	d6 0c f8	LDA	DAT_0cf8,X
0279	b7 53	STA	BYTE_0053
027b	b6 14	LDA	RAM_0014
027d	48	ASLA	
027e	49	ROLA	
027f	49	ROLA	
0280	49	ROLA	
0281	a4 07	AND	#0x7
0283	ab 10	ADD	#0x10
0285	97	TAX	
0286	d6 0c f8	LDA	DAT_0cf8,X
0289	b7 52	STA	BYTE_0052
028b	5f	CLR	
028c	a6 77	LDA	#0x77
	LAB_028e		XREF[1]: 0299(j)
028e	e1 52	CMP	0x52,X
0290	26 09	BNE	LAB_029b
0292	6f 52	CLR	0x52,X

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```

0294 5c          INCX
0295 a3 07      CPX      #0x7
0297 27 02      BEQ      LAB_029b
0299 20 f3      BRA      LAB_028e

LAB_029b
029b 08 1b 01   BRSET    0x4,RAM_001b,LAB_029f
029e 81         RTS

LAB_029f
029f a6 4f      LDA      #0x4f
02a1 b7 52      STA      BYTE_0052
02a3 a6 66      LDA      #0x66
02a5 b7 53      STA      BYTE_0053
02a7 1e 55      BSET     0x7,BYTE_0055
02a9 81         RTS

LAB_02aa
02aa b6 16      LDA      RAM_0016
02ac b7 5a      STA      PortC_SavedValue
02ae ae 03      LDX      #0x3
02b0 bf 51      STX      RAM_0051

LAB_02b2
02b2 b6 5a      LDA      PortC_SavedValue
02b4 a4 03      AND      #0x3
02b6 ab 04      ADD      #0x4
02b8 97         TAX
02b9 d6 0c f8   LDA      DAT_0cf8,X
02bc be 51      LDX      RAM_0051
02be e7 56      STA      0x56,X=>BYTE_0059
02c0 34 5a      LSR      PortC_SavedValue
02c2 34 5a      LSR      PortC_SavedValue
02c4 3a 51      DEC      RAM_0051
02c6 2a ea      BPL      LAB_02b2
02c8 b6 15      LDA      RAM_0015
02ca b7 5a      STA      PortC_SavedValue
02cc ae 03      LDX      #0x3
02ce bf 51      STX      RAM_0051

LAB_02d0
02d0 b6 5a      LDA      PortC_SavedValue
02d2 a4 03      AND      #0x3
02d4 ab 04      ADD      #0x4
02d6 97         TAX
02d7 d6 0c f8   LDA      DAT_0cf8,X
02da be 51      LDX      RAM_0051
02dc e7 52      STA      0x52,X=>BYTE_0055
02de 34 5a      LSR      PortC_SavedValue
02e0 34 5a      LSR      PortC_SavedValue
02e2 3a 51      DEC      RAM_0051
02e4 2a ea      BPL      LAB_02d0
02e6 81         RTS

LAB_02e7
02e7 ae 07      LDX      #0x7
02e9 bf 4f      STX      BYTE_004f
02eb ae 03      LDX      #0x3
02ed bf 51      STX      RAM_0051

LAB_02ef
02ef ee 22      LDX      0x22,X=>BYTE_0025
02f1 58         ASLX
02f2 5c          INCX
02f3 d6 0e 44   LDA      DAT_0e44,X
02f6 ab 10      ADD      #0x10
02f8 97         TAX
02f9 d6 0c f8   LDA      DAT_0cf8,X
02fc be 4f      LDX      BYTE_004f
02fe e7 52      STA      0x52,X=>BYTE_0059
0300 be 51      LDX      RAM_0051
0302 ee 22      LDX      0x22,X=>BYTE_0025
0304 58         ASLX
0305 d6 0e 44   LDA      DAT_0e44,X
0308 ab 10      ADD      #0x10
030a 97         TAX
030b d6 0c f8   LDA      DAT_0cf8,X
030e 3a 4f      DEC      BYTE_004f
0310 be 4f      LDX      BYTE_004f
0312 e7 52      STA      0x52,X=>BYTE_0058
0314 3a 4f      DEC      BYTE_004f
0316 3a 51      DEC      RAM_0051
0318 be 51      LDX      RAM_0051
031a 2a d3      BPL      LAB_02ef
031c 1e 59      BSET     0x7,BYTE_0059

```

XREF[2]: 0290(j), 0297(j)

XREF[1]: 029b(j)

XREF[1]: 01ff(j)

XREF[1]: 02c6(j)

XREF[1]: 02e4(j)

XREF[1]: 01f3(j)

XREF[1]: 031a(j)

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```

031e 1e 57      BSET      0x7,BYTE_0057
0320 1e 55      BSET      0x7,BYTE_0055
0322 81         RTS

LAB_0323
0323 b6 20      LDA      BYTE_0020
0325 a1 4f      CMP      #0x4f
0327 25 0a      BCS      LAB_0333
0329 ae 11      LDX      #0x11
032b bf 52      STX      BYTE_0052
032d ae 3f      LDX      #0x3f
032f bf 53      STX      BYTE_0053
0331 20 08      BRA      LAB_033b

LAB_0333
0333 ae 6b      LDX      #0x6b
0335 bf 52      STX      BYTE_0052
0337 ae 77      LDX      #0x77
0339 bf 53      STX      BYTE_0053

LAB_033b
033b 97         TAX
033c 58         ASLX
033d d6 0e 44   LDA      DAT_0e44,X
0340 ab 10      ADD      #0x10
0342 97         TAX
0343 d6 0c f8   LDA      DAT_0cf8,X
0346 b7 54      STA      BYTE_0054
0348 be 20      LDX      BYTE_0020
034a 58         ASLX
034b 5c         INCX
034c d6 0e 44   LDA      DAT_0e44,X
034f ab 10      ADD      #0x10
0351 97         TAX
0352 d6 0c f8   LDA      DAT_0cf8,X
0355 b7 55      STA      BYTE_0055
0357 3f 56      CLR      BYTE_0056
0359 a6 80      LDA      #0x80
035b b7 57      STA      BYTE_0057
035d be 21      LDX      BYTE_0021
035f 58         ASLX
0360 d6 0e 44   LDA      DAT_0e44,X
0363 ab 10      ADD      #0x10
0365 97         TAX
0366 d6 0c f8   LDA      DAT_0cf8,X
0369 b7 58      STA      BYTE_0058
036b be 21      LDX      BYTE_0021
036d 58         ASLX
036e 5c         INCX
036f d6 0e 44   LDA      DAT_0e44,X
0372 ab 10      ADD      #0x10
0374 97         TAX
0375 d6 0c f8   LDA      DAT_0cf8,X
0378 b7 59      STA      BYTE_0059
037a 81         RTS

*****
*                               *
*                               *
*****
undefined Something_PortC()
undefined      A:1      <RETURN>
Something_PortC
037b 02 1b 0b   BRSET     0x1,RAM_001b,LAB_0389
037e b6 1d      LDA      RAM_001d
0380 a4 03      AND      #0x3
0382 a1 00      CMP      #0x0
0384 26 03      BNE      LAB_0389
0386 cc 03 8c   JMP      LAB_038c

LAB_0389
0389 cc 04 3c   JMP      LAB_043c

LAB_038c
038c b6 18      LDA      RAM_0018
038e a4 07      AND      #0x7
0390 ab 10      ADD      #0x10
0392 97         TAX
0393 d6 0c f8   LDA      DAT_0cf8,X
0396 b7 59      STA      BYTE_0059
0398 b6 18      LDA      RAM_0018
039a 44         LSRA
039b 44         LSRA
039c 44         LSRA
039d a4 07      AND      #0x7
039f ab 10      ADD      #0x10
XREF[1]:      01f6(j)
XREF[1]:      0327(j)
XREF[1]:      0331(j)
XREF[1]:      RESET:0187(c)
XREF[2]:      037b(j), 0384(j)
XREF[1]:      0386(j)

```

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```

03a1 97          TAX
03a2 d6 0c f8   LDA      DAT_0cf8,X
03a5 b7 58      STA      BYTE_0058
03a7 be 18      LDX      RAM_0018
03a9 b6 17      LDA      RAM_0017
03ab 58         ASLX
03ac 49         ROLA
03ad 58         ASLX
03ae 49         ROLA
03af a4 07      AND      #0x7
03b1 ab 10      ADD      #0x10
03b3 97          TAX
03b4 d6 0c f8   LDA      DAT_0cf8,X
03b7 b7 57      STA      BYTE_0057
03b9 b6 17      LDA      RAM_0017
03bb 44         LSRA
03bc a4 07      AND      #0x7
03be ab 10      ADD      #0x10
03c0 97          TAX
03c1 d6 0c f8   LDA      DAT_0cf8,X
03c4 b7 56      STA      BYTE_0056
03c6 b6 17      LDA      RAM_0017
03c8 44         LSRA
03c9 44         LSRA
03ca 44         LSRA
03cb 44         LSRA
03cc a4 07      AND      #0x7
03ce ab 10      ADD      #0x10
03d0 97          TAX
03d1 d6 0c f8   LDA      DAT_0cf8,X
03d4 b7 55      STA      BYTE_0055
03d6 06 1b 24   BRSET    0x3,RAM_001b,LAB_03fd
03d9 b6 17      LDA      RAM_0017
03db 49         ROLA
03dc 49         ROLA
03dd a4 01      AND      #0x1
03df ab 10      ADD      #0x10
03e1 97          TAX
03e2 d6 0c f8   LDA      DAT_0cf8,X
03e5 b7 54      STA      BYTE_0054
03e7 3f 53      CLR      BYTE_0053
03e9 3f 52      CLR      BYTE_0052
03eb ae 02      LDX      #0x2
03ed a6 77      LDA      #0x77

LAB_03ef
03ef e1 52      CMP      0x52,X=>BYTE_0054
03f1 26 09      BNE      LAB_03fc
03f3 6f 52      CLR      0x52,X=>BYTE_0054
03f5 5c         INCX
03f6 a3 07      CPX      #0x7
03f8 27 02      BEQ      LAB_03fc
03fa 20 f3      BRA      LAB_03ef

LAB_03fc
03fc 81         RTS

LAB_03fd
03fd be 17      LDX      RAM_0017
03ff b6 16      LDA      RAM_0016
0401 58         ASLX
0402 49         ROLA
0403 a4 07      AND      #0x7
0405 ab 10      ADD      #0x10
0407 97          TAX
0408 d6 0c f8   LDA      DAT_0cf8,X
040b b7 54      STA      BYTE_0054
040d b6 16      LDA      RAM_0016
040f 44         LSRA
0410 44         LSRA
0411 a4 07      AND      #0x7
0413 ab 10      ADD      #0x10
0415 97          TAX
0416 d6 0c f8   LDA      DAT_0cf8,X
0419 b7 53      STA      BYTE_0053
041b b6 16      LDA      RAM_0016
041d 49         ROLA
041e 49         ROLA
041f 49         ROLA
0420 49         ROLA
0421 a4 07      AND      #0x7
0423 ab 10      ADD      #0x10
0425 97          TAX
0426 d6 0c f8   LDA      DAT_0cf8,X
0429 b7 52      STA      BYTE_0052

XREF[1]:      03fa(j)

XREF[2]:      03f1(j), 03f8(j)

XREF[1]:      03d6(j)

```

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```

042b 5f          CLRX
042c a6 77       LDA      #0x77

                                LAB_042e
                                XREF[1]: 0439(j)
042e e1 52       CMP      0x52,X
0430 26 09       BNE      LAB_043b
0432 6f 52       CLR      0x52,X
0434 5c          INCX
0435 a3 07       CPX      #0x7
0437 27 02       BEQ      LAB_043b
0439 20 f3       BRA      LAB_042e

                                LAB_043b
                                XREF[2]: 0430(j), 0437(j)
043b 81          RTS

                                LAB_043c
                                XREF[1]: 0389(j)
043c b6 18       LDA      RAM_0018
043e b7 5a       STA      PortC_SavedValue
0440 ae 03       LDX      #0x3
0442 bf 51       STX      RAM_0051

                                LAB_0444
                                XREF[1]: 0458(j)
0444 b6 5a       LDA      PortC_SavedValue
0446 a4 03       AND      #0x3
0448 ab 04       ADD      #0x4
044a 97          TAX
044b d6 0c f8    LDA      DAT_0cf8,X
044e be 51       LDX      RAM_0051
0450 e7 56       STA      0x56,X=>BYTE_0059
0452 34 5a       LSR      PortC_SavedValue
0454 34 5a       LSR      PortC_SavedValue
0456 3a 51       DEC      RAM_0051
0458 2a ea       BPL      LAB_0444
045a b6 17       LDA      RAM_0017
045c b7 5a       STA      PortC_SavedValue
045e ae 03       LDX      #0x3
0460 bf 51       STX      RAM_0051

                                LAB_0462
                                XREF[1]: 0476(j)
0462 b6 5a       LDA      PortC_SavedValue
0464 a4 03       AND      #0x3
0466 ab 04       ADD      #0x4
0468 97          TAX
0469 d6 0c f8    LDA      DAT_0cf8,X
046c be 51       LDX      RAM_0051
046e e7 52       STA      0x52,X=>BYTE_0055
0470 34 5a       LSR      PortC_SavedValue
0472 34 5a       LSR      PortC_SavedValue
0474 3a 51       DEC      RAM_0051
0476 2a ea       BPL      LAB_0462
0478 81          RTS

*****
*                               *
*                               FUNCTION                               *
*                               *
*****
undefined Something_RAM_050_051()
A:1      <RETURN>
Something_RAM_050_051
                                XREF[3]: RESET:0176(c), RESET:0184(c),
                                RESET:0192(c)
0479 a6 1f       LDA      #0x1f
047b b7 4f       STA      BYTE_004f
047d ae 03       LDX      #0x3
047f bf 51       STX      RAM_0051

                                LAB_0481
                                XREF[1]: 04a4(j)
0481 a6 07       LDA      #0x7
0483 b7 50       STA      BYTE_0050

                                LAB_0485
                                XREF[1]: 049e(j)
0485 4f          CLRA
0486 64 56       LSR      0x56,X=>BYTE_0059
0488 24 02       BCC      LAB_048c
048a ba 4b       ORA      BYTE_004b

                                LAB_048c
                                XREF[1]: 0488(j)
048c 64 52       LSR      0x52,X=>BYTE_0055
048e 24 02       BCC      LAB_0492
0490 ba 4c       ORA      BYTE_004c

                                LAB_0492
                                XREF[1]: 048e(j)
0492 be 4f       LDX      BYTE_004f
0494 3a 4f       DEC      BYTE_004f
0496 ea 27       ORA      0x27,X=>PortC_ValueToWrite
0498 e7 27       STA      0x27,X=>PortC_ValueToWrite
049a be 51       LDX      RAM_0051

```

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```

049c 3a 50      DEC      BYTE_0050
049e 2a e5      BPL      LAB_0485
04a0 3a 51      DEC      RAM_0051
04a2 be 51      LDX      RAM_0051
04a4 2a db      BPL      LAB_0481
04a6 81        RTS

*****
*                               *
*                               *
*****

void Read_Write_Port_C(void)
<VOID>      <RETURN>

Read_Write_Port_C                                XREF[1]:  RESET:019e(c)
04a7 b6 02      LDA      PORTC
04a9 b7 5a      STA      PortC_SavedValue
04ab b6 46      LDA      PortC_ValueToWrite
04ad 97        TAX
04ae aa 80      ORA      #0x80
04b0 bf 02      STX      PORTC
04b2 b7 02      STA      PORTC
04b4 b6 45      LDA      BYTE_0045
04b6 b7 02      STA      PORTC
04b8 1e 02      BSET     0x7,PORTC
04ba ae 1d      LDX      #0x1d

LAB_04bc                                XREF[1]:  04c3(j)
04bc e6 27      LDA      0x27,X=>BYTE_0044
04be b7 02      STA      PORTC
04c0 1e 02      BSET     0x7,PORTC
04c2 5a        DECC
04c3 2a f7      BPL      LAB_04bc
04c5 a6 1f      LDA      #0x1f

LAB_04c7                                XREF[1]:  04d1(j)
04c7 97        TAX
04c8 ee 27      LDX      0x27,X=>PortC_ValueToWrite
04ca ee 86      LDX      0x86,X
04cc bf 02      STX      PORTC
04ce 1e 02      BSET     0x7,PORTC
04d0 4a        DECA
04d1 2a f4      BPL      LAB_04c7
04d3 b6 5a      LDA      PortC_SavedValue
04d5 b7 02      STA      PORTC
04d7 81        RTS

*****
*                               *
*                               *
*****

undefined Read_Bytes_from_Port_A()
A:1      <RETURN>

Read_Bytes_from_Port_A                        XREF[1]:  RESET:0161(c)
04d8 cd 09 bc   JSR      Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
04db b7 1c      STA      RAM_001c
04dd 06 1c 03   BRSET    0x3,RAM_001c,LAB_04e3
04e0 cc 06 be   JMP      Output_Current_Date_Port_A_Maybe    undefinedOutput_Current_Date_Po...
-- Flow Override: CALL_RETURN (CALL_TERMINATOR)

LAB_04e3                                XREF[1]:  04dd(j)
04e3 b6 1c      LDA      RAM_001c
04e5 a4 07      AND      #0x7
04e7 48        ASLA
04e8 48        ASLA
04e9 97        TAX

switchD_04ea::switchD
04ea dc 04 fc   JMP      0x4fc,X

LAB_04ed                                XREF[10]:  055a(j), 0563(j), 0572(j),
                                                0591(j), 05c0(j), 05dc(j),
                                                0605(j), 060d(j), 0624(j),
                                                0668(j)
04ed 01 1d 03   BRCLR    0x0,RAM_001d,LAB_04f3
04f0 cd 06 6b   JSR      Something_Ram_17_18      undefinedSomething_Ram_17_18()

LAB_04f3                                XREF[1]:  04ed(j)
04f3 5f        CLRX
04f4 cd 06 94   JSR      SomeLogic_From_RAM_001D_store_0052_via_X    undefinedSomeLogic_From_RAM_001...
04f7 5c        INCX
04f8 cd 06 94   JSR      SomeLogic_From_RAM_001D_store_0052_via_X    undefinedSomeLogic_From_RAM_001...
04fb 81        RTS

switchD_04ea::caseD_0                    XREF[1]:  04ea(j)
04fc cc 05 1b   JMP      LAB_051b
04ff 9d        ??      9Dh

```

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```

switchD_04ea::caseD_1
0500 cc 05 75      JMP      LAB_0575
0503 9d           ??      9Dh

switchD_04ea::caseD_2
0504 cc 05 94      JMP      LAB_0594
0507 9d           ??      9Dh

switchD_04ea::caseD_3
0508 cc 05 c3      JMP      LAB_05c3
050b 9d           ??      9Dh

switchD_04ea::caseD_4
050c cc 05 df      JMP      LAB_05df
050f 9d           ??      9Dh

switchD_04ea::caseD_5
0510 cc 06 08      JMP      LAB_0608
0513 9d           ??      9Dh

switchD_04ea::caseD_6
0514 cc 06 10      JMP      LAB_0610
0517 9d           ??      9Dh

switchD_04ea::caseD_7
0518 cc 06 27      JMP      LAB_0627

LAB_051b
051b cd 09 bc      JSR      Clock_PB3_RMM_Return_Port_A
051e b7 14         STA      RAM_0014
0520 cd 09 bc      JSR      Clock_PB3_RMM_Return_Port_A
0523 b7 16         STA      RAM_0016
0525 cd 09 bc      JSR      Clock_PB3_RMM_Return_Port_A
0528 b7 15         STA      RAM_0015
052a cd 09 bc      JSR      Clock_PB3_RMM_Return_Port_A
052d b7 18         STA      RAM_0018
052f cd 09 bc      JSR      Clock_PB3_RMM_Return_Port_A
0532 b7 17         STA      RAM_0017
0534 13 1b         BCLR     0x1,RAM_001b
0536 17 1b         BCLR     0x3,RAM_001b
0538 19 1b         BCLR     0x4,RAM_001b
053a ae 50         LDX      #0x50
053c bf 10         STX      RAM_0010
053e 05 1a 25      BRCLR    0x2,RAM_001a,LAB_0566
0541 ae 54         LDX      #0x54
0543 bf 11         STX      RAM_0011
0545 b6 1a         LDA      RAM_001a
0547 a4 18         AND      #0x18
0549 44           LSRA
054a b7 52         STA      BYTE_0052
054c b6 1a         LDA      RAM_001a
054e a4 03         AND      #0x3
0550 ba 52         ORA      BYTE_0052
0552 a1 08         CMP      #0x8
0554 25 07         BCS      LAB_055d
0556 b7 13         STA      RAM_0013
0558 3f 12         CLR      RAM_0012
055a cc 04 ed      JMP      LAB_04ed

LAB_055d
055d ab 30         ADD      #0x30
055f b7 13         STA      RAM_0013
0561 3f 12         CLR      RAM_0012
0563 cc 04 ed      JMP      LAB_04ed

LAB_0566
0566 ae 45         LDX      #0x45
0568 bf 11         STX      RAM_0011
056a ae 58         LDX      #0x58
056c bf 12         STX      RAM_0012
056e ae 4d         LDX      #0x4d
0570 bf 13         STX      RAM_0013
0572 cc 04 ed      JMP      LAB_04ed

LAB_0575
0575 cd 09 bc      JSR      Clock_PB3_RMM_Return_Port_A
0578 b7 18         STA      RAM_0018
057a cd 09 bc      JSR      Clock_PB3_RMM_Return_Port_A
057d b7 17         STA      RAM_0017
057f cd 09 bc      JSR      Clock_PB3_RMM_Return_Port_A
0582 b7 16         STA      RAM_0016
0584 cd 09 bc      JSR      Clock_PB3_RMM_Return_Port_A
0587 b7 15         STA      RAM_0015
0589 3f 14         CLR      RAM_0014

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```

058b 18 1b      BSET      0x4,RAM_001b
058d 13 1b      BCLR      0x1,RAM_001b
058f 17 1b      BCLR      0x3,RAM_001b
0591 cc 04 ed    JMP       LAB_04ed

LAB_0594
0594 cd 09 bc    JSR       Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
0597 b7 18      STA       RAM_0018
0599 cd 09 bc    JSR       Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
059c b7 17      STA       RAM_0017
059e 12 1b      BSET      0x1,RAM_001b
05a0 19 1b      BCLR      0x4,RAM_001b
05a2 17 1b      BCLR      0x3,RAM_001b
05a4 a6 10      LDA       #0x10
05a6 b7 1d      STA       RAM_001d
05a8 a6 00      LDA       #0x0
05aa b7 1e      STA       RAM_001e
05ac b6 19      LDA       PortD_PONI_IONI_bit_4_5_Ring_3_0
05ae a4 0f      AND       #0xf
05b0 ab 10      ADD       #0x10
05b2 b7 12      STA       RAM_0012
05b4 b6 19      LDA       PortD_PONI_IONI_bit_4_5_Ring_3_0
05b6 a4 30      AND       #0x30
05b8 44         LSRA
05b9 44         LSRA
05ba 44         LSRA
05bb 44         LSRA
05bc ab 3a      ADD       #0x3a
05be b7 13      STA       RAM_0013
05c0 cc 04 ed    JMP       LAB_04ed

LAB_05c3
05c3 16 1b      BSET      0x3,RAM_001b
05c5 13 1b      BCLR      0x1,RAM_001b
05c7 19 1b      BCLR      0x4,RAM_001b
05c9 cd 09 bc    JSR       Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
05cc b7 16      STA       RAM_0016
05ce 3f 15      CLR       RAM_0015
05d0 3f 14      CLR       RAM_0014
05d2 cd 09 bc    JSR       Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
05d5 b7 18      STA       RAM_0018
05d7 cd 09 bc    JSR       Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
05da b7 17      STA       RAM_0017
05dc cc 04 ed    JMP       LAB_04ed

LAB_05df
05df cd 09 bc    JSR       Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
05e2 b7 52      STA       BYTE_0052
05e4 a4 03      AND       #0x3
05e6 48         ASLA
05e7 97         TAX
05e8 d6 0d 12    LDA       DAT_0d12,X      = 3Ah      :
05eb b7 13      STA       RAM_0013
05ed 5c         INCX
05ee d6 0d 12    LDA       DAT_0d12,X      = 3Ah      :
05f1 b7 12      STA       RAM_0012
05f3 b6 52      LDA       BYTE_0052
05f5 a4 18      AND       #0x18
05f7 44         LSRA
05f8 44         LSRA
05f9 97         TAX
05fa d6 0d 1a    LDA       DAT_0d1a,X      = 43h      C
05fd b7 11      STA       RAM_0011
05ff 5c         INCX
0600 d6 0d 1a    LDA       DAT_0d1a,X      = 43h      C
0603 b7 10      STA       RAM_0010
0605 cc 04 ed    JMP       LAB_04ed

LAB_0608
0608 cd 09 bc    JSR       Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
060b b7 1a      STA       RAM_001a
060d cc 04 ed    JMP       LAB_04ed

LAB_0610
0610 cd 09 bc    JSR       Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
0613 b7 11      STA       RAM_0011
0615 cd 09 bc    JSR       Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
0618 b7 10      STA       RAM_0010
061a cd 09 bc    JSR       Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
061d b7 13      STA       RAM_0013
061f cd 09 bc    JSR       Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
0622 b7 12      STA       RAM_0012
0624 cc 04 ed    JMP       LAB_04ed

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LAB_0627
0627 cd 09 bc JSR      Clock_PB3_RMM_Return_Port_A      XREF[1]: 0518(j)
062a b7 1d STA      RAM_001d      undefinedClock_PB3_RMM_Return_P...
062c cd 09 bc JSR      Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
062f b7 1e STA      RAM_001e
0631 a4 f0 AND      #0xf0
0633 a1 40 CMP      #0x40
0635 26 15 BNE      LAB_064c
0637 a6 40 LDA      #0x40
0639 b7 0a STA      MR_Misc_register
063b a6 47 LDA      #0x47
063d b7 09 STA      TCR_Timer_Control_Register
063f a6 01 LDA      #0x1
0641 b7 0b STA      PCR_Program_Control_Register
0643 3f 04 CLR      DDRA
0645 3f 05 CLR      DDRB
0647 3f 06 CLR      DDRC
0649 cc 01 10 JMP      RESET      undefined RESET()
-- Flow Override: CALL_RETURN (CALL_TERMINATOR)

LAB_064c
064c 15 1b BCLR     0x2,RAM_001b      XREF[1]: 0635(j)
064e a1 10 CMP      #0x10
0650 26 02 BNE      LAB_0654
0652 14 1b BSET     0x2,RAM_001b

LAB_0654
0654 b6 1d LDA      RAM_001d      XREF[1]: 0650(j)
0656 48 ASLA
0657 39 1e ROL      RAM_001e
0659 48 ASLA
065a 39 1e ROL      RAM_001e
065c b6 1e LDA      RAM_001e
065e a4 3f AND      #0x3f
0660 b7 1e STA      RAM_001e
0662 b6 1d LDA      RAM_001d
0664 a4 3f AND      #0x3f
0666 b7 1d STA      RAM_001d
0668 cc 04 ed JMP      LAB_04ed

*****
* FUNCTION *
*****
undefined Something_Ram_17_18()
A:1 <RETURN>
Something_Ram_17_18      XREF[1]: Read_Bytes_from_Port_A:04f0(c)
066b 3f 52 CLR      BYTE_0052
066d 07 1b 04 BRCLR   0x3,RAM_001b,LAB_0674
0670 b6 16 LDA      RAM_0016
0672 b7 52 STA      BYTE_0052

LAB_0674
0674 be 1e LDX      RAM_001e      XREF[1]: 066d(j)
0676 5d TSTX
0677 27 09 BEQ      LAB_0682

LAB_0679
0679 34 52 LSR      BYTE_0052      XREF[1]: 0680(j)
067b 36 17 ROR      RAM_0017
067d 36 18 ROR      RAM_0018
067f 5a DECX
0680 26 f7 BNE      LAB_0679

LAB_0682
0682 b6 18 LDA      RAM_0018      XREF[1]: 0677(j)
0684 a4 0f AND      #0xf
0686 97 TAX
0687 3f 17 CLR      RAM_0017
0689 3f 18 CLR      RAM_0018
068b 99 SEC

LAB_068c
068c 39 18 ROL      RAM_0018      XREF[1]: 0691(j)
068e 39 17 ROL      RAM_0017
0690 5a DECX
0691 2a f9 BPL      LAB_068c
0693 81 RTS

```

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```

*****
*                               *
*****
undefined SomeLogic_From_RAM_001D_store_0052_via_X)
A:1      <RETURN>
SomeLogic_From_RAM_001D_store_0052_via_X      XREF[2]:      Read_Bytes_from_Port_A:04f4(c),
                                                    Read_Bytes_from_Port_A:04f8(c)

0694 4f      CLRA
0695 09 1d 05  BRCLR      0x4,RAM_001d,LAB_069d
0698 e6 6d      LDA      0x6d,X
069a 43      COMA
069b e4 5e      AND      0x5e,X

LAB_069d                                XREF[1]:      0695(j)
069d b7 52      STA      BYTE_0052
069f e6 17      LDA      0x17,X
06a1 07 1d 07  BRCLR      0x3,RAM_001d,LAB_06ab
06a4 e6 6d      LDA      0x6d,X
06a6 43      COMA
06a7 ea 5e      ORA      0x5e,X
06a9 e4 17      AND      0x17,X

LAB_06ab                                XREF[1]:      06a1(j)
06ab ba 52      ORA      BYTE_0052
06ad e7 5e      STA      0x5e,X
06af e7 17      STA      0x17,X
06b1 81      RTS

*****
*                               *
*****
undefined PortD_Update_PONI_IONi_bits()
A:1      <RETURN>
PortD_Update_PONI_IONi_bits      XREF[1]:      TIMER_INTERRUPT:08d1(c)
06b2 b6 6f      LDA      BYTE_006f
06b4 43      COMA
06b5 b4 60      AND      BYTE_0060
06b7 ba 19      ORA      PortD_PONI_IONi_bit_4_5_Ring_3_0
06b9 b7 60      STA      BYTE_0060
06bb b7 19      STA      PortD_PONI_IONi_bit_4_5_Ring_3_0
06bd 81      RTS

*****
*                               *
*****
undefined Output_Current_Date_Port_A_Maybe()
A:1      <RETURN>
Output_Current_Date_Port_A_Maybe      XREF[1]:      Read_Bytes_from_Port_A:04e0(c)
06be be 1c      LDX      RAM_001c
06c0 9f      TXA
06c1 a4 07      AND      #0x7
06c3 b7 1c      STA      RAM_001c
06c5 b6 02      LDA      PORTC
06c7 a4 f8      AND      #0xf8
06c9 ba 1c      ORA      RAM_001c
06cb b7 02      STA      PORTC
06cd 9f      TXA
06ce a4 04      AND      #0x4
06d0 26 01      BNE      LAB_06d3
06d2 81      RTS

LAB_06d3                                XREF[1]:      06d0(j)
06d3 1b 01      BCLR      0x5,PORTB
06d5 9f      TXA
06d6 a4 03      AND      #0x3
06d8 a8 03      EOR      #0x3
06da b7 1c      STA      RAM_001c
06dc 9f      TXA
06dd a4 20      AND      #0x20
06df 26 19      BNE      LAB_06fa
06e1 1d 01      BCLR      0x6,PORTB
06e3 cd 09 bc  JSR      Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
06e6 be 1c      LDX      RAM_001c
06e8 e7 47      STA      0x47,X
06ea cd 09 c5  JSR      Write_RegA_To_PortA_And_Latch_to_IDB      undefinedWrite_RegA_To_PortA_An...
06ed 1a 01      BSET      0x5,PORTB
06ef a3 00      CPX      #0x0
06f1 26 06      BNE      LAB_06f9
06f3 cd 07 15  JSR      CopyData_In_Ram_Dest_0x46_0x4e      undefinedCopyData_In_Ram_Dest_0...
06f6 cd 09 ee  JSR      WriteDateBytesToPortA_LatchToIDB_7_0      undefinedWriteDateBytesToPortA_...

LAB_06f9                                XREF[1]:      06f1(j)
06f9 81      RTS

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LAB_06fa                                XREF[1]: 06df(j)
06fa 1c 01      BSET      0x6,PORTB
06fc cd 09 bc    JSR      Clock_PB3_RMM_Return_Port_A      undefinedClock_PB3_RMM_Return_P...
06ff be 1c      LDX      RAM_001c
0701 a3 03      CPX      #0x3
0703 26 06      BNE      LAB_070b
0705 cd 0a c0    JSR      RTC_Initialize_Maybe      undefinedRTC_Initialize_Maybe()
0708 cd 08 03    JSR      Calc_Something_Dest_0x48_0x4f      undefinedCalc_Something_Dest_0x...

LAB_070b                                XREF[1]: 0703(j)
070b be 1c      LDX      RAM_001c
070d e6 47      LDA      0x47,X
070f cd 09 c5    JSR      Write_RegA_To_PortA_And_Latch_to_IDB      undefinedWrite_RegA_To_PortA_An...
0712 1a 01      BSET      0x5,PORTB
0714 81          RTS

*****
*                               *
*                               *
*****
undefined CopyData_In_Ram_Dest_0x46_0x4d)
A:1      <RETURN>
CopyData_In_Ram_Dest_0x46_0x4e      XREF[1]: Output_Current_Date_Port_A_Mayb...
0715 ae 05      LDX      #0x5

LAB_0717                                XREF[1]: 071a(j)
0717 6f 20      CLR      0x20,X=>BYTE_0025
0719 5a          DECKX
071a 2a fb      BPL      LAB_0717
071c b6 80      LDA      BYTE_0080      = 2h
071e b7 4b      STA      BYTE_004b
0720 b6 81      LDA      BYTE_0081      = DAh
0722 b7 4c      STA      BYTE_004c
0724 a6 03      LDA      #0x3
0726 b7 26      STA      BYTE_0026
0728 b6 47      LDA      BYTE_0047
072a b7 4d      STA      BYTE_004d
072c b6 48      LDA      BYTE_0048
072e b7 4e      STA      BYTE_004e

LAB_0730                                XREF[1]: 0757(j)
0730 b6 4d      LDA      BYTE_004d
0732 b7 52      STA      BYTE_0052
0734 b6 4e      LDA      BYTE_004e
0736 b7 53      STA      BYTE_0053
0738 b6 4e      LDA      BYTE_004e
073a b0 4c      SUB      BYTE_004c
073c b7 4e      STA      BYTE_004e
073e b6 4d      LDA      BYTE_004d
0740 b2 4b      SBC      BYTE_004b
0742 b7 4d      STA      BYTE_004d
0744 a6 da      LDA      #0xda
0746 b7 4c      STA      BYTE_004c
0748 25 0f      BCS      LAB_0759
074a 3c 20      INC      BYTE_0020
074c 3c 26      INC      BYTE_0026
074e 05 26 06    BRCLR   0x2,BYTE_0026,LAB_0757
0751 3c 4c      INC      BYTE_004c
0753 3c 4c      INC      BYTE_004c
0755 3f 26      CLR      BYTE_0026

LAB_0757                                XREF[1]: 074e(j)
0757 20 d7      BRA      LAB_0730

LAB_0759                                XREF[1]: 0748(j)
0759 b6 52      LDA      BYTE_0052
075b b7 4d      STA      BYTE_004d
075d b6 53      LDA      BYTE_0053
075f b7 4e      STA      BYTE_004e
0761 b6 20      LDA      BYTE_0020
0763 ab 4f      ADD      #0x4f
0765 b7 20      STA      BYTE_0020
0767 3c 21      INC      BYTE_0021
0769 3f 4b      CLR      BYTE_004b
076b a6 3e      LDA      #0x3e
076d b7 4c      STA      BYTE_004c

LAB_076f                                XREF[1]: 0798(j)
076f b6 4d      LDA      BYTE_004d
0771 b7 52      STA      BYTE_0052
0773 b6 4e      LDA      BYTE_004e
0775 b7 53      STA      BYTE_0053
0777 b6 4e      LDA      BYTE_004e
0779 b0 4c      SUB      BYTE_004c
077b b7 4e      STA      BYTE_004e

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077d b6 4d	LDA	BYTE_004d	
077f b2 4b	SBC	BYTE_004b	
0781 b7 4d	STA	BYTE_004d	
0783 25 15	BCS	LAB_079a	
0785 3c 21	INC	BYTE_0021	
0787 be 21	LDX	BYTE_0021	
0789 d6 0d de	LDA	DAT_0dde,X	
078c a3 02	CPX	#0x2	
078e 26 06	BNE	LAB_0796	
0790 3d 26	TST	BYTE_0026	
0792 26 02	BNE	LAB_0796	
0794 ab 02	ADD	#0x2	
	LAB_0796		XREF[2]: 078e(j), 0792(j)
0796 b7 4c	STA	BYTE_004c	
0798 20 d5	BRA	LAB_076f	
	LAB_079a		XREF[1]: 0783(j)
079a b6 52	LDA	BYTE_0052	
079c b7 4d	STA	BYTE_004d	
079e b6 53	LDA	BYTE_0053	
07a0 b7 4e	STA	BYTE_004e	
07a2 44	LSRA		
07a3 24 04	BCC	LAB_07a9	
07a5 ae 0c	LDX	#0xc	
07a7 bf 23	STX	BYTE_0023	
	LAB_07a9		XREF[1]: 07a3(j)
07a9 4c	INCA		
07aa b7 22	STA	BYTE_0022	
07ac b6 49	LDA	BYTE_0049	
07ae b7 4d	STA	BYTE_004d	
07b0 b6 4a	LDA	BYTE_004a	
07b2 b7 4e	STA	BYTE_004e	
07b4 b6 82	LDA	BYTE_0082	= Eh
07b6 b7 4b	STA	BYTE_004b	
07b8 b6 83	LDA	BYTE_0083	= 10h
07ba b7 4c	STA	BYTE_004c	
	LAB_07bc		XREF[1]: 07d4(j)
07bc b6 4d	LDA	BYTE_004d	
07be b7 52	STA	BYTE_0052	
07c0 b6 4e	LDA	BYTE_004e	
07c2 b7 53	STA	BYTE_0053	
07c4 b6 4e	LDA	BYTE_004e	
07c6 b0 4c	SUB	BYTE_004c	
07c8 b7 4e	STA	BYTE_004e	
07ca b6 4d	LDA	BYTE_004d	
07cc b2 4b	SBC	BYTE_004b	
07ce b7 4d	STA	BYTE_004d	
07d0 25 04	BCS	LAB_07d6	
07d2 3c 23	INC	BYTE_0023	
07d4 20 e6	BRA	LAB_07bc	
	LAB_07d6		XREF[1]: 07d0(j)
07d6 b6 52	LDA	BYTE_0052	
07d8 b7 4d	STA	BYTE_004d	
07da b6 53	LDA	BYTE_0053	
07dc b7 4e	STA	BYTE_004e	
07de 3f 4b	CLR	BYTE_004b	
07e0 a6 3c	LDA	#0x3c	
07e2 b7 4c	STA	BYTE_004c	
	LAB_07e4		XREF[1]: 07fc(j)
07e4 b6 4d	LDA	BYTE_004d	
07e6 b7 52	STA	BYTE_0052	
07e8 b6 4e	LDA	BYTE_004e	
07ea b7 53	STA	BYTE_0053	
07ec b6 4e	LDA	BYTE_004e	
07ee b0 4c	SUB	BYTE_004c	
07f0 b7 4e	STA	BYTE_004e	
07f2 b6 4d	LDA	BYTE_004d	
07f4 b2 4b	SBC	BYTE_004b	
07f6 b7 4d	STA	BYTE_004d	
07f8 25 04	BCS	LAB_07fe	
07fa 3c 24	INC	BYTE_0024	
07fc 20 e6	BRA	LAB_07e4	
	LAB_07fe		XREF[1]: 07f8(j)
07fe b6 53	LDA	BYTE_0053	
0800 b7 25	STA	BYTE_0025	
0802 81	RTS		

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```

*****
*                               *
*****
undefined Calc_Something_Dest_0x48_0x4f)
A:1      <RETURN>
Calc_Something_Dest_0x48_0x4f      XREF[1]:      Output_Current_Date_Port_A_Mayba.

0803 b6 20      LDA      BYTE_0020
0805 a0 4f      SUB      #0x4f
0807 b7 20      STA      BYTE_0020
0809 3f 4d      CLR      BYTE_004d
080b 3f 4e      CLR      BYTE_004e
080d 3f 4f      CLR      BYTE_004f
080f a6 03      LDA      #0x3
0811 b7 26      STA      BYTE_0026
0813 b6 80      LDA      BYTE_0080      = 2h
0815 b7 4b      STA      BYTE_004b
0817 b6 81      LDA      BYTE_0081      = DAh
0819 b7 4c      STA      BYTE_004c

LAB_081b      XREF[1]:      083e(j)
081b 3c 4f      INC      BYTE_004f
081d b6 4f      LDA      BYTE_004f
081f b1 20      CMP      BYTE_0020
0821 22 1d      BHI      LAB_0840
0823 b6 4e      LDA      BYTE_004e
0825 bb 4c      ADD      BYTE_004c
0827 b7 4e      STA      BYTE_004e
0829 b6 4d      LDA      BYTE_004d
082b b9 4b      ADC      BYTE_004b
082d b7 4d      STA      BYTE_004d
082f a6 da      LDA      #0xda
0831 b7 4c      STA      BYTE_004c
0833 3c 26      INC      BYTE_0026
0835 05 26 06   BRCLR    0x2,BYTE_0026,LAB_083e
0838 3c 4c      INC      BYTE_004c
083a 3c 4c      INC      BYTE_004c
083c 3f 26      CLR      BYTE_0026

LAB_083e      XREF[1]:      0835(j)
083e 20 db      BRA      LAB_081b

LAB_0840      XREF[1]:      0821(j)
0840 b6 21      LDA      BYTE_0021
0842 3d 26      TST      BYTE_0026
0844 26 02      BNE      LAB_0848
0846 ab 0d      ADD      #0xd

LAB_0848      XREF[1]:      0844(j)
0848 48      ASLA
0849 97      TAX
084a 5c      INCX
084b d6 0d eb   LDA      DAT_0deb,X
084e bb 4e      ADD      BYTE_004e
0850 b7 4e      STA      BYTE_004e
0852 5a      DECX
0853 d6 0d eb   LDA      DAT_0deb,X
0856 b9 4d      ADC      BYTE_004d
0858 b7 4d      STA      BYTE_004d
085a b6 22      LDA      BYTE_0022
085c 4a      DECA
085d 48      ASLA
085e bb 4e      ADD      BYTE_004e
0860 b7 4e      STA      BYTE_004e
0862 24 02      BCC      LAB_0866
0864 3c 4d      INC      BYTE_004d

LAB_0866      XREF[1]:      0862(j)
0866 b6 4d      LDA      BYTE_004d
0868 b7 47      STA      BYTE_0047
086a b6 4e      LDA      BYTE_004e
086c b7 48      STA      BYTE_0048
086e b6 23      LDA      BYTE_0023
0870 a1 0c      CMP      #0xc
0872 25 0a      BCS      LAB_087e
0874 a0 0c      SUB      #0xc
0876 3c 48      INC      BYTE_0048
0878 3d 48      TST      BYTE_0048
087a 26 02      BNE      LAB_087e
087c 3c 47      INC      BYTE_0047

LAB_087e      XREF[2]:      0872(j), 087a(j)
087e 48      ASLA
087f 97      TAX
0880 5c      INCX

```

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```

0881 d6 0e 1f    LDA    DAT_0e1f,X
0884 b7 4e      STA    BYTE_004e
0886 5a         DECX
0887 d6 0e 1f    LDA    DAT_0e1f,X
088a b7 4d      STA    BYTE_004d
088c ae 05      LDX    #0x5
088e 3f 4b      CLR    BYTE_004b
0890 a6 3c      LDA    #0x3c
0892 b7 4c      STA    BYTE_004c
0894 b6 24      LDA    BYTE_0024
0896 b7 52      STA    BYTE_0052

LAB_0898
0898 34 52      LSR    BYTE_0052                XREF[1]: 08ad(j)
089a 24 0c      BCC    LAB_08a8
089c b6 4e      LDA    BYTE_004e
089e bb 4c      ADD    BYTE_004c
08a0 b7 4e      STA    BYTE_004e
08a2 b6 4d      LDA    BYTE_004d
08a4 b9 4b      ADC    BYTE_004b
08a6 b7 4d      STA    BYTE_004d

LAB_08a8
08a8 38 4c      ASL    BYTE_004c                XREF[1]: 089a(j)
08aa 39 4b      ROL    BYTE_004b
08ac 5a         DECX
08ad 2a e9      BPL    LAB_0898
08af b6 25      LDA    BYTE_0025
08b1 bb 4e      ADD    BYTE_004e
08b3 b7 4e      STA    BYTE_004e
08b5 24 02      BCC    LAB_08b9
08b7 3c 4d      INC    BYTE_004d

LAB_08b9
08b9 b6 4d      LDA    BYTE_004d                XREF[1]: 08b5(j)
08bb b7 49      STA    BYTE_0049
08bd b6 4e      LDA    BYTE_004e
08bf b7 4a      STA    BYTE_004a
08c1 b6 20      LDA    BYTE_0020
08c3 ab 4f      ADD    #0x4f
08c5 b7 20      STA    BYTE_0020
08c7 81         RTS

*****
*                               *
*                               *
*****
undefined TIMER_INTERRUPT()
A:1    <RETURN>
INT2 or TIMER interrupt
TIMER_INTERRUPT                XREF[1]: 0ff8(*)
08c8 a6 03      LDA    #0x3
08ca b7 08      STA    TDR_Timer_Data_Register
08cc 1f 09      BCLR   0x7,TCR_Timer_Control_Register
08ce cd 09 d4    JSR    Read_Port_D_Update_CLR          undefinedRead_Port_D_Update_CLR()
08d1 cd 06 b2    JSR    PortD_Update_PONI_IONI_bits        undefinedPortD_Update_PONI_IONI...
08d4 03 1b 03    BRCLR  0x1,RAM_001b,LAB_08da
08d7 cd 09 85    JSR    Read_Port_D()                    undefinedRead_Port_D()

LAB_08da
08da 3a 5b      DEC     RAM_005b                XREF[1]: 08d4(j)
08dc 26 07      BNE     LAB_08e5
08de cd 09 48    JSR    MoveDataBytes_061_06f          undefinedMoveDataBytes_061_06f()
08e1 a6 10      LDA    #0x10
08e3 b7 5b      STA    RAM_005b

LAB_08e5
08e5 3a 5c      DEC     RAM_005c                XREF[1]: 08dc(j)
08e7 26 0f      BNE     LAB_08f8
08e9 a6 c8      LDA    #0xc8
08eb b7 5c      STA    RAM_005c
08ed 3a 5d      DEC     RAM_005D
08ef 26 07      BNE     LAB_08f8
08f1 a6 02      LDA    #0x2
08f3 b7 5d      STA    RAM_005D
08f5 cd 08 f9    JSR    Something_RAM_20_25          undefinedSomething_RAM_20_25()

LAB_08f8
08f8 80         RTI                XREF[2]: 08e7(j), 08ef(j)

```

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```

*****
*                                     *
*****
undefined Something_RAM_20_25()
A:1      <RETURN>
Something_RAM_20_25                                XREF[1]:    TIMER_INTERRUPT:08f5(c)
08f9 a6 3c      LDA      #0x3c
08fb 3c 25      INC      BYTE_0025
08fd b1 25      CMP      BYTE_0025
08ff 22 46      BHI      LAB_0947
0901 3f 25      CLR      BYTE_0025
0903 a6 3c      LDA      #0x3c
0905 3c 24      INC      BYTE_0024
0907 b1 24      CMP      BYTE_0024
0909 22 3c      BHI      LAB_0947
090b 3f 24      CLR      BYTE_0024
090d a6 18      LDA      #0x18
090f 3c 23      INC      BYTE_0023
0911 b1 23      CMP      BYTE_0023
0913 22 32      BHI      LAB_0947
0915 3f 23      CLR      BYTE_0023
0917 be 21      LDX      BYTE_0021
0919 d6 0e 37   LDA      DAT_0e37,X
091c a1 1c      CMP      #0x1c
091e 26 05      BNE      LAB_0925
0920 3d 26      TST      BYTE_0026
0922 26 01      BNE      LAB_0925
0924 4c         INCA

LAB_0925                                XREF[2]:    091e(j), 0922(j)
0925 3c 22      INC      BYTE_0022
0927 b1 22      CMP      BYTE_0022
0929 24 1c      BCC      LAB_0947
092b a6 01      LDA      #0x1
092d b7 22      STA      BYTE_0022
092f a6 0c      LDA      #0xc
0931 3c 21      INC      BYTE_0021
0933 b1 21      CMP      BYTE_0021
0935 22 10      BHI      LAB_0947
0937 a6 01      LDA      #0x1
0939 b7 21      STA      BYTE_0021
093b 3c 20      INC      BYTE_0020
093d 3c 26      INC      BYTE_0026
093f b6 26      LDA      BYTE_0026
0941 a1 03      CMP      #0x3
0943 23 02      BLS      LAB_0947
0945 3f 26      CLR      BYTE_0026

LAB_0947                                XREF[6]:    08ff(j), 0909(j), 0913(j),
                                                0929(j), 0935(j), 0943(j)
0947 81         RTS

*****
*                                     *
*****
undefined MoveDataBytes_061_06f()
A:1      <RETURN>
MoveDataBytes_061_06f                            XREF[1]:    TIMER_INTERRUPT:08de(c)
0948 b6 6c      LDA      BYTE_006c
094a b7 6f      STA      BYTE_006f
094c b6 6b      LDA      BYTE_006b
094e b7 6e      STA      BYTE_006e
0950 b6 6a      LDA      BYTE_006a
0952 b7 6d      STA      BYTE_006d
0954 b6 69      LDA      BYTE_0069
0956 b7 6c      STA      BYTE_006c
0958 b6 68      LDA      BYTE_0068
095a b7 6b      STA      BYTE_006b
095c b6 67      LDA      BYTE_0067
095e b7 6a      STA      BYTE_006a
0960 b6 66      LDA      BYTE_0066
0962 b7 69      STA      BYTE_0069
0964 b6 65      LDA      BYTE_0065
0966 b7 68      STA      BYTE_0068
0968 b6 64      LDA      BYTE_0064
096a b7 67      STA      BYTE_0067
096c b6 63      LDA      BYTE_0063
096e b7 66      STA      BYTE_0066
0970 b6 62      LDA      BYTE_0062
0972 b7 65      STA      BYTE_0065
0974 b6 61      LDA      BYTE_0061
0976 b7 64      STA      BYTE_0064
0978 b6 60      LDA      BYTE_0060
097a b7 63      STA      BYTE_0063

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```

097c b6 5f      LDA      BYTE_005f
097e b7 62      STA      BYTE_0062
0980 b6 5e      LDA      BYTE_005e
0982 b7 61      STA      BYTE_0061
0984 81         RTS

*****
*                                     *
*                               FUNCTION                               *
*                                     *
*****
undefined Read_Port_D()
    A:1      <RETURN>
    Read_Port_D
XREF[1]:    TIMER_INTERRUPT:08d7(c)
0985 3a 71      DEC      RAM_0071
0987 26 26      BNE      LAB_09af
0989 a6 80      LDA      #0x80
098b b7 71      STA      RAM_0071
098d b6 72      LDA      BYTE_0072
098f 4d         TSTA
0990 27 08      BEQ      LAB_099a
0992 44         LSRA
0993 b7 72      STA      BYTE_0072
0995 44         LSRA
0996 44         LSRA
0997 44         LSRA
0998 44         LSRA
0999 4c         INCA

    LAB_099a
XREF[1]:    0990(j)
099a ab 21      ADD      #0x21
099c b7 11      STA      RAM_0011
099e b6 73      LDA      BYTE_0073
09a0 4d         TSTA
09a1 27 08      BEQ      LAB_09ab
09a3 44         LSRA
09a4 b7 73      STA      BYTE_0073
09a6 44         LSRA
09a7 44         LSRA
09a8 44         LSRA
09a9 44         LSRA
09aa 4c         INCA

    LAB_09ab
XREF[1]:    09a1(j)
09ab ab 21      ADD      #0x21
09ad b7 10      STA      RAM_0010

    LAB_09af
XREF[1]:    0987(j)
09af 09 03 02   BRCLR    0x4,PORTD,LAB_09b4
09b2 3c 72      INC      BYTE_0072

    LAB_09b4
XREF[1]:    09af(j)
09b4 0a 03 02   BRSET    0x5,PORTD,LAB_09b9
09b7 3c 73      INC      BYTE_0073

    LAB_09b9
XREF[1]:    09b4(j)
09b9 81         RTS

    SWI_INTERRUPT
XREF[1]:    0ffc(*)
09ba 9d         NOP
09bb 80         RTI

```


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```

*****
*                               *
*****
undefined Clock_PB3_RMM_Return_Port_A()
A:1      <RETURN>
Clock_PB3_RMM_Return_Port_A      XREF[25]:  Read_Bytes_from_Port_A:04d8(c),
                                           Read_Bytes_from_Port_A:051H(c),
                                           Read_Bytes_from_Port_A:0520(c),
                                           Read_Bytes_from_Port_A:0525(c),
                                           Read_Bytes_from_Port_A:052d(c),
                                           Read_Bytes_from_Port_A:052f(c),
                                           Read_Bytes_from_Port_A:0575(c),
                                           Read_Bytes_from_Port_A:057d(c),
                                           Read_Bytes_from_Port_A:057f(c),
                                           Read_Bytes_from_Port_A:0584(c),
                                           Read_Bytes_from_Port_A:0594(c),
                                           Read_Bytes_from_Port_A:0599(c),
                                           Read_Bytes_from_Port_A:05c9(c),
                                           Read_Bytes_from_Port_A:05d2(c),
                                           Read_Bytes_from_Port_A:05d7(c),
                                           Read_Bytes_from_Port_A:05d8(c),
                                           Read_Bytes_from_Port_A:0608(c),
                                           Read_Bytes_from_Port_A:0610(c),
                                           Read_Bytes_from_Port_A:0615(c),
                                           Output_Current_Date_Port_A_Mayba,
                                           [more]

09bc 9b      SEI
09bd 17 01   BCLR      0x3,PORTB
09bf b6 00   LDA      PORTA
09c1 16 01   BSET      0x3,PORTB
09c3 9a      CLI
09c4 81      RTS

*****
*                               *
*****
undefined Write_RegA_To_PortA_And_Latch_to_IDH()
A:1      <RETURN>
Write_RegA_To_PortA_And_Latch_to_IDB      XREF[2]:  Output_Current_Date_Port_A_Mayba,
                                           Output_Current_Date_Port_A_Mayba,

09c5 9b      SEI
09c6 b7 00   STA      PORTA
09c8 a6 ff   LDA      #0xff
09ca b7 04   STA      DDRA
09cc 11 01   BCLR      0x0,PORTB
09ce 10 01   BSET      0x0,PORTB
09d0 3f 04   CLR      DDRA
09d2 9a      CLI
09d3 81      RTS

*****
*                               *
*****
undefined Read_Port_D_Update_CLR()
A:1      <RETURN>
Read_Port_D_Update_CLR      XREF[1]:  TIMER_INTERRUPT:08ce(c)

09d4 b6 03   LDA      PORTD
09d6 b7 70   STA      PortD_SavedValue
09d8 a4 0c   AND      #0xc
09da 48      ASLA
09db 48      ASLA
09dc b7 19   STA      PortD_PONI_IONI_bit_4_5_Ring_3_0
Value 4 is 0100. The logic checks if PB2 != 0, which is PONI ...
If PONI = TRUE, read memory [0x0f0c + PCR] (PB0/PB1) and OR t...
In memory starting at 0x0F0C we have the values
1
2
4
8

In effect, the logic is that

IF (PONI=TRUE)
{
    PortD_PONI_IONI_BIT_4_5 = 1<<PCR[1:0]; // Set bit 0 to 3 ...
}

09de 05 70 0c BRCLR      0x2,PortD_SavedValue,LAB_09ed
09e1 b6 70   LDA      PortD_SavedValue
09e3 a4 03   AND      #0x3
09e5 97      TAX
09e6 d6 0f 0c LDA      PCR_bits,X      = 1h
09e9 ba 19   ORA      PortD_PONI_IONI_bit_4_5_Ring_3_0
09eb b7 19   STA      PortD_PONI_IONI_bit_4_5_Ring_3_0

```

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```

LAB_09ed                                XREF[1]: 09de(j)
09ed 81                                RTS

*****
*                                     FUNCTION
*****
undefined WriteDateBytesToPortA_LatchToIDB_7_0)
A:1                                     <RETURN>
WriteDateBytesToPortA_LatchToIDB_7_0    XREF[1]: Output_Current_Date_Port_A_Maybo.

09ee a6 ff    LDA    #0xff
09f0 b7 04    STA    DDRA
09f2 a6 0f    LDA    #0xf
09f4 b7 00    STA    PORTA
09f6 13 01    BCLR   0x1,PORTB
09f8 12 01    BSET   0x1,PORTB
09fa a6 f0    LDA    #0xf0
09fc b7 00    STA    PORTA
09fe 13 01    BCLR   0x1,PORTB
0a00 12 01    BSET   0x1,PORTB
0a02 a6 05    LDA    #0x5
0a04 b7 00    STA    PORTA
0a06 13 01    BCLR   0x1,PORTB
0a08 12 01    BSET   0x1,PORTB
0a0a b6 26    LDA    BYTE_0026
0a0c a4 03    AND     #0x3
0a0e 48       ASLA
0a0f 48       ASLA
0a10 aa f1    ORA     #0xf1
0a12 b7 00    STA    PORTA
0a14 13 01    BCLR   0x1,PORTB
0a16 12 01    BSET   0x1,PORTB
0a18 be 20    LDX     BYTE_0020
0a1a 58       ASLX
0a1b d6 0e 44    LDA    DAT_0e44,X
0a1e aa d0    ORA     #0xd0
0a20 b7 00    STA    PORTA
0a22 13 01    BCLR   0x1,PORTB
0a24 12 01    BSET   0x1,PORTB
0a26 5c       INCX
0a27 d6 0e 44    LDA    DAT_0e44,X
0a2a aa c0    ORA     #0xc0
0a2c b7 00    STA    PORTA
0a2e 13 01    BCLR   0x1,PORTB
0a30 12 01    BSET   0x1,PORTB
0a32 be 21    LDX     BYTE_0021
0a34 58       ASLX
0a35 d6 0e 44    LDA    DAT_0e44,X
0a38 aa b0    ORA     #0xb0
0a3a b7 00    STA    PORTA
0a3c 13 01    BCLR   0x1,PORTB
0a3e 12 01    BSET   0x1,PORTB
0a40 5c       INCX
0a41 d6 0e 44    LDA    DAT_0e44,X
0a44 aa a0    ORA     #0xa0
0a46 b7 00    STA    PORTA
0a48 13 01    BCLR   0x1,PORTB
0a4a 12 01    BSET   0x1,PORTB
0a4c be 22    LDX     BYTE_0022
0a4e 58       ASLX
0a4f d6 0e 44    LDA    DAT_0e44,X
0a52 aa 90    ORA     #0x90
0a54 b7 00    STA    PORTA
0a56 13 01    BCLR   0x1,PORTB
0a58 12 01    BSET   0x1,PORTB
0a5a 5c       INCX
0a5b d6 0e 44    LDA    DAT_0e44,X
0a5e aa 80    ORA     #0x80
0a60 b7 00    STA    PORTA
0a62 13 01    BCLR   0x1,PORTB
0a64 12 01    BSET   0x1,PORTB
0a66 be 23    LDX     BYTE_0023
0a68 58       ASLX
0a69 d6 0e 44    LDA    DAT_0e44,X
0a6c aa 70    ORA     #0x70
0a6e b7 00    STA    PORTA
0a70 13 01    BCLR   0x1,PORTB
0a72 12 01    BSET   0x1,PORTB
0a74 5c       INCX
0a75 d6 0e 44    LDA    DAT_0e44,X
0a78 aa 60    ORA     #0x60
0a7a b7 00    STA    PORTA
0a7c 13 01    BCLR   0x1,PORTB
0a7e 12 01    BSET   0x1,PORTB
0a80 be 24    LDX     BYTE_0024

```

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```

0b13 b7 00      STA      PORTA
0b15 15 01      BCLR     0x2,PORTB
0b17 b6 00      LDA      PORTA
0b19 14 01      BSET     0x2,PORTB
0b1b a4 0f      AND      #0xf
0b1d 97         TAX
0b1e 58         ASLX
0b1f 58         ASLX
0b20 58         ASLX
0b21 bf 52      STX      BYTE_0052
0b23 48         ASLA
0b24 bb 52      ADD      BYTE_0052
0b26 bb 21      ADD      BYTE_0021
0b28 b7 21      STA      BYTE_0021
0b2a a6 80      LDA      #0x80
0b2c b7 00      STA      PORTA
0b2e 15 01      BCLR     0x2,PORTB
0b30 b6 00      LDA      PORTA
0b32 14 01      BSET     0x2,PORTB
0b34 a4 0f      AND      #0xf
0b36 b7 22      STA      BYTE_0022
0b38 a6 90      LDA      #0x90
0b3a b7 00      STA      PORTA
0b3c 15 01      BCLR     0x2,PORTB
0b3e b6 00      LDA      PORTA
0b40 14 01      BSET     0x2,PORTB
0b42 a4 0f      AND      #0xf
0b44 97         TAX
0b45 58         ASLX
0b46 58         ASLX
0b47 58         ASLX
0b48 bf 52      STX      BYTE_0052
0b4a 48         ASLA
0b4b bb 52      ADD      BYTE_0052
0b4d bb 22      ADD      BYTE_0022
0b4f b7 22      STA      BYTE_0022
0b51 a6 60      LDA      #0x60
0b53 b7 00      STA      PORTA
0b55 15 01      BCLR     0x2,PORTB
0b57 b6 00      LDA      PORTA
0b59 14 01      BSET     0x2,PORTB
0b5b a4 0f      AND      #0xf
0b5d b7 23      STA      BYTE_0023
0b5f a6 70      LDA      #0x70
0b61 b7 00      STA      PORTA
0b63 15 01      BCLR     0x2,PORTB
0b65 b6 00      LDA      PORTA
0b67 14 01      BSET     0x2,PORTB
0b69 a4 0f      AND      #0xf
0b6b 97         TAX
0b6c 58         ASLX
0b6d 58         ASLX
0b6e 58         ASLX
0b6f bf 52      STX      BYTE_0052
0b71 48         ASLA
0b72 bb 52      ADD      BYTE_0052
0b74 bb 23      ADD      BYTE_0023
0b76 b7 23      STA      BYTE_0023
0b78 a6 40      LDA      #0x40
0b7a b7 00      STA      PORTA
0b7c 15 01      BCLR     0x2,PORTB
0b7e b6 00      LDA      PORTA
0b80 14 01      BSET     0x2,PORTB
0b82 a4 0f      AND      #0xf
0b84 b7 24      STA      BYTE_0024
0b86 a6 50      LDA      #0x50
0b88 b7 00      STA      PORTA
0b8a 15 01      BCLR     0x2,PORTB
0b8c b6 00      LDA      PORTA
0b8e 14 01      BSET     0x2,PORTB
0b90 a4 0f      AND      #0xf
0b92 97         TAX
0b93 58         ASLX
0b94 58         ASLX
0b95 58         ASLX
0b96 bf 52      STX      BYTE_0052
0b98 48         ASLA
0b99 bb 52      ADD      BYTE_0052
0b9b bb 24      ADD      BYTE_0024
0b9d b7 24      STA      BYTE_0024
0b9f a6 20      LDA      #0x20
0ba1 b7 00      STA      PORTA
0ba3 15 01      BCLR     0x2,PORTB
0ba5 b6 00      LDA      PORTA
0ba7 14 01      BSET     0x2,PORTB

```

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```

0ba9 a4 0f      AND      #0xf
0bab b7 25      STA      BYTE_0025
0bad a6 30      LDA      #0x30
0baf b7 00      STA      PORTA
0bb1 15 01      BCLR     0x2,PORTB
0bb3 b6 00      LDA      PORTA
0bb5 14 01      BSET     0x2,PORTB
0bb7 a4 0f      AND      #0xf
0bb9 97         TAX
0bba 58         ASLX
0bbb 58         ASLX
0bbc 58         ASLX
0bbd bf 52      STX      BYTE_0052
0bbf 48         ASLA
0bc0 bb 52      ADD      BYTE_0052
0bc2 bb 25      ADD      BYTE_0025
0bc4 b7 25      STA      BYTE_0025
0bc6 a6 00      LDA      #0x0
0bc8 b7 00      STA      PORTA
0bca 15 01      BCLR     0x2,PORTB
0bcc b6 00      LDA      PORTA
0bce 14 01      BSET     0x2,PORTB
0bd0 a4 0f      AND      #0xf
0bd2 a4 08      AND      #0x8
0bd4 a1 08      CMP      #0x8
0bd6 26 03      BNE      LAB_Obdb
0bd8 cc 0a c0    JMP      RTC_Initialize_Maybe

LAB_Obdb
0bdb 3f 04      CLR      DDRA
0bdd 81      RTS
0bde 00      ??      00h
0bdf 00      ??      00h
0be0 00      ??      00h
0be1 00      ??      00h
0be2 00      ??      00h
0be3 00      ??      00h
0be4 00      ??      00h
0be5 00      ??      00h
0be6 00      ??      00h
0be7 00      ??      00h
0be8 00      ??      00h
0be9 00      ??      00h
0bea 00      ??      00h
0beb 00      ??      00h
0bec 00      ??      00h
0bed 00      ??      00h
0bee 00      ??      00h
0bef 00      ??      00h
0bf0 00      ??      00h
0bf1 00      ??      00h
0bf2 00      ??      00h
0bf3 00      ??      00h
0bf4 00      ??      00h
0bf5 00      ??      00h
0bf6 00      ??      00h
0bf7 00      ??      00h
0bf8 00      ??      00h
0bf9 00      ??      00h
0bfa 00      ??      00h
0bfb 00      ??      00h
0bfc 00      ??      00h
0bfd 00      ??      00h
0bfe 00      ??      00h
0bff 00      ??      00h
0c00 00      ??      00h
0c01 00      ??      00h
0c02 00      ??      00h
0c03 00      ??      00h
0c04 00      ??      00h
0c05 00      ??      00h
0c06 00      ??      00h
0c07 00      ??      00h
0c08 00      ??      00h
0c09 00      ??      00h
0c0a 00      ??      00h
0c0b 00      ??      00h
0c0c 00      ??      00h
0c0d 00      ??      00h
0c0e 00      ??      00h
0c0f 00      ??      00h
0c10 00      ??      00h
0c11 00      ??      00h
0c12 00      ??      00h
0c13 00      ??      00h

```

XREF[1]: 0bd6(j)

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0c14	00	??	00h
0c15	00	??	00h
0c16	00	??	00h
0c17	00	??	00h
0c18	00	??	00h
0c19	00	??	00h
0c1a	00	??	00h
0c1b	00	??	00h
0c1c	00	??	00h
0c1d	00	??	00h
0c1e	00	??	00h
0c1f	00	??	00h
0c20	00	??	00h
0c21	00	??	00h
0c22	00	??	00h
0c23	00	??	00h
0c24	00	??	00h
0c25	00	??	00h
0c26	00	??	00h
0c27	00	??	00h
0c28	00	??	00h
0c29	00	??	00h
0c2a	00	??	00h
0c2b	00	??	00h
0c2c	00	??	00h
0c2d	00	??	00h
0c2e	00	??	00h
0c2f	00	??	00h
0c30	00	??	00h
0c31	00	??	00h
0c32	00	??	00h
0c33	00	??	00h
0c34	00	??	00h
0c35	00	??	00h
0c36	00	??	00h
0c37	00	??	00h
0c38	00	??	00h
0c39	00	??	00h
0c3a	00	??	00h
0c3b	00	??	00h
0c3c	00	??	00h
0c3d	00	??	00h
0c3e	00	??	00h
0c3f	00	??	00h
0c40	00	??	00h
0c41	00	??	00h
0c42	00	??	00h
0c43	00	??	00h
0c44	00	??	00h
0c45	00	??	00h
0c46	00	??	00h
0c47	00	??	00h
0c48	00	??	00h
0c49	00	??	00h
0c4a	00	??	00h
0c4b	00	??	00h
0c4c	00	??	00h
0c4d	00	??	00h
0c4e	00	??	00h
0c4f	00	??	00h
0c50	00	??	00h
0c51	00	??	00h
0c52	00	??	00h
0c53	00	??	00h
0c54	00	??	00h
0c55	00	??	00h
0c56	00	??	00h
0c57	00	??	00h
0c58	00	??	00h
0c59	00	??	00h
0c5a	00	??	00h
0c5b	00	??	00h
0c5c	00	??	00h
0c5d	00	??	00h
0c5e	00	??	00h
0c5f	00	??	00h
0c60	00	??	00h
0c61	00	??	00h
0c62	00	??	00h
0c63	00	??	00h
0c64	00	??	00h
0c65	00	??	00h
0c66	00	??	00h
0c67	00	??	00h
0c68	00	??	00h

Ghidra - MC68705U3_35C.BIN

0c69 00	??	00h
0c6a 00	??	00h
0c6b 00	??	00h
0c6c 00	??	00h
0c6d 00	??	00h
0c6e 00	??	00h
0c6f 00	??	00h
0c70 00	??	00h
0c71 00	??	00h
0c72 00	??	00h
0c73 00	??	00h
0c74 00	??	00h
0c75 00	??	00h
0c76 00	??	00h
0c77 00	??	00h
0c78 00	??	00h
0c79 00	??	00h
0c7a 00	??	00h
0c7b 00	??	00h
0c7c 00	??	00h
0c7d 00	??	00h
0c7e 00	??	00h
0c7f 00	??	00h
0c80 00	??	00h
0c81 00	??	00h
0c82 00	??	00h
0c83 00	??	00h
0c84 00	??	00h
0c85 00	??	00h
0c86 00	??	00h
0c87 00	??	00h
0c88 00	??	00h
0c89 00	??	00h
0c8a 00	??	00h
0c8b 00	??	00h
0c8c 00	??	00h
0c8d 00	??	00h
0c8e 00	??	00h
0c8f 00	??	00h
0c90 00	??	00h
0c91 00	??	00h
0c92 00	??	00h
0c93 00	??	00h
0c94 00	??	00h
0c95 00	??	00h
0c96 00	??	00h
0c97 00	??	00h
0c98 00	??	00h
0c99 00	??	00h
0c9a 00	??	00h
0c9b 00	??	00h
0c9c 00	??	00h
0c9d 00	??	00h
0c9e 00	??	00h
0c9f 00	??	00h
0ca0 00	??	00h
0ca1 00	??	00h
0ca2 00	??	00h
0ca3 00	??	00h
0ca4 00	??	00h
0ca5 00	??	00h
0ca6 00	??	00h
0ca7 00	??	00h
0ca8 00	??	00h
0ca9 00	??	00h
0caa 00	??	00h
0cab 00	??	00h
0cac 00	??	00h
0cad 00	??	00h
0cae 00	??	00h
0caf 00	??	00h
0cb0 00	??	00h
0cb1 00	??	00h
0cb2 00	??	00h
0cb3 00	??	00h
0cb4 00	??	00h
0cb5 00	??	00h
0cb6 00	??	00h
0cb7 00	??	00h
0cb8 00	??	00h
0cb9 00	??	00h
0cba 00	??	00h
0cbb 00	??	00h
0cbc 00	??	00h
0cbd 00	??	00h

Ghidra - MC68705U3_35C.BIN

```

0cbe 00 ?? 00h
0cbf 00 ?? 00h
0cc0 00 ?? 00h
0cc1 00 ?? 00h
0cc2 00 ?? 00h
0cc3 00 ?? 00h
0cc4 00 ?? 00h
0cc5 00 ?? 00h
0cc6 00 ?? 00h
0cc7 00 ?? 00h
0cc8 00 ?? 00h
0cc9 00 ?? 00h
0cca 00 ?? 00h
0ccb 00 ?? 00h
0ccc 00 ?? 00h
0ccd 00 ?? 00h
0cce 00 ?? 00h
0ccf 00 ?? 00h
0cd0 00 ?? 00h
0cd1 00 ?? 00h
0cd2 00 ?? 00h
0cd3 00 ?? 00h
0cd4 00 ?? 00h
0cd5 00 ?? 00h
0cd6 00 ?? 00h
0cd7 00 ?? 00h
0cd8 00 ?? 00h
0cd9 00 ?? 00h
0cda 00 ?? 00h
0cdb 00 ?? 00h
0cdc 00 ?? 00h
0cdd 00 ?? 00h
0cde 00 ?? 00h
0cdf 00 ?? 00h
0ce0 00 ?? 00h
0ce1 00 ?? 00h
0ce2 00 ?? 00h
0ce3 00 ?? 00h
0ce4 00 ?? 00h
0ce5 00 ?? 00h
0ce6 00 ?? 00h
0ce7 00 ?? 00h
0ce8 00 ?? 00h
0ce9 00 ?? 00h
0cea 00 ?? 00h
0ceb 00 ?? 00h
0cec 00 ?? 00h
0ced 00 ?? 00h
0cee 00 ?? 00h
0cef 00 ?? 00h
0cf0 00 ?? 00h
0cf1 00 ?? 00h
0cf2 00 ?? 00h
0cf3 00 ?? 00h
0cf4 00 ?? 00h
0cf5 00 ?? 00h
0cf6 00 ?? 00h
0cf7 00 ?? 00h

```

DAT_0cf8

```

XREF[27]: Something_RAM_0052_0059:021a(*),
Something_RAM_0052_0059:0229(*),
Something_RAM_0052_0059:02b9(*),
Something_RAM_0052_0059:02d7(*),
Something_RAM_0052_0059:02f9(*),
Something_RAM_0052_0059:0304(*),
Something_RAM_0052_0059:0343(*),
Something_RAM_0052_0059:0352(*),
Something_RAM_0052_0059:0368(*),
Something_RAM_0052_0059:0375(*),
Something_PortC:0393(*),
Something_PortC:03a2(*),
Something_PortC:03b4(*),
Something_PortC:03c1(*),
Something_PortC:03d1(*),
Something_PortC:03e2(*),
Something_PortC:0408(*),
Something_PortC:0416(*),
Something_PortC:0426(*),
Something_PortC:044k(*), [more]

```

```

0cf8 00 ?? 00h
0cf9 20 ?? 20h
0cfa 28 ?? 28h (
0cfb 2a ?? 2Ah *
0cfc 50 ?? 50h P
0cfd 51 ?? 51h Q

```


Ghidra - MC68705U3_35C.BIN

0cfe	54	??	54h	T	
0cff	55	??	55h	U	
0d00	5f	??	5Fh	_	
0d01	66	??	66h	f	
0d02	6e	??	6Eh	n	
0d03	4e	??	4Eh	N	
0d04	5d	??	5Dh]	
0d05	08	??	08h		
0d06	44	??	44h	D	
0d07	4f	??	4Fh	O	
0d08	77	??	77h	w	
0d09	11	??	11h		
0d0a	6b	??	6Bh	k	
0d0b	3b	??	3Bh	;	
0d0c	1d	??	1Dh		
0d0d	3e	??	3Eh	>	
0d0e	7e	??	7Eh	~	
0d0f	13	??	13h		
0d10	7f	??	7Fh		
0d11	3f	??	3Fh	?	
					DAT_0d12
					XREF[2]: Read_Bytes_from_Port_A:05e8*), Read_Bytes_from_Port_A:05ed*)
0d12	3a	??	3Ah	:	
0d13	3a	??	3Ah	:	
0d14	52	??	52h	R	
0d15	3a	??	3Ah	:	
0d16	3a	??	3Ah	:	
0d17	57	??	57h	W	
0d18	52	??	52h	R	
0d19	57	??	57h	W	
					DAT_0d1a
					XREF[2]: Read_Bytes_from_Port_A:05fa*), Read_Bytes_from_Port_A:060Q*)
0d1a	43	??	43h	C	
0d1b	44	??	44h	D	
0d1c	44	??	44h	D	
0d1d	44	??	44h	D	
0d1e	43	??	43h	C	
0d1f	41	??	41h	A	
0d20	44	??	44h	D	
0d21	41	??	41h	A	
					DAT_0d22
					XREF[8]: Intialize_Ram_52_59_From_0xD22_0., Intialize_Ram_52_59_From_0xD22_0., Intialize_Ram_52_59_From_0xD22_0., Intialize_Ram_52_59_From_0xD22_0., Intialize_Ram_52_59_From_0xD22_0., Intialize_Ram_52_59_From_0xD22_0., Intialize_Ram_52_59_From_0xD22_0., Intialize_Ram_52_59_From_0xD22_0.
0d22	00	??	00h		
0d23	00	??	00h		
0d24	55	??	55h	U	
0d25	11	??	11h		
0d26	55	??	55h	U	
0d27	11	??	11h		
0d28	55	??	55h	U	
0d29	11	??	11h		
0d2a	55	??	55h	U	
0d2b	11	??	11h		
0d2c	55	??	55h	U	
0d2d	11	??	11h		
0d2e	55	??	55h	U	
0d2f	11	??	11h		
0d30	55	??	55h	U	
0d31	11	??	11h		
0d32	4d	??	4Dh	M	
0d33	9a	??	9Ah		
0d34	41	??	41h	A	
0d35	82	??	82h		
0d36	45	??	45h	E	
0d37	99	??	99h		
0d38	45	??	45h	E	
0d39	8b	??	8Bh		
0d3a	49	??	49h	I	
0d3b	83	??	83h		
0d3c	4c	??	4Ch	L	
0d3d	83	??	83h		
0d3e	4c	??	4Ch	L	
0d3f	9b	??	9Bh		
0d40	45	??	45h	E	
0d41	82	??	82h		
0d42	88	??	88h		
0d43	11	??	11h		

Ghidra - MC68705U3_35C.BIN

0d44	8d	??	8Dh
0d45	11	??	11h
0d46	88	??	88h
0d47	1b	??	1Bh
0d48	8d	??	8Dh
0d49	1b	??	1Bh
0d4a	88	??	88h
0d4b	b1	??	B1h
0d4c	8d	??	8Dh
0d4d	b1	??	B1h
0d4e	88	??	88h
0d4f	bb	??	BBh
0d50	8d	??	8Dh
0d51	bb	??	BBh
0d52	d8	??	D8h
0d53	11	??	11h
0d54	dd	??	DDh
0d55	11	??	11h
0d56	d8	??	D8h
0d57	1b	??	1Bh
0d58	dd	??	DDh
0d59	1b	??	1Bh
0d5a	d8	??	D8h
0d5b	b1	??	B1h
0d5c	dd	??	DDh
0d5d	b1	??	B1h
0d5e	d8	??	D8h
0d5f	bb	??	BBh
0d60	dd	??	DDh
0d61	bb	??	BBh
0d62	00	??	00h
0d63	00	??	00h
0d64	08	??	08h
0d65	00	??	00h
0d66	0e	??	0Eh
0d67	00	??	00h
0d68	0f	??	0Fh
0d69	01	??	01h
0d6a	0f	??	0Fh
0d6b	07	??	07h
0d6c	0f	??	0Fh
0d6d	1f	??	1Fh
0d6e	0f	??	0Fh
0d6f	7f	??	7Fh
0d70	8f	??	8Fh
0d71	ff	??	FFh
0d72	ef	??	EFh
0d73	ff	??	FFh
0d74	ff	??	FFh
0d75	ff	??	FFh
0d76	aa	??	AAh
0d77	55	??	55h
0d78	88	??	88h
0d79	11	??	11h
0d7a	00	??	00h
0d7b	40	??	40h
0d7c	80	??	80h
0d7d	01	??	01h
0d7e	00	??	00h
0d7f	20	??	20h
0d80	02	??	02h
0d81	40	??	40h
0d82	0d	??	0Dh
0d83	1a	??	1Ah
0d84	03	??	03h
0d85	02	??	02h
0d86	05	??	05h
0d87	19	??	19h
0d88	05	??	05h
0d89	0b	??	0Bh
0d8a	09	??	09h
0d8b	03	??	03h
0d8c	0c	??	0Ch
0d8d	0b	??	0Bh
0d8e	0c	??	0Ch
0d8f	1b	??	1Bh
0d90	05	??	05h
0d91	02	??	02h
0d92	0d	??	0Dh
0d93	1b	??	1Bh
0d94	0d	??	0Dh
0d95	0b	??	0Bh
0d96	00	??	00h
0d97	00	??	00h
0d98	0d	??	0Dh

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Ghidra - MC68705U3_35C.BIN

0d99	11	??	11h	
0d9a	40	??	40h	@
0d9b	80	??	80h	
0d9c	4d	??	4Dh	M
0d9d	91	??	91h	
0d9e	00	??	00h	
0d9f	00	??	00h	
0da0	55	??	55h	U
0da1	11	??	11h	
0da2	95	??	95h	
0da3	ba	??	BAh	
0da4	d5	??	D5h	
0da5	83	??	83h	
0da6	1d	??	1Dh	
0da7	3b	??	3Bh	;
0da8	54	??	54h	T
0da9	a8	??	A8h	
0daa	1d	??	1Dh	
0dab	3a	??	3Ah	:
0dac	d4	??	D4h	
0dad	a8	??	A8h	
0dae	d4	??	D4h	
0daf	80	??	80h	
0db0	54	??	54h	T
0db1	ab	??	ABh	
0db2	c1	??	C1h	
0db3	83	??	83h	
0db4	1c	??	1Ch	
0db5	38	??	38h	8
0db6	1c	??	1Ch	
0db7	b0	??	B0h	
0db8	c2	??	C2h	
0db9	84	??	84h	
0dba	40	??	40h	@
0dbb	a8	??	A8h	
0dbc	63	??	63h	c
0dbd	82	??	82h	
0dbe	61	??	61h	a
0dbf	86	??	86h	
0dc0	55	??	55h	U
0dc1	aa	??	AAh	
0dc2	d5	??	D5h	
0dc3	81	??	81h	
0dc4	55	??	55h	U
0dc5	ae	??	AEnh	
0dc6	d5	??	D5h	
0dc7	85	??	85h	
0dc8	d4	??	D4h	
0dc9	2b	??	2Bh	+
0dca	1c	??	1Ch	
0dcb	10	??	10h	
0dcc	41	??	41h	A
0dcd	aa	??	AAh	
0dce	42	??	42h	B
0dcf	c0	??	C0h	
0dd0	41	??	41h	A
0dd1	c6	??	C6h	
0dd2	22	??	22h	"
0dd3	44	??	44h	D
0dd4	22	??	22h	"
0dd5	10	??	10h	
0dd6	16	??	16h	
0dd7	68	??	68h	h
0dd8	dc	??	DCh	
0dd9	99	??	99h	
0dda	57	??	57h	W
0ddb	ea	??	EAh	
0ddc	13	??	13h	
0ddd	43	??	43h	C
DAT_0dde				
0dde	00	??	00h	
0ddf	00	??	00h	
0de0	38	??	38h	8
0de1	3e	??	3Eh	>
0de2	3c	??	3Ch	<
0de3	3e	??	3Eh	>
0de4	3c	??	3Ch	<
0de5	3e	??	3Eh	>
0de6	3e	??	3Eh	>
0de7	3c	??	3Ch	<
0de8	3e	??	3Eh	>
0de9	3c	??	3Ch	<
0dea	3e	??	3Eh	>
			XREF[1]:	CopyData_In_Ram_Dest_0x46_0x4e:0.

Ghidra - MC68705U3_35C.BIN

	DAT_0deb			XREF[2]:	Calc_Something_Dest_0x48_0x4f:0&.
					Calc_Something_Dest_0x48_0x4f:0&.
0deb 00	??	00h			
0dec 00	??	00h			
0ded 00	??	00h			
0dee 00	??	00h			
0def 00	??	00h			
0df0 3e	??	3Eh	>		
0df1 00	??	00h			
0df2 76	??	76h	v		
0df3 00	??	00h			
0df4 b4	??	B4h			
0df5 00	??	00h			
0df6 f0	??	F0h			
0df7 01	??	01h			
0df8 2e	??	2Eh	.		
0df9 01	??	01h			
0dfa 6a	??	6Ah	j		
0dfb 01	??	01h			
0dfc a8	??	A8h			
0dfd 01	??	01h			
0dfe e6	??	E6h			
0dff 02	??	02h			
0e00 22	??	22h	"		
0e01 02	??	02h			
0e02 60	??	60h	'		
0e03 02	??	02h			
0e04 9c	??	9Ch			
0e05 00	??	00h			
0e06 00	??	00h			
0e07 00	??	00h			
0e08 00	??	00h			
0e09 00	??	00h			
0e0a 3e	??	3Eh	>		
0e0b 00	??	00h			
0e0c 78	??	78h	x		
0e0d 00	??	00h			
0e0e b6	??	B6h			
0e0f 00	??	00h			
0e10 f2	??	F2h			
0e11 01	??	01h			
0e12 30	??	30h	0		
0e13 01	??	01h			
0e14 6c	??	6Ch	l		
0e15 01	??	01h			
0e16 aa	??	AAh			
0e17 01	??	01h			
0e18 e8	??	E8h			
0e19 02	??	02h			
0e1a 24	??	24h	\$		
0e1b 02	??	02h			
0e1c 62	??	62h	b		
0e1d 02	??	02h			
0e1e 9e	??	9Eh			
	DAT_0elf			XREF[2]:	Calc_Something_Dest_0x48_0x4f:0&.
					Calc_Something_Dest_0x48_0x4f:0&.
0elf 00	??	00h			
0e20 00	??	00h			
0e21 0e	??	0Eh			
0e22 10	??	10h			
0e23 1c	??	1Ch			
0e24 20	??	20h			
0e25 2a	??	2Ah	*		
0e26 30	??	30h	0		
0e27 38	??	38h	8		
0e28 40	??	40h	@		
0e29 46	??	46h	F		
0e2a 50	??	50h	P		
0e2b 54	??	54h	T		
0e2c 60	??	60h	`		
0e2d 62	??	62h	b		
0e2e 70	??	70h	p		
0e2f 70	??	70h	p		
0e30 80	??	80h			
0e31 7e	??	7Eh	~		
0e32 90	??	90h			
0e33 8c	??	8Ch			
0e34 a0	??	A0h			
0e35 9a	??	9Ah			
0e36 b0	??	B0h			
	DAT_0e37			XREF[1]:	Something_RAM_20_25:0919(*)
0e37 00	??	00h			

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0e44	00	??	00h
0e45	00	??	00h
0e46	00	??	00h
0e47	01	??	01h
0e48	00	??	00h
0e49	02	??	02h
0e4a	00	??	00h
0e4b	03	??	03h
0e4c	00	??	00h
0e4d	04	??	04h
0e4e	00	??	00h
0e4f	05	??	05h
0e50	00	??	00h
0e51	06	??	06h
0e52	00	??	00h
0e53	07	??	07h
0e54	00	??	00h
0e55	08	??	08h
0e56	00	??	00h
0e57	09	??	09h
0e58	01	??	01h
0e59	00	??	00h
0e5a	01	??	01h
0e5b	01	??	01h
0e5c	01	??	01h
0e5d	02	??	02h
0e5e	01	??	01h
0e5f	03	??	03h
0e60	01	??	01h
0e61	04	??	04h
0e62	01	??	01h
0e63	05	??	05h
0e64	01	??	01h
0e65	06	??	06h
0e66	01	??	01h
0e67	07	??	07h
0e68	01	??	01h
0e69	08	??	08h
0e6a	01	??	01h
0e6b	09	??	09h
0e6c	02	??	02h
0e6d	00	??	00h
0e6e	02	??	02h
0e6f	01	??	01h
0e70	02	??	02h
0e71	02	??	02h
0e72	02	??	02h
0e73	03	??	03h
0e74	02	??	02h
0e75	04	??	04h
0e76	02	??	02h
0e77	05	??	05h
0e78	02	??	02h
0e79	06	??	06h

[illegible]

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0e7a	02	??	02h
0e7b	07	??	07h
0e7c	02	??	02h
0e7d	08	??	08h
0e7e	02	??	02h
0e7f	09	??	09h
0e80	03	??	03h
0e81	00	??	00h
0e82	03	??	03h
0e83	01	??	01h
0e84	03	??	03h
0e85	02	??	02h
0e86	03	??	03h
0e87	03	??	03h
0e88	03	??	03h
0e89	04	??	04h
0e8a	03	??	03h
0e8b	05	??	05h
0e8c	03	??	03h
0e8d	06	??	06h
0e8e	03	??	03h
0e8f	07	??	07h
0e90	03	??	03h
0e91	08	??	08h
0e92	03	??	03h
0e93	09	??	09h
0e94	04	??	04h
0e95	00	??	00h
0e96	04	??	04h
0e97	01	??	01h
0e98	04	??	04h
0e99	02	??	02h
0e9a	04	??	04h
0e9b	03	??	03h
0e9c	04	??	04h
0e9d	04	??	04h
0e9e	04	??	04h
0e9f	05	??	05h
0ea0	04	??	04h
0ea1	06	??	06h
0ea2	04	??	04h
0ea3	07	??	07h
0ea4	04	??	04h
0ea5	08	??	08h
0ea6	04	??	04h
0ea7	09	??	09h
0ea8	05	??	05h
0ea9	00	??	00h
0eaa	05	??	05h
0eab	01	??	01h
0eac	05	??	05h
0ead	02	??	02h
0eae	05	??	05h
0eaf	03	??	03h
0eb0	05	??	05h
0eb1	04	??	04h
0eb2	05	??	05h
0eb3	05	??	05h
0eb4	05	??	05h
0eb5	06	??	06h
0eb6	05	??	05h
0eb7	07	??	07h
0eb8	05	??	05h
0eb9	08	??	08h
0eba	05	??	05h
0ebb	09	??	09h
0ebc	06	??	06h
0ebd	00	??	00h
0ebe	06	??	06h
0ebf	01	??	01h
0ec0	06	??	06h
0ec1	02	??	02h
0ec2	06	??	06h
0ec3	03	??	03h
0ec4	06	??	06h
0ec5	04	??	04h
0ec6	06	??	06h
0ec7	05	??	05h
0ec8	06	??	06h
0ec9	06	??	06h
0eca	06	??	06h
0ecb	07	??	07h
0ecc	06	??	06h
0ecd	08	??	08h
0ece	06	??	06h

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```

0ecf 09    ??    09h
0ed0 07    ??    07h
0ed1 00    ??    00h
0ed2 07    ??    07h
0ed3 01    ??    01h
0ed4 07    ??    07h
0ed5 02    ??    02h
0ed6 07    ??    07h
0ed7 03    ??    03h
0ed8 07    ??    07h
0ed9 04    ??    04h
0eda 07    ??    07h
0edb 05    ??    05h
0edc 07    ??    07h
0edd 06    ??    06h
0ede 07    ??    07h
0edf 07    ??    07h
0ee0 07    ??    07h
0ee1 08    ??    08h
0ee2 07    ??    07h
0ee3 09    ??    09h
0ee4 08    ??    08h
0ee5 00    ??    00h
0ee6 08    ??    08h
0ee7 01    ??    01h
0ee8 08    ??    08h
0ee9 02    ??    02h
0eea 08    ??    08h
0eeb 03    ??    03h
0eec 08    ??    08h
0eed 04    ??    04h
0eee 08    ??    08h
0eeF 05    ??    05h
0ef0 08    ??    08h
0ef1 06    ??    06h
0ef2 08    ??    08h
0ef3 07    ??    07h
0ef4 08    ??    08h
0ef5 08    ??    08h
0ef6 08    ??    08h
0ef7 09    ??    09h
0ef8 09    ??    09h
0ef9 00    ??    00h
0efa 09    ??    09h
0efb 01    ??    01h
0efc 09    ??    09h
0efd 02    ??    02h
0efe 09    ??    09h
0eff 03    ??    03h
0f00 09    ??    09h
0f01 04    ??    04h
0f02 09    ??    09h
0f03 05    ??    05h
0f04 09    ??    09h
0f05 06    ??    06h
0f06 09    ??    09h
0f07 07    ??    07h
0f08 09    ??    09h
0f09 08    ??    08h
0f0a 09    ??    09h
0f0b 09    ??    09h

```

```

PCR_bits
0f0c 01    db    1h
0f0d 02    db    2h
0f0e 04    db    4h
0f0f 08    db    8h
0f10 00    ??    00h
0f11 00    ??    00h
0f12 00    ??    00h
0f13 00    ??    00h
0f14 00    ??    00h
0f15 00    ??    00h
0f16 00    ??    00h
0f17 00    ??    00h
0f18 00    ??    00h
0f19 00    ??    00h
0f1a 00    ??    00h
0f1b 00    ??    00h
0f1c 00    ??    00h
0f1d 00    ??    00h
0f1e 00    ??    00h
0f1f 00    ??    00h
0f20 00    ??    00h
0f21 00    ??    00h

```

```

XREF[1]:      Read_Port_D_Update_CLR:09e0*)

```

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```
0f22 00    ??    00h
0f23 00    ??    00h
0f24 00    ??    00h
0f25 00    ??    00h
0f26 00    ??    00h
0f27 00    ??    00h
0f28 00    ??    00h
0f29 00    ??    00h
0f2a 00    ??    00h
0f2b 00    ??    00h
0f2c 00    ??    00h
0f2d 00    ??    00h
0f2e 00    ??    00h
0f2f 00    ??    00h
0f30 00    ??    00h
0f31 00    ??    00h
0f32 00    ??    00h
0f33 00    ??    00h
0f34 00    ??    00h
0f35 00    ??    00h
0f36 00    ??    00h
0f37 00    ??    00h
```

```
Mask bits 0x25 = 0010_0101
CLK = 0 (Clock Oscillation type) 0=Crystal (1=resistor capacit...
TOPT = 0 (Timer Mask/Programmable option) (0=All TCR bits are...
CLS = 1 (Timer Clock Source) (1=External TIMER PIN. 0=Internal...
TIE = 0 (Timer External Input Enable)
SNM = 0 (Secure/Non-Secure Mode Option)
P2 = 1
P1 = 0
P0 = 1
```

P2-P0 = (Prescaler option) => 101 => Divide by 32.

```
MOR_Mask_Option_Register
0f38 25    db    25h    Mask Option Register
*** START: Unused hole from 0xF39 to 0xF7F ***
0f39 00    db    0h
0f3a 00    db    0h
0f3b 00    db    0h
0f3c 00    db    0h
0f3d 00    db    0h
0f3e 00    db    0h
0f3f 00    db    0h
0f40 00    db    0h
0f41 00    db    0h
0f42 00    db    0h
0f43 00    db    0h
0f44 00    db    0h
0f45 00    db    0h
0f46 00    db    0h
0f47 00    db    0h
0f48 00    db    0h
0f49 00    db    0h
0f4a 00    db    0h
0f4b 00    db    0h
0f4c 00    db    0h
0f4d 00    db    0h
0f4e 00    db    0h
0f4f 00    db    0h
0f50 00    db    0h
0f51 00    db    0h
0f52 00    db    0h
0f53 00    db    0h
0f54 00    db    0h
0f55 00    db    0h
0f56 00    db    0h
0f57 00    db    0h
0f58 00    db    0h
0f59 00    db    0h
0f5a 00    db    0h
0f5b 00    db    0h
0f5c 00    db    0h
0f5d 00    db    0h
0f5e 00    db    0h
0f5f 00    db    0h
0f60 00    db    0h
0f61 00    db    0h
0f62 00    db    0h
0f63 00    db    0h
0f64 00    db    0h
0f65 00    db    0h
0f66 00    db    0h
0f67 00    db    0h
```


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0f68	00	db	0h
0f69	00	db	0h
0f6a	00	db	0h
0f6b	00	db	0h
0f6c	00	db	0h
0f6d	00	db	0h
0f6e	00	db	0h
0f6f	00	db	0h
0f70	00	db	0h
0f71	00	db	0h
0f72	00	db	0h
0f73	00	db	0h
0f74	00	db	0h
0f75	00	db	0h
0f76	00	db	0h
0f77	00	db	0h
0f78	00	db	0h
0f79	00	db	0h
0f7a	00	db	0h
0f7b	00	db	0h
0f7c	00	db	0h
0f7d	00	db	0h
0f7e	00	db	0h
0f7f	00	db	0h
*** END: Unused hole from 0xF39 to 0xF7F ***			
0f80	00	??	00h
0f81	00	??	00h
0f82	00	??	00h
0f83	00	??	00h
0f84	00	??	00h
0f85	00	??	00h
0f86	00	??	00h
0f87	00	??	00h
0f88	00	??	00h
0f89	00	??	00h
0f8a	00	??	00h
0f8b	00	??	00h
0f8c	00	??	00h
0f8d	00	??	00h
0f8e	00	??	00h
0f8f	00	??	00h
0f90	00	??	00h
0f91	00	??	00h
0f92	00	??	00h
0f93	00	??	00h
0f94	00	??	00h
0f95	00	??	00h
0f96	00	??	00h
0f97	00	??	00h
0f98	00	??	00h
0f99	00	??	00h
0f9a	00	??	00h
0f9b	00	??	00h
0f9c	00	??	00h
0f9d	00	??	00h
0f9e	00	??	00h
0f9f	00	??	00h
0fa0	00	??	00h
0fa1	00	??	00h
0fa2	00	??	00h
0fa3	00	??	00h
0fa4	00	??	00h
0fa5	00	??	00h
0fa6	00	??	00h
0fa7	00	??	00h
0fa8	00	??	00h
0fa9	00	??	00h
0faa	00	??	00h
0fab	00	??	00h
0fac	00	??	00h
0fad	00	??	00h
0fae	00	??	00h
0faf	00	??	00h
0fb0	00	??	00h
0fb1	00	??	00h
0fb2	00	??	00h
0fb3	00	??	00h
0fb4	00	??	00h
0fb5	00	??	00h
0fb6	00	??	00h
0fb7	00	??	00h
0fb8	00	??	00h
0fb9	00	??	00h
0fba	00	??	00h
0fbb	00	??	00h

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0fbc	00	??	00h	
0fbd	00	??	00h	
0fbe	00	??	00h	
0fbf	00	??	00h	
0fc0	00	??	00h	
0fc1	00	??	00h	
0fc2	00	??	00h	
0fc3	00	??	00h	
0fc4	00	??	00h	
0fc5	00	??	00h	
0fc6	00	??	00h	
0fc7	00	??	00h	
0fc8	00	??	00h	
0fc9	00	??	00h	
0fca	00	??	00h	
0fcb	00	??	00h	
0fcc	00	??	00h	
0fcd	00	??	00h	
0fce	00	??	00h	
0fcf	00	??	00h	
0fd0	00	??	00h	
0fd1	00	??	00h	
0fd2	00	??	00h	
0fd3	00	??	00h	
0fd4	00	??	00h	
0fd5	00	??	00h	
0fd6	00	??	00h	
0fd7	00	??	00h	
0fd8	00	??	00h	
0fd9	00	??	00h	
0fda	00	??	00h	
0fdb	00	??	00h	
0fdc	00	??	00h	
0fdd	00	??	00h	
0fde	00	??	00h	
0fdf	00	??	00h	
0fe0	00	??	00h	
0fe1	00	??	00h	
0fe2	00	??	00h	
0fe3	00	??	00h	
0fe4	00	??	00h	
0fe5	00	??	00h	
0fe6	00	??	00h	
0fe7	00	??	00h	
0fe8	00	??	00h	
0fe9	00	??	00h	
0fea	00	??	00h	
0feb	00	??	00h	
0fec	00	??	00h	
0fed	00	??	00h	
0fee	00	??	00h	
0fef	00	??	00h	
0ff0	00	??	00h	
0ff1	00	??	00h	
0ff2	00	??	00h	
0ff3	00	??	00h	
0ff4	00	??	00h	
0ff5	00	??	00h	
0ff6	00 00	addr	0000	BOOTSTRAP Vector (Not used in th...
0ff8	08 c8	addr	TIMER_INTERRUPT	Timer Interrupt Vector
0ffa	00 00	addr	0000	External Interrupt Vector
0ffc	09 ba	addr	SWI_INTERRUPT	SWI Vector
0ffe	01 10	addr	RESET	RESET Vector