Cassette no.:	1	
Video taped:	17.02.87	
Product:	DELILAH	
Contents:	Hardware introduction	
Lecturer:	L. Bockelie and C.Cherrington	EN

Trimming Response Times to the Bone

FEATURES.

* Added CPU Performance
* On Board Memory
* Lower Component Cost
* Lower Power Consumption
* Fully software compatible with all previous ND-100 models.
* Battery backed up clock.

Added CPU Performance:

* 1.5 times ND-110/CX due to shorter cycle times.
* Shorter memory access time.
* Simplified cache leads to shorter buffered write cycles.

On board memory

* 2 or 4 Mb DRAM on CPU board
* Configured from address 0. (fixed)
* Can be disabled with a switch.
* Dual ported between CPU and ND-100 Bus
* 100 ns access time, fast page mode.
* Parity

FEATURES.

The calendar power is backed up with a battery, so that it is no longer necessary to update the clock. (As on RASK 2).

Bus bandwidth is 20% higher than RASK. (As on RASK 2).

Only RS-232 provided for the console, not Current Loop. (As on JAMES).

A new OPCOM command, LCS is provided. This will load the Control Store and do a Master Clear.

The old command MACL will do a Master Clear, without reloading the Control Store. (As on ND110 & ND110/CX).

Possible configurations:

Memory:	Speed:	Floating point format:
4Mb	1.5 x ND110/CX	32 bit
2Mb	1.5 x ND110/CX	32 bit
4Mb	1.5 x ND110/CX	48 bit
2Mb	1.5 x ND110/CX	48 bit
4Mb	1.0 x ND110/CX	32 bit
2Mb	1.0 x ND110/CX	32 bit
4Mb	1.0 x ND110/CX	48 bit
2Mb	1.0 x ND110/CX	48 bit

TECHNOLOGY.

* Two gate arrays in 1.5 um CMOS

* 1 megabit DRAM in SIP´s

* Static RAM with increased performance

* PAL´s with increased performance

* CMOS high speed/low power buffers

Gate array ND-DELILAH:

* LSI LOGIC LL10K series Compacted Array
* Channelless architecture
* 14000 gates used of 50000
* 224 pin Ceramic (later plastic) PGA
* 1.5 um CMOS technology
* 0.7 ns typical gate delay
* 1.5 times LL7K series performance (used in ND110/CX and SAMSON)
* Price initially the same as ND110/CX gate arrays.

Gate array ND-DELILAH:

Contains, from ND 110/CX:

* Gate array RMIC (1800 gates)
* Gate array RMAC (2500 gates)
* Gate array BUFALU (4900 gates)
* Interrupt System (2 x 2914)
* Trap System (4 x PAL)
* Decoding (3 x PAL + 12 x DIP)

TECHNOLOGY.

Gate array ND-DELDGA:

* NEC CMOS4A series Gate Array
* Channelled architecture
* 1400 gates used of 1600
* 120 pin Plastic PGA
* 1.5 um CMOS technology
* 0.9 ns typical gate delay
* Reduced performance compared to PAL´s
* Price ca. 50 NOK. (same as 1 x 9403)

Gate array ND-DELDGA:

Contains, from ND 110/CX:

* Panel FIFO (2 x 9403)
* Decode (6 x PAL + 1 DIP)
* Panel interrupt (2913)
* Power up (6 x DIP)
* Refresh control (4 x DIP)

Dynamic Random Access Memory:

* Used to implement 4 Mb on board memory
* 1 Megabit devices
* 100ns access time
* Fast page mode
* Mounted on SIP´s 4 on one side and 5 on the other.
* Low profile, can be fitted vertically
* 16 times more compact than 2MB board
* 4 times more compact than 8MB board
* 4 times more compact than Butterfly

Static Random Access Memory:

* 4Kx4 (Control store) 20-25ns access
  Gives 1.5 times ND-110/CX performance

* 2Kx8 (Cache, page tables) 25ns access
  Saves 8 packages. Improved performance

* 2Kx8 (Register file) 25ns access
  Saves 2 packages. Improved performance

PAL´s with 30% performance increase available at 2.5 times the price.

CMOS high speed buffers:

	delay	current sink	power consumption
74F244	6.5ns	64mA	60-90mA
74PCT244	6.5ns	64mA	25-50mA

These devices are still priced high.

	Delilah:	Rask:
No. of Cache Banks:	2	4
Microcode space:	7K	6K
Cache clear:	1 cycle	Up to 1K cycles

Instructions	Cache Bank	1K
Micro Instructions	Cache Bank	1K
Data	Cache Bank	1K

If we have the address we are writing to in the Instructions Cache, we must invalidate this before writing (to the Data Cache).

Buffered Write Cycles are approxemately twice as fast as on ND110/CX.

Instruction Cache and Micro Instruction Cache updated on FETCH.

Data Cache updated on Read and Write (Write through).

Only one set of used bits needed for the Instruction Cache and one set for the Data Cache.

This is because cache clear is instantaneous.

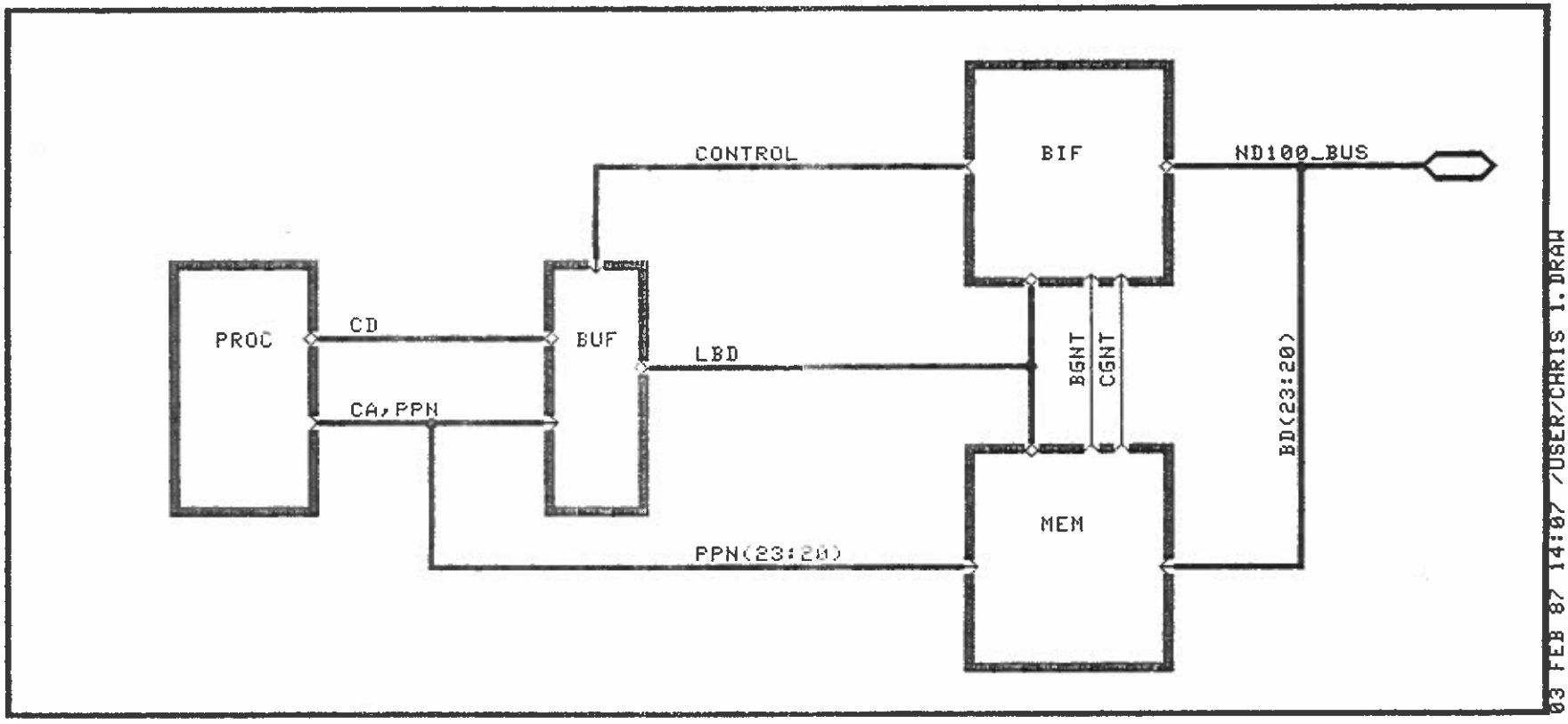
Only 1K microinstruction cache will free 1K to more microcode.

Cache Status Register format:

INHIBIT	Bit 4	=1 if last write only went to memory
CFIN	Bit 3	Allways 1
MANDIS	Bit 2	Cache off (switch)
CON	Bit 1	Cache on (switch)
CUP	Bit 0	Cache UPdated

Norsk Data

BUS INTERFACE & DUAL PORT MEMORY



BUS, PROCESSOR AND MEMORY INTERFACE

DUAL PORT MEMORY

- MAY BE CONFIGURED WITH:

  1) 2 MBYTES RAM

  OR 2) 4 MBYTES RAM

- USES 2 OR 4 1Mx9 SIP DRAM STRIPS
- BYTE WIDE PARITY
- PARITY ERROR ADDRESS/STATUS STORED FOR LOCAL MEMORY
- MEMORY SIZE CONTROLLED BY PAL
- ALL LOCAL MEMORY CAN BE SWITCHED OFF
- LOCAL MEMORY STARTS FROM ADDRESS 0
- HANDLES 2 SEMAPHORES:

  1) CPU
  2) BUS

  ACCESSES TO LOCAL MEMORY

- LOCAL MEMORY ARBITRATION PRIORITY:

  1) REFRESH — HIGHEST
  2) CPU (LAST WAS REFRESH)
  3) BUS (DMA)
  4) CPU — LOWEST

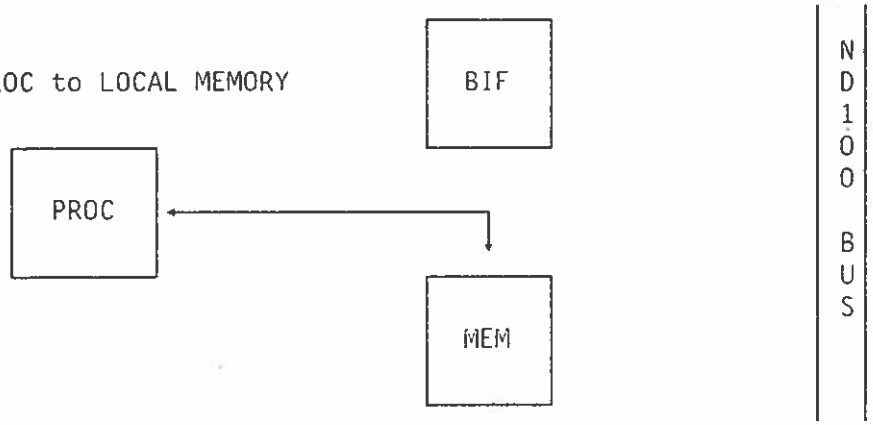
ND100 BUS INTERFACE

- Handles all ND100 Bus signals and timing
- Controls multiplexing of local BD
- Handles semaphore for ND100 Bus Memory
- Parity error address/status stored for ND100 memory
- Bus arbitration priority:

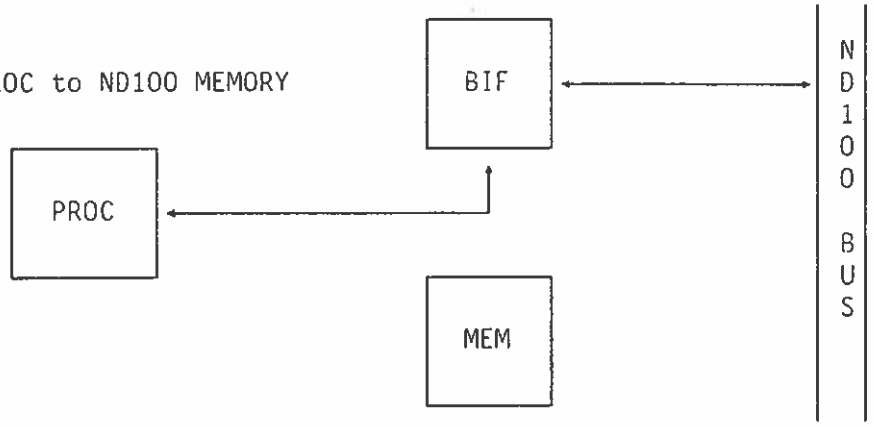
1) Refresh	HIGHEST
2) CPU (Last was Refresh)	.
3) DMA devices	.
4) CPU	. LOWEST

DATA PATHS

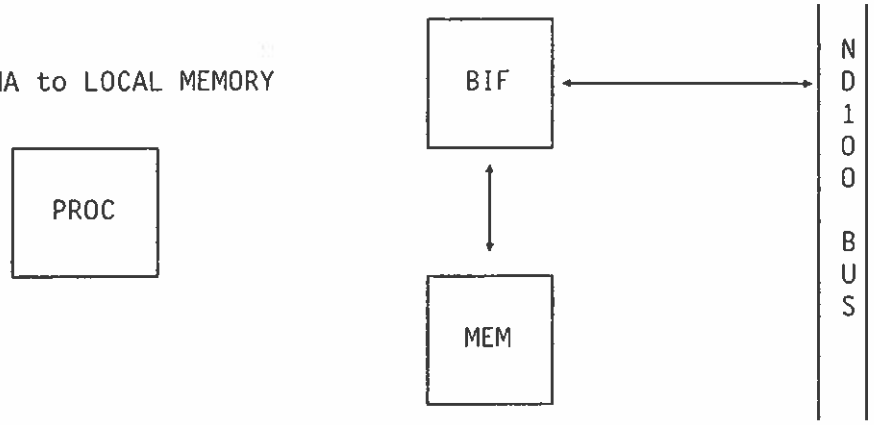
1) PROC to LOCAL MEMORY

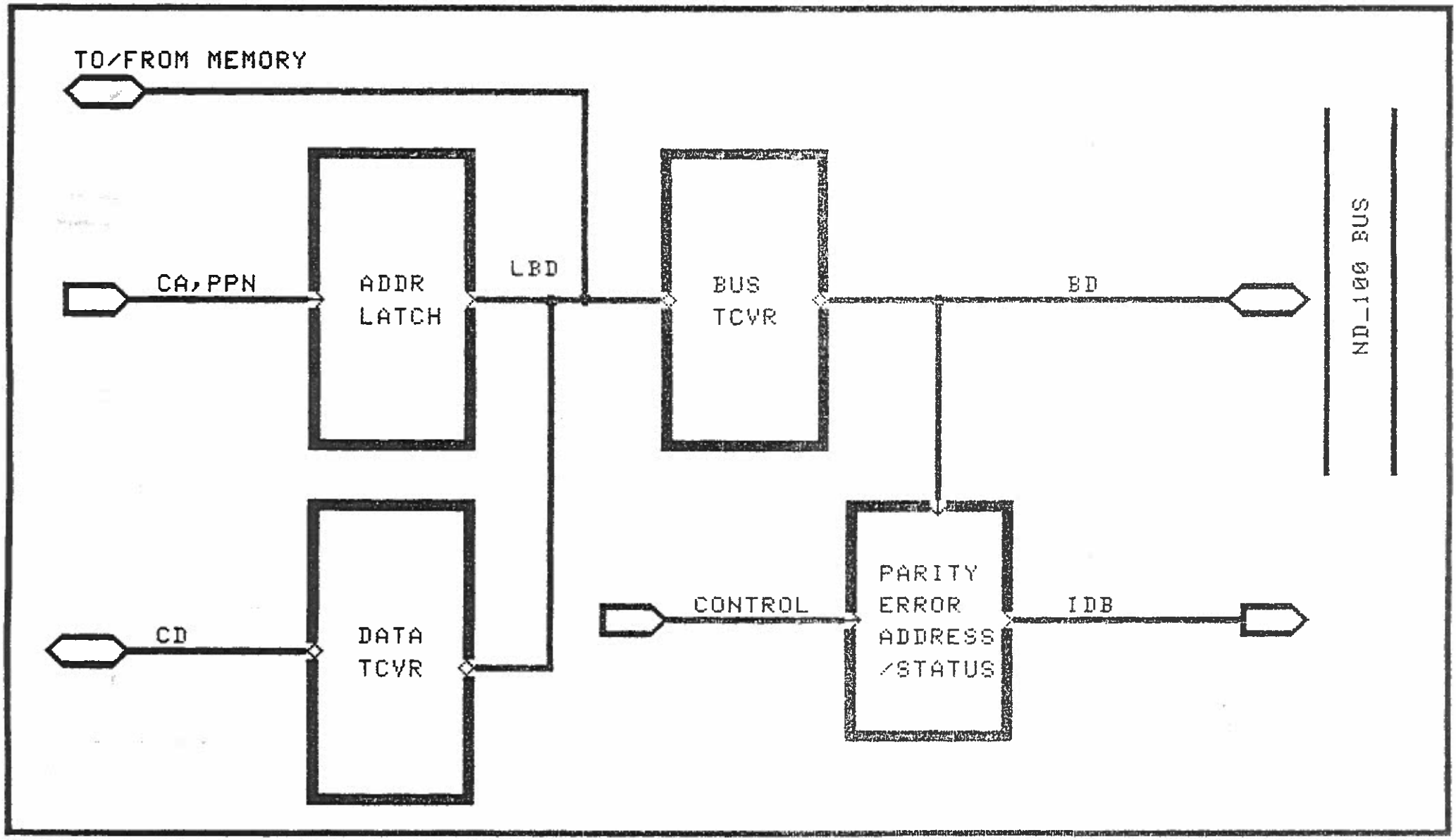


2) PROC to ND100 MEMORY



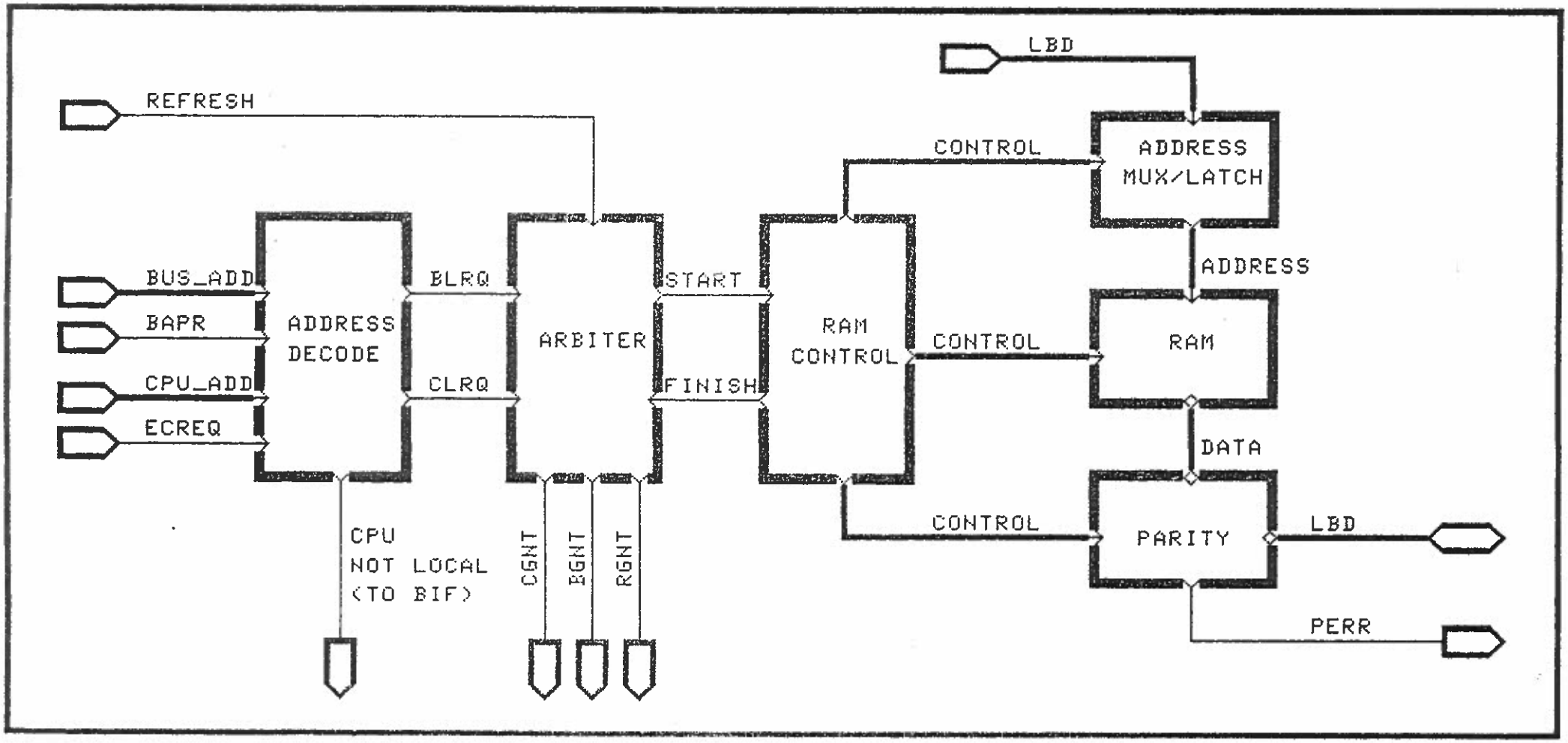
3) DMA to LOCAL MEMORY



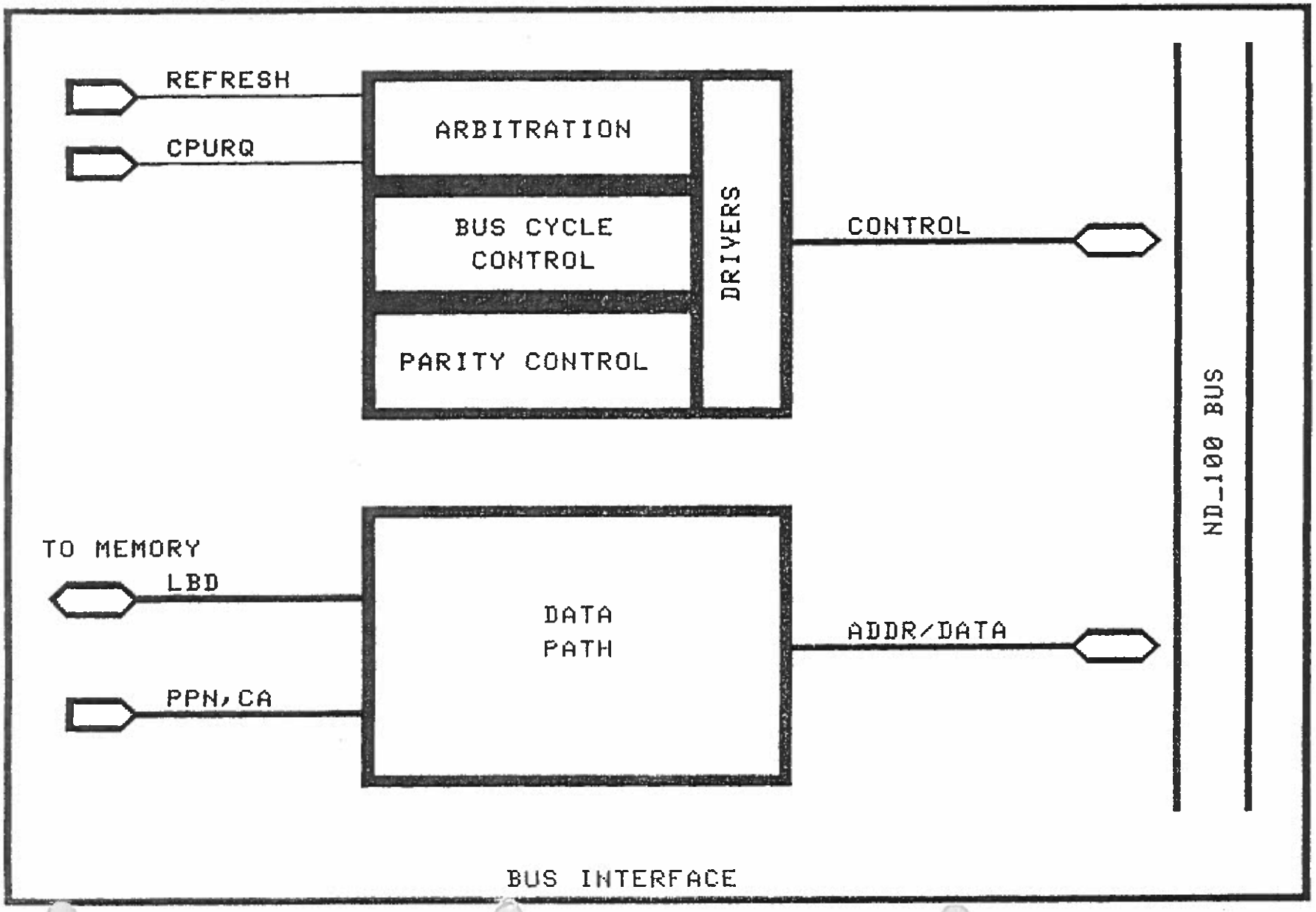


DELILAH BUS INTERFACE

DATA PATH



DELILAH MEMORY


REFRESH
CPURQ
ARBITRATION
BUS CYCLE CONTROL
PARITY CONTROL
DRIVERS
CONTROL
ND_100 BUS
TO MEMORY
LBD
PPN, CA
DATA PATH
ADDR/DATA
BUS INTERFACE

DELILAH INFORMATION PACK

CONTENTS: Page

SWITCHES AND INDICATORS

SW1 - Cache ON/OFF (illuminates LED1)

SW2 - switches local memory on/off

LED1 (RED) - indicates that cache has been switched OFF with SW1

LED2 (RED) - indicates that CPU is stopped

LED3 (GREEN) - indicates that CPU is running

LED4 (RED) - shows parity error in low byte of a word in local memory

LED5 (RED) - shows parity error in high byte of a word in local memory

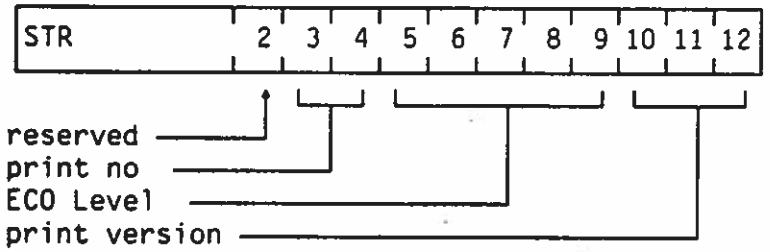
LED6 (GREEN) - shows that local memory has been granted to the CPU

LED7 (YELLOW)- shows that local memory has been granted to the ND100 Bus

STRAPS

STR1 - no strap => CD to tracer
strap => IDB to tracer

STR2-STR12 - hardware configuration strap field :



(• = STRAP)
(0 = NO STRAP)

print no: STR 3 4:

•	0	=	3202 (Delilah)

ECO level: STR 5 6 7 8 9

•	•	•	•	0	=	A
•	•	•	•	•	=	B
0	0	0	0	0	=	C
0	0	0	0	•	=	D
0	0	0	•	0	=	E
0	0	0	•	•	=	F
0	0	•	0	0	=	G
0	0	•	0	•	=	H
0	0	•	•	0	=	J
0	0	•	•	•	=	K
0	•	0	0	0	=	L
0	•	0	0	•	=	M
0	•	0	•	0	=	N
0	•	0	•	•	=	P
0	•	•	0	0	=	Q
0	•	•	0	•	=	R
0	•	•	•	0	=	S
0	•	•	•	•	=	T
•	0	0	0	0	=	U
•	0	0	0	•	=	V
•	0	0	•	0	=	W
•	0	0	•	•	=	X
•	0	•	0	0	=	Y
•	0	•	0	•	=	Z
•	0	•	•	0	=	BA
•	0	•	•	•	=	BB
•	•	0	0	0	=	BC
•	•	0	0	•	=	BD
•	•	0	•	0	=	BE
•	•	0	•	•	=	BF
•	•	•	0	0	=	BG
•	•	•	0	•	=	BH

Print version - to be defined

STR13-STR15 - see "CGA TEST MULTIPLEXER"

STR16 - no strap => traps enabled
strap => traps disabled

TEST POINTS

TP1	- INTRQ~ from CGA
TP2-TP6	- see "CGA TEST MULTIPLEXER"

DELILAH CGA - TEST MULTIPLEXER

There are a number of nodes within the Delilah CGA which are brought out to test points on the PCB, to allow monitoring of events internal to the gate array. Three jumpers, STR13 - STR15 determine the signals which will appear on test points TP2 - TP6 according to the following table (• = link IN, blank = no link):

STR			TP				
15	14	13	2	3	4	5	6
			0	TVEC3	TVEC2	TVEC1	TVEC0
		•	DEEP	SC6	SC5	SC4	SC3
	•		RESTR	CFETCH	ODD	DZD	LCZ~
	•	•	1	T~	P~	COND	UP~
•			CRY	SGR	F15	ZF	OVF
•		•	1	XFETCH~	WP~	PTM	MI
•	•		OSTOP~	WRITE~	CBRK~	IND~	VACC~
•	•	•	1	VEX	LDIRV	CSMREQ	1

DELILAH IDB SOURCE SELECTION

IDBS (4:0)		EXPLANATION	COMMENTS
0	ALU	ALUF OR A-OPR	CGA (ALU)
1	BMG	BIT MASK GENERATOR	CGA (ALU)
2	GPR	GENERAL PURPOSE REGISTER	CGA (ALU)
3	DBR	DB/CACHE READ REGISTER	CGA (ALU)
4	ARG	MICRO ARGUMENT REGISTER	CGA (ALU)
5	REG	REGISTER FILE	CPU
6	STS	MACRO STATUS REGISTER	CGA (ALU)
7		UNUSED	OLD MMU
10	BARG	B OPERAND AS ARG(3:0)	CGA (ALU)
11	SWAP	BYTE SWAP REGISTER	CGA (ALU)
12	PEA	PARITY ERROR ADDRESS	MEM & BIF
13	PES	PARITY ERROR STATUS & ADDRESS	MEM & BIF
14	AARG	A OPERAND AS ARG(6:3)	CGA (ALU)
15	PICS	PIC STATUS	CGA (INTR)
16	IOR	IO REGISTER	IO
17		UNUSED	
20	MIPANS	PANEL STATUS	IO
21	MAPANS	PANEL STATUS, RESET BIT12	IO
22	GPR,SEXT	GPR, SIGN EXTENDED	CGA (ALU)
23	PGS	PAGING STATUS REGISTER	CGA (IDBCTL)
24	CSR	CACHE STATUS REGISTER	CPU/MMU/CSR
25	PCR	PAGING CONTROL REGISTER	CGA (MAC)
26	ALD	ALD & PRINT STATUS	IO
30	RCS	CONTROL STORE WORD Does not directly enable onto IDB except via Command RWCS (36.1)	
31	PICV	PIC VECTOR	CGA (INTR)
32		UNUSED (OLD LBR)	
33		UNUSED (OLD PTC)	
34		UNUSED (OLD JMPA)	
35	RINR	INSTALLATION NUMBER	IO
36	PICMASK	PIC MASK REGISTER	CGA (INTR)
37	UART	READ UART - In conjunction with Command CEUART (05)	IO

DELILAH COMMAND DECODING

COMMAND	MNEMONIC	SHORT WORD	SHORT LONG WORD	RDTRIG	DWTRIG	WRITE	FETCH	FORCE	MREQ	LDIRV	LDGPR	LDBRR
0	NONE	*	*	.	.	.	.	.	.	.	.	.
1	LDPIL	*	*	.	.	.	.	.	.	.	.	.
2	LDGPR	*	*	.	.	.	.	.	.	.	*	.
3	EWRF	*	*	.	.	.	.	.	.	.	.	.
4	CLIRQ	*	*	.	.	.	.	.	.	.	.	.
5.0	UART,DATA	.	.	.	.	.	.	.	.	.	.	.
5.1	UART,STATUS	.	.	.	.	.	.	.	.	.	.	.
5.2	UART,MODE	.	.	.	.	.	.	.	.	.	.	.
5.3	UART,COMM	.	.	.	.	.	.	.	.	.	.	.
6.0		.	*	.	.	.	.	.	.	.	.	.
6.1		*	*	.	.	.	.	.	.	.	.	.
6.2	LDPANC	.	*	.	.	.	.	.	.	.	.	.
6.3	LDPCR	*	*	.	.	.	.	.	.	.	.	.
7.0	SIOC	.	*	.	.	.	.	.	.	.	.	.
7.1	SIOC	*	*	.	.	.	.	.	.	.	.	.
7.2	SIOC	.	*	.	.	.	.	.	.	.	.	.
7.3	SIOC	*	*	.	.	.	.	.	.	.	.	.
10	SLOW	.	*	.	.	.	.	.	.	.	.	.
11	EPIC	.	*	.	.	.	.	.	.	.	.	.
12	SMPID	.	*	.	.	.	.	.	.	.	.	.
13	START	.	*	.	.	.	.	.	.	.	.	.
14	STOP	*	*	.	.	.	.	.	.	.	.	.
15	CLRTC	*	*	.	.	.	.	.	.	.	.	.
16	CLFF	*	*	.	.	.	.	.	.	.	.	.
17	LDLC	*	*	.	.	.	.	.	.	.	.	.

COMMAND	MNEMONIC	SHORT	SLOW	RT	DT	WRITEH	FETCH	FORM	MREQ	LDIRV	LDGPR	LDDBR
20.0	LDSEG	*	*	.	.	.	.	.	.	.	.	.
20.1		*	*	.	.	.	.	.	.	.	.	.
20.2		*	*	.	.	.	.	.	.	.	.	.
20.3	LDIRV	*	*	.	.	.	.	.	.	*	.	.
21.0	WCHIM	.	*	.	.	.	.	.	.	.	.	.
21.1	SSEMA	*	*	.	.	.	.	.	.	.	.	.
21.2	CCLR	*	*	.	.	.	.	.	.	.	.	.
21.3	LDEXM	*	*	.	.	.	.	.	.	.	.	.
22.0	IREAD,PT	.	*	*	*	.	.	.	*	.	.	*
22.1	IREAD,APT	.	*	*	*	.	.	.	*	.	.	*
22.2	MAP	.	*	.	.	.	.	*	.	*	*	.
22.3	CNEXT,NWP	.	*	*	.	.	*	*	*	*	.	*
23.0	CJMP,F15	.	*	*	.	.	*	*	*	*	.	*
23.1	CJMP,NF15	.	*	*	.	.	*	*	*	*	.	*
23.2	CJMP,F=0	.	*	*	.	.	*	*	*	*	.	*
23.3	CJMP,NF=0	.	*	*	.	.	*	*	*	*	.	*
24.0	CNEXT,SGR	.	*	*	.	.	*	*	*	*	.	*
24.1	CNEXT,NSGR	.	*	*	.	.	*	*	*	*	.	*
24.2	CNEXT,CRY	.	*	*	.	.	*	*	*	*	.	*
24.3	CNEXT,NCRY	.	*	*	.	.	*	*	*	*	.	*
25.0	CNEXT,F15	.	*	*	.	.	*	*	*	*	.	*
25.1	CNEXT,NF15	.	*	*	.	.	*	*	*	*	.	*
25.2	CNEXT,F=0	.	*	*	.	.	*	*	*	*	.	*
25.3	CNEXT,NF=0	.	*	*	.	.	*	*	*	*	.	*
26.0	JMP,*	.	*	*	.	.	*	*	*	*	.	*
26.1	JMP,B	.	*	*	.	.	*	*	*	*	.	*
26.2	JMP,I	.	*	*	.	.	*	*	*	*	.	*
26.3	JMP,X	.	*	*	.	.	*	*	*	*	.	*
27.0	JMP,XB	.	*	*	.	.	*	*	*	*	.	*
27.1	JMP,XI (,B)	.	*	*	.	.	*	*	*	*	.	*
27.2		.	*	*	.	.	*	*	*	*	.	*
27.3	CONTINUE	.	*	*	.	.	*	*	*	*	.	*

COMMAND	MNEMONIC	SHORT	SLOW	RT	DT	WRITE	FETCH	FORM	MREQ	LDIRV	LDGPR	LDDBR
30.0	AREAD,*	.	*	*	*	.	.	.	*	.	.	*
30.1	AREAD,B	.	*	*	*	.	.	.	*	.	.	*
30.2	AREAD,I (,B)	.	*	*	*	.	.	.	*	.	.	*
30.3	AREAD,X	.	*	*	*	.	.	.	*	.	.	*
31.0	AREAD,XB	.	*	*	*	.	.	.	*	.	.	*
31.1	AREAD,XI (,B)	.	*	*	*	.	.	.	*	.	.	*
31.2		.	*	*	*	.	.	.	*	.	.	*
31.3	AREAD,NEXT	.	*	*	*	.	.	.	*	.	.	*
32.0	AWRITE,*	.	*	.	*	*	.	.	*	.	.	.
32.1	AWRITE,B	.	*	.	*	*	.	.	*	.	.	.
32.2	AWRITE,I (,B)	.	*	.	*	*	.	.	*	.	.	.
32.3	AWRITE,X	.	*	.	*	*	.	.	*	.	.	.
33.0	AWRITE,XB	.	*	.	*	*	.	.	*	.	.	.
33.1	AWRITE,XI (,B)	.	*	.	*	*	.	.	*	.	.	.
33.2	AWRITE,HOLD	.	*	.	*	*	.	.	*	.	.	.
33.3	AWRITE,NEXT	.	*	.	*	*	.	.	*	.	.	.
34.0	READ,PT	.	*	*	*	.	.	.	*	.	.	*
34.1	READ,APT	.	*	*	*	.	.	.	*	.	.	*
34.2	READ,HOLD	.	*	*	*	.	.	.	*	.	.	*
34.3	EXAMINE	.	*	*	*	.	.	.	*	.	.	*
35.0	WRITE,PT	.	*	.	*	*	.	.	*	.	.	.
35.1	WRITE,APT	.	*	.	*	*	.	.	*	.	.	.
35.2	WRITE,HOLD		*	.	*	*	.	.	*	.	.	.
35.3	DEPOSIT	.	*	.	*	*	.	.	*	.	.	.
36.0	ADCS (LWCA)	.	*	.	.	.	.	.	.	.	.	.
36.1	RWCS	.	.	.	.	.	.	.	.	.	.	.
36.2	MACL	.	*	.	.	.	.	.	.	.	.	.
36.3	XSLOW	.	.	.	.	.	.	.	.	.	.	.
37.0		.	*	.	.	.	.	.	.	.	.	.
37.1		.	*	.	.	.	.	.	.	.	.	.
37.2	IDENT	.	*	.	.	.	.	.	.	.	.	*
37.3	IOX	.	*	.	.	.	.	.	.	.	.	*

20 June 1986

DELILAH - LA SOURCE

	SHADOW			$\overline{\text{SHADOW}}$						
LA	REX	SEX	EX	PEX	POF	EX		SEX-REX		VEX
						PT	APT	PT	APT	
23	0	0	0	SEG7	0	0	0	0	0	0
22	0	0	0	SEG6	0	0	0	0	0	0
21	0	0	0	SEG5	0	0	0	0	0	SEG5
20	0	0	0	SEG4	0	0	0	0	0	SEG4
19	0	0	$\overline{\text{A10}}$	SEG3	0	$\overline{\text{PCR14}}$	$\overline{\text{PCR10}}$	0	0	SEG3
18	0	0	A9	SEG2	0	PCR13	PCR9	0	0	SEG2
17	A7	A8	A8	SEG1	0	PCR12	PCR8	PCR10	PCR8	XPT1
16	A6	A7	A7	SEG0	0	PCR11	PCR7	PCR9	PCR7	XPT0
15	A5	A6	A6	A15	SAME					A15
14	A4	A5	A5	A14						A14
13	A3	A4	A4	A13						A13
12	A2	A3	A3	A12						A12
11	A1	A2	A2	A11						A11
10	A0	A1	A1	A10						A10
9	A9	SAME								A9
8	A8									A8
7	A7									A7
6	A6									A6
5	A5									A5
4	A4									A4
3	A3									A3
2	A2									A2
1	A1									A1
0	A0									A0

12 October 1986

DELILAH TRAP SYSTEM

PRIORITY	VECT	FTRAP	VTRAP	VACC	WIRE	FETCH	ENTC	IRQ	IPAUSE	DSTOP	PPP 543	PP 21	PP 09	PP 10	TRAP	LEVEL	PVIO
1	0001	X	X	1	X	X	X	X	X	X	000	XX	XX	XX	PGF	1	1
2	0010	X	X	1	1	X	X	X	X	X	0XX	XX	XX	XX	WPV	1	1
		X	X	1	X	1	X	X	X	X	X00	XX	XX	XX	IPV	1	1
		X	X	1	X	X	1	X	X	X	XX0	XX	XX	XX	FPV	1	1
		X	X	1	0	0	0	X	X	X	X0X	XX	XX	XX	RPV	1	1
		X	X	1	X	X	X	X	X	X	XXX	XX	1X	0X	RV	1	0
		X	X	1	X	X	X	X	X	X	XXX	XX	X1	00	RV	1	0
		X	X	1	X	X	X	X	X	X	XXX	XX	11	X0	RV	1	0
3	0101	X	X	1	1	X	X	X	X	X	1XX	0X	XX	XX	WIP	2	0
6	0100	X	X	1	X	X	X	X	X	X	XXX	X0	XX	XX	PGU	2	0
8	0011	X	X	1	X	X	1	X	X	X	XX1	XX	0X	1X	RD	2	0
		X	X	1	X	X	1	X	X	X	XX1	XX	00	X1	RD	2	0
		X	X	1	X	X	1	X	X	X	XX1	XX	X0	11	RD	2	0
12	1100	1	X	1	X	X	1	X	X	X	XXX	XX	XX	XX	FTRP	3	0
13	1101	X	1	1	X	X	X	X	X	X	XXX	XX	XX	XX	VTRP	3	0
14	1110	X	X	X	X	X	1	1	1	0	XXX	XX	XX	XX	PAN	3	0
15	1111	X	X	X	X	X	1	1	0	X	XXX	XX	XX	XX	MAC	3	0

VTRP = Spare Trap when VACC
FTRP = Spare Trap when FETCH * VACC (see note below)

Priority: Level 1 > Level 2 > Level 3
(Level 3 = /Level 1 * /Level 2)

NOTE:
If a PANel or MACro interrupt is pending when a FETCH is executed, VACC will be suppressed. This will result in the suppression of all other traps (which are dependant on VACC) until the MACro or PANel interrupt has been processed.