# Verilog code

The Verilog code has been split into subfolder matching the structure of the LogiSim and Design Documents

1. DELILAH-CPU
2. DECODE-GateArray
3. CPU-BOARD-3202

|------------------|----------|

| **Folder** | **Status** |
| --- | --- |
| DELILAH-CPU | Started |
| DECODE-GateArray | Started |
| CPU-BOARD-3202 | Started |
| ---------- | ---------- |