TEL AVIV UNIVERSITY אוניברסיטת תל אביב

Iby and Aladar Fleischman Faculty of Engineering Tel Aviv University
הפקולטה להנדסה ע"ש איבי ואלדר פליישמן אוניברסיטת תל-אביב

0512.4490 Advanced Computer Architecture Lab syllabus - fall 2021

Lab Instructor:
Roger Kahn – rogerka@tauex.tau.ac.il

Schedule:
The lab meets at 8am-11am on Tuesdays. The meetings are 3 hours long and your attendance is important for succeeding in the assignments. Pay attention to the detailed schedule below, as some of the weeks are different due to vacations.

	Group 01	Subject
Week #1	12.10.21	Lab #1a
Week #2	19.10.21	Lab #1b
Week #3	26.10.21	Lab #2a
Week #4	2.11.21	Lab #2b
Week #5	9.11.21	Lab #3a
Week #6	16.11.21	Lab #3b
Week #7	23.11.21	Lab #4a
Week #8	7.12.21	Lab #4b
Week #9	14.12.21	Lab #5a
Week #10	21.12.21	Lab #5b
Week #11	28.12.21	Lab #6

Syllabus:

In this lab we'll design and implement an embedded processor, suited for integration into ASIC SoC. We'll learn hierarchical design methodology with emphasis on verification, implementing the processor in high level ISA simulator, low level cycle accurate simulator, and the Verilog hardware description language. We'll start with a simple RISC processor, and enhance it with pipelining and branch prediction. Assignments are to be done in pairs.

Lab 1 High level ISA RISC simple processor simulator and verification.
Lab 2 Low level cycle accurate simple processor simulator, verification vs the high-level simulator.
Lab 3 Verilog introduction.
Lab 4 Verilog simple processor implementation and verification vs the low-level simulator.
Lab 5 Pipelining the processor + branch prediction, low level C simulation.
Lab 6 Pipelining the processor + branch prediction, Verilog implementation.

Grades: the final grade will be the average of the best 5 lab reports out of the 6 reports.