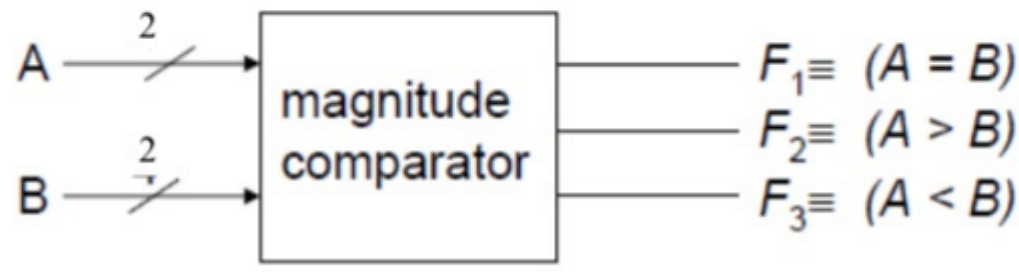
# DIGITAL LOGC DESIGN
# HOMEWORK

# Design the following circuits using Logisim Software:

## 1. 2-bit Magnitude Comparator Circuit:

Magnitude Comparator is a combinational circuit that compares 2 bits. It generates three outputs F1, F2, and F3.




### Truth TAble of 2-Bit Magnitude comparator

| INPUT | | | | OUTPUT | | |
|---|---|---|---|---|---|---|
| A1 | A0 | B1 | B0 | A<B | A=B | A>B |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

# iii. Simplify the function using (K-Map)

A<B

| A1A0 \ B1B0 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 1 | 1 |
| 01 | 0 | 0 | 1 | 1 |
| 11 | 0 | 0 | 0 | 0 |
| 10 | 0 | 0 | 1 | 0 |

=A1’B1+A1’A0’B0+A0’B1B0

A>B

| A1A0 \ B1B0 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 |
| 01 | 1 | 0 | 0 | 0 |
| 11 | 1 | 1 | 0 | 1 |
| 10 | 1 | 1 | 0 | 0 |

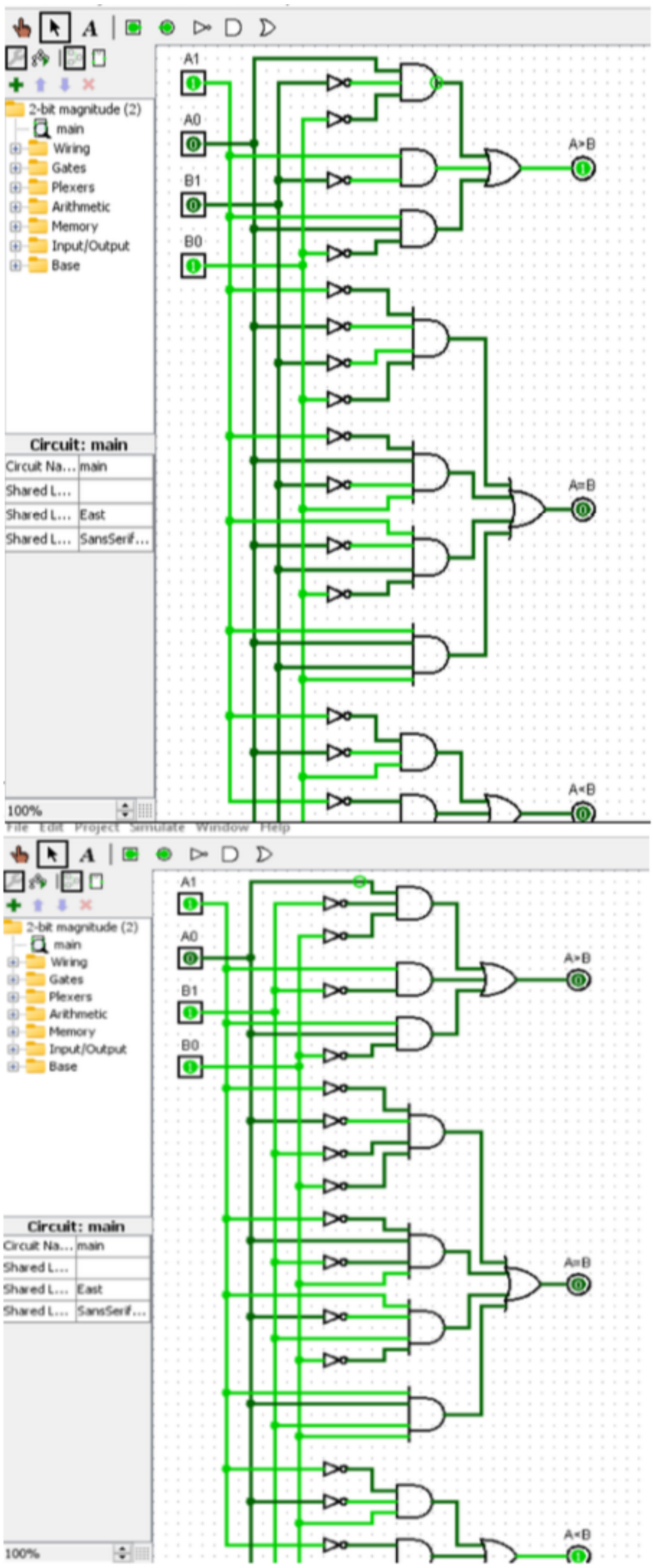
=A1B1’+A0B1'B0’+A1A0B0’

A=B

| 1A0 \ B1B0 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 0 | 0 | 0 |
| 01 | 0 | 1 | 0 | 0 |
| 11 | 0 | 0 | 1 | 0 |
| 10 | 0 | 0 | 0 | 1 |

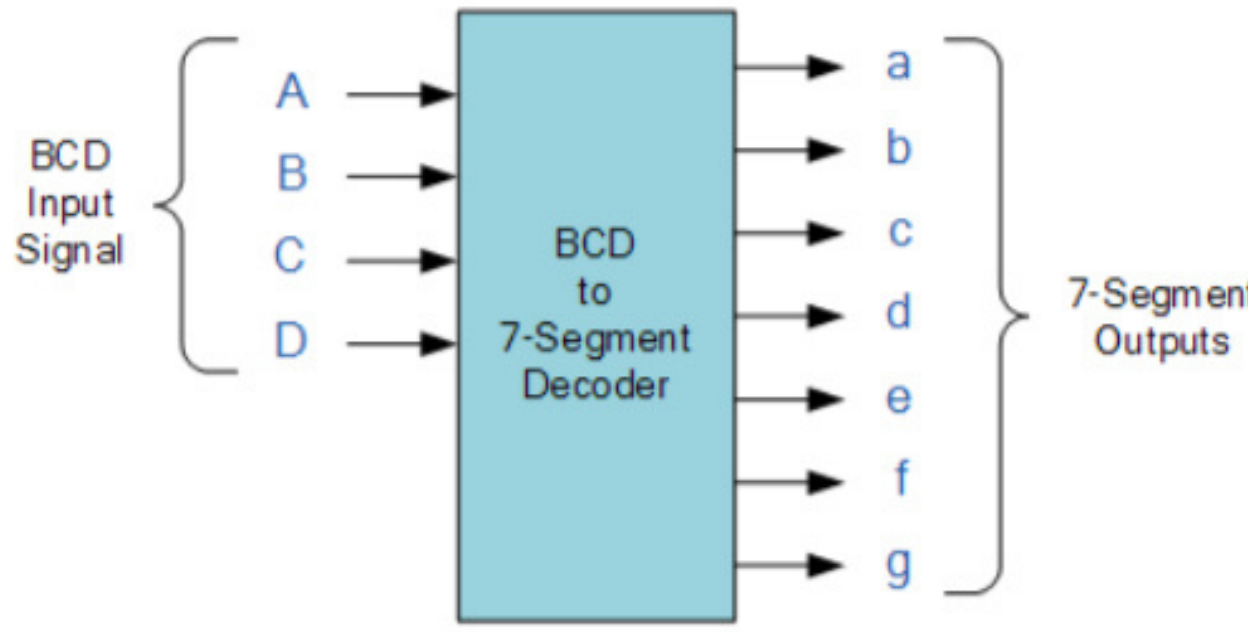
=A1’A0’B1’B0’+A1’A0B1'B0+A1A0B1B0+A1A0’B1B0’

# Draw logic gates



## 2. BCD to 7-Segment Decoder Circuit:

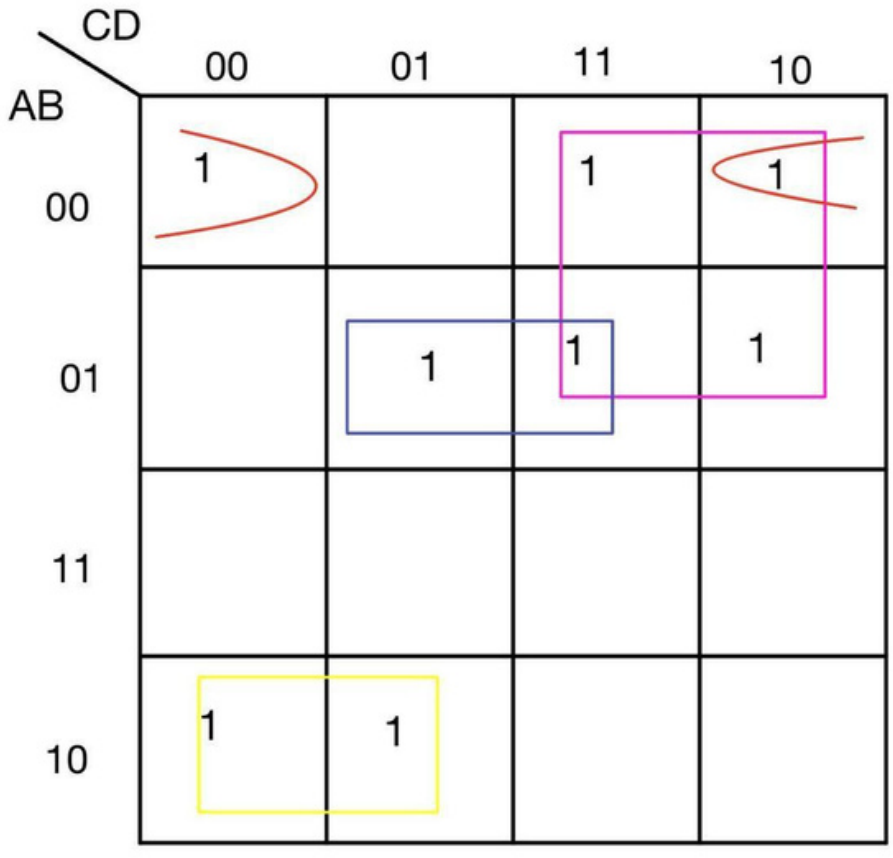
A seven-segment decoder is a digital circuit designed to drive a very common type of digital display device: a set of LED (or LCD) segments that render numerals 0 through 9 at the command of a four-bit code: in Logisim use 7-segment display.



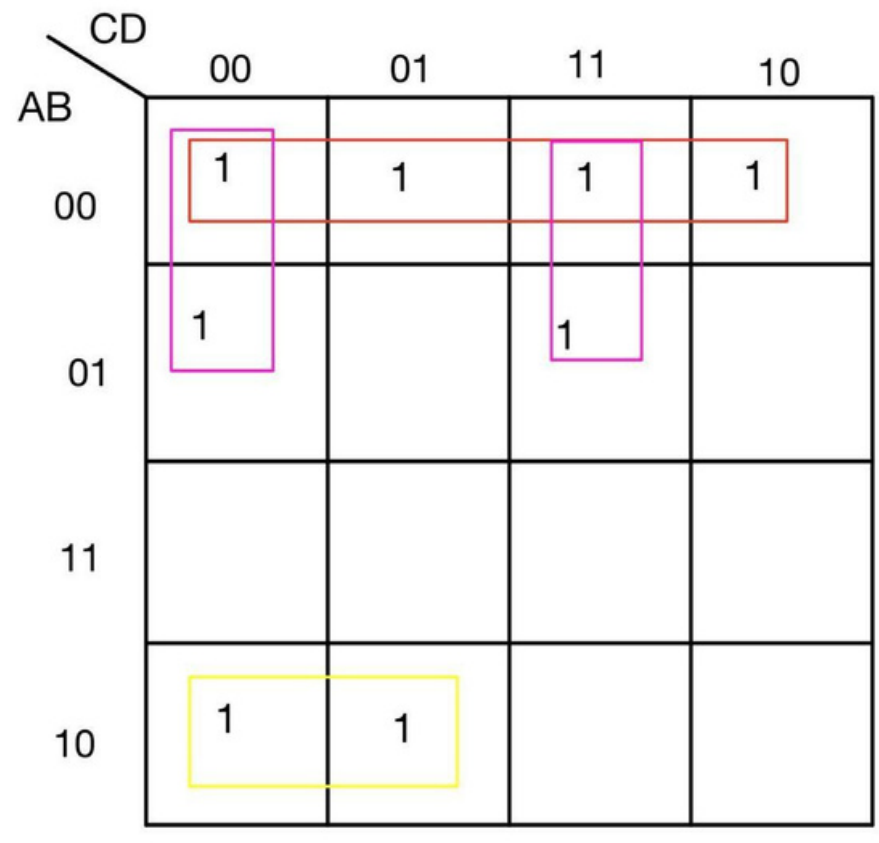

## ii. Build a truth table for input and output

| A | B | C | D | a | b | c | d | e | f | g |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

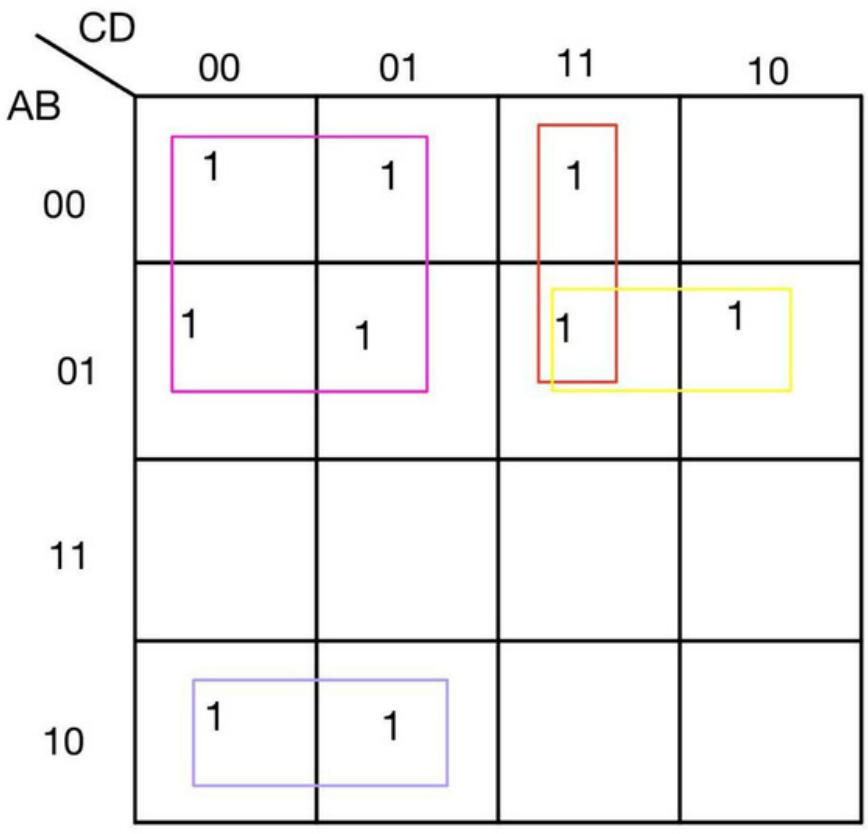
## iii. Simplify the function using (K-Map)



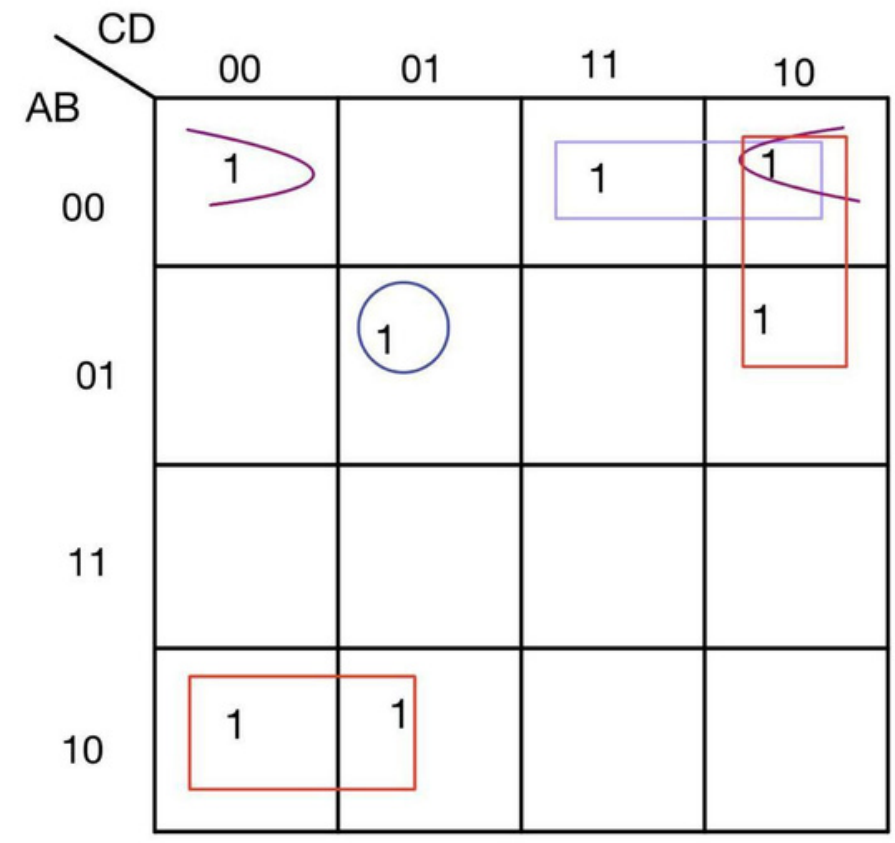

a=A’C+A’BD+AB’C’+A’B’D’



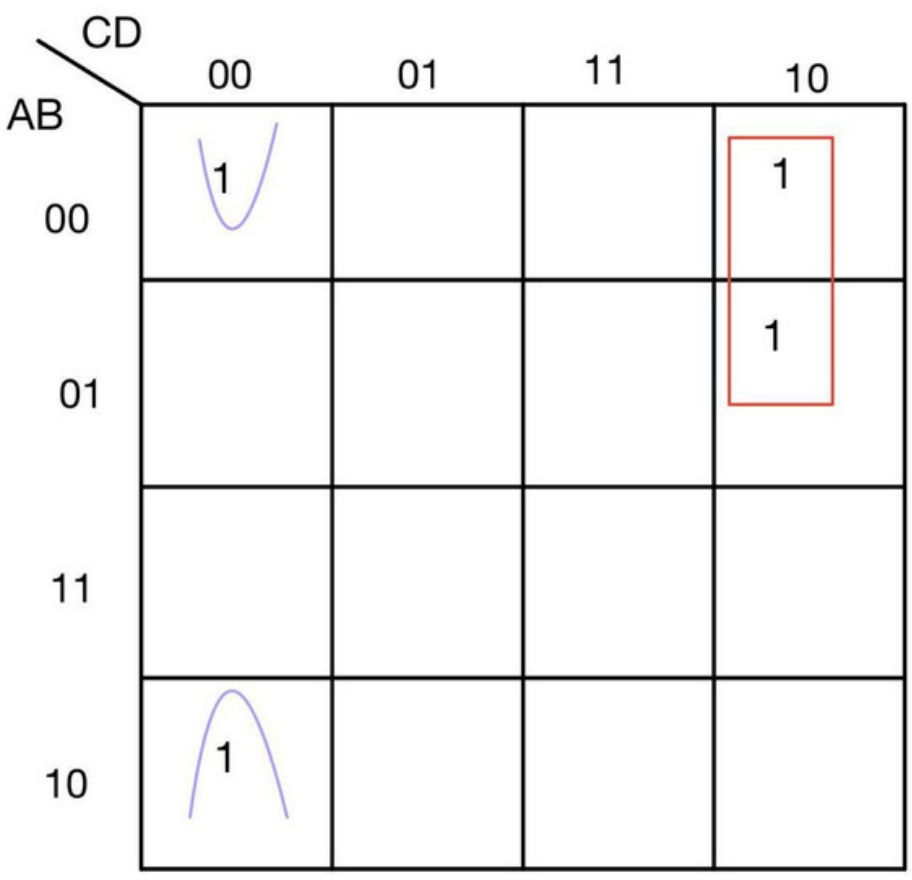

b=A’B’+A’C’D’+A’CD+AB’C”



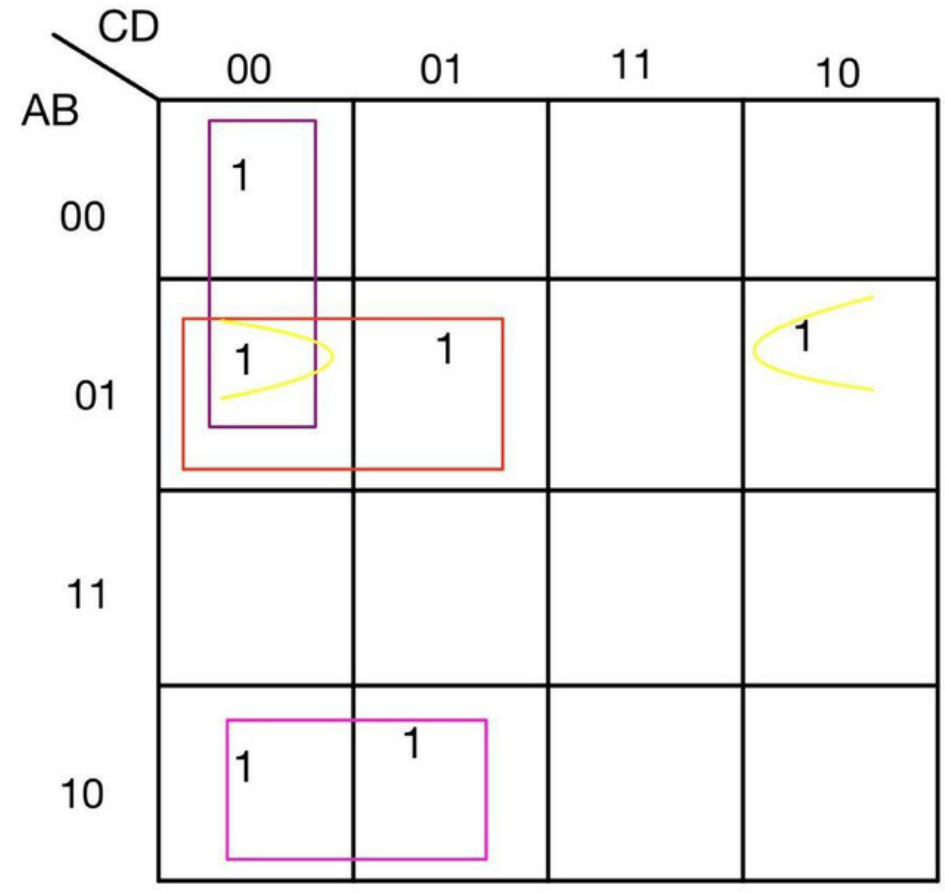

c=A’C’+A’CD+A’BC+AB’C’



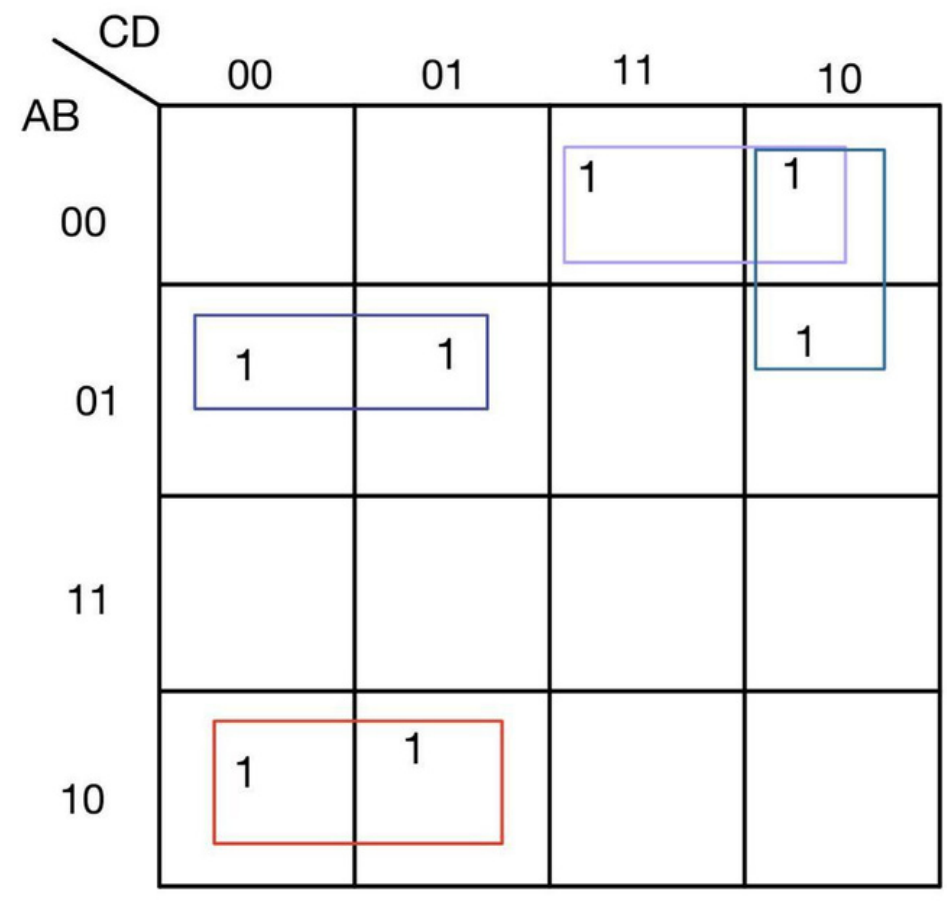

d=A’B’C+A’CD’+A’BC’D+AB’C’+A’B’D’




e=A’CD’+B’C’D’

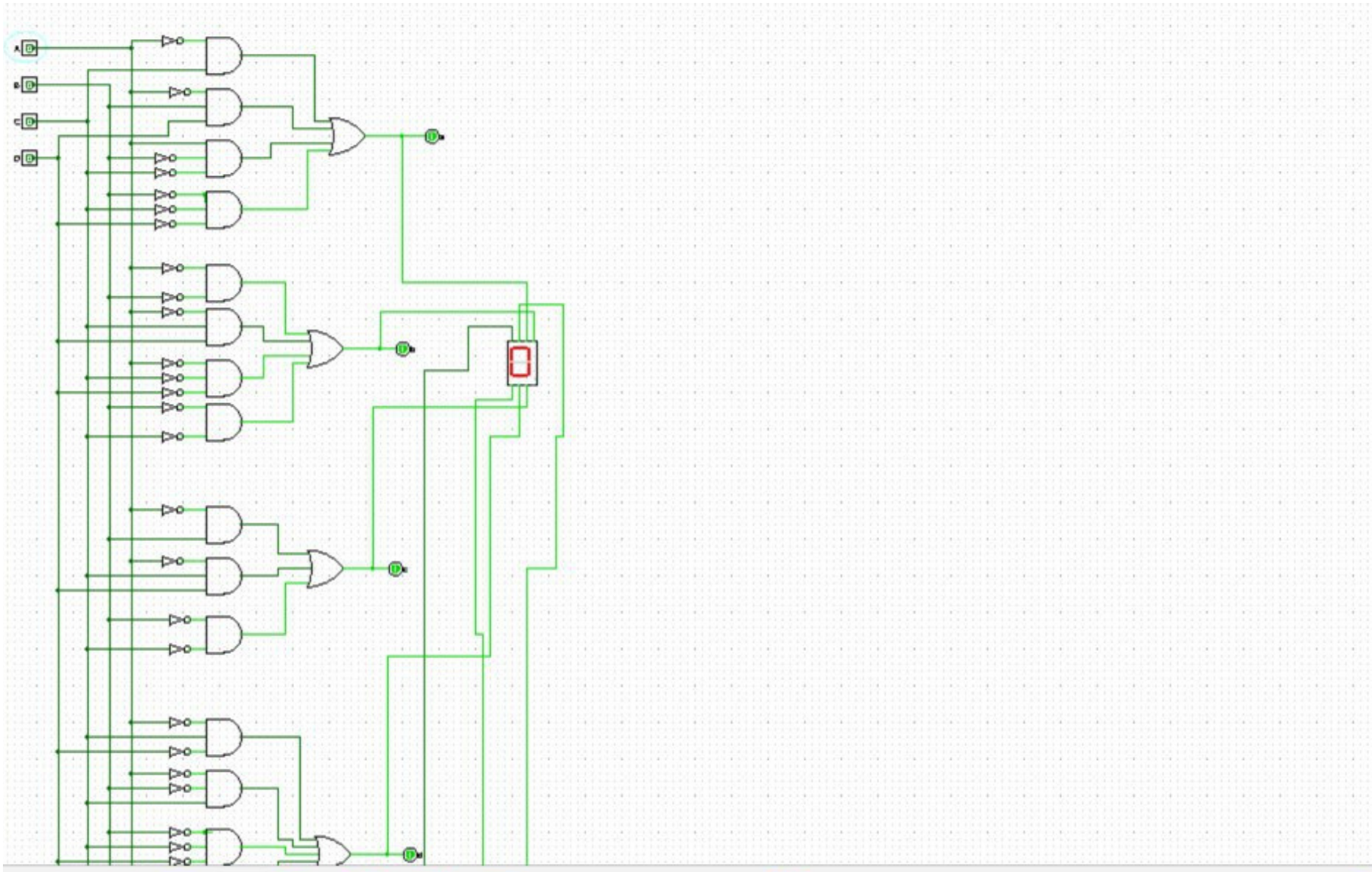


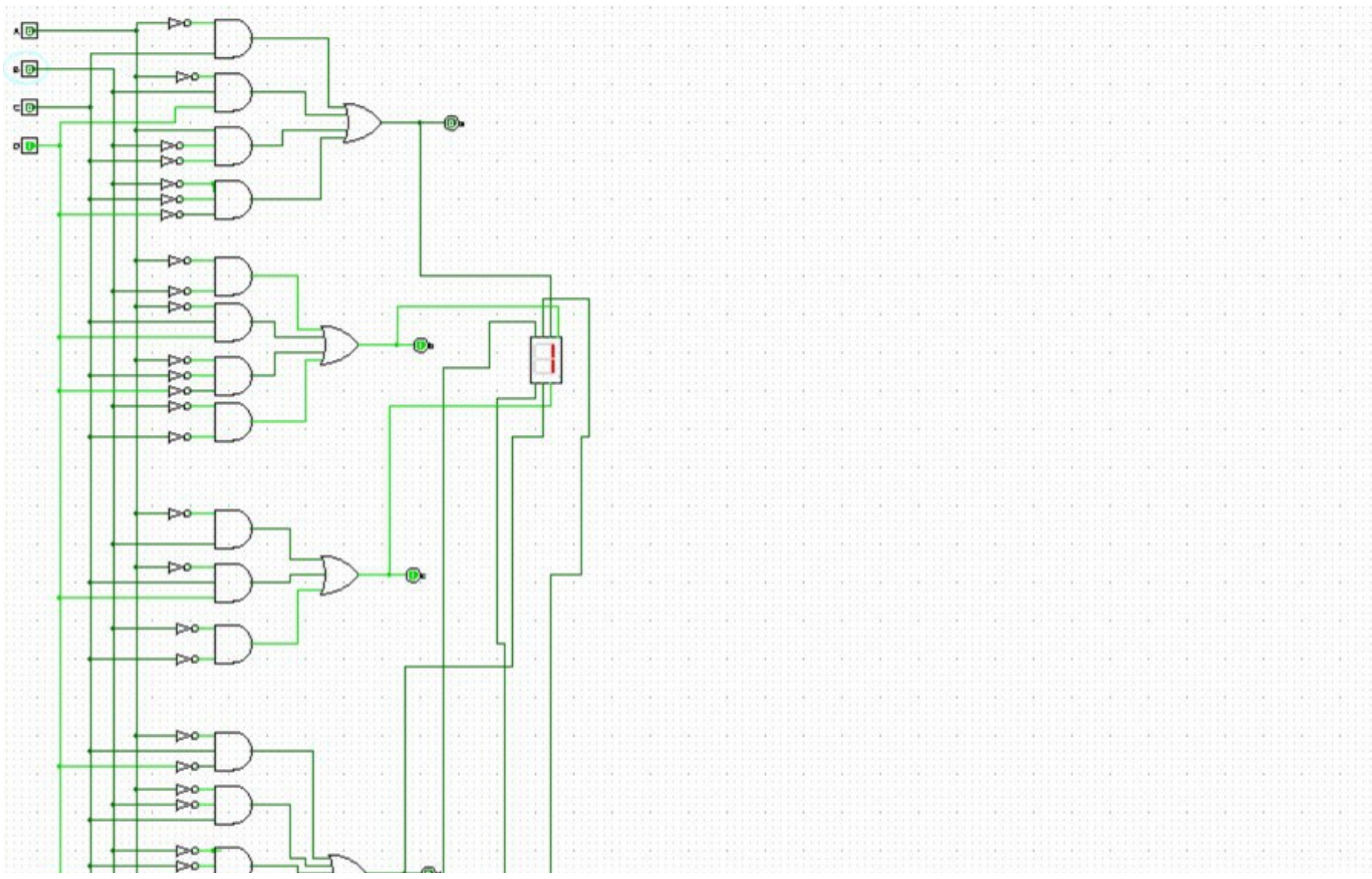

f=A’C’D’+A’BC’+A’BD’+AB’C’

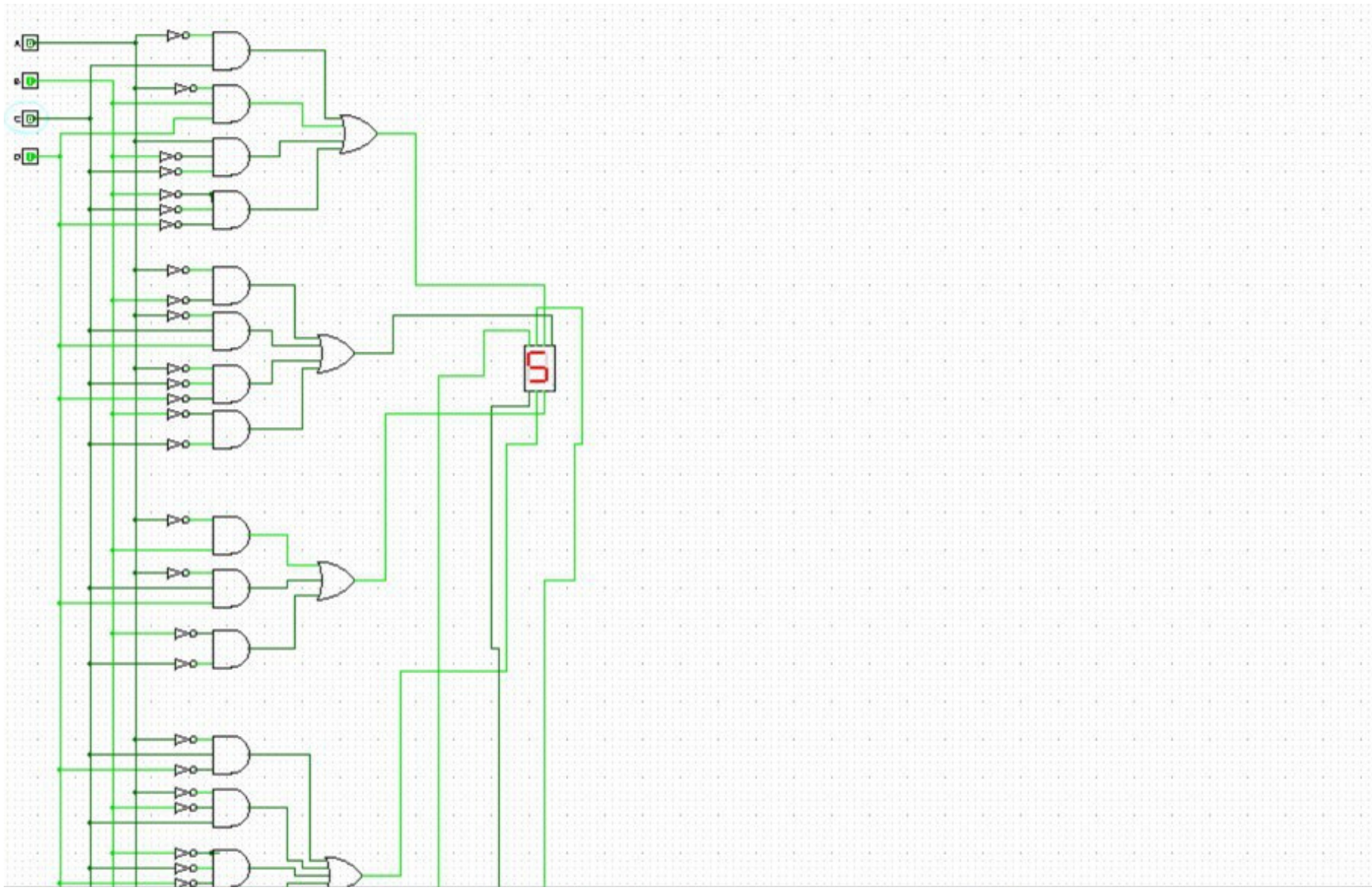


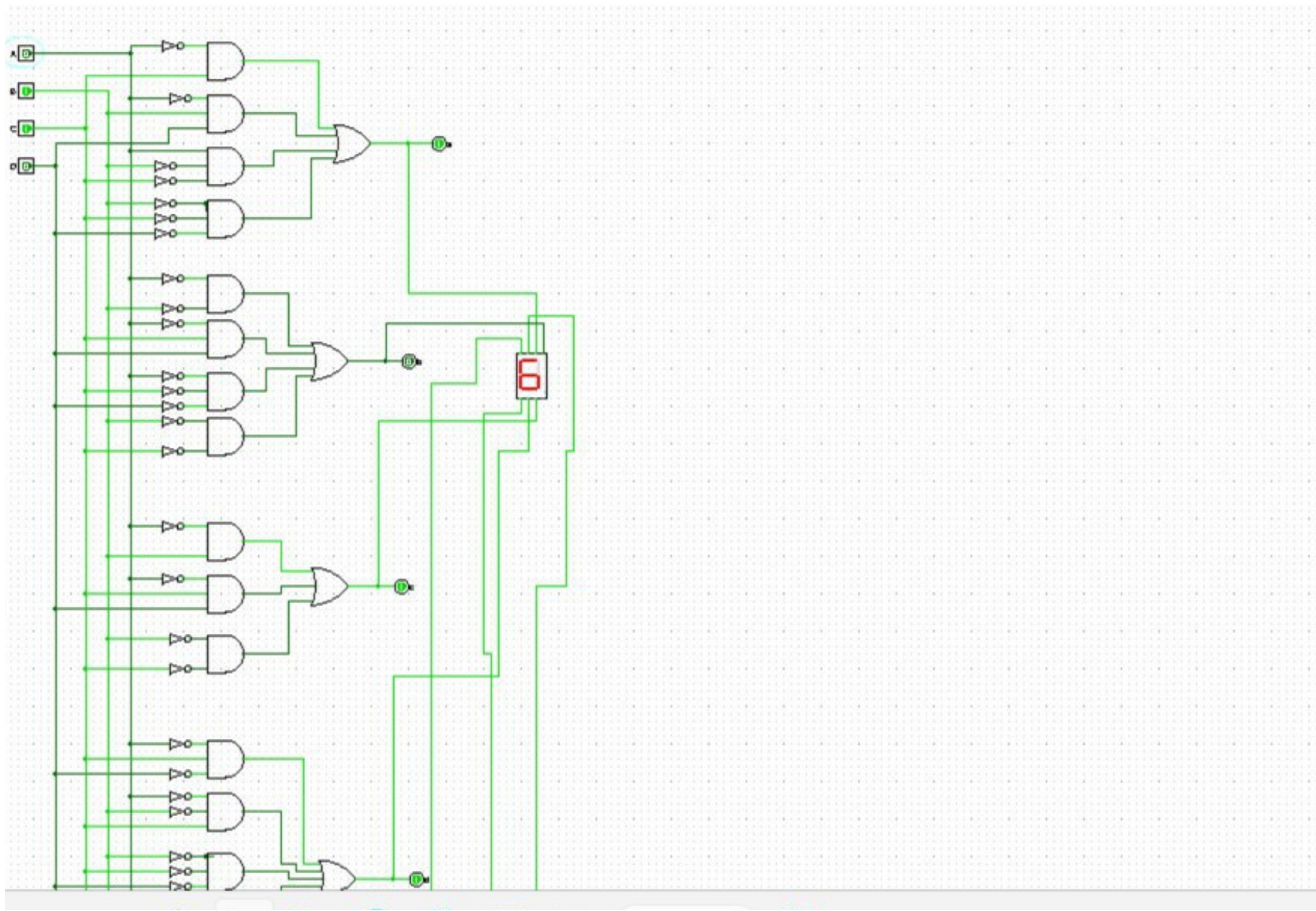

g=A’B’C+A’CD’+A’BC’+AB’C’

# Draw logic gates



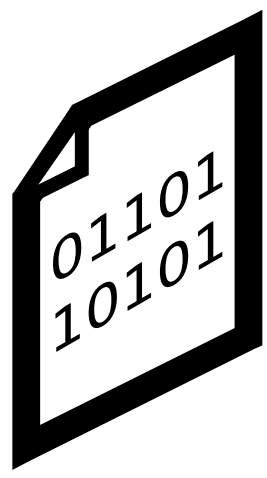



A
B
C
D
5


A
B
C
D
6

# Students Name:


Amal Al-Zubaidi

Salemah Al-Issa

Roaa Al-Rizqi