Optimizing Tree-structure Indexes for CXL-based Heterogeneous Memory with SINLK

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Abstract

On heterogeneous memory (HM) where fast memory (i.e., CPU-attached DRAM) and slow memory (e.g., remote NUMA memory, RDMA-connected memory, Persistent Memory (PM)) coexist, optimizing the placement of tree-structure indexes (e.g., B+tree) is crucial to achieving high performance while enjoying memory expansion. Nowadays, CXL-based heterogeneous memory (CXL-HM) is emerging due to its high efficiency and memory semantics. Prior tree-structure index placement schemes for HM cannot effectively boost performance on CXL-HM, as they fail to adapt to the changes in hardware characteristics and semantics. Additionally, existing CXL-HM page-level data placement schemes are not efficient for tree-structure indexes due to the granularity mismatch between the tree nodes and the page.

In this paper, we argue for a *CXL native, tree-structure aware* data placement scheme to optimize tree-structure indexes on CXL-HM. Our key insight is that *the placement of tree-structure indexes on CXL-HM should match the tree's inherent characteristics with CXL-HM features.* We present SINLK, a tree-structure aware, node-grained data placement scheme for tree-structure indexes on CXL-HM. With SINLK, developers can easily adapt existing tree-structure indexes to CXL-HM. We have integrated the B+tree and radix tree with SINLK to demonstrate its effectiveness. Evaluations show that SINLK improves throughput by up to 71% and reduces P99 latency by up to 81% compared with state-of-the-art data placement schemes (e.g., MEMTIS) and HM-optimized tree-structure indexes in YCSB and real-world workloads.

1 Introduction

In-memory tree-structure indexes [1–11] (e.g., B+tree) are fundamental in various domains, such as databases [12–18], storage engines [19, 20] and big data analytics [21–25]. Their efficiency is crucial for overall system performance [3, 4, 13, 26]. With the increasing data scale in datacenters, the memory demand of tree-structure indexes is growing rapidly [3, 27–32]. In order to expand memory capacity and enhance memory elasticity, heterogeneous memory (HM) has emerged. Many efforts [33–48] have been made to build tree-structure indexes on HM to leverage the large memory capacity while mitigating the slow memory's impact on performance.

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Nowadays, Compute Express Link (CXL) [49] becomes a promising HM solution to expand memory capacity. For example, Samsung CMM-B [50] scales memory capacity up to 24 TB with CXL memory pool. Due to CXL's cache-coherent memory semantics (i.e., CXL provides byte-addressable memory accessed in a cache-coherent way in the same address space as CPU-attached DRAM, i.e., fast memory), large tree-structure indexes designed for fast memory can easily adapt to CXL-HM, where fast and CXL-attached memory coexist.

However, placing these tree-structure indexes designed for fast memory directly onto CXL-HM results in poor performance, as there is still a performance gap between CXL-attached memory and fast memory (latency ~2×, bandwidth ~60%, as shown in Figure 1(c)). For instance, directly placing 75% of the tree's memory on CXL-attached memory can lead to a performance drop of ~70% (Figure 2). Therefore, it is vital to optimize the placement of tree-structure indexes on CXL-HM to reduce performance degradation while taking advantage of the increased memory capacity.

Previous optimizations for tree-structure index placement on HM (e.g., NUMA, RDMA, PM) are inefficient for CXL-HM. Replication, partitioning, and delegation methods used in NUMA-optimized indexes [33–35] are not suitable for CXL-HM because CXL-attached memory lacks local processors like NUMA nodes. Indexes optimized for RDMA [36–40] maintain a cache for accessed data in fast memory. However, the narrowed performance gap between slow and fast memory in CXL-HM makes cache maintenance overhead outweigh the benefits of caching. In indexes optimized for PM [42–48], placing the internal nodes of trees in fast memory is commonly used to mitigate slow memory's limited write bandwidth and higher latency. For CXL-HM, this static approach is insufficient because it neglects the capacity limit of fast memory, leading to fast memory exhaustion or underutilization, and fails to adapt to dynamic workloads.

Moreover, applying existing CXL-HM data placement schemes [51–55] to tree-structure indexes is also inefficient. As these schemes manage data at page granularity while tree nodes are typically smaller, this granularity mismatch leads to inaccurate hotness detection, increased migration overhead, and suboptimal data placement.

Our key insight is that *the placement of tree-structure indexes on CXL-HM should match the tree's inherent characteristics with the features of CXL-HM.* We identify three key characteristics of trees: (1) *node granularity*: node is the unit of data usage and management in trees; (2) *layered hotness*:

nodes in upper levels are accessed more frequently (i.e., hot) than those in lower levels; (3) *path-style access*: the access granularity of trees is the path (i.e., all nodes from the root to a leaf [1]), and nodes along paths to hot leaf nodes (i.e., hot path) contribute to considerable memory access.

Therefore, on CXL-HM we should focus on: (1) Match the node granularity with CXL-HM's cache-coherent memory semantics. Instead of caching, we should store hot nodes in fast memory and less frequently accessed (i.e., cold) nodes in slow memory, track node hotness, and migrate nodes between fast and slow memory based on the hotness to adapt to dynamic workloads. (2) Match the layered hotness and path-style access with the performance differences between fast and slow memory by prioritizing upper-level nodes (i.e., *layer principle*) and hot paths (i.e., *path principle*) in fast memory.

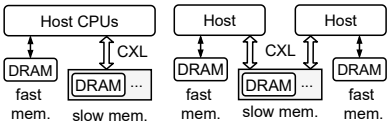
We design SINLK, a node-grained, tree-structure aware data placement scheme to optimize tree-structure indexes on CXL-HM. First, SINLK introduces *leaf-centric access tracking*, capturing the hotness of all access paths while minimizing interference with tree operations by only tracking leaf nodes. Second, SINLK incorporates *structure-aware migration* which considers node relationships instead of migrating each node independently to keep upper-level nodes in fast memory and achieve the quick promotion (i.e., moving to fast memory) of the entire hot path. Finally, SINLK proposes *hyper watermark mechanism* that holistically coordinates system behaviors (i.e., node allocation and migration) based on real-time fast memory usage rather than static thresholds, thereby ensuring stable high performance for indexes.

To demonstrate SINLK's effectiveness and generality, we integrate SINLK with two widely used tree-structure indexes—B+ tree [1] and radix tree [10, 11]—with less than 3% trees' internal code modification. Evaluation on a real CXL platform with synthetic workloads shows that SINLK achieves up to 133% higher throughput and 67% lower P99 latency than the SOTA data placement scheme MEMTIS [52]. For YCSB [56], SINLK achieves up to 71% and 60% higher throughput than MEMTIS and optimized HM index (optimized PACTree [57]), respectively. For real-world workloads [58], SINLK achieves up to 66% higher throughput and 81% lower P99 latency than MEMTIS, with 44% higher throughput and 63% lower P99 latency than optimized PACTree.

In summary, we make the following contributions:

- **Analyses.** We thoroughly analyze existing solutions for the placement of tree-structure index on CXL-HM and propose that the key to efficient placement lies in matching the tree's inherent characteristics with CXL-HM features.
- **Design.** We design SINLK, an efficient and generic data placement scheme for tree-structure indexes on CXL-HM.
- **Evaluation.** We integrate SINLK with B+ tree and radix tree. Evaluation on a real CXL platform with various workloads demonstrates the advantages of SINLK.

[1]We mainly focus on tree-structure indexes that store values in leaves, the most common form of such indexes [10].



(a) CXL 1.0/1.1 **(b)** CXL 2.0/3.0

	B/W(MB/s)	Lat. (ns)
Fast	33095.3	111.2
Slow (CXL)	21724.3	276.9

(c) Performance

Figure 1. CXL-based heterogeneous memory system. *(a,b) System architecture. (c) Comparison of fast and slow memory latency and bandwidth tested by Intel MLC [63] on our CXL1.1 platform.*

2 Background and Motivation

2.1 CXL-based Heterogeneous Memory

CXL [49, 59] is an emerging interconnect technology notable for its memory expansion capability, cache-coherent memory semantics, and high performance. As illustrated in Figure 1(a), CXL-HM with CXL 1.0/ 1.1 [60] allows host CPUs to access CXL-attached memory with cache-coherent load/store. CXL-HM with CXL 2.0/3.0 [61, 62] (Figure 1(b)) further allows the hosts to expand the memory by CXL memory pool, enhancing memory expansion's flexibility. As CXL-HM provides a unified physical address space of fast memory and CXL-attached memory, existing tree-structure indexes for fast memory can be effortlessly migrated to CXL-HM.

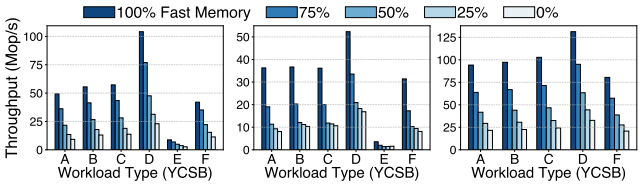
2.2 Tree-structure Indexes on CXL-HM

Figure 1(c) shows that there is still a performance gap between fast and slow memory in CXL-HM: slow memory has higher latency (~2×) and lower bandwidth (~60%) than fast memory on our CXL1.1 platform. Moreover, this gap will be widened with the introduction of CXL-switch since CXL2.0 [64]. Thus, directly migrating tree-structure indexes designed for fast memory to CXL-HM leads to poor performance. We illustrate this via Masstree [1], Wormhole [2], and adaptive radix tree (ART) [10, 11], three typical tree-structure indexes. The setup of the following experiments is the same as our evaluation (§6.1). As shown in Figure 2[2], when employing the default weighted memory allocation policy [65], the performance of all three indexes drops by about 70% with 25% fast memory usage compared to 100% fast memory across all workloads. Therefore, *optimizing the placement of tree-structure indexes on CXL-HM is essential to achieve better performance.*

2.3 Issues with Optimized HM-Indexes on CXL-HM

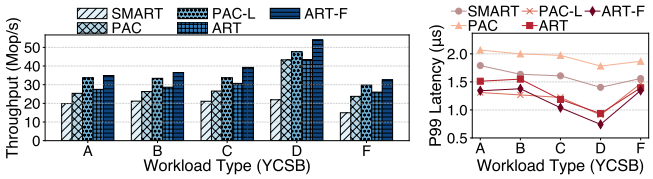
In this section, we study existing tree-structure indexes optimized for other types of HM (e.g., NUMA, RDMA-based HM, PM-based HM) and data placement schemes for CXL-HM to demonstrate that:

[2]We don't test workload E for ART because its source code does not implement the scan operation.



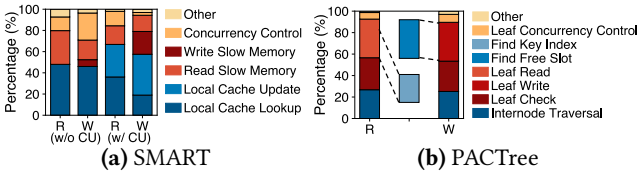
(a) Masstree (b) Wormhole (c) ART

Figure 2. Throughput (tput.) of indexes with different fast memory usage ratios in YCSB [56] benchmark.



(a) Throughput **(b)** P99 Latency

Figure 3. Comparison of SMART, PACTree, and ART on CXL-HM. *PAC stands for PACTree. All indexes have a fast memory usage ratio of 20%, except ART-F at 40%. PAC, ART, and ART-F use the same memory allocation policy as Figure 2.*



(a) SMART **(b)** PACTree

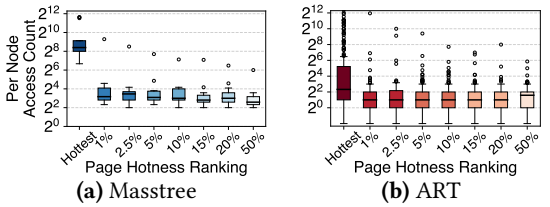
Figure 4. Performance breakdown per operation type. *(w/o CU)&(w/ CU) means without/with local cache update.*

- Prior optimizations for tree-structure index placement on HM are either impractical or inefficient on CXL-HM due to CXL-HM's unique hardware characteristics and semantics. We compare the original ART, the RDMA-optimized ART (SMART [38]), and the PM-optimized ART (PACTree [57]) using YCSB. Figure 3 shows that *the original ART outperforms SMART and PACTree on CXL-HM.*
- Applying existing CXL-HM data placement schemes to tree-structure indexes is also inefficient due to granularity mismatch between tree nodes and pages.

NUMA-Index. Indexes optimized for NUMA reduce cross-node communication and minimize accesses to remote memory through replication [35, 66, 67], partitioning [33], or delegation [34, 68]. These methods are not applicable to CXL-HM because *CXL-attached memory lacks local processors for data processing, unlike the memory in the NUMA node.*

RDMA-Index Case Study (SMART). SMART optimizes ART's data placement by maintaining a fast memory cache for accessed internal nodes (a.k.a., local cache), which is a common optimization in RDMA-Indexes [37–39, 41]. Figure 3(a) shows that SMART's throughput is only 50%–74% of ART[3]. Our profiling (Figure 4(a)) reveals that the primary overhead (~50%) in SMART comes from the local cache.

[3]The congestion control design of SMART (RDWC) is disabled because it causes about a 15% performance drop when there is no congestion.



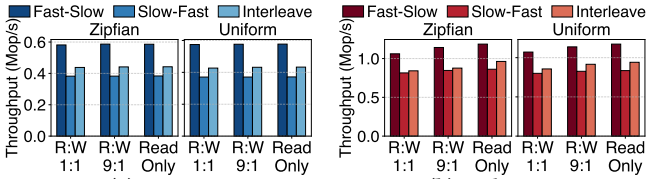
(a) Masstree **(b)** ART

Figure 5. Node access count distribution across pages of varying hotness. *We analyze distribution of node access counts in the page with the highest access frequency (Hottest) and those ranked top 1%–50% by access frequency.*

Since the latency gap between CXL-attached memory and fast memory is much smaller than that of RDMA-connected memory [69], the costs of cache maintenance and querying outweigh the benefits of reducing slow memory accesses. Specifically, while the local cache significantly reduces access to slow memory (nearly all internal node accesses hit the cache in the Zipfian read/update-only workloads), querying the local cache incurs more overhead than direct tree traversal due to the additional cache miss checks and eviction management.

PM-Index Case Study (PACTree). PACTree optimizes ART's data placement by using fat (64 entries), unordered leaf nodes, which is a common optimization [42, 43, 46–48, 70–72] in PM-indexes, along with asynchronous tree structural modification (a.k.a., async SMO). Figure 3 shows that PACTree's throughput is only 90% of ART, and its tail latency is 1.3~1.9× of ART. Our breakdown (Figure 4(b)) indicates that the main source of performance overhead (~61%) is the fat, unordered leaf and async SMO. *These optimizations incur additional overhead in CXL-HM because CXL-attached DRAM does not suffer from the read-write asymmetry present in PM [31, 73], and the high allocation costs associated with persistence [57, 70].* Although fat, unordered leaf nodes reduce write amplification and allocation overhead, they impose significant search overhead, with nearly 99% of the time in the leaf write operation spent finding a free position. Additionally, while async SMO decouples the write overhead of slow memory from the critical path, it introduces substantial overhead—particularly harming tail latency—through leaf checking, which ensures the correctness of async SMO.

Another common placement optimization in PM-indexes is to place only leaves in slow memory and keep internal nodes in fast memory (a.k.a., fast memory internode) [42, 43, 45–48]. We apply this technique to PACTree (PAC-L in Figure 3). Although it can improve PACTree's performance on CXL-HM, this static placement strategy is insufficient because: (1) It neglects fast memory capacity, which can result in fast memory underutilization or exhaustion. For example, ART outperforms PAC-L when fast memory capacity is larger (ART-F in Figure 3), and PAC-L's performance drops by ~17% when fast memory is full. (2) It ignores workload characteristics, requiring access to the leaf in slow memory for each request.



(a) B+ tree **(b)** Radix tree

Figure 6. Tput. of different node placement strategies. *The fast memory usage ratio is ~50% in all configurations.*

Applying CXL-HM Data Placement Schemes. Existing data placement schemes [51–55] for dynamic data placement (i.e., migrating data based on workload demands) on CXL-HM manage data at page granularity (e.g., 4 KiB), such as MEMTIS [52]. However, since tree nodes are typically smaller than pages, this granularity mismatch can lead to inaccurate hotness detection. As shown in Figure 5, even for the top 1% of frequently accessed pages, the majority of nodes remain cold—the upper quartile of nodes' access count is just 16 and 4 for Masstree and ART, respectively. Additionally, the hottest node on each page contributes 82% and 85% of total accesses, respectively. Therefore, page-level migration may misplace cold nodes in fast memory, causing suboptimal data placement and increasing migration overhead.

3 Design Principles and Challenges

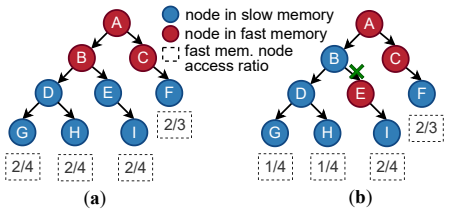
Our key insight is that the efficient placement of tree-structured indexes on CXL-HM should match the tree's inherent characteristics with the features of CXL-HM, which involves: (1) matching the tree's node-granularity data usage with CXL-HM's cache-coherent memory semantics to achieve node-grained flexible data placement; (2) matching node hotness indicated by the tree's hierarchical structure and access pattern with the performance gap between fast and slow memory to efficiently utilize fast and slow memory.

In this section, we present the principles of data placement derived from tree characteristics and the challenges in designing an efficient node-grained data placement scheme.

3.1 Principles from Tree Characteristics

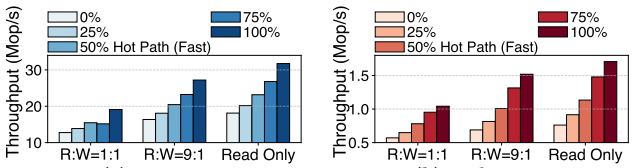
3.1.1 Structural Characteristics. Due to the tree's branching structure and the downward access from its root, nodes at upper levels (i.e., upper nodes) are fewer but have higher access frequency than lower nodes. For instance, in a B+ tree [74] and radix tree [75] with 50 million keys, nodes in the upper half levels comprise less than 1% of total nodes but have average access frequency three orders of magnitude higher than those in the lower half levels. Thus, *upper nodes are naturally hot and well-suited for fast memory.*

We validate this observation using the B+ tree and radix tree in three settings: *Fast-Slow* (upper nodes in fast memory), *Slow-Fast* (the reverse of *Fast-Slow*), and *Interleave* (levels interleaved in two memory types). Figure 6 shows *Fast-Slow* performs best, as fewer upper nodes allow more nodes along the path to be placed in fast memory. Notably, *Interleave* outperforms *Slow-Fast* but still trails *Fast-Slow*, highlighting the benefits of placing upper nodes in fast memory.



(a) **(b)**

Figure 7. *Single-boundary structure.* *(a) The tree follows this structure. (b) When tree violates this, putting E in fast memory and B in slow memory, the fast memory access ratio of the paths from A to G and A to H decreases from $\frac{2}{4}$ to $\frac{1}{4}$.*



(a) B+ tree **(b)** Radix tree

Figure 8. Tput. at different hot path ratios in fast memory. *Percentages of* HotPath(Fast) *indicate the proportion of hot paths in fast memory. For nodes not on* HotPath(Fast)*, their placement follows the* Fast − Slow *config. in Figure 6.*

Layer Principle. It is beneficial to store the tree's upper nodes in the fast memory as many as possible.

Building on the *layer principle*, we propose a guarantee to improve the expected ratio of fast memory access in each path to target nodes: *all ancestors of a fast memory node should be placed in fast memory.* As shown in Figure 7(a), this guarantee ensures only one boundary between fast and slow memory nodes along all paths, so we term it as *single-boundary structure.* Figure 7(b) illustrates that when the placement of nodes B and E violates this guarantee, the paths from A to G and H lose a fast memory node, potentially degrading the performance when accessing the data of nodes G and H.

3.1.2 Access Characteristics. Trees are accessed from the root downwards, forming access paths from the root to target nodes (e.g., leaf nodes in B+ trees and radix trees). In real-world workloads, where accesses are often skewed [29, 76–79], *certain paths are accessed much more frequently.* We identify these paths as *hot paths.*

To investigate how hot paths can affect the performance of trees on CXL-HM, we evaluate a multi-threaded B+ tree [80] and the radix tree under a skewed workload, where 90% of requests targeted 10% data. We vary the proportion of hot paths in fast memory and measure throughput. As illustrated in Figure 8, tree performance improves across all workloads with the higher proportion of hot paths in fast memory.

Path Principle. It is crucial to identify the hot paths and endeavor to place them in fast memory as many as possible.

3.2 Challenges

To adapt to dynamic workloads, an efficient data placement scheme should be able to (1) track node hotness and migrate nodes based on their hotness; and (2) adjust the allocation and migration strategy according to current memory usage. Therefore, although these principles offer valuable guidance, several challenges still need to be addressed.

Fine-grained access tracking incurs high overhead for tree operations. Tree-structure indexes have high requirements for both latency and throughput [3, 4, 13, 26]. Per-node access tracking introduces high overhead (over a 50% performance drop) on the critical path. This is because the tree's access pattern requires updating the access information of multiple nodes along the path for each data access. Thus, we should relax the tracking granularity from nodes to paths.

Migration cannot guarantee single-boundary structure and may break the locality of hot paths. When using the path-grained tracking, existing migration mechanisms [31, 51–54, 81] that treat each object (e.g, page, node) independently are no longer suitable due to missing per-node hotness data. Moreover, simply migrating by path is insufficient. Since an internal node belongs to multiple paths, demoting it (i.e., moving to slow memory) may (1) break the *single-boundary structure* if it has fast memory children; (2) disrupt hot path locality, as it may be part of other hot paths.

Allocation and migration require complicated control to meet the complexity of tree structure. Given the complexity of trees' hierarchical structure, more parameters are needed to control allocation and migration than page-level data placement schemes. For example, migration requires two metrics for deciding the path and the number of nodes in each path that need to be migrated. Additionally, allocation needs a threshold to determine whether a node should be placed in fast memory based on the *layer principle*. For these parameters, using static values cannot adapt to the dynamic workloads, and manual adjustments are error-prone and labor-intensive. Moreover, compared to existing allocation and migration strategies that are either passive (e.g., demotion only when fast memory is scarce [52, 53]) or lack coordination between allocation and migration [51], we need proactive and holistic strategies to meet the performance stability requirements of the trees.

4 Design of SINLK

To address the challenges in §3.2, we design SINLK, an efficient and generic data placement scheme for tree-structure indexes on CXL-HM. As depicted in Figure 9, SINLK consists of a lightweight frontend module and a background module.

The frontend module is invoked in the critical path of the tree operations so that it is designed to be lightweight to minimize its impact on performance. It determines the initial position of a new node (❶) based on the *layer principle* while maintaining the *single-boundary structure*. It also updates the access frequency of leaf nodes (❷), laying the groundwork for hot path and cold node identification.

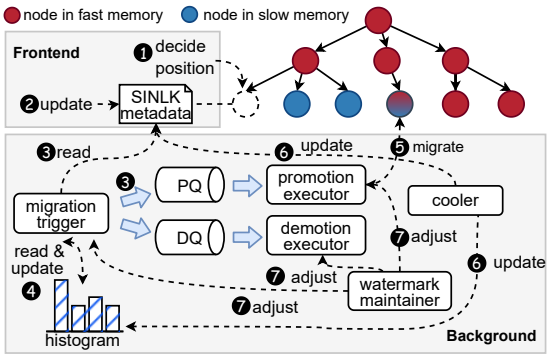


Figure 9. Architecture and interactions of SINLK. *PQ stands for promotion queue, DQ stands for demotion queue.*

The background module consists of several background workers to conduct node migration (§4.2) and system adjustment (§4.3) asynchronously to optimize fast memory usage. The *migration trigger* decides whether migration is needed and picks the appropriate nodes for migration based on their access frequency (❸) and the distribution (i.e., the histogram) of all leaf nodes' access frequency (❹). The *promotion executor* and *demotion executor* get nodes from the corresponding queues and carry out the migration tasks (❺). The *cooler* periodically halves the nodes' access frequency (❻) to ensure the freshness of access information. To coordinate all workers, the *watermark maintainer* monitors the fast memory usage and adjusts system parameters and the execution of other workers to ensure efficient utilization of fast memory (❼).

To reduce the impact of the data placement scheme on tree performance (Challenge 1), we propose a lightweight node allocation and tracking scheme (§4.1). To maintain the *single-boundary structure* and localize hot paths during node migration (Challenge 2), we introduce the structure-aware migration procedures (§4.2). Additionally, we holistically adjust allocation and migration using the hyper watermark mechanism (§4.3) to ensure stable high performance while optimizing fast memory utilization (Challenge 3).

4.1 Lightweight Node Allocation and Tracking

SINLK only leaves two essential and lightweight tasks on the critical path of tree operations: Determining each node's initial position based on the *layer principle* while maintaining the *single-boundary structure*, and tracking access frequency for each path through leaf nodes as guided by the *path principle*. All other tasks are executed in the background asynchronously, minimizing the impact on trees' performance.

Layer-aware Allocation. Guided by the *layer principle*, SINLK allocates upper nodes in fast memory while ensuring that the relationship between the new node and its ancestors conforms to the *single-boundary structure*. Specifically, SINLK maintains the highest level of fast memory node allocation, L_{fast}, which is adjusted based on current fast memory usage.

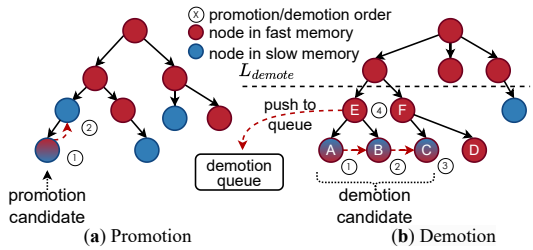


Figure 10. Promotion and demotion procedures.

When allocating new nodes or changing the node's position by auto-balancing, the decision on the node's placement is based on its current level l and its parent's type. If $l < L_{fast}$ and its parent is in fast memory, the node is allocated in fast memory; otherwise, it is placed in slow memory. Such a layer-aware allocation incurs little overhead on the critical path and effectively maintains the *single-boundary structure*.

Leaf-centric Access Tracking. The *path principle* highlights the necessity of placing hot paths in fast memory. Since data access ultimately reaches the leaf node, we can identify the path leading to the frequently accessed leaf as the hot path. Essentially, determining hot paths is based on leaf nodes' access frequency.

Therefore, SINLK maintains access frequency information only for leaf nodes. For each data access, instead of updating the access information of all nodes along the path, SINLK only updates the access frequency information of the leaf node. This leaf-centric approach significantly reduces the overhead of access tracking while providing sufficient information to identify hot paths and cold nodes for effective migration.

4.2 Structure-Aware Migration

SINLK designs the migration mechanism tailored for tree structures, ensuring that the hot paths can be quickly migrated to fast memory (§4.2.1) and that node demotion does not disrupt the *single-boundary* structure (§4.2.2). Additionally, SINLK employs a histogram-based approach to precisely identify hot paths and cold nodes (§4.2.3). To achieve efficient migration, SINLK decouples the preparation and execution of migration processes, assigning the migration trigger and promotion/demotion executors to work collaboratively (§4.2.4).

4.2.1 Promotion Procedure. When a leaf node in slow memory is identified as a hot node that needs promotion, following the *path principle*, it is necessary to quickly migrate the entire hot path to fast memory. As shown in Figure 10(a), SINLK's promotion procedure starts with the leaf node (①), recursively migrating all of its ancestor nodes in slow memory (②) upwards to fast memory.

4.2.2 Demotion Procedure. When a leaf node in fast memory is identified as a cold node, it is essential to demote not only this leaf node but also some of its ancestors to better utilize the limited fast memory resources. The specific number of ancestor nodes to be migrated depends on two key factors. The first is the system parameter L_{demote}, which reflects the intensity of demotion required under the current fast memory usage. The second factor is to ensure that the demotion does not disrupt the *single-boundary structure*. As illustrated in Figure 10(b), nodes A, B, and C are current demotion candidates. Migrating node C and then its parent node F breaches the *single-boundary structure* because node D is still in fast memory. Therefore, to demote parent node F, node D must also be demoted simultaneously. However, if node D, which is not a demotion candidate at that time, is demoted, it may inadvertently migrate a node in a hot path to slow memory, potentially degrading system performance.

Algorithm 1: Demotion Algorithm

```
1  Initialization: The migration trigger traverses all leaf
     nodes, finds the leaf nodes that need to be demoted, and
     adds them to the demotion queue;
2  while demotion queue is not empty do
3      pop node cur from demotion queue;
5      if cur.level < L_demote then
6          break;
7      end
9      if cur is internal node and at least one of its children is
         in fast memory then
10         continue;
11     end
12     demote cur to slow memory;
13     add cur's parent to the demotion queue if it is not in
         the queue;
14 end
```

To address this, SINLK adopts the demotion procedure as depicted in algorithm 1: once a node is demoted, its parent node is queued for demotion (line 13). The decision to demote the parent node is deferred until all its cold children have been processed by the demotion executor. If all of the parent node's children have been in slow memory by then, it indicates that the parent node is not part of any hot path, making it safe to demote. Conversely, if not all children are in slow memory, the parent node is kept in fast memory to prevent the demotion of hot paths while maintaining the *single-boundary structure* (line 9). Additionally, the lowest level for demotion is denoted by L_{demote}, nodes below L_{demote} will not participate in the demotion process (line 5). Therefore, for the tree in Figure 10(b), the demotion process follows the labels ①~④.

4.2.3 Histogram-based Hotness Identification. Like prior studies [52, 82, 83], SINLK employs a logarithmic histogram to represent access frequency distribution, thereby identifying hot paths and cold nodes for migration.

The migration trigger and the cooler collaborate to maintain the histogram. The migration trigger updates the histogram with leaf nodes' latest access frequency. The cooler halves all leaf nodes' access frequency and reflects the reduction in the histogram. Note that as the histogram is on a

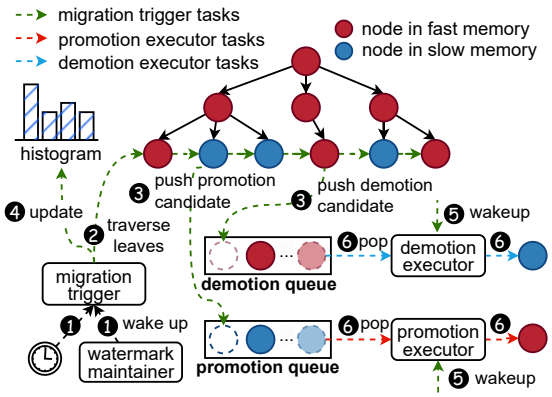


Figure 11. Migration workflow.

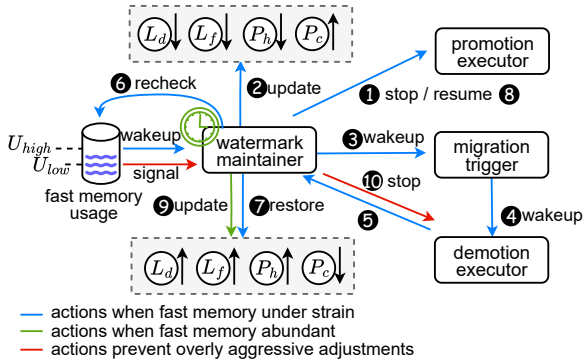


Figure 12. System parameter adjustments and the collaboration of workers in the hyper watermark mechanism. *L_d is L_{demote}, L_f is L_{fast}, P_c is P_{cold}, and P_h is P_{hot}.*

logarithmic scale, the reduction can be efficiently conducted by shifting all bins to the left by one position.

Based on the histogram, SINLK uses a hot threshold T_{hot} and a cold threshold T_{cold} to identify hot paths and cold nodes for migration. Leaf nodes with access frequency higher than T_{hot} are leaves of hot paths; while leaf nodes with access frequency lower than T_{cold} are deemed cold nodes.

As static thresholds cannot adapt to dynamic workloads, SINLK periodically updates the hot and cold thresholds using two parameters, P_{cold} and P_{hot}. These two parameters[4] determine the percentage of cold and hot leaves, respectively. SINLK scans the histogram to set T_{hot} to a value where nodes with frequency higher than T_{hot} just exceeds P_{hot}. Similarly, T_{cold} is set to a value where nodes with frequency lower than T_{cold} just fall below P_{cold}. Note that the interval between T_{hot} and T_{cold} prevents premature classification of less accessed nodes as cold, avoiding aggressive node migration.

4.2.4 Migration Workflow. As shown in Figure 11, the migration trigger is activated when fast memory usage is under pressure or on a schedule (❶). It scans all leaf nodes (❷) and selects cold ones in fast memory as demotion candidates, and hot ones in slow memory as promotion candidates. These nodes are pushed into respective demotion/promotion queue (❸). During scanning, the migration trigger also updates the histogram recording access frequency distribution (❹). When the queue is too long or the migration trigger has checked all leaf nodes, the corresponding executor is awakened (❺) to carry out the migration according to the procedures described in §4.2.1 and §4.2.2 (❻). It is worth noting that migration is executed by independent workers, enabling the trigger to continue selecting migration candidates without being blocked by the migration process.

4.3 Hyper Watermark Mechanism

To achieve high performance, SINLK selects appropriate initial positions for nodes based on their level (§4.1) and periodically migrates cold nodes and hot paths (§4.2). These procedures involve a series of tree-related parameters, including L_{fast} (§4.1), P_{cold}/P_{hot} (§4.2), and L_{demote} (§4.2). Manually adjusting these parameters is challenging, as it is difficult to adapt to workload changes and may cause conflicting fast memory usage intentions between node migration and allocation, causing performance instability.

Therefore, SINLK introduces a hyper watermark mechanism that synthetically adjusts these parameters and coordinates the behavior of background workers based on the current fast memory usage. It ensures consistent fast memory usage trends for node allocation and migration under various conditions. By trying to maximize the utilization of fast memory without exhausting it, the hyper watermark mechanism effectively prevents performance degradation from burst migrations and other extreme behaviors.

4.3.1 Asymmetric Adjustment. The impacts of fast memory strain and abundance are different. Depletion of fast memory can force the new upper-level nodes to be allocated to slow memory, obstruct hot path promotions, or trigger burst demotions, resulting in severe performance degradation that is unacceptable for high-performance tree-structure indexes. Conversely, when fast memory is abundant, although it leaves some fast memory underutilized, it does not have such a significant impact on performance stability and is advantageous for handling burst insertions of new nodes and promoting hot paths in the future.

Therefore, SINLK employs asymmetric adjustments. When the fast memory usage ratio exceeds the high watermark U_{high}, SINLK adopts an aggressive adjustment strategy to promptly bring the fast memory usage back to a reasonable range. Conversely, when the fast memory usage ratio falls below the low watermark U_{low}, a conservative adjustment is taken to optimize fast memory usage while reserving space for new nodes and hot path promotions.

4.3.2 Fast Memory Under Strain. When the fast memory usage ratio exceeds U_{high}, the watermark maintainer is immediately awakened to regulate the system parameters and background workers. The blue lines in Figure 12 illustrate

[4] P_{cold} and P_{hot} are initialized based on the maximum fast memory usage and further dynamically adjust through the hyper watermark mechanism (§4.3) based on the current fast memory usage.

this process. First, the watermark maintainer temporarily halts all ongoing promotion tasks (❶). Subsequently, it adjusts system parameters to increase demotion likelihood by increasing P_{cold} and decreasing P_{hot}, intensify demotion by decreasing L_{demote}, and reduce the number of nodes initialized in fast memory by decreasing L_{fast} (❷). The watermark maintainer then awakens the migration trigger to select cold nodes for demotion (❸), which in turn activates the demotion executor to migrate these cold nodes (❹). Following this, the watermark maintainer waits for the demotion executor to complete the demotion tasks (❺), then rechecks the fast memory usage (❻), and repeats steps ❷–❻ until the fast memory usage ratio falls below U_{high}. Upon achieving this, the watermark maintainer resets these system parameters to their pre-adjustment states (❼) and re-enables the execution of the promotion executor (❽).

4.3.3 Fast Memory Abundant.

As depicted by the green line and clock icon of Figure 12, the watermark maintainer periodically checks if the fast memory usage ratio drops below U_{low}. If so, it increases P_{hot}, L_{demote}, L_{fast}; and decreases P_{cold} (❾). This raises chances of promotion and fast memory allocation while reducing demotion likelihood. This approach is deemed conservative as it only adjusts parameters without instantly triggering migration executions.

4.3.4 Optimizations.

When fast memory is under strain, SINLK uses an aggressive adjustment strategy that sometimes over-identifies cold nodes, leading to excessive demotions and potentially dropping the fast memory usage ratio below U_{low}. To mitigate this and protect performance, SINLK acts promptly when the fast memory usage ratio falls below U_{low} and adjustments for prior memory pressure are still in progress. The watermark maintainer is signaled to halt current demotion tasks (❿). Subsequently, SINLK restores system parameters to their original states (❼) and reactivates the promotion executor (❽), safeguarding system performance through efficient fast memory utilization.

When fast memory is under pressure, the watermark maintainer may need multiple attempts, involving several adjustments to system parameters. If the adjustments to L_{demote} and L_{fast} are too aggressive, they can lead to excessive demotion and an overly pessimistic fast memory usage trend, hurting performance. To prevent this, we limit changes to L_{demote} and L_{fast} based on the maximum fast memory usage, avoiding excessively aggressive adjustments.

The demotion procedure in §4.2.2 only considers demoting the ancestors of leaf nodes in fast memory. To prevent cold ancestors of slow memory leaf nodes from being stuck in fast memory and to demote more cold internal nodes under fast memory strain, the migration trigger adds some cold leaf nodes in slow memory to the demotion queue, creating the opportunity to demote their ancestors later.

Table 1. Workload composition. *SP is Skewed Partition.*

Workload	Request Composition
Update Heavy (SP, YCSB-A)	50% Read, 50% Update
Read Mostly (SP, YCSB-B)	95% Read, 5% Update
Read Only (SP, YCSB-C)	100% Read
With Insert (SP), Read Latest (YCSB-D)	95% Read, 5% Insert
Short Ranges (YCSB-E)	95% Scan, 5% Insert
Read Modify Write (RMW) (YCSB-F)	50% Read, 50% RMW

5 Implementation

SINLK Framework. We provide a lightweight and easy-to-use framework for integrating SINLK into various existing tree-structure indexes. For SINLK metadata, the framework requires developers to add one byte in internal nodes to record the node's level and memory type. Leaf nodes need two additional bytes for the access frequency. This memory overhead is acceptable because tree nodes are typically equal to or larger than the cacheline [84], and sometimes the node size is unaffected due to memory alignment. For the frontend module, SINLK framework provides helper functions that implement layer-aware allocation and leaf-centric access tracking for developers to use. Additionally, developers need to implement tree-specific logic in the interfaces defined by SINLK framework for the background module to interact with the tree. Notably, while SINLK requires some user-implemented functions, many of them can leverage the existing logic of the tree, such as node splitting for migration and the iterator for leaf traversal.

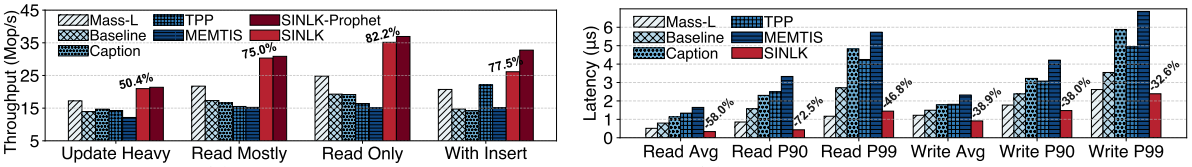
Integration. We have integrated ART and Masstree (a B+ tree variant optimized for multicore architecture) with SINLK framework, termed as S-ART and S-Masstree, respectively. In contrast to Masstree's 25 k LoC and ART's 1.7 k LoC, SINLK only modifies ~150 and ~50 LOC respectively. Moreover, we use ~1.8 k LoC to implement the framework, along with ~450 and ~320 LoC to implement its interfaces for Masstree and ART, respectively. This lightweight integration shows that SINLK can be easily applied to existing tree-structure indexes.

Concurrency Control. To prevent concurrent writes to the migrating node, we lock the node and its parent until the node's migration completes. For concurrent reads, we use an unused version bit to indicate the node's migration status. Read correctness is ensured by the optimistic read, which checks version numbers before/after each read and retries if changed. Note that there is no lock contention between background workers, which use atomic operations (e.g., CAS) to access shared state (e.g., parameters, histogram).

Configuration. In SINLK's runtime, the migration trigger, the cooler, and the watermark maintainer wake up every 500 ms, 2000 ms, and 100 ms, respectively. The high watermark and low watermark are set to 95% and 85%, respectively.

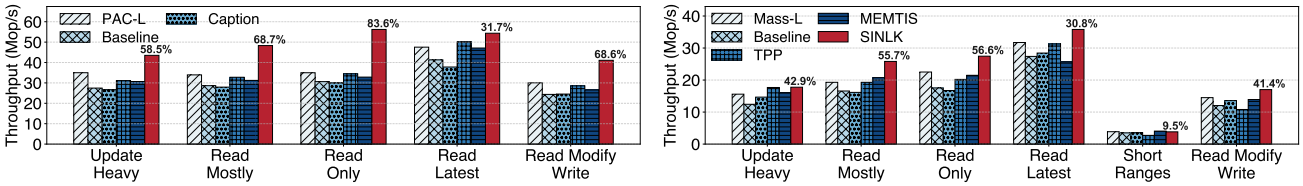
6 Evaluation

In this section, we evaluate SINLK from multiple perspectives to answer the following questions:



(a) Throughput **(b)** Latency of *Update Heavy* workload

Figure 13. Performance of SINLK (S-Masstree) and compared systems in the microbenchmark.



(a) S-ART **(b)** S-Masstree

Figure 14. Throughput of SINLK and compared systems in the macrobenchmark.

- Does SINLK perform well in various scenarios? (§6.2)
- Can SINLK maintain good performance in dynamic changing workloads and different initial system settings? (§6.3)
- How scalable is SINLK when varying the number of threads and dataset sizes? (§6.4)
- How do SINLK's techniques contribute to the final performance, and how does SINLK perform across various key/value sizes? (§6.5)
- How significant is SINLK's overhead? (§6.6)
- How does SINLK perform in real-world workload? (§6.7)

6.1 Environment Setup

Testbed. We run all experiments on Intel® Xeon® Platinum 8468V CPUs (48 cores), equipped with 395 MiB CPU cache, 32 GiB DRAM, and 32 GiB CXL-attached DRAM (connected through a CXL memory expansion card [85]). We use a single socket to avoid NUMA effects. All experiments except the concurrency scalability are conducted with 28 threads.

Workloads. We use the Skewed Partition (SP) synthetic workload as the microbenchmark, where 90% of requests target 5% of contiguous keys (termed *hot region*). This pattern closely matches the strong locality of hot keys in production environments [86]. We use YCSB[5] [56] with the default Zipfian distribution as the macrobenchmark. Details of both benchmarks are shown in Table 1. Additionally, we evaluate SINLK using Alibaba Block Traces [58, 87] which is a real-world workload collected from production.

Compared Systems. The baseline uses the default weighted allocation policy [65] to allocate a specified ratio of memory to CXL-attached DRAM. Moreover, we compare SINLK with three SOTA data placement schemes for CXL-HM: TPP [51], MEMTIS [52], and Caption [88]. For S-ART, we compare it with PAC-L, the optimized PACTree [57] with small leaves and fast memory internode (§2.3). For S-Masstree, we compare it with Mass-L (i.e., Masstree with fast memory internode[6]). As Caption does not specify the maximum fast memory usage, we set its limit to be the same as the baseline.

6.2 Overall Performance

6.2.1 Microbenchmark. SINLK-Prophet represents an ideal scenario where all hot paths are allocated in fast memory during initialization. To ensure fair comparison, we measure SINLK-Prophet's fast memory usage (~10% of total memory) and use this fast memory amount as the limit for other systems. Figure 13(a) shows that S-Masstree outperforms the baseline by 50%–82%[7]. Furthermore, SINLK performs similarly to SINLK-Prophet in the first three workloads, showing its ability to effectively identify and promote hot paths at runtime. For *With Insert*, SINLK-Prophet outperforms SINLK because it allocates most new nodes in fast memory, exceeding SINLK's maximum fast memory usage by 1.3–1.5×.

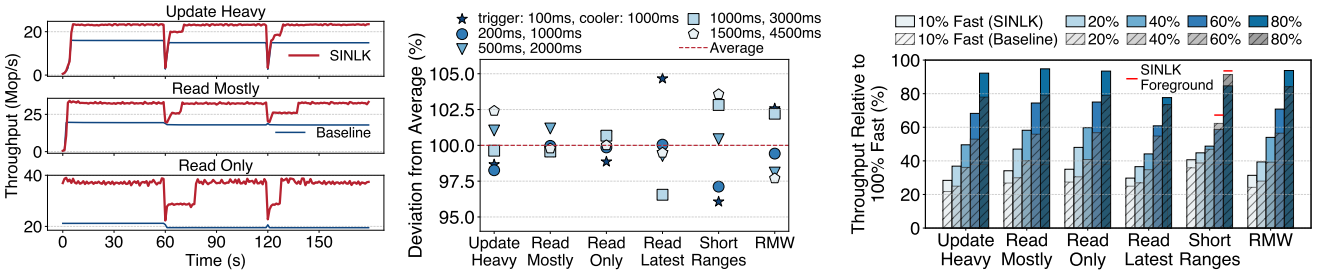
For other systems, Caption performs similarly to the baseline due to its interleave allocation method, which is similar to the baseline. TPP performs well in *With Insert* because it allocates all nodes in fast memory at the beginning when fast memory is abundant. However, TPP struggles to identify cold nodes and demote them in read-heavy workloads, hurting performance. MEMTIS performs comparatively poorly across all workloads because its default usage of huge pages does not adapt well to workload characteristics. Mass-L outperforms other baselines but still lags behind SINLK as static placement cannot adapt to dynamic workloads.

6.2.2 Macrobenchmark In the macrobenchmark, we set the baseline maximum fast memory usage at 20% and use its corresponding memory consumption as the limit for other systems, based on Zipfian access patterns and the dataset size. Note that this setting with low fast memory usage is consistent with previous work [31, 52, 54]. Besides this set-

[5]We don't evaluate *Short Range* for S-ART as its source code lacks scan.

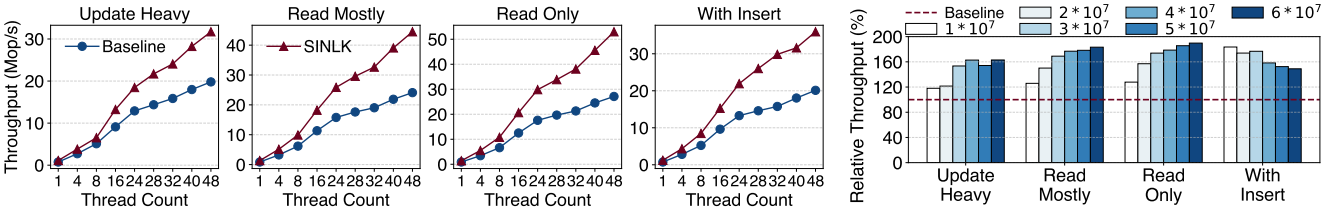
[6]Internodes are allocated to slow memory when fast memory runs out.

[7]In Figure 13, Figure 14, Figure 21(a) and Figure 22(a), the marked improvements are compared with the baseline.



(a) Dynamic workload **(b)** Different worker wake-up intervals **(c)** Different maximum fast memory usage

Figure 15. Sensitivity analysis of SINLK (S-Masstree).



(a) Scalability with different thread counts **(b)** Scalability with different dataset sizes

Figure 16. Scalability of SINLK (S-Masstree) in microbenchmark.

ting, we further evaluate SINLK's performance across various data scales and fast memory usage later to demonstrate its performance stability (§6.3.3, §6.4 part1).

As shown in Figure 14, S-ART outperforms the baseline by 32%–84%, while S-Masstree outperforms the baseline by 31%–57% (except for *Short Ranges*). *Short Ranges*'s performance depends on the number of leaves in fast memory. Due to the limited fast memory and SINLK prioritizing upper nodes in fast memory, the performance gain in this workload is not as significant. SINLK performs better in read-dominant workloads because migration interferes less with read operations.

PAC-L performs worse than S-ART because its static memory layout is unable to adjust to the dynamic workload. Other data placement systems fail to perform well across all workloads. For instance, while TPP performs similarly to S-Masstree in *Update Heavy*, it fails to maintain comparable performance for *Read Only* and *Read Modify Write*.

6.2.3 Latency Analysis We measure SINLK's latency under both micro and macro benchmarks. Due to the limited space, we only present the result of S-Masstree under the microbenchmark *Update Heavy* workload, though similar improvements are observed across other workloads. In Figure 13(b), SINLK's average read/write latencies are both under 1 μs. Moreover, SINLK sharply reduces read latency, with P90 latency 73% lower than the baseline. SINLK significantly reduces P90/P99 latency versus TPP and MEMTIS by continuously detecting and demoting cold nodes, along with the watermark mechanism, thereby preventing burst migrations.

6.3 Sensitivity Analysis

An ideal data placement scheme should be able to adapt to changing workloads and perform well across various configurations. In SINLK, most parameters are dynamically adjusted during runtime, except for workers' wake-up intervals and maximum fast memory usage. To evaluate SINLK's performance stability, we conduct a sensitivity analysis that shows its performance under dynamic changing workloads (§6.3.1) and different system parameter settings (§6.3.2, §6.3.3).

6.3.1 Dynamic Workload Changes. To simulate dynamic workload changes, we shift the entire hot region in the microbenchmark every 60 s. As shown in Figure 15(a), although SINLK suffers a temporary performance decline when the hot region changes—due to factors like the invalidation of hot paths and CPU cache misses—it quickly detects the new hot paths and migrates them to fast memory. SINLK can fully recover its performance in up to 17 s, showing its ability to quickly adapt to changes in hot paths for stable high performance in dynamic workloads.

6.3.2 Different Worker Wake-up Intervals. In SINLK, the migration worker, cooler, and watermark maintainer are regularly awakened. The watermark maintainer's wake-up interval has minimal impact because it only adjusts some parameters during regular awakenings. Therefore, we only evaluate the impact of wake-up intervals using five sets of different intervals for the other two workers. Figure 15(b) shows that SINLK's performance is relatively stable to wake-up interval choices, with less than 5% deviations from the average. In real-world scenarios, wake-up intervals can be adjusted based on system conditions, such as extending the intervals when CPU resources are tight to reduce overhead.

6.3.3 Different Maximum Fast Memory Usage To evaluate SINLK's performance with different maximum fast memory usage, Figure 15(c) compares SINLK with the baseline

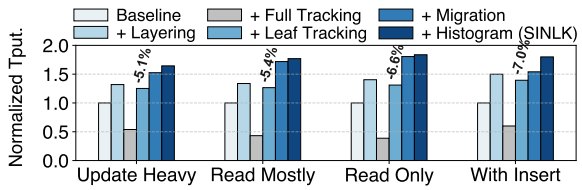


Figure 17. The factor analysis for techniques in SINLK.

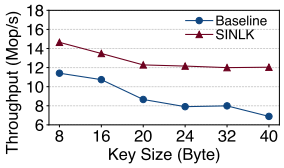


Figure 18. *Impact of key sizes (Micro Update Heavy).*

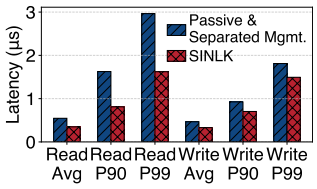


Figure 19. *Impact of passive and separated management (YCSB-D).*

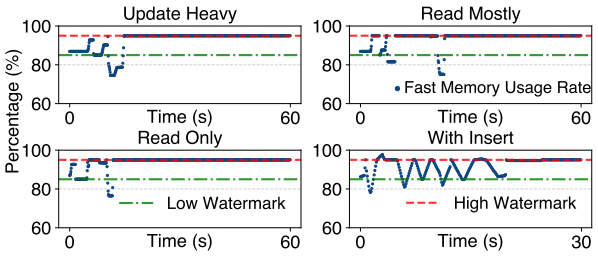


Figure 20. Fast memory usage ratio variation over time.

in the macrobenchmark, varying maximum fast memory usage from 10% to 80% of the baseline's total memory. As the fast memory usage increases, SINLK's performance improves steadily. When 80% data is in fast memory, SINLK's performance is close to all data in fast memory for most workloads. When the maximum fast memory usage exceeds 60%, SINLK slightly lags the baseline in *Short Ranges* because the higher fast memory usage intensifies competition for CPU cache between background workers and the scan operation. Nevertheless, when only the frontend module is enabled (red line in Figure 15(c)), SINLK still outperforms the baseline.

6.4 Scalability Performance

In this section, we evaluate the scalability of SINLK by varying the number of threads and dataset sizes.

Concurrency Scalability. Concurrency scalability is a key metric for assessing index performance [1, 2, 8]. Comparing SINLK with the baseline (Figure 16(a)) reveals that SINLK not only guarantees the index's scalability but also derives amplified performance gains over the baseline with more threads. The gains is amplified because SINLK benefits each thread, accumulating as the thread count grows. At 48 threads, SINLK's throughput is 28.6–38.1 × that of a single thread.

Dataset Size Scalability. An important aspect in evaluating data placement schemes is their ability to maintain high performance across varying data scales [31, 52, 89]. Figure 16(b) shows the performance gains of SINLK compared to the baseline when loading data varying from 10 to 60 million records. In the first three workloads, SINLK's improvement grows with the dataset size as the longer data access paths in larger datasets emphasize the benefits of promoting hot paths. However, for *With Insert*, new nodes creates new hot paths, requiring time for SINLK to identify and promote them, slightly reducing gains at larger scales. Nonetheless, SINLK outperforms the baseline by over 50% even at larger scales.

6.5 Performance Breakdown

This section evaluates the impact of each technique and key/value size in SINLK. We first present the factor analysis (§6.5.1), then evaluate the holistic management (§6.5.2).

6.5.1 Factor Analysis for SINLK

Contributions of techniques. We begin with the naive Masstree and gradually apply each proposed technique to conduct S-Masstree. Figure 17 shows how each technique contributes to SINLK's performance.

+ Layering. This step implements layer-aware allocation. With this design, SINLK exhibits performance gains ranging from 31.9% to 49.8% compared to the baseline.

+ Access Tracking. In this step, we evaluate the overhead of access tracking. Tracking only leaf nodes incurs a minimal performance loss of 5.1% to 7.0% compared to the last step, while tracking all nodes incurs about 60% performance degradation. This indicates that the overhead of updating only the leaf's information for access tracking is acceptable.

+ Migration. In this step, we begin to migrate hot paths and cold nodes, improving SINLK's performance by 2.8% to 28.7% over only using layer-aware allocation. However, the fixed hot/cold thresholds are not suitable for the *With Insert* workload, resulting in less noticeable performance gains.

+ Histogram. By introducing a histogram to dynamically adjust the hot/cold thresholds, SINLK achieves performance gains ranging from 1.7% to 16.8% over the static thresholds.

Impact of key and value size. We evaluate S-Masstree with various key and value sizes. Figure 18 shows that SINLK achieves stable performance improvement (up to 75%) across different key sizes. SINLK also stably outperforms the baseline (30%–40%) with value sizes from 8 to 256 bytes (we do not present the details here due to the limited space).

6.5.2 Effectiveness of Holistic Management.

Figure 19 shows that the passive (demotion only when fast memory is tight) and separated (the watermark only cares about migration) management significantly worsens the tail latency due to burst migrations when fast memory is tight.

To assess the watermark mechanism's effectiveness, we monitor the S-Masstree's fast memory usage ratio over time. Figure 20 shows that as hot paths are promoted, fast memory usage gradually increases. When exceeding the high watermark, it declines due to increased demotion. The watermark mechanism adjusts allocation and migration to maintain fast

Table 2. Runtime proportion of background worker execution. *MT is migration trigger, PE/DE is promotion/demotion executor, CL is cooler, WM is watermark maintainer.*

Run Time Ratio (‰)	MT	PE	DE	CL	WM	Total
Update Heavy	1.69	1.37×10^{-2}	1.12×10^{-2}	1.04×10^{-2}	0.799	2.52
Read Mostly	1.52	2.36×10^{-2}	8.39×10^{-3}	3.64×10^{-3}	0.529	2.09
Read Only	1.13	6.77×10^{-3}	9.01×10^{-3}	4.29×10^{-3}	0.365	1.51
Read Latest	1.84	1.46×10^{-1}	4.65×10^{-2}	1.03×10^{-1}	0.828	2.97
Short Ranges	1.55	6.91×10^{-6}	5.40×10^{-2}	4.02×10^{-2}	0.636	2.28
RMW	1.76	1.01×10^{-1}	1.44×10^{-2}	1.06×10^{-2}	0.839	2.73

memory usage within the watermark bounds. This ensures that once hot paths are promoted, fast memory usage ratio stabilizes near the high watermark across all workloads.

6.6 Overhead Analysis

CPU Time Overhead. We assess the overhead of each background worker in SINLK by measuring the proportion of its execution time to the total CPU time. Table 2 shows that the background workers only accounts for 1.51‰–2.97‰ of the total runtime. The migration trigger takes the longest time among all workers, as it scans all leaf nodes to identify hot paths and cold nodes. Next is the watermark maintainer, which is frequently activated to monitor fast memory usage.
Memory Overhead. SINLK only increase memory usage of Masstree's internal/leaf nodes by only 0.36%/0.93%. For ART's internal/leaf nodes, the increase is 0.04%–1.3%/2.0%.

6.7 Real-world Workload Evaluation

Alibaba Block Traces, collected from Alibaba Cloud elastic block service [90], reflect representative user behaviors in the cloud [87]. We choose two traces with the largest working set (i.e., those with the greatest need for memory expansion) for evaluation (Trace 7 as Trace A, and Trace 40 as Trace B). Figure 21 shows that S-ART outperforms the baseline by up to 90% in throughput while reducing P99 latency by up to 79% compared to MEMTIS and 63% compared to PAC-L. Figure 22 reveals that S-Masstree increases throughput by up to 39% compared to the baseline and reduces P99 latency by up to 54% compared to MEMTIS. This result demonstrates that SINLK is also effective in real-world scenarios.

7 Discussion and Future Work

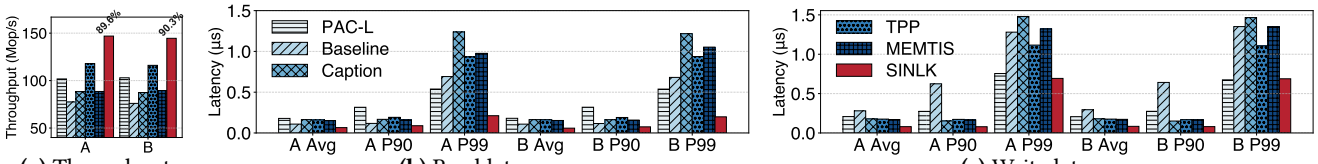
False Negative Internal Nodes. SINLK selects promotion candidates starting from hot leaf nodes. In this case, a large group of infrequently accessed leaf nodes may not trigger promotion individually, but their aggregated accesses could trigger promotion of the ancestors (i.e., false negative internal nodes). However, we find this situation is rare in practice. We break down the accesses to a B+ tree with 20 million keys following the standard Zipfian distribution and find that false negative internal nodes only appear in the last level internal nodes with a probability of less than 0.9%.
Hardware-based Access Tracking. SINLK updates the access frequency on each leaf access and traverses all leaves to select migration candidates. The former inevitably affects tree operation performance, and the latter is the main overhead in SINLK's background processing (§6.6). In the future, we will explore hardware-based sampling, like Intel Precise Event Based Sampling (PEBS) [91] and AMD Instruction-Based Sampling (IBS) [92], to further reduce this overhead.
Multi-layer Memory Hierarchy. Currently, SINLK targets two-layer memory hierarchies with fast and slow memory. To extend SINLK to multi-layer memory hierarchies, we can attempt to rank various memory types by their latency and throughput, and then apply SINLK's mechanisms and strategies between each pair of adjacent layers.

8 Related Work

Page-level Data Placement. Page-level data placement schemes aim to store hot pages in the fast memory and cold pages in the slow memory, while migrating pages to meet the workload demands [51–54, 81–83, 88, 93–97]. These schemes typically involve three major tasks: access tracking [89, 98, 99], hotness detection [52, 93, 100], data migration [94, 101, 102]. SINLK is inspired by the ideas and methods from these works, and designs the data placement scheme for tree-structure indexes on CXL-HM. Note that SINLK does not consider memory contention, Colloid [54] may further enhance SINLK when memory contention occurs.
Object-granularity Data Placement. The first type of user-space object-granularity data placement includes libraries [103–107] like CacheLib [103, 104] and X-Mem [105], which require specialized APIs or offline profiling for statistics. HeMem [31] avoids offline profiling and new APIs but does not manage the small allocation and migrates data at page granularity. The second type is hardware-based cache-line granularity placement [108–110], such as Intel Flat Memory Mode and Johnny Cache. Additionally, many databases are exploring data placement for CXL-HM [111–115]. Unlike these works, SINLK leverages the tree's characteristics to achieve fine-grained management and get more semantics than hardware-based solutions without offline profiling.
Far Memory Management. Far memory systems [116–120] utilize remote memory connected via network as the memory expansion. Unlike CXL-HM, far memory requires different interfaces and protocols to access remote memory, such as RDMA and RPCs. They usually focus on reducing network overhead [121, 122], read/write amplification [123, 124], and synchronization costs [125]. Far memory systems and SINLK are both related and orthogonal, as far memory indexes can benefit from SINLK's insights and SINLK can leverage far memory as a new slow memory layer to extend memory.

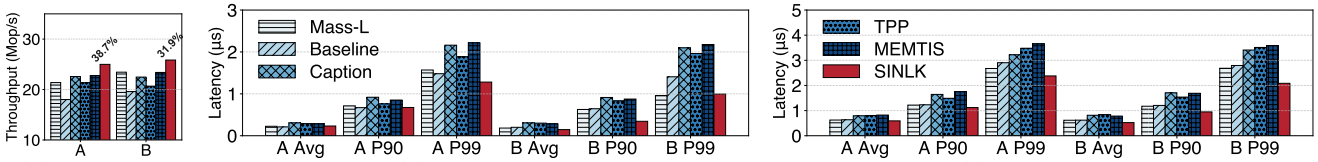
9 Conclusion

This paper proposes SINLK, a fine-grained, structure-aware data placement scheme for tree-structure indexes that utilizes the tree's inherent characteristics to achieve high stable performance.



(a) Throughput **(b)** Read latency **(c)** Write latency

Figure 21. Performance comparison between S-ART and compared systems with Alibaba Block Traces.



(a) Throughput **(b)** Read latency **(c)** Write latency

Figure 22. Performance comparison between S-Masstree and compared systems with Alibaba Block Traces.

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