Electronic Circuits lab assignment:

Experiments using LTspice

Submitted by:

Batch: B11

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RC Low Pass Filter

Aim

To design and simulate a 2 stage RC low pass filter with upper cutoff frequency at 20kHz and plot its frequency response.

Design

Upper cutoff frequency at n^{th} stage: $f_H(n) = \dfrac{f_H \text{ per stage}}{1.1 \times \sqrt{n}}$

Number of stage, n = 2, and $f_H(2) = f'_H = 20\text{kHz}$

For f'_H to be 20kHz:

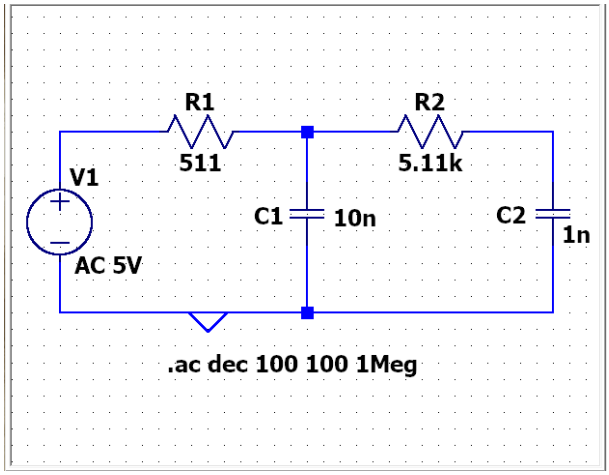
f_H per stage $= f_H \times 1.1\sqrt{n} = 20\text{kHz} \times 1.1\sqrt{2} \approx 31.113\text{kHz}$

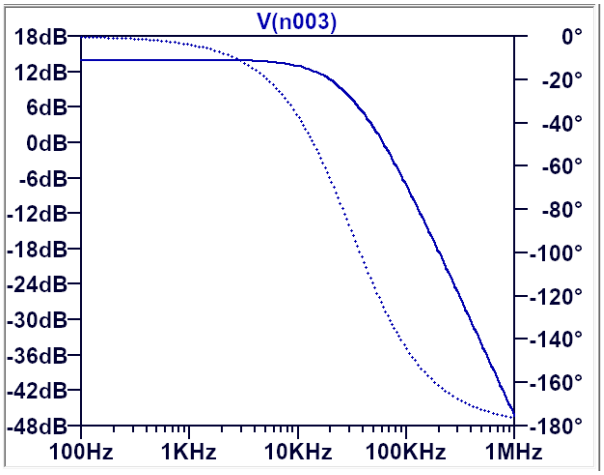
Let $C_1 = 10\text{nF}$

$$\therefore R_1 = \frac{1}{2\pi C_1 f'_H} = \frac{1}{2\pi \times 10\text{nF} \times 31.113\text{kHz}} \approx 511\Omega$$

$$\left.\begin{aligned} C_2 = C_1/10 \quad &= 1\text{nF} \\ R_2 = R_1 \times 10 \quad &= 5.11\text{k}\Omega \end{aligned}\right\} \text{ To avoid loading effect}$$

Circuit & frequency response





-3 dB cutoff frequency = **18.672kHz**

Result

Designed and simulated a 2 stage RC low pass filter.

It's cutoff frequency was found to be: **18.672kHz**

Zener Series Regulator

Aim

1. To design and simulate a zener series voltage regulator for a output voltage of +10V and maximum current of 100mA. (input voltage varies from 12V to 22V)
2. Plot and its load regulation and line regulation and find percentage load regulation

Design

- $V_Z = 5.1\text{V}$ (using modified BZX84B8V2L with BV=5.1V)
- $V_o = 10\text{V}$ $V_{in}(max) = 22\text{V}$
- $I_D = I_Z(min) = 5\text{mA}$ $I_{C2} = 2\text{mA}$
- h_{fe} for Q1 (2N3055): $\beta_1 = 15$ h_{fe} for Q2 (BC547): $\beta_2 = 100$

$$V_{RD} = V_o - V_Z = 4.9\text{V}$$

$$R_D = \frac{V_{RD}}{I_Z(min)} = \frac{4.9\text{V}}{5\text{mA}} = 980\Omega$$

For transistor Q2:

$$I_{B2} = \frac{I_{C2}}{\beta_2} = 20\mu\text{A}$$

$$V_{R2} = V_Z + V_{BE2} = 5.1\text{V} + 0.7\text{V} = 5.8\text{V}$$

$$V_{R1} = V_o + V_{R2} = 10\text{V} + 5.8\text{V} = 4.2\text{V}$$

$$I_{R1} = 10I_{B2} = 0.2\text{mA} \qquad I_{R2} = 9I_{B2} = 0.18\text{mA}$$

$$R_2 = \frac{V_{R2}}{I_{R2}} = \frac{5.8\text{V}}{0.18\text{mA}} \approx 32\text{k}\Omega$$

$$R_1 = \frac{V_{R1}}{I_{R1}} = \frac{4.2\text{V}}{0.2\text{mA}} = 21\text{k}\Omega$$

For transistor Q1:

$$I_{E1} = I_L + I_{R1} + I_D = 100\text{mA} + 0.2\text{mA} + 5\text{mA} \approx 105\text{mA}$$

$$I_{B1} = \frac{I_{E1}}{\beta_1} = \frac{105\text{mA}}{15} = 7\text{mA}$$

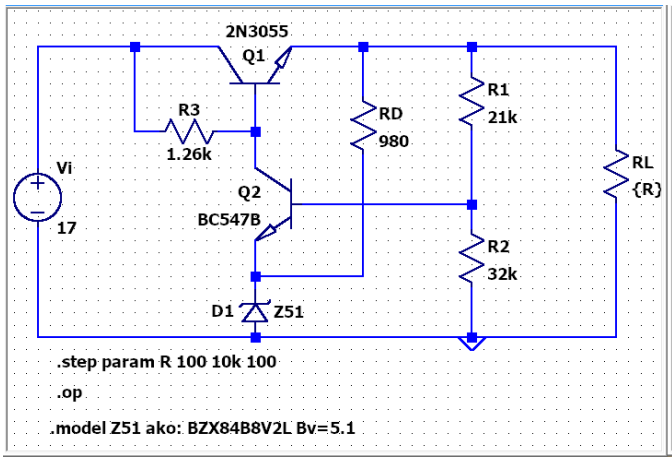
$$I_{R3} = I_{B1} + I_{C2} = 7\text{mA} + 2\text{mA} = 9\text{mA}$$

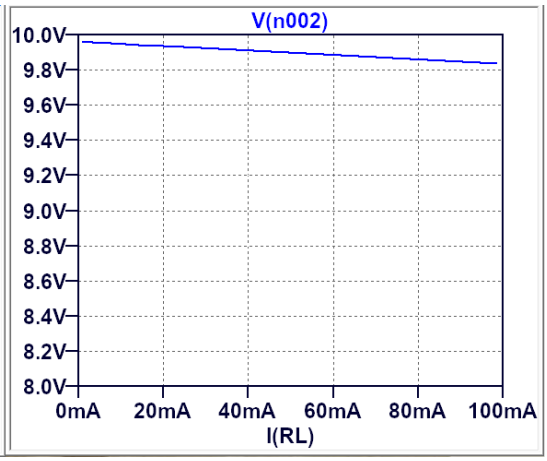
$$\therefore R_3 = \frac{V_{in}(max) - (V_{BE1} + V_o)}{I_{R3}}$$

$$= \frac{22\text{V} - (0.7\text{V} + 10\text{V})}{9\text{mA}} = 1.26\text{k}\Omega$$

Circuit, Load & line regulation

Load regulation



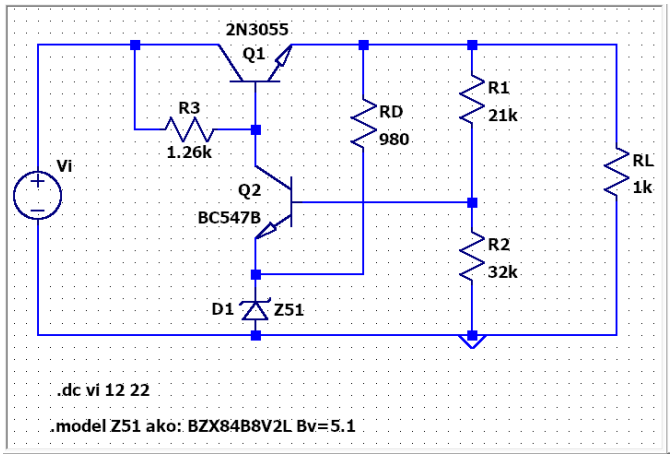


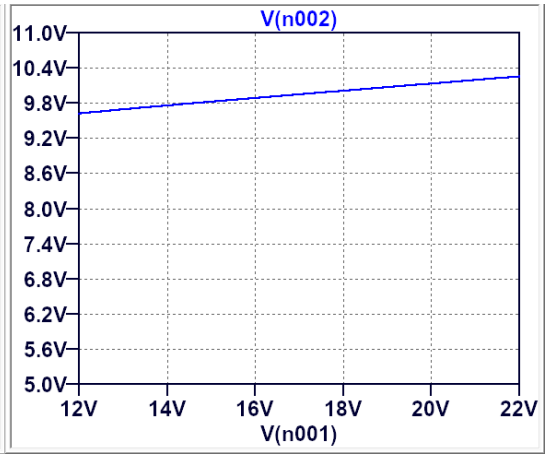
$$\text{Load Regulation} = \frac{V_{NL} - V_{FL}}{V_{NL}} \times 100\%$$

$$= \frac{9.9587 - 9.8387}{9.9587} \times 100\%$$

$$= \underline{\underline{\mathbf{1.20\%}}}$$

Line regulation





$$\begin{aligned}\text{Line Regulation} &= \frac{\Delta V_{out}}{\Delta V_{in}} \times 100\% \\ &= \frac{\Delta V(n002)}{\Delta V(n001)} \times 100\% \\ &= \frac{10.2544 - 9.6197}{22 - 12} \times 100\% \\ &= \underline{\underline{\mathbf{6.35\%}}}\end{aligned}$$

Result

Design and simulated a zener series voltage regulator and obtained its regulation parameters:

Load regulation = 6.35%

Line regulation = 1.20%