

October 1987 Revised March 2002

CD4021BC 8-Stage Static Shift Register

General Description

The CD4021BC is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual JAM inputs to each of 8 stages. Q outputs are available from the sixth, seventh, and eighth stages. All outputs have equal source and sink current capabilities and conform to standard "B" series output drive.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control is in the logical "1" state, data is jammed into each stage of the register asynchronously with the clock.

All inputs are protected against static discharge with diodes to $\rm V_{DD}$ and $\rm V_{SS}.$

Features

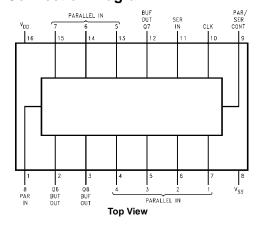
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility:
 - Fan out of 2 driving 74L or 1 driving 74LS
- 5V-10V-15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 µA at 15V over full temperature range

Ordering Code:

Order Number	Order Code	Package Description
CD4021BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4021BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Truth Table

C _L (Note 1)	Serial Input	Parallel/ Serial Control	PI 1		Q1 (Internal)	Q _n (Note 2)
Х	Х	1	0	0	0	0
Х	X	1	0	1	0	1
Х	Χ	1	1	0	1	0
Х	Χ	1	1	1	1	1
~	0	0	Х	Х	0	Q_{n-1}
~	1	0	Х	Х	1	Q_{n-1} Q_{n-1}
~	Х	0	Х	Х	Q1	Q_n

X = Don't care case

Note 1: Level change Note 2: No change

Logic Diagram SERIAL 11 CLOCK 10 PARALLEL/SERIAL 9 PARALLEL/SERIA

Absolute Maximum Ratings(Note 3)

(Note 4)

 $\begin{tabular}{ll} Supply Voltage (V_{DD}) & -0.5V to +18V \\ Input Voltage (V_{IN}) & -0.5V to V_{DD} +0.5V \\ \end{tabular}$

Storage Temperature Range (Ts) -65°C to +150°C

Power Dissipation (P_D)

Dual-In-Line 700 mW Small Outline 500 mW

Lead Temperature (T_L)

(Soldering, 10 seconds) 260°C

Recommended Operating Conditions (Note 4)

Supply Voltage (V_{DD}) 3V to 15V Input Voltage (V_{IN}) 0 to V_{DD}

Operating Temperature Range (T_A)

Note 3: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 4: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	-5	–55°C		+25°C			+125°C	
	i arailletei	Conditions	Min	Max	Min	Тур	Max	Min	Max	Units
I _{DD}	Quiescent Device	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		5		0.1	5		150	
	Current	$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		10		0.2	10		300	μΑ
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		20		0.3	20		600	
V _{OL}	LOW Level	$V_{DD} = 5V$		0.05		0	0.05		0.05	
	Output Voltage	$V_{DD} = 10V \qquad I_O < 1 \; \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	
V _{OH}	HIGH Level	$V_{DD} = 5V$	4.95		4.95	5		4.95		
	Output Voltage	$V_{DD} = 10V$ $ I_O < 1 \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		
V _{IL}	LOW Level	$V_{DD} = 5V, V_{O} = 0.5V \text{ or } 4.5V$		1.5		2	1.5		1.5	
	Input Voltage	$V_{DD} = 10V, V_{O} = 1.0V \text{ or } 9.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V$, $V_{O} = 1.5V$ or $13.5V$		4.0		6	4.0		4.0	
V _{IH}	HIGH Level	$V_{DD} = 5V, V_{O} = 0.5V \text{ or } 4.5V$	3.5		3.5	3		3.5		
	Input Voltage	$V_{DD} = 10V, V_{O} = 1.0V \text{ or } 9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V$, $V_{O} = 1.5V$ or $13.5V$	11.0		11.0	9		11.0		
I _{OL}	LOW Level Output	$V_{DD} = 5V, V_{O} = 0.4V$	0.64		0.51	0.88		0.36		
	Current (Note 5)	$V_{DD} = 10V, V_{O} = 0.5V$	1.6		1.3	2.2		0.90		mA
		$V_{DD} = 15V, V_{O} = 1.5V$	4.2		3.4	8		2.4		
I _{OH}	HIGH Level Output	$V_{DD} = 5V, V_{O} = 4.6V$	-0.64		-0.51	-0.88		-0.36		
	Current (Note 5)	$V_{DD} = 10V, V_{O} = 9.5V$	-1.6		-1.3	-2.2		-0.90		mA
		$V_{DD} = 15V, V_{O} = 13.5V$	-4.2		-3.4	-8		-2.4		
I _{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		-0.1		-10 ⁻⁵	-0.1		-1.0	μА
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10 ⁻⁵	0.1		1.0	μΛ

Note 5: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 6) $T_A = 25$ °C, input t_r , $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ k Ω

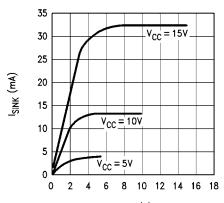
Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{PLH} , t _{PHL}	Propagation Delay Time	$V_{DD} = 5V$		240	350	
		V _{DD} = 10V		100	175	ns
		V _{DD} = 15V		70	140	
t _{THL} , t _{TLH}	Transition Time	$V_{DD} = 5V$		100	200	
		V _{DD} = 10V		50	100	ns
		$V_{DD} = 15V$		40	80	
f _{CL}	Maximum Clock	$V_{DD} = 5V$	2.5	3.5		
	Input Frequency	V _{DD} = 10V	5	10		MHz
		V _{DD} = 15V	8	16		
W	Minimum Clock	$V_{DD} = 5V$		100	200	
	Pulse Width	V _{DD} = 10V		50	100	ns
		V _{DD} = 15V		40	80	
t _r CL, t _f CL	Clock Rise and	$V_{DD} = 5V$			15	
	Fall Time (Note 6)	V _{DD} = 10V			15	μs
		V _{DD} = 15V			15	
t _s	Minimum Set-Up Time					
	Serial Input	$V_{DD} = 5V$		60	120	
	t _H ≥ 200 ns	V _{DD} = 10V		40	80	ns
	(Ref. to CL)	V _{DD} = 15V		30	60	
	Parallel Inputs	$V_{DD} = 5V$		25	50	
	t _H ≥ 200 ns	V _{DD} = 10V		15	30	ns
	(Ref. to P/S)	V _{DD} = 15V		10	20	
Н	Minimum Hold Time	$V_{DD} = 5V$			0	
	Serial In, Parallel In, $t_s \ge 400 \text{ ns}$	V _{DD} = 10V			10	ns
	Parallel/Serial Control	V _{DD} = 15V			15	
WH	Minimum P/S	$V_{DD} = 5V$		150	250	
	Pulse Width	V _{DD} = 10V		75	125	ns
		V _{DD} = 15V		50	100	
t _{REM}	Minimum P/S Removal	$V_{DD} = 5V$		100	200	
	Time (Ref. to CL)	$V_{DD} = 10V$		50	100	ns
		V _{DD} = 15V		40	80	
C _I	Average Input Capacitance	Any Input		5	7.5	pF
C _{PD}	Power Dissipation			100		pF
	Capacitance (Note 8)					

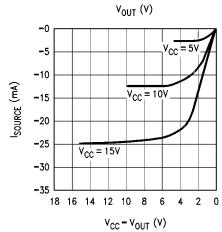
Note 6: AC Parameters are guaranteed by DC correlated testing.

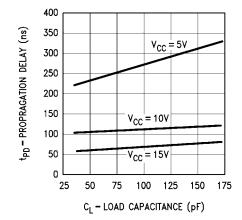
Note 7: If more than one unit is cascaded t_fCL should be made less than or equal to the fixed propagation delay of the output of the driving stage for the esti-

Note 8: CPD determines the no load AC power consumption of any CMOS device. For complete explanation, see 74C family characteristics application note AN-90.

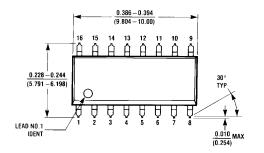
Typical Performance Characteristics

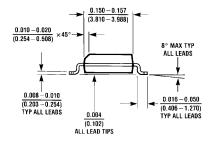


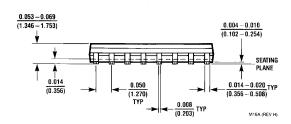




Physical Dimensions inches (millimeters) unless otherwise noted







16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.090 $\overline{(18.80 - 19.81)}$ (2.286)16 15 14 13 12 11 10 9 16 15 INDEX AREA 0.250 ± 0.010 $\overline{(6.350 \pm 0.254)}$ PIN NO. 1 PIN NO. 1 1 2 3 4 5 6 7 8 1 2 IDENT IDENT OPTION 01 OPTION 02 0.065 (1.651) 0.130 ± 0.005 0.060 (1.524) TYP 4º TYP OPTIONAL 0.300 - 0.320 (3.302 ± 0.127) (7.620 - 8.128)0.145 - 0.200(3.683 - 5.080)95°±5° 0.008 = 0.016 (0.203 = 0.406) TYP 0.020 $\frac{0.280}{(7.112)}$ (0.508)0.125 - 0.150 (3.175 - 3.810) 0.030 ± 0.015 (0.762 ± 0.381) 0.014 - 0.023 0.100 ± 0.010 (0.325 +0.040 -0.015 (0.356 - 0.584) (2.540 ± 0.254) 0.050 ± 0.010 N16E (REV F) TYP (1.270 ± 0.254)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com