Overview
The DC/DC converter is operated in a voltage range from 200 V to 600 V (limited by undervoltage and overvoltage measurement)
and delivers a maximum continuous output power of 500 W at 24 V.

Overload at the output
The output power is limited by a 20 A fuse (F2) with a melting integral of 130.5 A^2*s.
The converter can deliver 750 W (31.25 A) for 60 s, which would equal to 58593.75 A^2*s, therefore the fuse F2 would trip before
the thermal power limit of the converter would be exceedet.
A 1.6 A fuse (F1) with a melting integral of 0.768 A^2*s was selected for TS as it still ensures a continuous output power of 500 W at 400 V.
The LV fuse trips first in the event of a permanent overload.
At an output load of max. 750 W the input power is approx. 775 W (with efficiency loss) with worst case current (400 V input) of 1.94 A
and an equivalent melting integral of 3.75 A^2*s, therefore the fuse F1 would trip before the thermal power limit of the converter would be exceedet.

The following calculations are based on the maximum allowabe current for the FETs in the high current path.
The actual current might be different depending on input impedance and switching/failure conditions.

Overload of Q1 & Q2
These two MOSFETs together form a half-bridge, which controls the resonant circuit consisting of the transformer and Cr.
In the event of a Q1 or Q2 fault (permanently conductive), the TS current would flow through F1, Q1, Q2 and Q3.

Q1, Q2 and Q3 must therefore withstand the current until the fuse blows.

The maximum permissible pulse current for Q1 and Q2 is 114 A. The melting integral of F1 is 0.768 A^2*s.
This results in a tripping time at 114A of 59.1 µs. The normalized thermal impedance of Q3 at this pulse length.
for a single pulse is ≈0.1. R_th_JC is 0.87°C/W and R_DC(on) is max. 0.062 Ω.
According to the calculation (Texas Instruments, Application Note sluaat8)

ΔTj = P x Z x R_th_JC
with P = I^2 x R_DC(on)

this would result in a temperature increase of
I^2 x R_DC(on) x Z x R_th_JC = 70.1 K

The maximum permissible junction temperature for this MOSFETs is 175°C.
This means that even at an elevated MOSFET operating temperature of 100°C the fuse would trigger before the MOSFETs would be thermally destroyed.

The maximum permissible pulse current for Q3 is 51 A. The melting integral of F1 is 0.768 A^2*s.
This results in a tripping time at 51A of 295 µs. The normalized thermal impedance of Q3 at this pulse length
for a single pulse is < 0.018. R_th_JC is 0.6°C/W and R_DC(on) is max. 0.184 Ω.

This would result in a temperature increase of
I^2 x R_DC(on) x Z x R_th_JC = 5.17 K

The maximum permissible junction temperature for this MOSFET is 150°C.
This means that even at an elevated MOSFET operating temperature of 100°C the fuse would trigger before the MOSFET would be thermally destroyed.

In the event that the fault of Q1 or Q2 does not cause the fuse to blow within 59.1 µs, it can be assumed that a lower current would flow
for a longer time and Q3 would be overloaded after. In this case, up to 51A would flow through Q1 and Q2 for 295 µs (normalized thermal impedance of 0.18).
This would result in a temperature increase of 25.3 K in Q1 and Q2.
This means that even at an elevated MOSFET operating temperature of 100°C the fuse would trigger before the MOSFETs would be thermally destroyed.

In case of Q1 and Q2 beeing permanently destroyed, a pulse current of 114 A for Q3 is 51 A. The melting integral of F1 is 0.768 A^2*s.
This results in a tripping time at 51A of 295 µs. The normalized thermal impedance of Q3 at this pulse length
for a single pulse is < 0.018. R_th_JC is 0.6°C/W and R_DC(on) is max. 0.184 Ω.

This would result in a temperature increase of
I^2 x R_DC(on) x Z x R_th_JC = 5.17 K

The maximum permissible junction temperature for this MOSFET is 150°C.
This means that even at an elevated MOSFET operating temperature of 100°C the fuse would trigger before the MOSFET would be thermally destroyed.

The error case that Q1 or Q2 do not switch is not relevant, as this does not lead to an excess current.
Rather, this is a normal and safe behavior, e.g. when overvoltage is detected.

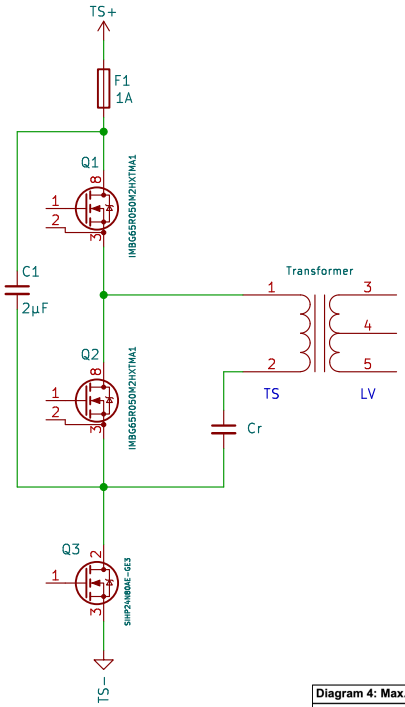
Turn-Off Overload of Q3
This MOSFET is responsible for precharging C1 and is permanently closed during operation.
In principle, the converter can also be operated without precharging, but the rapid charging of
of C1 leads to a high charging current when connecting the converter to the permanently live TS battery.
The fault case (Q3 switch-off during operation) would not lead to a fault in other components.
However, if the switch-off process takes an unexpectedly long time while current is still flowing, so that it is not in the SOA of the MOSFET,
the MOSFET could be damaged and be in a permanently low resistance state.
However, this would also not affect the normal operation of the converter.

TI Application Note: https://www.ti.com/lit/an/sluaat8/sluaat8.pdf

# PRELIMINARY

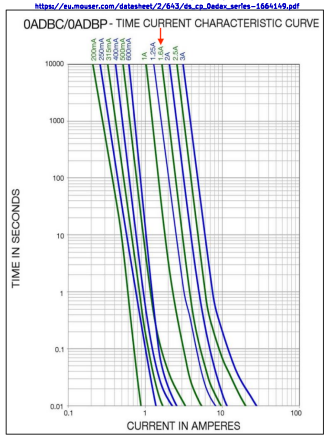
This file might change in the future.
Althought an older version has passed ESF,
it is unclear whether the calculations
provided are either needed nor correct.
If you like to improve this file, please
open up a new discussion on GitHub. Thanks!

https://github.com/Rootthecause/DCDC/discussions



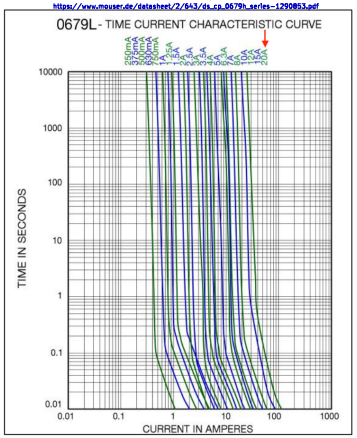

## TS Fuse (F1)

https://eu.mouser.com/datasheet/2/643/ds_cp_0adxx_series_1664149.pdf




## LV Fuse (F2)

https://www.mouser.de/datasheet/2/643/ds_cp_0679h_series_1290853.pdf




## Q3

https://www.vishay.com/docs/92296/slhp24n80ae.pdf

**ORDERING INFORMATION**

| | |
|---|---|
| Package | TO-220AB |
| Lead (Pb)-free and halogen-free | SiHP24N80AE-GE3 |

**ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-source voltage | | | $V_{DS}$ | 800 | V |
| Gate-source voltage | | | $V_{GS}$ | ± 30 | |
| Continuous drain current ($T_J$ = 150 °C) | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 21 | A |
| | | $T_C$ = 100 °C | | 13 | |
| Pulsed drain current [a] | | | $I_{DM}$ | 51 | |

a. Repetitive rating; pulse width limited by maximum junction temperature

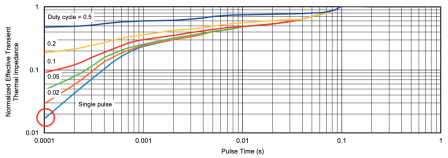



Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

## Q1 & Q2

https://www.mouser.de/datasheet/2/196/infineon_IMBG65R050M2H_DataSheet_v01_00_EN-3421343.pdf

CoolSiC™ MOSFET 650 V G2
IMBG65R050M2H

**1 Maximum ratings**
at $T_j$ = 25 °C, unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

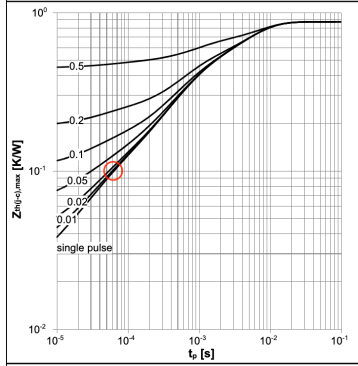
**Table 2 Maximum ratings**

| Parameter | Symbol | Values Min. | Values Typ. | Values Max. | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| Continuous DC drain current[1] | $I_{DDC}$ | - | - | 41 | A | $T_C$ = 25 °C |
| | | - | - | 28 | | $T_C$ = 100 °C |
| Peak drain current[2] | $I_{DM}$ | - | - | 114 | A | $T_C$ = 25 °C, $V_{GS}$ = 18 V |

2) Pulse width $t_{pulse}$ limited by $T_{j,max}$

## Q1 & Q2

**Diagram 4: Max. transient thermal impedance**




$Z_{th(j-c),max}$=f($t_p$); parameter: D=$t_p$/T

| | | |
|---|---|---|
| Sheet: / | | |
| File: DCDCv9-3 ESF.kicad_sch | | |
| **Title: DC/DC v9-3 ESF** | | |
| Size: A4 | Date: 2025-01-26 | **Rev:** |
| KiCad E.D.A. 8.0.5 | | Id: 1/1 |