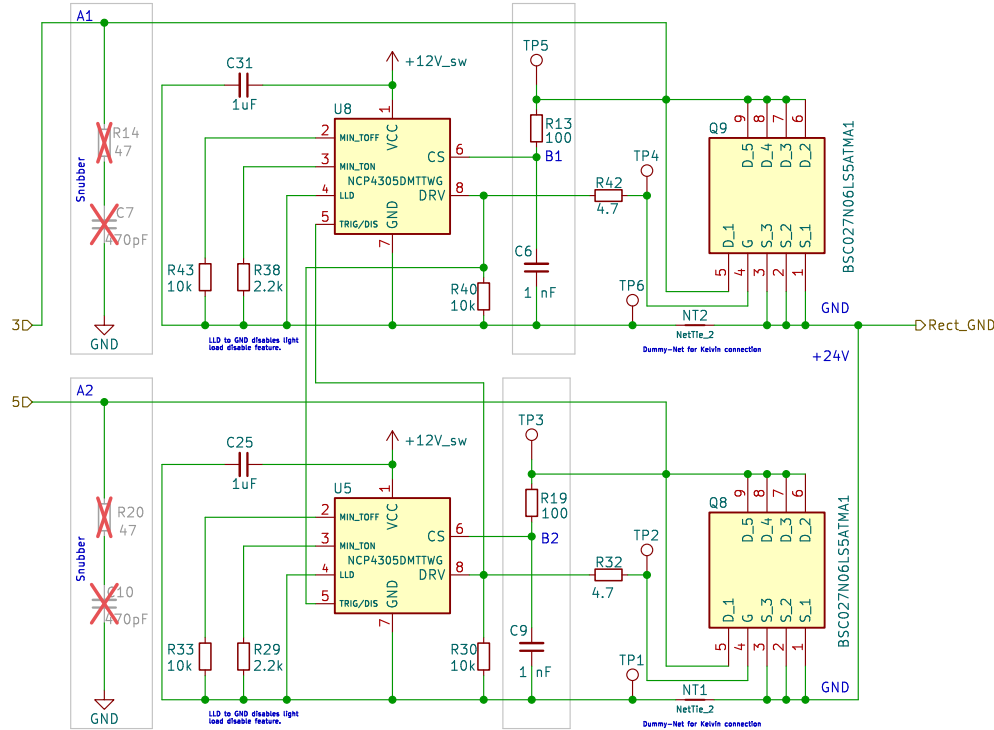




Note:  
There are two "snubbers" per SR FET (A and B).  
One is meant for snubbing (A), the other is meant as a lowpass for Cs trigger (B).  
If for some reason one or the other is not enough, both center taps can be connected on the PCB by adding enough solder.  
After some tests it turned out that the A1/A2 snubbers were not necessary -> DNP



B1 / B2 Lowpass  
 $V\_RSHIFT\_CS = R\_SHIFT\_CV * (-100 \mu A)$

$R_{ds\_on}(Q8, Q9, 60^\circ C) \approx 2.7 \text{ m}\Omega$   
Body Diode:  $0.6 \text{ V} @ 10 \text{ A}$   
-> From measurements assuming 5A passive rectification (both Body diodes) seem thermally okay (3W total / 1.5 W per device)  
5A would be the lower limit where we want to trigger active rectification.  
 $5 \text{ A} * 2.7 \text{ m}\Omega = 13.5 \text{ mV} (V\_RSHIFT\_CS)$   
 $V\_RSHIFT\_CS / 100 \mu A = R\_SHIFT\_CV (\text{max.}) = 135 \Omega$

$f_{ring} = 4.48 \text{ MHz} / 223 \text{ ns}$   
Note: There is a Snubber calculator available <http://paulorenato.com/index.php/197>  
However I ended up testing values from experience.

->  $1 \text{ nF}$  and  $100 \Omega$  could be okay ( $0.115 \text{ W}_{loss} @ 200 \text{ kHz} / 24 \text{ V}$ )  
->  $2.2 \text{ nF}$  and  $47 \Omega$  -> less voltage drop, better triggering ( $0.23 \text{ W}_{loss} @ 200 \text{ kHz} / 24 \text{ V}$ )

Edit:  $241118 \text{ } 1 \text{ nF}$  and  $100 \Omega$  tested to trigger better than  $2.2 \text{ nF}$  and  $47 \Omega$  for unknown reasons.  
The  $2.2 \text{ nF} / 47 \Omega$  variant also gets too hot.  
Untested till now:  $470 \text{ pF}$  and  $200 \Omega$  might be okay too -> Even fewer losses

Current through the MIN\_TON adjust resistor can be calculated as:

$$I_{R\_MIN\_TON} = \frac{V_{ref}}{R_{TON\_RHS}} \quad (\text{eq. 5})$$

If the internal current mirror creates the same current through  $R_{MIN\_TON}$  as used the internal timing capacitor ( $C_t$ ) charging, then the minimum on-time duration can be calculated using this equation:

$$t_{MIN\_TON} = C_t \cdot \frac{V_{ref}}{I_{R\_MIN\_TON}} = C_t \cdot \frac{V_{ref}}{\frac{V_{ref}}{R_{MIN\_TON}}} = C_t \cdot R_{MIN\_TON} \quad (\text{eq. 6})$$

The internal capacitor size would be too large if  $R_{MIN\_TON}$  was used. The internal current mirror uses a proportional current, given by the internal current mirror ratio. One can then calculate the MIN\_TON and MIN\_TOFF blanking periods using below equations:

$$t_{MIN\_TON} = 1.00 \cdot 10^{-4} \cdot R_{MIN\_TON} [\mu s] \quad (\text{eq. 7})$$

$$t_{MIN\_TOFF} = 1.00 \cdot 10^{-4} \cdot R_{MIN\_TOFF} [\mu s] \quad (\text{eq. 8})$$

Note that the internal timing comparator delay affects the accuracy of Equations 7 and 8 when MIN\_TON/ MIN\_TOFF times are selected near to their minimum possible values. Please refer to Figures 69 and 70 for measured minimum on and off time charts.

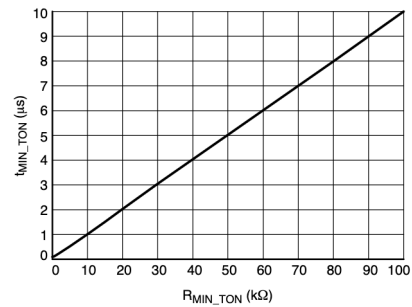


Figure 69. MIN\_TON Adjust Characteristics

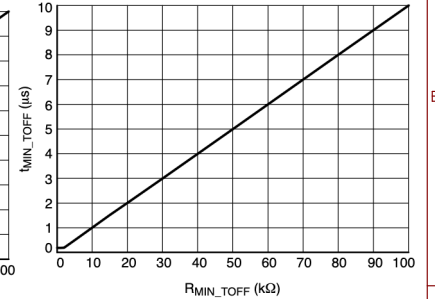


Figure 70. MIN\_TOFF Adjust Characteristics

Author: Roothecaue

Sheet: /Synchronous Rectification/  
File: Synchronous Rectification.kicad\_sch

Title:

Size: A4  
KiCad E.D.A. 8.0.9

Date:

Rev:  
Id: 2/2