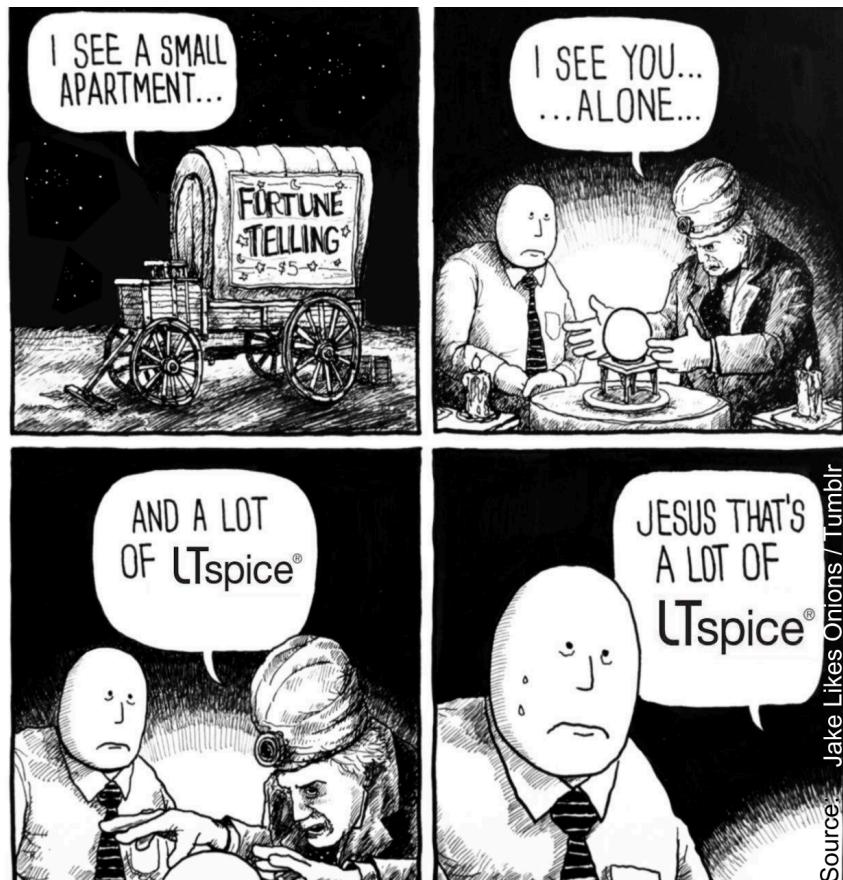


Open Source DC/DC converter Documentation



Good things take their struggle

Author:

Rootthecause

Date:

01/28/2025

Manual for hardware:

v9-3 / v9-3r

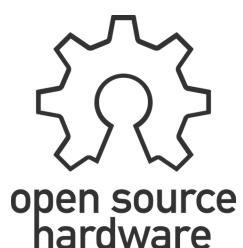
Language:

English

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GitHub: <https://github.com/Rootthecause/DCDC>



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1 Introduction

A DC/DC converter has been developed as part of Formula Student (FS) since 2020 to supply low-voltage components from a high-voltage source. This documentation is especially dedicated to FS teams who are looking for an alternative to expensive purchased modules or are not satisfied with the current solution.

Although the converter was already functioning satisfactorily in 2022 (version 8), there were some unused potentials, but also ambiguities that required further discussion for personal reasons. The unexpected complexity of some problems led to a delay in the open source release of around 2 years. In retrospect, the experience gained from these, albeit very time-consuming, further developments are irreplaceable for future in-house developments in the field of power electronics.

The author has tried to record the information for this project in this document to the best of his knowledge and belief. It provides an insight into the many difficulties encountered in practice and documents various, sometimes unsuccessful, approaches to solutions. However, some parts may be simplified due to the complexity and may not meet scientific standards. You are welcome to clarify open questions in the [discussion area](#) on GitHub, which will be included in updated versions of this document if necessary. Furthermore, the author would like to point out that this is a voluntary, largely self-financed leisure project and asks you to bear this in mind if you have any questions or criticism.

2 Acknowledgments

The basic idea for this project was born at the end of 2019. TzTz, a good friend of mine, has been supporting me ever since. The recommendation for the LLC topology and a large part of the precharge circuit can be traced back to him. Thanks to his experience and helpful tips, many problems could be solved quickly. Without him, the converter would not have been as small and reliable as it is today. Many thanks TzTz!

I would also like to thank my Formula Student team and the team's supporters. Without the team, the development of a DC/DC converter would not have been necessary and would not have undergone the necessary testing on the vehicle, which was essential for the further development of the design.

Note on translated content

This document has been translated from the German source file using DeepL. However, the translation has been reviewed and manually edited to ensure accuracy and clarity.

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3 Vocabulary and list of abbreviations

241018	...	Date in the format YYMMDD
Cr / Cres	...	Resonant capacitor in LC resonant circuits
CC/CV	...	Constant Current / Constant Voltage
CW/CCW	...	Clockwise / Counterclockwise (viewed from top)
DCDCv9-3	...	Version 9 of the DCDC converter in the third improvement
FET	...	Field Effect Transistor, usually meaning MOSFET
fsw	...	switching frequency
fres	...	Resonant frequency
GaN HEMT	...	Gallium Nitride High Electron Mobility Transistor
HV	...	High voltage (often also referred to as TS, as the battery generally supplies usually supplies high voltage)
Iso/ISO	...	Isolated, galvanically isolated
Lr / Lres	...	Resonance inductance or leakage inductance of a transformer
Lm / Lmag	...	Magnetization inductance of a transformer
Lp / Lprim	...	Primary inductance of a transformer (Lr + Lm)
LV	...	Low Voltage
HV	...	High-voltage battery in the automotive/formula student sector
Pre-charge	...	Circuit for controlled charging of the DC link capacitor
PFC	...	Power Factor Correction, a circuit for generating direct voltage from an DC voltage from an AC voltage source with an almost ideal sinusoidal current draw
TS	...	Tractive System, usually voltage supply from a
UVLO/OVLO	...	Undervoltage Lockout / Overvoltage Lockout
Via	...	Vertical Interconnect Access (through PCB)
Vpp	...	Peak-Peak Voltage
Vmax	...	Maximum Voltage
Vmin	...	Minimum Voltage
Vrms	...	RMS voltage

Colors / Text styles

Bold	...	In continuous text: Important information, Stand alone as title/heading
<i>Italics</i>	...	Informal comment by the author
Red	...	to be updated, inaccurate, not sufficiently documented
Text	...	Standard text

4 Concept and version history

4.1 Version 1 to 4 (2019 - 2021)

Initial research was carried out at the end of 2019. One candidate was the LT8316 as a flyback converter, although after extensive calculations it turned out that hardly more than 100 W output power would actually have been feasible due to the necessary inductance. Jörg Rehrmann's [website](#) offers various converter topologies with good explanations and complete circuit diagrams. Of these, a classic push-pull converter with a half-bridge was adapted to the requirements and, after a test setup on a breadboard (versions 1 to 4), was also produced as a PCB (version 5).

4.2 Version 5 (Jan. 2022)

With almost 200 components and 150 hours of simulation and development time, the first DCDC was tested. It showed a very good efficiency of 96.3 % at 470 V input and 500 W at the output as well as a maximum power of 540 W. However, this converter was anything but reliable and was difficult to regulate. Small errors in setting the frequency and dead time led to a loss of up to 10 components. This was repeated several times during 75 tests. Furthermore, at 600 V it was hardly possible to achieve more than 280 W at the output without overloading components. Later research then revealed a fundamental problem in understanding the topology used.

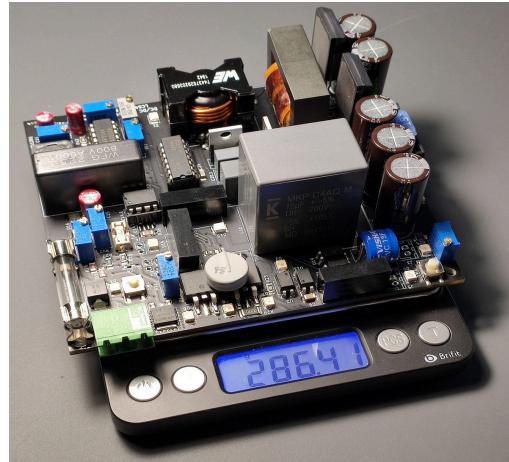


Fig. 2: DCDCv5 (first PCB),
100 x 115 mm, 286g, 48 V

4.3 Version 6 (Feb. 2022)

Initially, the plan was to solve the problems with version 5 for a DCDC version 6, but so many changes would have been necessary that an almost complete redevelopment was easier and version 6 was ultimately skipped.

4.4 Version 7 (April 2022)

For version 7, the topology was changed to an LLC converter. This offered the advantage that the resonant circuit requires fewer components, has lower EMI emissions and covers a wider voltage range. At the same time, circuits were simplified, unreliable components were removed and components in SMD housings were selected wherever possible. These changes led to a reduction to 100 components and a 40% reduction in size. The target power was increased to 750 W continuous and 1000 W peak for 10 seconds.

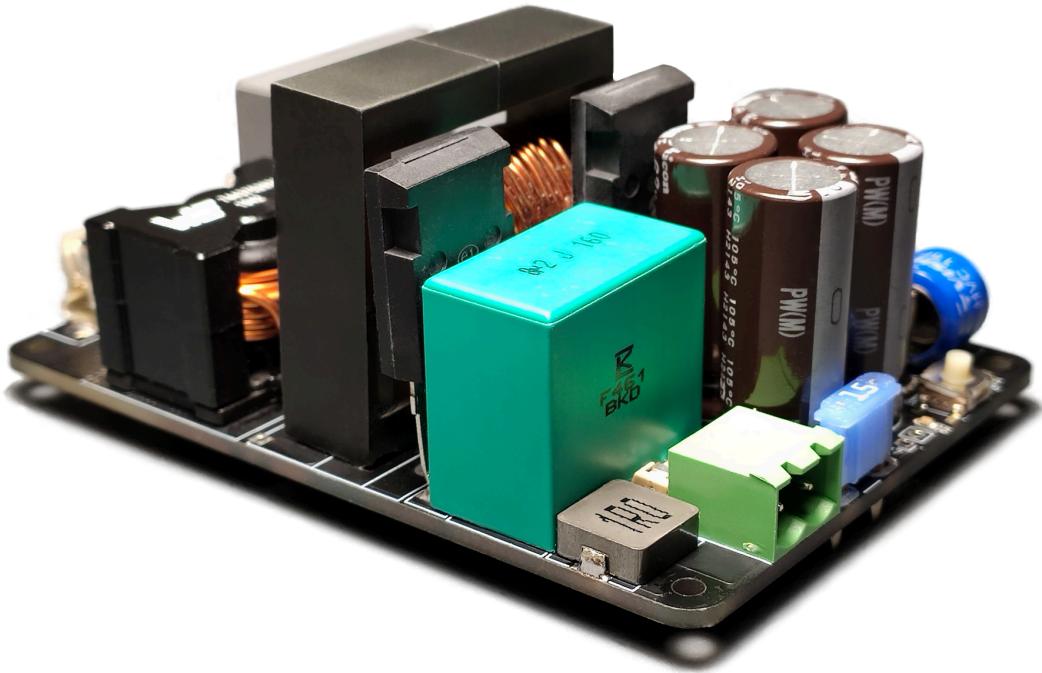


Fig. 3: DCDCv7, 100 x 70 mm, 235 g, 48 V

The aim of this new converter was to be as simple and reliable as possible. Therefore, a gate driver was dispensed and a gate transformer was used instead. Unfortunately, after many attempts, it turned out that the gate transformer only caused new difficulties (see Appendix Lessons Learned). A modified version with the gate driver IC from the previous version, on the other hand, delivered very good results. For the first time, the targeted power was not only achieved, but exceeded. It was possible to achieve 1000 W for 30 seconds and even 1500 W for 10 seconds. The biggest problem was the heat generated by the transformer and the rectifier diodes.

4.5 Version 8 (Juli 2022)

Even though version 7 was realized quite successfully with a 2-layer circuit board, significant improvements in the layout were only possible with a 4-layer circuit board, taking into account parasitic line inductances and capacitances. This meant that important current paths could be shortened by half and cable cross-sections quadrupled in some cases. In addition, both passive and active rectification could be used. In the test, the active rectification increased the efficiency by an average of 2 % and thus solved the overheating problem of the rectifier diodes at the output.

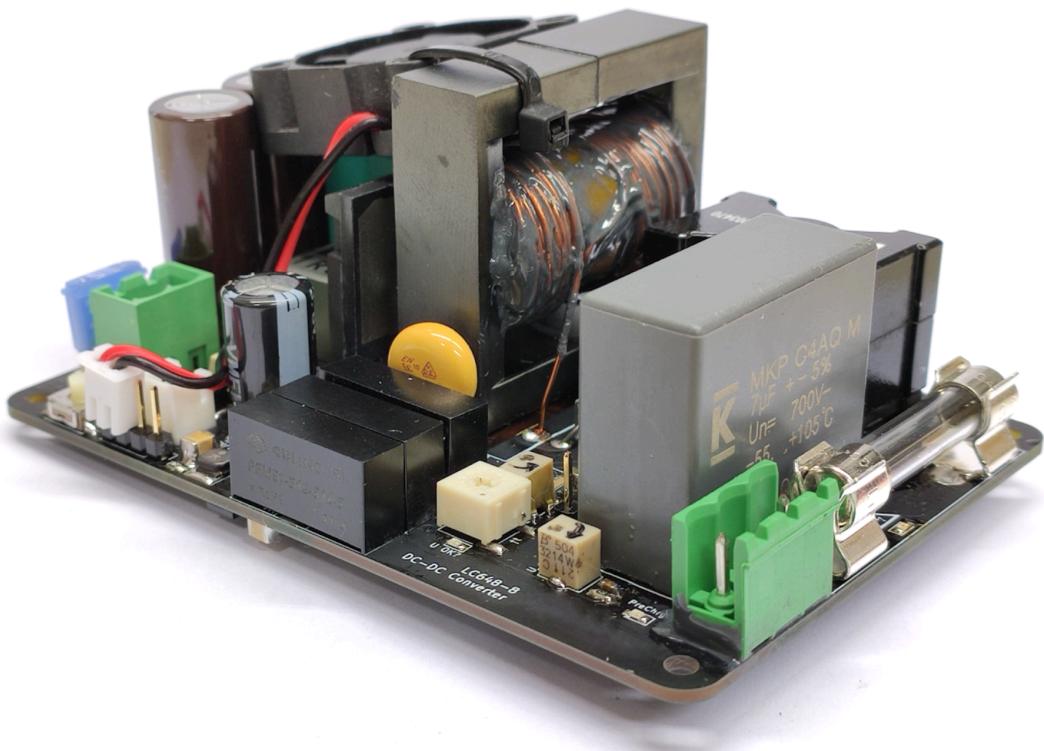


Fig. 4: DCDCv8, 100 x 70 x 45 mm, 228 g, 48 V

Efficiency vs. Power for multiple Voltages

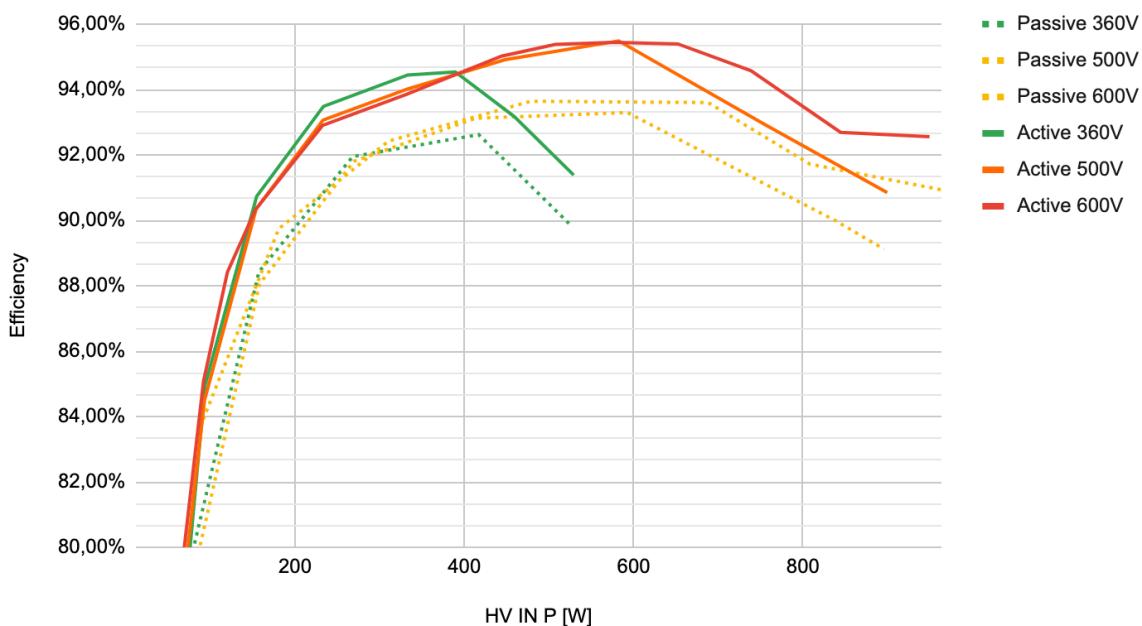


Fig. 5: DCDCv8, load-dependent efficiency at different voltages with comparison between active and passive rectification

4.6 Pre-Version 9 (Okt. 2022)

For the upcoming version 9, there was a test version in which new components and circuits were tested on the old circuit board. By optimizing the winding design, it was not only possible to integrate the resonant inductance into the transformer, which saves costs and space, but also to increase the peak efficiency by 3 % to 98.5 %; a new record!

Note: It was probably closer to 96-97 %, as the current measuring shunt and the measuring devices were not sufficiently calibrated at the time. Furthermore, the precharge was often bridged for testing, so that the losses had no influence on this.

4.7 Version 9 (Jan. 2023)

As with (unfortunately) every version to date, the 9th version also had to be redesigned from scratch in order to achieve good space utilization. During a presentation on version 8, it was jokingly said that the converter is about the size of two credit cards. Therefore, the size of a single credit card (85.6 mm x 54 mm) was targeted as a test for the next version. This would correspond to a 34% reduction in the size of the circuit board, but with the components of version 8 and the improvements and new features such as temperature monitoring and a revised precharge, this was not feasible in the space available. Furthermore, during tests of the previous version, the temperature increase of the half-bridge and rectifier FETs was recorded using a thermal imaging camera. The result showed that active cooling is necessary at continuous loads above 400 W to prevent overheating. As a solution, the heat sink, which is integrated into the circuit board as a copper surface, should not only become larger, but also use vias to transfer the heat to both sides of the circuit board in order to passively radiate more heat. However, this means that no SMD components can be placed on the opposite side and intermediate layers cannot be used for power or signal transmission.

Therefore, all components were packed as close together as possible (taking into account the clearance for high voltages) so that the cooling surface is maximized. Furthermore, some components were previously oversized or not utilized to their full potential. With the help of circuit simulation, the number of smoothing capacitors at the output could be reduced from 3 to 2 and the residual ripple decreased at the same time. In addition, the high-voltage side could be realized with only one isolating power supply transformer and bootstrapping instead of 3. The arrangement of the 12 V supply on the HV side also ensures that the oscillator can only be supplied when the precharge process is almost complete. Until the last trace between the components, it was not clear whether this design would stand up to further testing. It took 5 months from the first ideas for version 9 in August 2022 to the first review. Another month was spent just reviewing and correcting the design.

On January 11, 2023, the design of version 9 was presented to the racing team - and received very positively.

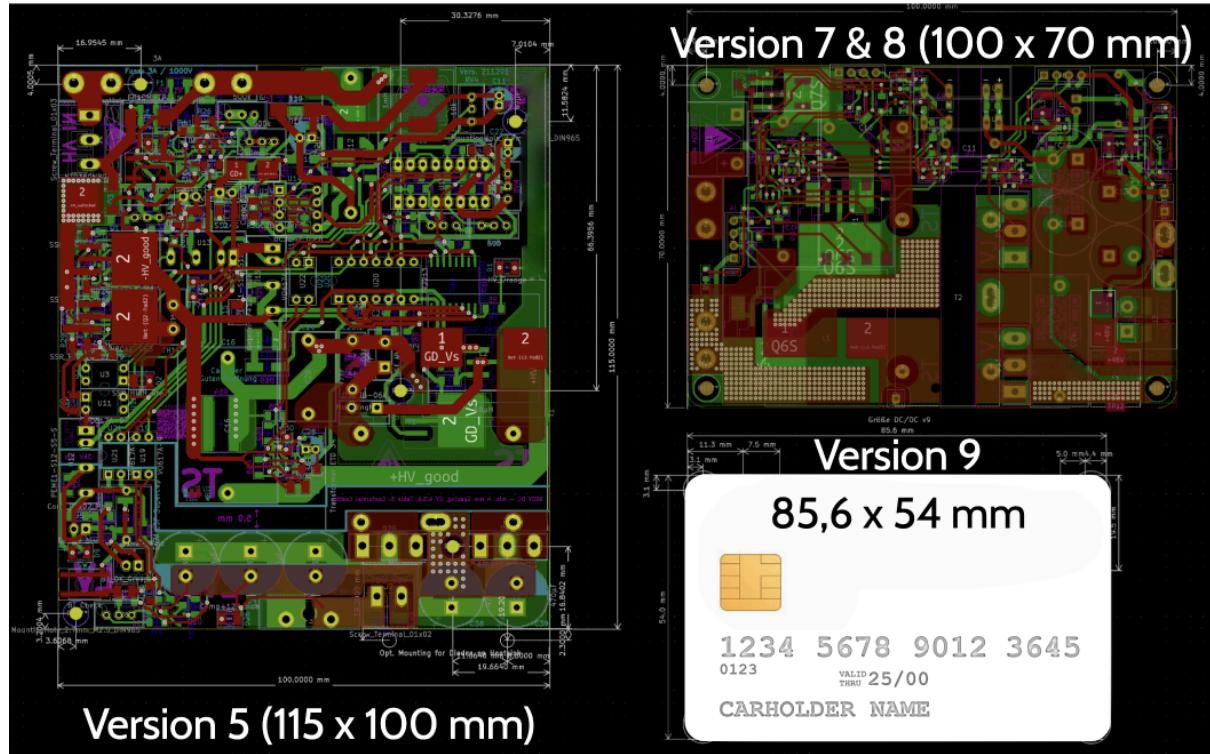


Fig. 6: Excerpt from the online presentation Design Freeze 11.1.23 DCDC converter v9

Over the next few days, the design was given the finishing touches and was ordered on 21. January 2023. Due to the Chinese New Year and long transportation times, delivery was delayed until the end of February. In the meantime, work was carried out on a DC high-voltage source, which was implemented in the form of active power factor correction (PFC). Voltages of up to 600 V and 1000 W output power were now possible.

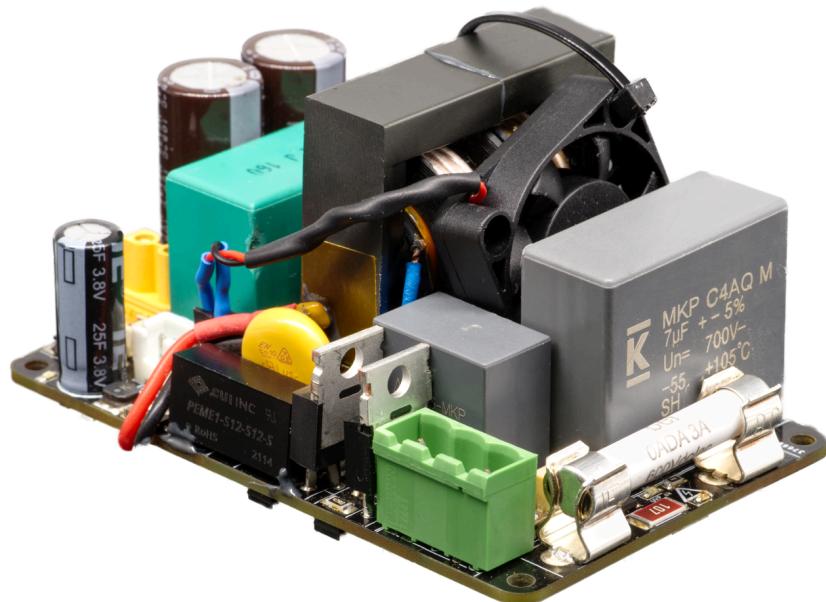


Fig. 7: DCDCv9-1, 85.6 x 54 x 45 mm, approx. 175 g, 48 V

4.8 Version 9-2 (May 2024), 24 V

This version has been designed for the first time with an output voltage of 24 V instead of the previous 48 V and fixes minor layout problems that were identified with version 9. An alternative soft start frequency ensures reduced inrush currents and a Power-ON LED (on the TS side) simplifies diagnostics in the event of faults. GAN HEMTs are used for the first time for active rectification. Even though the efficiency with the HEMTs was very good, there were problems with cooling and reliability. The delicate footprint of the HEMTs was susceptible to damage during replacement, which ultimately led to its destruction. A meaningful inspection of the solder joints beneath the HEMTs is virtually impossible using home appliances. In addition, replacement is difficult due to the required temperatures (max. 260 °C) and large cooling surfaces with hot air. Low-temperature solders with bismuth are expressly not recommended as the alloy is very brittle!

4.9 Version 9-3 (Sep. 2024)

An additional Power-ON LED (LV side) has been added. The trim potentiometer for setting the output voltage has been replaced by resistors. A split-cap topology is used for the first time, which reduces the input-side HV ripple by a factor of around 3.5 with the same DC-Link capacitor (simulation at 500 W). This made it possible to reduce the DC link capacitor from 7 µF to 2 µF with a slightly lower ripple. The space gained benefits the cooling of the transformer. The active rectification was again realized with MOSFETs (albeit a smaller package, TDSON-8 instead of TO-263-3) in order to achieve high reliability and better solderability. However, an adapter board for use with GaN HEMTs was already foreseen in the design. The so-called GaNapter can be soldered onto the DCDCv9-3 as an extension and can be replaced if the GaN footprints are damaged. A mounting hole in the board for optional installation of a heat sink has been retained from version 9-2.



Fig. 8: DCDCv9-3, 85.6 x 54 x 45 mm, approx. 167 g, 24 V

4.10 Version 9-3r (January 2025)

This is the release version for the public open source release. Small improvements have been made with buffer capacitors in the LV power supply to increase performance when using larger fans. When measuring the ripple voltage at the output, 1.5 Vpp voltage peaks were measured, which were associated with the step-down. Nevertheless, the exact cause is still unclear. The problem could be mitigated almost down to the measurement noise by using 1 nF capacitors and snubbers over certain components. The footprint for the 9 V LDO has been adjusted as the originally intended model is not available. The lowpass on the CS pin of the SR drivers was changed from $47 \Omega / 470 \text{ pF}$ to $100 \Omega / 1 \text{ nF}$ for more reliable triggering. The secondary-side snubbers were marked as DNP, as they were no longer necessary in tests (lowpass also acts as a snubber). The HV input connector was rotated 180° on the PCB.

4.11 Version 10 ?

Whether there will ever be a version 10 is not yet foreseeable due to time constraints. It will most likely not become smaller in terms of footprint, if it does, then only flatter, lighter and more powerful. If there will be one, here are a few ideas:

- Synchronous (full bridge?) rectification with GaN?
- Bidirectional (complicated! Not needed for FS)
- PCB transformer, matrix transformer (possibly too many losses :/ but could make isolation testing unnecessary)
- CLLC topology? (Requires own software / microcontroller?)
- GaN HEMTs for rectification and half bridge
- $f_{\text{sw}} > 500 \text{ kHz} \rightarrow$ Smaller/lighter, but more losses?
- C0G and ceramic capacitors, no more Film capacitors
- Pi filter at the input
- Load sharing
- Prechargeless design

5 Requirements by the Formula Student rules

The Formula Student Germany rules form the basis for most international Formula Student events. It also contains some rules on the use of high voltage on circuit boards. However, there are no specific rules on DC/DC directly.

The following rules have been summarized from the [Formula Student Rules 2025 v1.1](#).

Regel	Inhalt
T 11.1 ff.	The LV system refers to all electrical components of the vehicle, except HV components. The maximum voltage is 60 V DC or 50 V AC RMS.
EV 1.1	The Tractive System includes all components electrically connected to the accumulator and motor. The LV system may be supplied by TS if galvanic isolation is ensured.
EV 1.2.1	Galvanic isolation fulfills the following conditions: <ul style="list-style-type: none">- The resistance between the two circuits is $\geq 500 \Omega/V$ in relation to the maximum HV voltage of the vehicle- The isolation test voltage for 1 min. AC RMS is three times the maximum HV voltage- The isolation barrier, if specified in the data sheet, is higher than the maximum HV voltage

	Capacitors that bridge the galvanic isolation must be Y capacitors.																							
EV 1.2.2	A high current path is any path that carries more than 1 A in normal operation.																							
EV 4.1.1	The maximum permissible voltage between two electrical connections is 600 V DC, internal signals with low power are permissible up to 630 V DC.																							
EV 4.1.2	All components must be approved for the maximum HV voltage. The HV area on a circuit board is treated as one component. Each input to the HV must be capable of the maximum HV voltage.																							
EV 4.1.3	Alle Komponenten müssen für die maximal mögliche Temperatur beim Betrieb zugelassen sein.																							
EV 4.3.1	Das gesamte HV- und LV-System muss galvanisch isoliert sein.																							
EV 4.3.6	If HV and LV are present on the same PCB, the areas must be clearly marked with "TS" and "LV" as well as an outline and the distances must be in accordance with Table 5. <table border="1" style="margin-top: 10px;"> <thead> <tr> <th rowspan="2">Voltage</th> <th colspan="2">Clearance Distance</th> <th>Creepage Distance</th> </tr> <tr> <th>General</th> <th>conformal coating</th> <th></th> </tr> </thead> <tbody> <tr> <td>0 VDC to 50 VDC</td> <td>1.0 mm</td> <td>4 mm</td> <td>1.0 mm</td> </tr> <tr> <td>50 VDC to 150 VDC</td> <td>1.0 mm</td> <td>5 mm</td> <td>1.0 mm</td> </tr> <tr> <td>150 VDC to 300 VDC</td> <td>1.5 mm</td> <td>10 mm</td> <td>2.0 mm</td> </tr> <tr> <td>300 VDC to 600 VDC</td> <td>3.0 mm</td> <td>20 mm</td> <td>4.0 mm</td> </tr> </tbody> </table>	Voltage	Clearance Distance		Creepage Distance	General	conformal coating		0 VDC to 50 VDC	1.0 mm	4 mm	1.0 mm	50 VDC to 150 VDC	1.0 mm	5 mm	1.0 mm	150 VDC to 300 VDC	1.5 mm	10 mm	2.0 mm	300 VDC to 600 VDC	3.0 mm	20 mm	4.0 mm
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300 VDC to 600 VDC	3.0 mm	20 mm	4.0 mm																					
	Table 5: Spacing required between TS and LV.																							
EV 4.5.3	HV cables, connectors and isolators must be approved for an ambient temperature of at least 85°C.																							
EV 4.5.13	All electrical connections, including screws, nuts and other fastening elements in the high-current path must be secured against unintentional loosening and be suitable for high temperatures. Components that are certified for the automotive sector may also be permitted without protection against unintentional loosening if they have been implemented in accordance with the manufacturer's standards and no other solution is possible.																							
EV 4.5.15	Soldering in the HV high current path is only permitted if the following conditions are met: <ul style="list-style-type: none"> - Connections on a PCB - there is no connection to a battery cell or cable - the components are also mechanically secured against unintentional loosening 																							
EV 5.4.3	The LV system must not be accommodated in the HV accumulator housing, except for necessary components such as DC/DC converters [...].																							
EV 6.1.5	If the shutdown circuit is opened, the HV voltage in the DC link must fall below 60 V DC in less than 5 seconds [...].																							
T11.7 ff.	LV batteries are all cells that are connected to the LV system. They must be housed in a stable, waterproof, non-conductive housing. LV batteries must be protected against short circuits. With the exception of LiFePo4 cells, all lithium cells must be housed in a fire-resistant enclosure and include a monitorable battery management system with overcurrent, overtemperature, overvoltage and undervoltage monitoring. <p style="margin-top: 10px;"><i>Rules 2026: Cells for maintaining time and position information or for starting DC/DC converters are excluded from this rule.</i></p>																							

6 Assembly (v9-3 / v9-3r)

6.1 Overview

The DCDC consists of a high-voltage side (also known as the HV or TS side) and a low-voltage side (LV side). Both sides are separated by a 4.5 mm wide isolation gap.

The HV side contains:

- HV input connection and HV fuse
- Precharge
- Undervoltage and overvoltage monitoring
- Control IC (UCC25600)
- Gate driver IC (UCC21520)
- FET half bridge with transformer and resonant capacitors

Located on the LV side:

- Start capacitor and step-down for charging the capacitor
- Step-up for 12 V
- Active rectification with driver ICs and FETs
- Pi filter
- Temperature monitoring with fan control
- Temperature sensor connection
- LV output and output fuse
- LV fuse
- Enable connection
- Fan connection

Located between the HV and LV side:

- Transformer
- Y capacitor
- Isolated 1W power supply
- Optocoupler
- Fan and temperature sensor

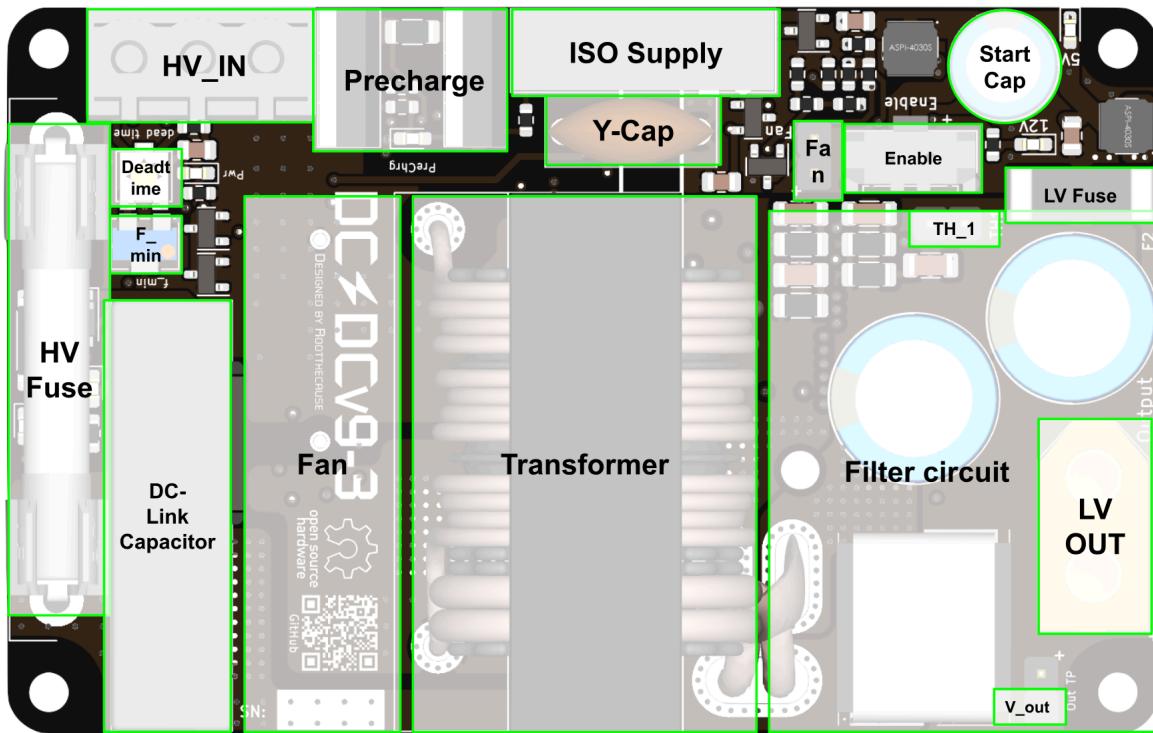


Fig. 9: Top side

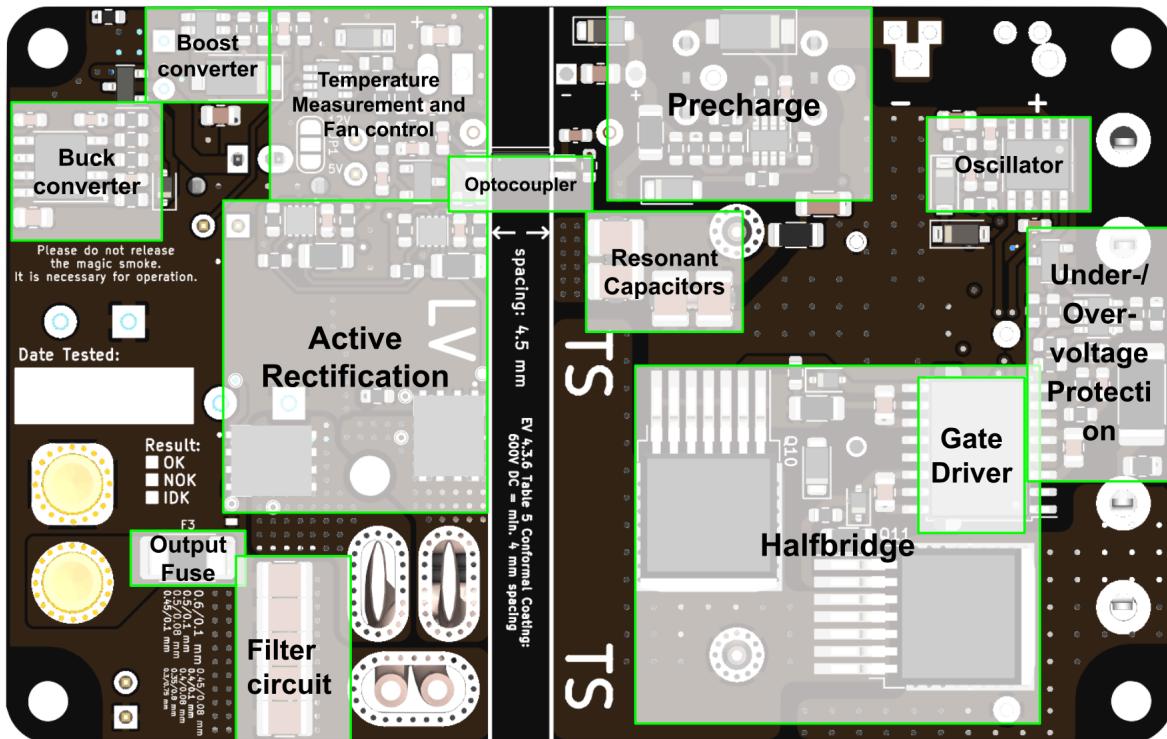


Fig. 10: Bottom side

6.2 Signal and power path

The following modules are described on the basis of the signal and power path over time.

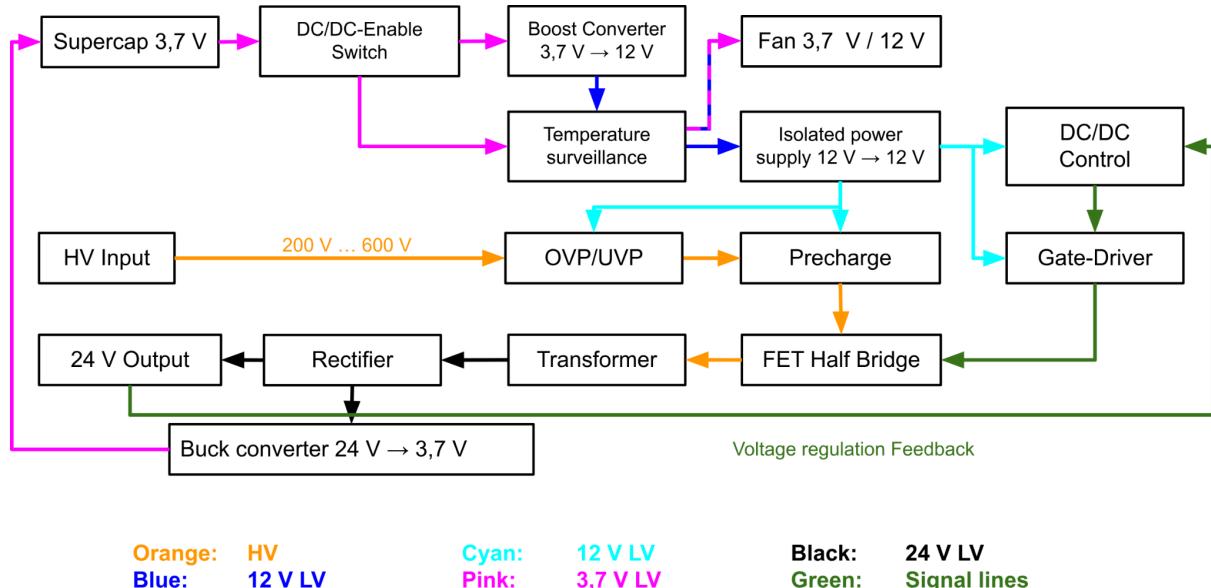


Fig. 11: Signal and power path of the DCDCv9-3

6.3 Modules

For the description of the modules, the circuit diagram has been limited to all relevant components as well as inputs and outputs of the respective module for a better overview.

6.3.1 Start capacitor, buck converter, boost converter

In version 5, the power supply for operating the control IC was implemented via an HV buck converter. This had the advantage that in the event of a discharged storage capacitor (which was necessary for galvanically isolated switch-on), the DCDC could be started manually via a pushbutton. However, several problems occurred:

- The HV buck converter had an efficiency of only 20% at 300 V (even less at 600 V)
- High EMI radiation due to low switching frequency
- Large space requirement for FET, capacitors and isolation clearances
- If the battery housing has to remain closed (passed scrutineering at an FS event), a discharged storage capacitor could not be recharged manually.

For these reasons, a buck converter was implemented at the output from version 7 onwards in order to be able to recharge the storage capacitor externally via the LV system and dispense the HV step-down.

Start procedure (starting with version 7)

Initial energy is required to put the converter into operation. Once the converter is in operation, it supplies itself via the output. The initial energy can be provided by small batteries or an HV buck converter. However, batteries were considered unsuitable for long-term use due to the need to change them. The HV buck converter was no longer used for the reasons mentioned before.

This limitation opened up the option of using supercapacitors. Tests showed that the voltage could be maintained for several months. However, some supercapacitors aged so much within a year that they only reached a few percent of their original capacity.

Useful life	4.13.2	$T_{amb} = 70^{\circ}\text{C} / 85^{\circ}\text{C}$; rated voltage U_R applied; 4.0 F, 15 F: 1000 h 90 F: 2000 h	$\Delta\text{C/C: } \pm 30\%$ $R_i \leq 4 \times \text{spec. limit}$ $I_L \leq 2 \times \text{spec. limit}$
-------------	--------	---	---

Fig. 12: Extract from data sheet: <https://www.vishay.com/docs/28409/196hvc.pdf>

In the end, a lithium supercapacitor was used as it had a relatively high voltage range of 2.5 V to 3.8 V and a high energy density. A boost converter is used to increase the voltage to 12 V so that the isolated energy transformer, fan controller and active rectification are supplied. On the HV side, the isolated energy supply provides power to the undervoltage and overvoltage monitoring, precharge, control IC and gate driver.

The precharge process takes between 70 and 230 ms, depending on the input voltage. The soft start of the control IC takes another 250 ms until the regulation voltage is reached. From around 5 V at the output, the buck converter can recharge the start capacitor with up to 800 mA to 3.7 V for renewed start processes.

The power loop is closed. Approx. 200 to 240 mA are drawn from the starting capacitor both during the starting process and in continuous operation (depending on the input voltage). The starting capacitor with 25 F has enough energy to maintain the starting process for approx. 100 seconds, provided that no high voltage is applied (in this case the current is only 100 mA). The voltage range of the capacitor is maintained by the limits of the buck and boost converters. If the capacitor has been discharged (e.g. by switching on the converter for a long time without HV supply), it can be recharged with 5 - 24 V via the LV output.

6.3.2 Pre-Charge

An DC link capacitor is required to enable clean operation. This capacitor (C1) is located directly at the half-bridge to reduce the current ripple at the HV input. However, if the converter is connected to a permanently charged voltage source with an empty DC link capacitor, a very large current would flow for a short time, charging the capacitor. This current could not only damage or destroy the connection contacts and the capacitor, but also trigger the fuse. To prevent this, various options were considered and tested:

- Time-controlled precharging via MOSFET and a resistor
- Time-controlled precharging via MOSFET and a PTC (DCDCv5)
- Precharging via step-down (not realized)
- DC link-controlled precharging via MOSFET and a resistor
- Time-controlled precharging via IGBT (DCDCv8)
- Constant current precharging with IGBT and voltage monitoring with voltage divider (v9/v9-2)
- Constant current precharging with IGBT and voltage monitoring with diode (v9-3)

Requirements:

- Suitable for a wide voltage range (200 V to 600 V)
- Precharging in max. 1 second
- low current consumption in ON state
- Low leakage current in OFF state
- Low conduction losses
- small footprint
- solid state

Although time-controlled precharging via an IGBT had worked successfully on the DCDCv8 for over two years of use, the conduction losses of the IGBT are quite high and it is difficult to maintain the safe operating area. The constant current precharge enabled a significant reduction in the precharge resistance as well as clearly defined switching thresholds. During more than 100 test series and over 6 months of use in the vehicle and additional Mad Scrut tests, no defects occurred. The latest variant from the DCDCv9-3 onwards uses only one diode instead of a voltage divider to detect complete precharging, which reduces the current consumption in the switched-off state to the leakage current of the diode used (measured 75 nA @ 21°C / 600 V input).

Operating principle

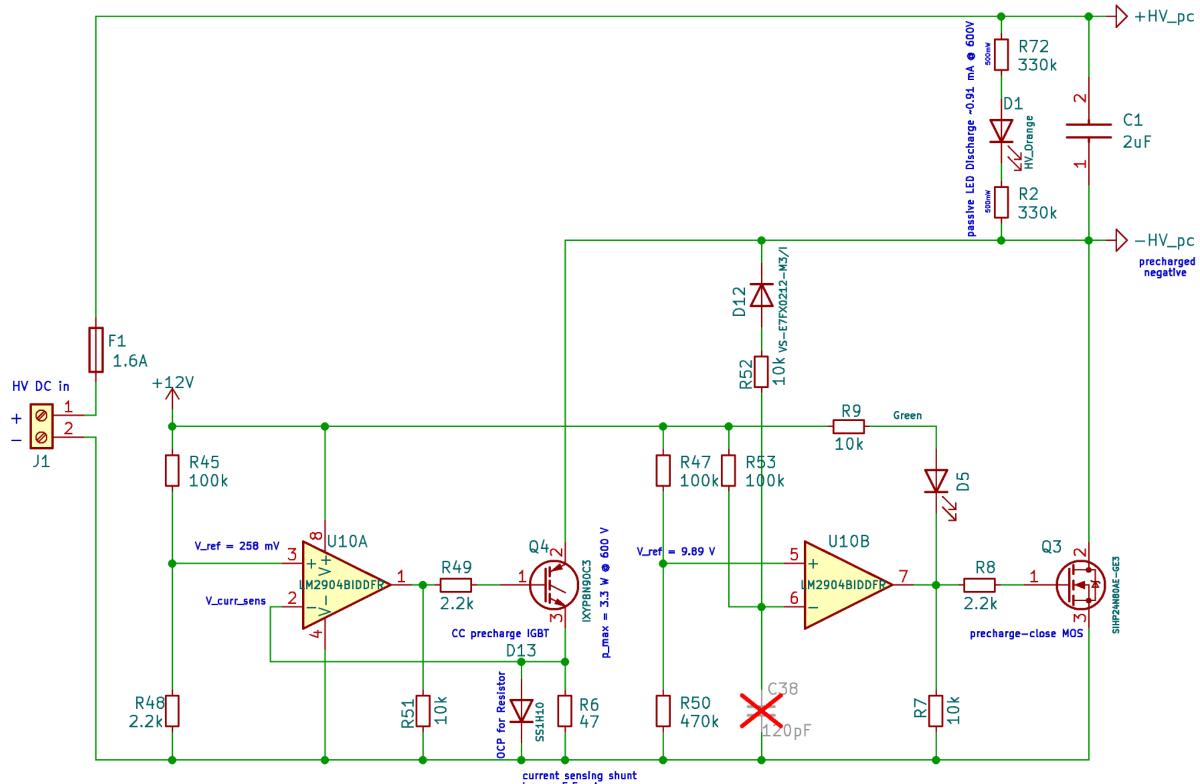


Abb. 13: Precharge Schaltung

When switched off, Q4 and Q3 are blocked, so no current flows in C1 (DC link capacitor). The half-bridge with transformer, voltage monitoring and control IC is located between +HV_pc and -HV_pc. The precharge itself is located below the DC link capacitor which is to be charged and is therefore also referred to as a low-side precharge.

If the precharge is supplied with 12 V, a low voltage is present at the output of U10A so that Q4 is slightly conductive (linear operation). U10A regulates the current through Q4 so that the voltage drop across R6 (for current measurement) corresponds to the same voltage as at the voltage divider R45/R48. The voltage divider designed for 258 mV allows a current of 5.5 mA through Q4 and uses this current to charge the DC link capacitor.

The following applies:

$$I_{precharge} = \frac{U_{+U10A}}{R_6} = \frac{12V \cdot R_{48}}{(R_{45} + R_{48}) \cdot R_6}$$

During the charging process, the voltage in the DC link increases and the voltage between -HV_pc and GND decreases.

The operational amplifier U10B uses the voltage divider R47/R50 as a reference at the non-inverting input. If the voltage between -HV_pc and GND falls below the 12 V supply voltage, a current can flow out via D12, causing the inverting input to fall below the reference voltage. Q3 is then switched on and the precharge process is complete.

D13 is used to protect R6 in the event of unexpected current peaks. R50 and R51 serve as a pull-down when switched off. R49 and R8 serve as current limit of the OPVs when charging the gate capacitances. R52 and R53 limit the current through D12, which also results in a voltage divider in the conductive state. This voltage divider must be taken into account if the exact switching point is to be determined. D5 (green LED) with its series resistor R9 indicates whether the precharge is currently precharging and whether Q3 is not yet closed. C38 is a placeholder in case a low-pass filter would have been necessary.

Q4 is designed as an IGBT, as the Safe Operation Area (SOA) of MOSFETs can withstand significantly less current in continuous linear operation at high voltages than IGBTs.

If the precharge process is not completed after max. 300 ms (D5 lights up continuously), an error has occurred. Either the DC link is permanently discharged (e.g. MOSFETs of the half bridge are defective) or the shunt R6 is high-impedance/defective. In the former case, a maximum input voltage of 600 V would result in a power loss of 3.3 W across the precharge IGBT. After approx. 100 seconds, the start capacitor would then be discharged so that the precharge process is aborted.

6.3.3 Discharge

According to the FSG rules (EV 6.1.5), the DC link capacitor must be below 60 V DC within 5 seconds of switching off. Although this rule only applies to the drivetrain of a Formula Student vehicle, it has also been implemented in this case for safe handling after the converter has been disconnected from the voltage source. R72 and R2 limit the current through D1 (orange LED), which indicates the presence of high voltage on the DC link and also serves as a passive discharge. The exact discharge times can be found in the [data sheet](#) on page 5.

6.3.4 DC link capacitor

The design was simulated at maximum continuous load (500 W) and minimum input voltage (400 V) and a voltage source with 600 mΩ internal resistance (corresponds approximately to the ESR of the HV battery used in the vehicle). The key criteria was a maximum ripple voltage of 1 Vpp. In practice, this value has not yet caused any electromagnetic or galvanic interference to other components in the HV system. A higher or lower value should also be possible depending on the application.

Initially, a capacitor of 470 µF was used, as this was taken from a circuit diagram for a mains-powered converter (50 Hz AC with bridge rectification). For DC operation, however, only a capacitor with 7 µF was required. From version 9-3 onwards, a change was made from a single resonant circuit capacitor to a split-cap topology, which simulatively reduced the ripple voltage by a factor of 3.5 with the same capacitance. As a result, a 2 µF capacitor is now sufficient. This not only reduces space and costs, but also the charging time.

6.3.5 Control IC UCC25600

The UCC25600 is a current-controlled oscillator with 50/50 duty cycle and adjustable dead time. The maximum switching frequency is 350 kHz, with burst mode being activated if a higher switching frequency is required to maintain the output voltage. The controller designed for the LLC topology is completed with a soft start and overcurrent measurement.

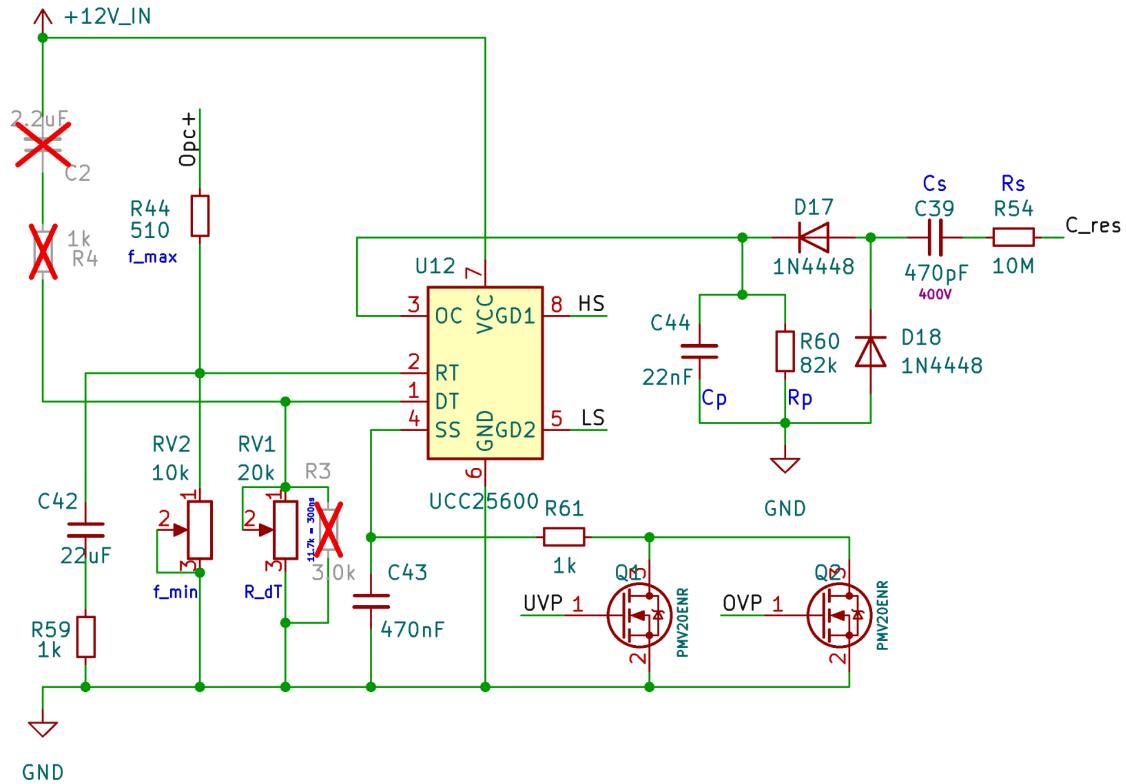


Fig. 14: Oscillator circuit

RV1 sets the dead time. A larger value increases the dead time respectively turning the potentiometer counterclockwise. A longer dead time means higher losses due to longer current flow via the body diode (forward voltage) instead of the conductive channel when switched on. A dead time that is too short leads to a (partial) bridge short. The optimum dead time is set at maximum input voltage and no load (highest switching frequency) by reaching the lowest HV current consumption.

According to the data sheet, the minimum dead time of the controller is 120 ns. In practice, an optimum resistance value for RV1 of 3.0 kΩ was determined for the DCDCv9-3, which would correspond to a dead time of 90.6 ns. Therefore, the minimum dead time of 120 ns should be output. Nevertheless, a change in the converter current consumption was observed in practice for resistors below the minimum dead time, which was interpreted as a reduction in the dead time. Contradictorily, an earlier measurement showed an actual minimum dead time of 119 ns. It is possible that reducing the resistance below the minimum dead time leads to a reduced current consumption of the controller, which is reflected in the total current consumption. This behavior was not investigated further, but it can be assumed that the minimum dead time of 120 ns could be even lower, especially considering the fall and rise times of the FETs used of less than 20 ns.

The internal soft start of the UCC25600 carries a risk that only became known when the transformer design of the v9-1 was used: Since the frequency at which the half-bridge is switched when the converter is started depends on the current of the RT pin, it is influenced by the minimum switching frequency.

F_min [kHz]	F_ss [kHz]	Ratio F_ss/F_min
50	149.15	2.98
75	172.7	2.30
100	196.2	1.96
125	219.7	1.76
150	243.3	1.62
175	266.85	1.52
200	290.4	1.45
225	314	1.40
250	337.6	1.35
300	384.8	1.28

The following gain curves for the resonant circuit of the v9-3 show that the minimum switching frequency is approx. 93 kHz ($U_{in} = 400$ V) and the maximum is 155 kHz ($U_{in} = 600$ V). It can now be estimated from the table that the soft start frequency for F_{min} is correspondingly approx. 185 kHz, i.e. only slightly above the maximum switching frequency. In practice, this means that the desired effect of a low starting current is hardly present at a high input voltage, especially in the sense that the output capacitors are being charged during start-up. In the v9-1, this occasionally led to the destruction of the active rectification. Measurements using the voltage rise of the output capacitors showed that the charging current was up to 500 A.

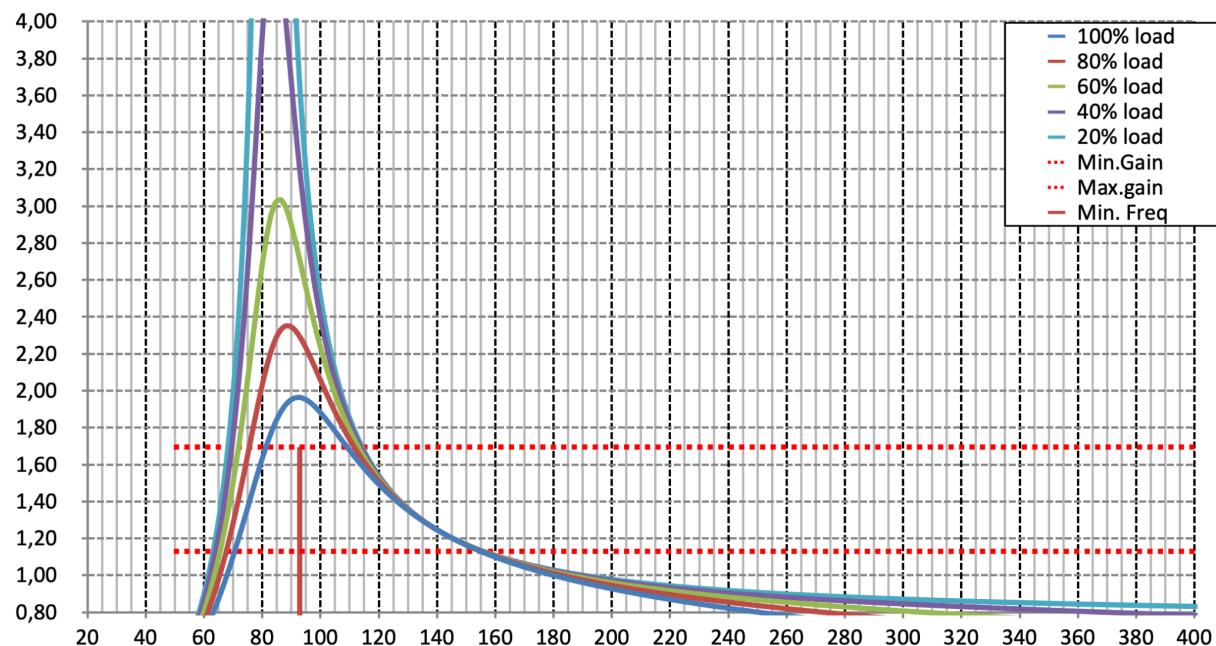


Fig. 15: Gain curves for the DCDCv9-3, horizontal red lines: min./max. gain for 400 to 600 Vin

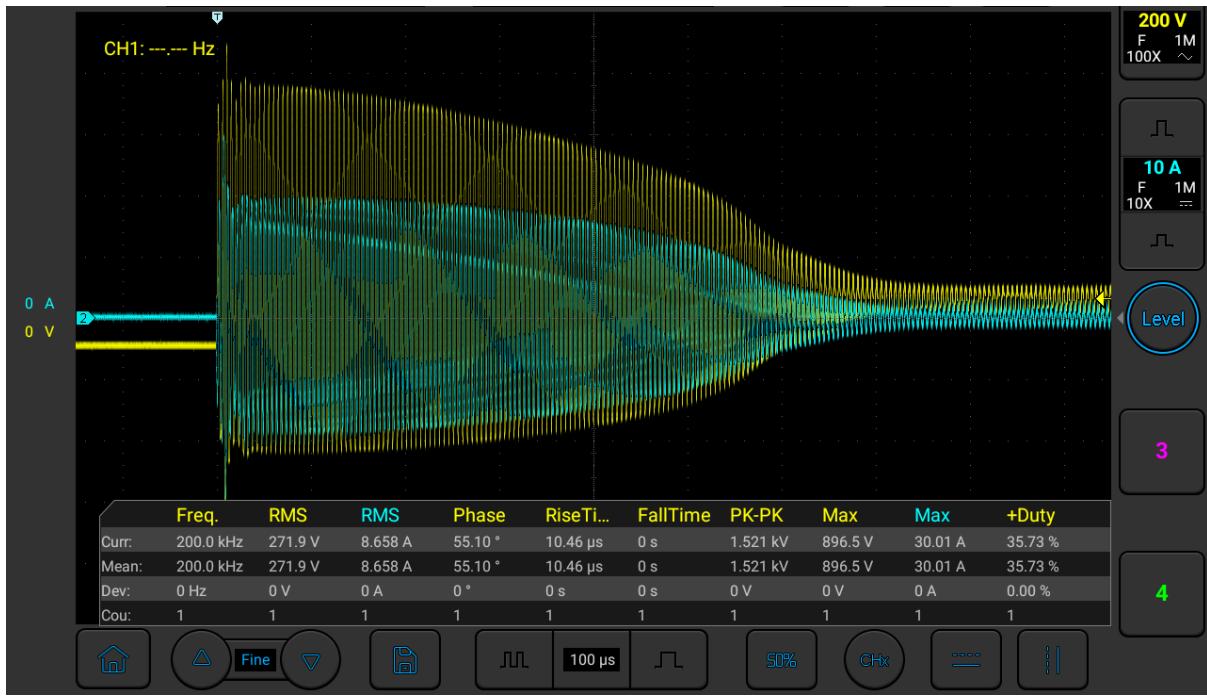


Fig. 16: Measurement at the start of the converter v9-1 at 500 V input voltage, cyan: transformer current on the primary side (presumably inverted), yellow: voltage across the resonant capacitor

Two approaches were considered as a solution:

- PMW ramp
- Increasing the soft start frequency

Research has shown that some converter ICs use a smaller but still symmetrical pulse width instead of a 50/50 duty cycle for the half bridge during the start-up process. However, the UCC25600 does not have direct PWM control, but a similar effect can be achieved by greatly increasing the dead time. An increase can be achieved by reducing the current from the DT pin. As a simple solution, a capacitor with resistor (to limit the current) was connected between Vcc and DT (C2 + R4). When the converter is switched on, a decreasing current ramp is achieved at the DT pin. However, the actual result was unexpected: If the current flow of the ramp is too high, the switching frequency is halved or even quartered. This approach was not pursued further due to safety concerns as well as the small reduction in the duty cycle.



Fig. 17: Measurement at the start of the converter v9-1 at 600 V input voltage with dead time soft start, cyan: transformer current on the primary side (presumably inverted), yellow: voltage across the resonant capacitor, purple: lowside gate signal, green: output voltage across the capacitors (2350µF)

As already described, the soft start frequency depends on the current of the RT pin. Here again, the idea arose of using a capacitor and resistor between the RT pin and ground to increase the RT current during the start process, thereby increasing the switching frequency. In tests, a 1 kΩ resistor with a 22 µF capacitor proved its effectiveness. The initial switching frequency is now approx. 340 kHz, independent of RV2.

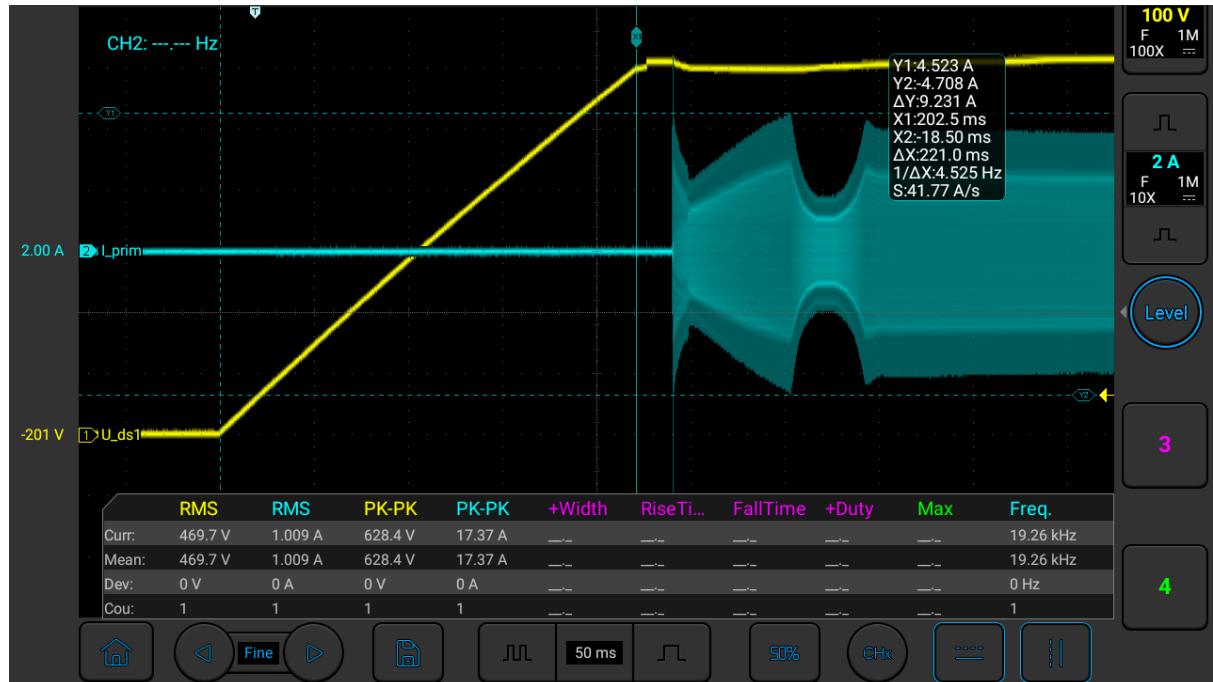


Fig. 18: Measurement at the start of the converter v9-3 at 600 V input voltage incl. precharge, cyan: transformer current on the primary side, yellow: voltage across the DC link capacitor, purple: lowside gate signal, green: output voltage across the capacitors (940 µF)

Switching frequency time profile v9-3

Time after [ms]	0	20	50	100	200	300
Switching frequency [kHz]	341	209	177	156	117	96

The tau of the RC element is 22 ms, so the influence of the external soft start is expected to be short. However, this is sufficient for limiting the inrush current. The internal soft start then takes effect with a duration of approx. 265 ms (470 nF) until the nominal switching frequency is reached. If the soft start is pulled to ground by the undervoltage or overvoltage measurement, the UCC25600 is deactivated and the RC element on the RT pin is discharged. The control behavior of the IC is not significantly influenced by the RC element, as it is current-controlled and a constant voltage is applied to the RT pin.

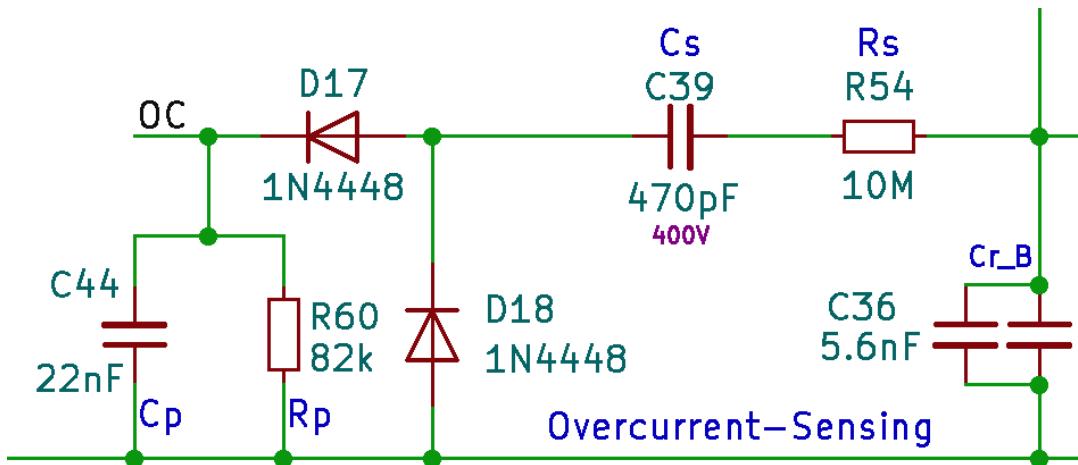


Fig. 19: Overcurrent measurement of the v9-3

The overcurrent measurement is realized by rectification with diodes across the resonant capacitors, as the primary current is proportional to the voltage across the resonant capacitors. R60 forms a voltage divider with R54, whereby R54 also functions as a current limiter. C39 is used as a DC current block. C44 delays the response time to peak voltage. The overcurrent threshold can be set via R60. The output of the UCC25600 is deactivated when the voltage at the OC pin reaches 1 V and is reactivated when the voltage falls below 0.6 V. With loads that do not behave ohmically, such as step-up/down converters, this can lead to the load drawing a higher current at low voltage than at nominal voltage when restarting after an overcurrent event, causing it to turn off again due to overcurrent. As a result, the converter may oscillate in the lower Hz range, which could damage both the load and the converter in the long term. As a countermeasure, step-up/down should only be switched on from an input voltage of approx. 80 to 90 % of the nominal voltage (24 V). Although the IC also has overcurrent latching, this only triggers at 2 V. However, due to the capacitors at the output, the slow control circuit and the delay of C44, latch-up is hardly possible, as the 2 V would have to be reached instantaneously at the OC pin before the switch-off at 1 V occurs. A short circuit could perhaps lead to a latch-up, but this has not been verified.

The response value of the overcurrent detection, however, leads to a problem with the large input voltage range of the v9-3: As the switching frequency decreases with decreasing input voltage, the voltage at the resonant capacitors increases with constant transformer primary current.

$$U_{Cres} = \frac{I_{prim}}{2 \cdot \pi \cdot C_{res} \cdot f_{sw}}$$

For example, at an input voltage of 200 V and $f_{sw} = 93.2$ kHz, around 3.8 A primary (approx. 300 W load) is possible, whereas at 300 V and $f_{sw} = 104.7$ kHz, 4.2 A (approx. 500 W) is already possible. Meaningful current limiting over the entire input voltage range is therefore only possible to a limited extent.

The overcurrent measurement, as currently implemented in the UCC25600 data sheet, can cause more difficulties than an ordinary fuse at the output due to the characteristics shown. For this reason, overcurrent detection was often deactivated in older versions. During the measurements on the v9-3, no unwanted oscillations with the overcurrent measurement have been observed in the intended input voltage range. However, it cannot be completely ruled out that large inrush currents could lead to this.

6.3.6 Resonant capacitors

The capacitors for the resonant circuit are exposed to high frequencies and voltages. The correct choice is therefore essential for reliable operation. Up to v9-2, film capacitors were used as they prove to be particularly robust, depending on the manufacturer. However, the voltage derating depending on the frequency is scary. A 700 V AC film capacitor with 22 nF only has a dielectric strength of around 130 V AC at 200 kHz. Fortunately, this switching frequency is only achieved without load at $V_{in} = 600$ V, so that only approx. 60 V AC is actually measured at the capacitor. The situation is more problematic at $V_{in} = 300$ V and 105 kHz: Here, approx. 280 V are present at the film capacitor.

The maximum permissible currents are also frequency-dependent. Fortunately, the current carrying capacity increases with increasing frequency and capacitance. For the same capacitor, up to 4 Arms would be permissible starting at 100 kHz. The measurements with the DCDCv9-3 show up to 4.9 Arms at $V_{in} = 400$ V and $P_{out} = 740$ W, $F_{sw} = 117$ kHz. Therefore, a maximum output power of 550 W is permitted when using this capacitor.

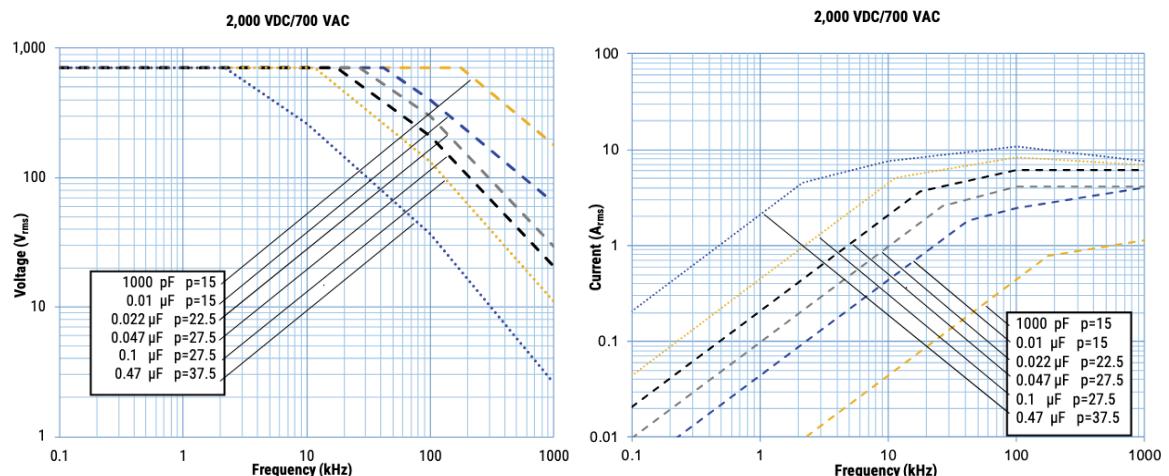


Fig. 20: Derating curves for voltage and current of a film capacitor, [KEMET](#)

Ceramic capacitors were also considered to reduce the space required. However, conventional MLCCs with X5R or X7R are not suitable without further ado due to the strong change in capacitance depending on the voltage applied. Ceramic capacitors with a C0G or PNO dielectric, meanwhile, have excellent capacitance stability over the entire voltage and temperature range.

But they also have deratings: at $F_{sw} = 117$ kHz, only 1.44 Arms would be permissible.

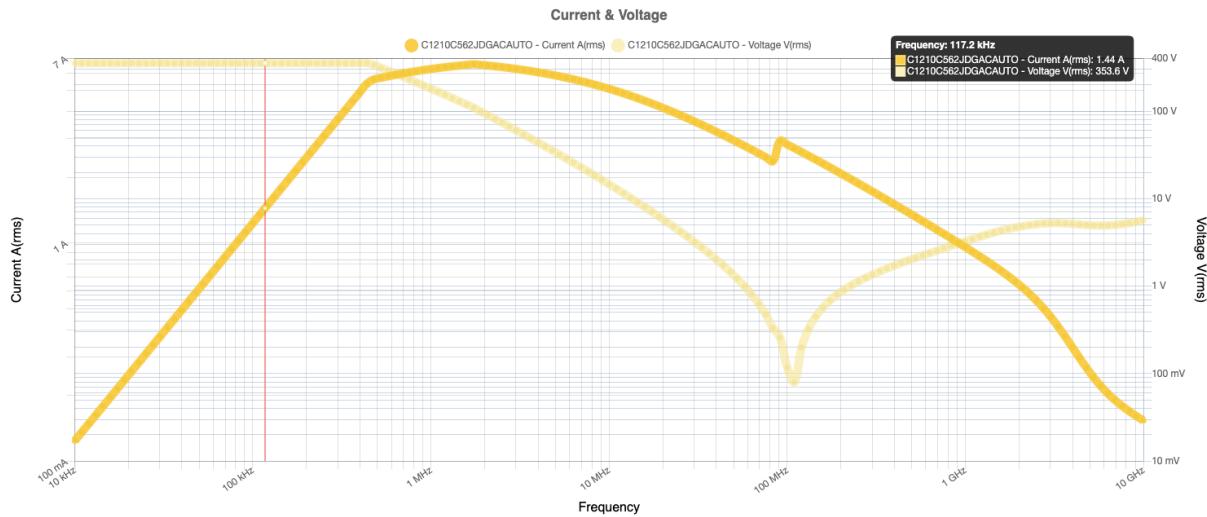


Fig. 21: Derating curves for voltage and current of a C0G capacitor, [KEMET](#)

For this reason, 4 units were used in parallel or 2 units in parallel on each side for the split-cap topology. This allows a transformer current of up to 5.76 Arms and $P_{out} = 740 \text{ W}$ at $V_{in} = 400 \text{ V}$.

However, care must be taken when setting F_{min} (see Build Guide) at low input voltages: Large currents may already be present in the resonant circuit here. For example, at $V_{in} = 50 \text{ V}$, $P_{out} = 41 \text{ W}$, $f_{sw} = 83 \text{ kHz}$, 3.3 Arms are already present. The current carrying capacity of the capacitors is only 1.02 Arms or 4.04 Arms in total. Overloading the C0G capacitors can lead to fires and should be avoided by all means.

6.3.7 Gate Driver UCC21520

This gate driver has an isolated high-side and low-side driver with a current of up to 4 A / 6 A (source/sink). The voltage difference between the high-side and low-side driver can be up to 1500 V. The IC was difficult to obtain during the 2020- 2023 chip crisis and is to be replaced by a modern solution in a possible version 10 (smaller package, more current, separate source/sink connections). The chip also has its own dead time control, but this is deactivated as the one already present in the UCC25600 is used. The UCC21520 is available in two versions with different UVLO. For this project, 8 V (UCC21520DW) is used.

6.3.8 Active rectification with NCP4305

The small chip in the WDFN-8_2x2 housing enables a FET to be controlled in such a way that it behaves like a diode. This circuit is known as active rectification or synchronous rectification (SR). By selecting a suitable FET, losses can be greatly reduced compared to conventional diodes. The switching thresholds are detected via the drain-source voltage of the MOSFET, whereby the FET is switched on when the voltage falls below -75 mV. The FET is switched off when the voltage falls below a voltage drop of around 0 mV via the R_{ds_on} of the FET. However, this detection led to problems with the DCDCv9-2, as the switch-off process was triggered too early due to the overshoot of the leakage inductance of the LLC transformer. This problem also occurred with the previous SR controller UCC24612, but was only discovered later during tests with GaN HEMTs, as the much more sensitive HEMTs were quickly destroyed as a result of switching incorrectly.

[Assumption] In this case, significant currents in reverse operation lead to a large voltage drop in the switched-off HEMT, causing the chip temperature to reach unacceptable values. However, this is difficult to prove as the mechanisms of destruction take place very quickly. The problem with overshoot may only occur in secondary windings with a center tap and full-wave rectification of such magnitude.

FETs, on the other hand, can withstand higher currents due to the intrinsic body diode and better heat dissipation of the larger housing.

During the tests with the v9-2, the problem was solved using a low-pass filter on the CS-Pin. However, mechanical influences led to the destruction of the filigree footprint before further tests could be carried out to fully evaluate the GaN HEMTs. The low-pass filter was implemented as standard on the v9-3. However, as it is uncertain whether HEMTs with this change will really function error-free and withstand the required power, FETs were used. When redesigning the SR FETs, a FET was found in a type comparison that has only a third of the power loss of the previous FETs and a significantly smaller footprint. This means that it performs only slightly worse than the best HEMT and is within a very acceptable power loss range.

Name	Package	Type	Voltage [V]	Current cont. [A]	total_loss [W]
GAN3R2-100CBEAZ	WLCSP-8	GaN	100	60	0,62
BSC027N06LS5ATMA1	TDSON-8	Si	60	134	0,94
CSD19532KTT	TO-263-3	Si	100	200	3,12
NTB7D3N15MC	TO-263-3	Si	150	101	3,22
CSD19531KCS	TO-263-3	Si	100	200	3,29
CSD19535KTTT	TO-263-3	Si	100	197	3,39

The complete table can be found in the [DCDCv9-3 Table](#) on the FET Selection page

For experiments with HEMTs on the v9-3, an adapter board “GaNapter” was developed, which can be soldered onto the footprints of the FETs. When changing to GaN, it is essential to replace U5 and U8 from the NCP4305DMTTWG (9.5 V gate voltage) to the NCP4305AMTTWG (4.5 V gate voltage)! At the time of publication, the GaNapter had not yet been tested. This could take efficiency and output power to new heights, as the power dissipation of the previous FETs was the limiting factor.

For a possible version 10, a change to GaN HEMTs is being considered for both synchronous rectification and HV half-bridge, which promises a significant improvement in efficiency due to its extremely fast switching times, very small junction capacitance and low driving energy.

6.3.9 LLC-Topology

The heart of the LLC converter is the series resonant circuit, consisting of a magnetizing inductor, a leakage inductor and a resonant capacitor. The half-bridge consists of two FETs, which alternately switch the resonant circuit to the supply or to ground, so that the capacitor in the resonant circuit is charged and discharged. The resulting alternating current is used to transfer energy within the transformer. Due to the resonant behavior, a specific voltage boost is also possible, which makes a large input voltage range usable.

This comparatively simple-sounding topology was first described in 1988 [\[Source\]](#). Yet due to its complicated regulation and difficult design, it received little attention. It was only in the last decade that this topology regained importance, as the trend towards more powerful and smaller voltage converters required ever higher switching frequencies. In conventional push-pull converters with hard switching behavior, the higher switching frequencies result in greater switching losses. Resonant converters such as the LLC converter, however, have a soft switching behavior (depending on the operating point), which significantly reduces current and voltage peaks.

In LLC converters, the half-bridge is usually operated at a frequency slightly above the resonant frequency of the resonant circuit in order to operate in the inductive range. The currents across the power switches (MOSFETs in this case) lag behind the voltage, which enables zero voltage switching (ZVS) in the half bridge and zero current switching (ZCS) in the rectification and reduces switching losses.

6.3.10 Resonant circuit

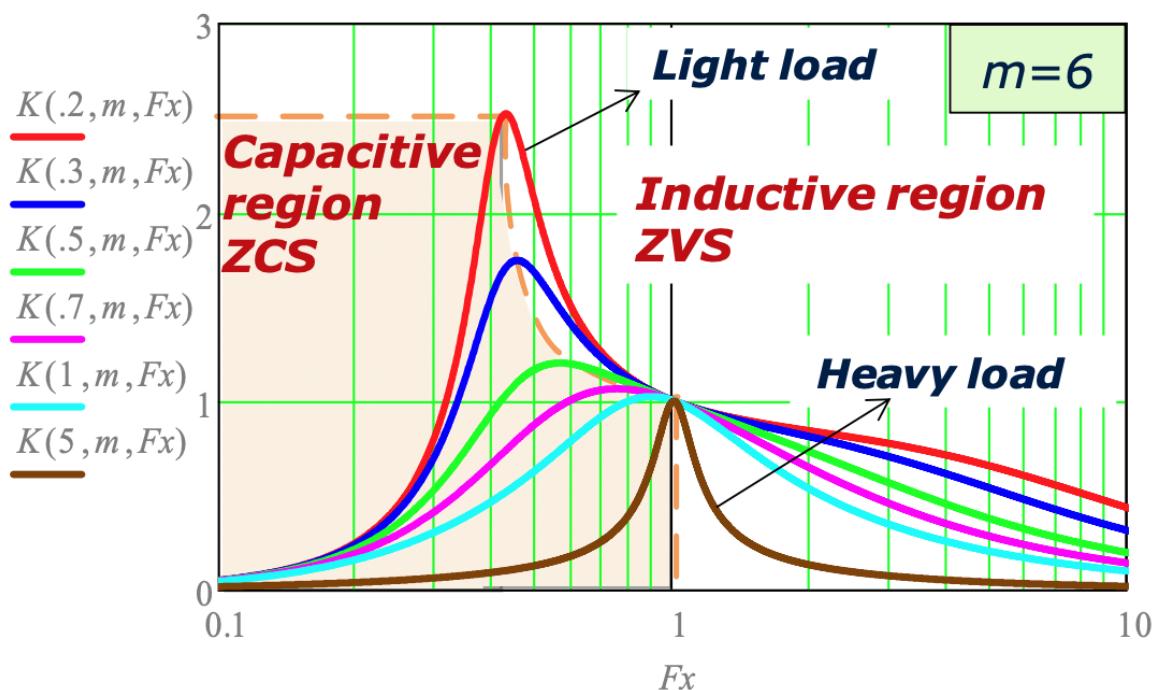


Fig. 22: Gain vs. switching frequency (normalized), [Infineon Design Note](#), page 6, V1.0 March. 2013

Due to the resonant properties of the LLC resonant circuit, the voltage increases when the half bridge is switched in the resonant frequency range. As already mentioned, the switching frequency should preferably be slightly higher than the load-dependent resonant frequency (to the right of the orange dashed line) in order to avoid hard switching. The voltage boost in relation to the input voltage is referred to as "gain". The maximum required gain depends on the input voltage range, whereby the minimum gain is usually close to 1 in order to avoid switching losses due to high switching frequencies and hard switching.

$$Gain_{max} = \frac{U_{max}}{U_{min}} \cdot Gain_{min}$$

For this converter with an input voltage range of 200 V to 600 V, a maximum gain of 3 with a minimum gain of 1 would therefore be necessary. With an input voltage of 200 V, the switching frequency is reduced to such an extent that three times the voltage boost occurs in the resonant circuit (i.e. 600 V is actually present in the resonant circuit). The voltage boost also results in a higher current in the resonant circuit, which increases the losses in the resonant circuit.

However, the minimum gain for the DCDCv9-3 is 1.12. This is because a winding ratio for a gain of 1.0 would have led to a higher flux density.

The voltage applied to the transformer depends not only on the gain in the resonant circuit, but also on the topology. The bridge gain of a full bridge is 1, whereas it is only 0.5 for a half bridge. The output voltage is calculated as follows:

$$U_{out} = U_{in} \cdot G_{bridge} \cdot G_{res-circuit} \cdot \frac{N_{sec}}{N_{prim}}$$

$$U_{out} = 600V \cdot 0.5 \cdot 1.12 \cdot \frac{2}{28} = 24V$$

6.3.11 Regelkreis

The control circuit consists of a TL431, which works as a comparator with an internal 2.5 V reference voltage. If the voltage at the REF pin exceeds the reference voltage, a current flows between the cathode and anode so that the current at the optocoupler increases. The optocoupler provides the galvanically isolated feedback between the LV and the UCC25600 (HV). If the current from Opc+ to ground increases on the isolated side, the UCC25600 increases the switching frequency and thus reduces the output voltage (see resonant circuit). Unlike an ideal comparator, however, the current does not increase steeply, but has a dynamic impedance of typ. 0.2 Ω, which is important for continuous analog control.

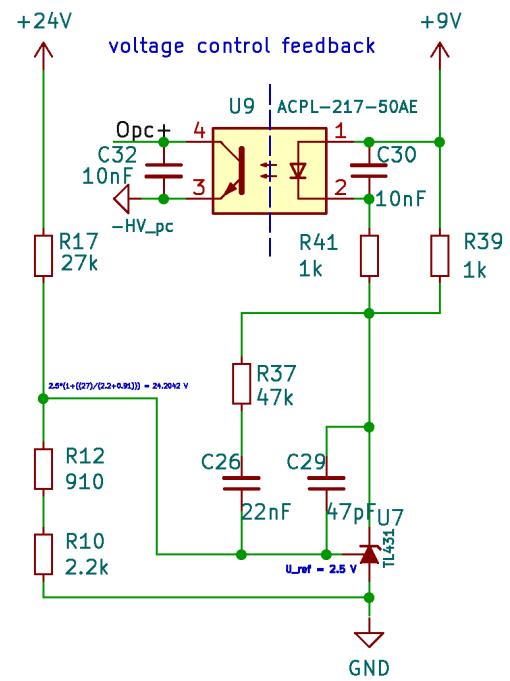


Fig. 23: Circuit diagram control loop

A voltage divider on the REF pin allows the TL431 to be used as an adjustable Zener diode. For the DCDC v9-3, the voltage divider was designed for 24 V, whereby an output voltage of 24.2 V is achieved by using E24 resistors.

Earlier versions used a 10-turn trimming potentiometer for voltage adjustment. By adapting the test procedure, however, changing the voltage became unnecessary. An unexplained phenomenon in this context was that despite careful turning of the potentiometer, some

output voltages could not be set precisely, e.g. 24.0 V did not work, but 23.9 V and 24.1 V did. The potentiometer used was of the same type as RV2 and was used from v7 to v9-2. Possibly because the control circuit is a P-controller and not a PI-controller?

Other components of the control loop are C26 and R37, which damp the control loop and significantly adjust the control speed and overshoot. C29 is used to dampen high-frequency voltage components. Calculations and LTSpice simulations revealed that the behavior matched the observed practice only slightly. Oscillations of the control loop were observed below 1/2 to 1/20 of Fsw (therefore also referred to as “sub-oscillation” in tests), which should hardly be possible with damping.

$$f_{limLF} = \frac{1}{2\pi \cdot R_{37} \cdot C_{26}} = \frac{1}{2\pi \cdot 47k\Omega \cdot 22nF} \approx 154Hz$$

$$f_{limHF} = \frac{1}{2\pi \cdot R_{37} \cdot C_{29}} = \frac{1}{2\pi \cdot 47k\Omega \cdot 47pF} \approx 72kHz$$



Fig. 24: Oscillations on the converter, yellow: voltage across Cres, cyan: primary current

Changes to C26, C29 or R37 had hardly any influence on the observed behavior. It was assumed that EMI had an effect on the control circuit. On closer investigation of the v9-2, ceramic capacitors were placed at various points as a last resort.

This resulted in capacitors C32 and C30 in the v9-3, which effectively prevented the sub-oscillations. They also have a low-pass effect (C30 → 16 kHz, C32 → 31 kHz), which is why at the current state of knowledge it cannot be completely ruled out that the EMI effect is not already taking place at T431. Further disturbances in the control loop were detected with incorrect triggering of the active rectification in the partial load range (Pout = 15 to 50 W). Better values for the low-pass filter on the CS pin completely eliminated this interference.

Load jumps were then applied to the output of the converter in order to examine its control behavior in more detail. Due to a lack of suitable equipment, the steepness of the load jumps achieved is only relatively low, meaning that there is a lack of significance.

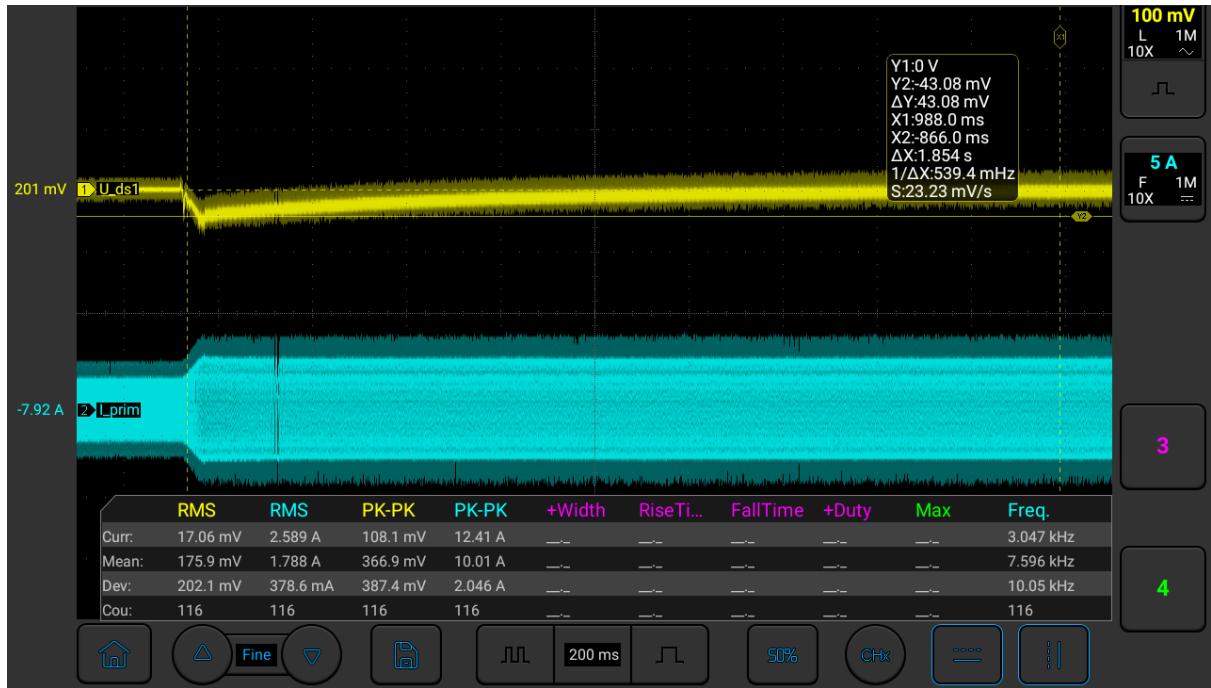


Fig. 25: Yellow: output voltage (AC coupling), cyan: current of the primary winding

Due to the necessary AC coupling at the output voltage of 24 V, it is also not clear whether the slow increase in the output voltage is caused by a sluggish regulation or by the AC coupling. It is therefore difficult to check the control parameters effectively for the time being. Nevertheless, it should be investigated whether very large load jumps, such as those that occur when large capacitors are connected in the LV system, lead to overshoot. This behavior was achieved using external capacitors with 4700 μ F and the LVMS switches ([HELLA](#)) commonly used in Formula Student.

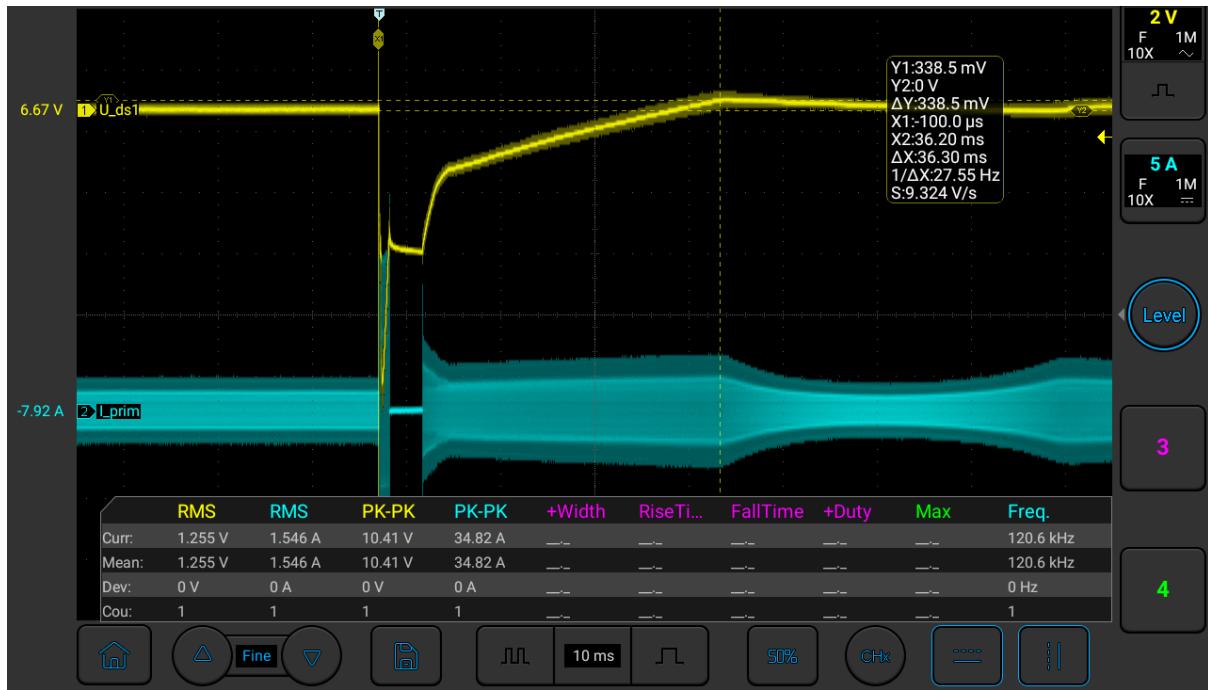


Fig. 26: Load step with 4700 μ F (uncharged) on the output, yellow: output voltage (AC coupling), cyan: current of the primary winding, large time range (10ms/div), Vin = 600 V



Fig. 27: Load step with 4700 μ F (uncharged) on the output, yellow: output voltage (AC coupling), cyan: current of the primary winding, small time range (1ms/div), same measurement, Vin = 600 V

On closer inspection, it can be seen that the control loop reaches a peak after just 1 ms of the load jump. Another peak occurs at the first vertical cursor with the subsequent switching off of the half-bridge as a result of overcurrent detection. After falling below the

OC threshold voltage at the overcurrent pin of the UCC25600, it switches on again with a soft start. The overshoot with $V_{in} = 600$ V was 0.34 V_p, whereby the control circuit did not regulate the load step but the soft start. This behavior is considered permissible for the intended use.

At this point, there would also be a need for a project that only deals with the design and testing of the control loop.

6.3.12 Transformer

6.3.12.1 Transformers crash course

A simple transformer consists of two coils (windings) and a material between the coils. This medium can be air (e.g. inductive charging in cell phones) or a material that has magnetic conductivity (permeability). The relative permeability μ_r of air is almost one. Ferrite cores can have a μ_r between 15 and 20000, depending on their composition. Transformer sheets achieve a μ_r of around 4000 [\[Source\]](#). It is important to know that the different materials have different conductivity and also different saturation. Saturation means that the magnetic field per cross-sectional area (flux density, B_{max}) in a material is so large that it can no longer absorb any further field (all elementary magnets in the material are aligned in one direction) and is usually undesirable. Air can be saturated to any degree. For ferrites, a B_{max} of 0.2 ... 0.3 Tesla usually applies. For transformer sheets, the B_{max} is around 1.2 ... 1.8 Tesla. At first glance, you might think that transformer sheets are better. However, the elementary magnets in the sheet can only be remagnetized slowly (leads to excessive heat build-up at higher frequencies), so such transformers can only be used up to a few kHz. Ferrites for power applications, on the other hand, can be used up to the lower MHz range.

The following section is contradictory and should be improved. The author cannot save himself from confusion. Please help him.

There are several approaches to calculating the flux density in the core, which lead to different results.

Approach 1) Converting the equation for the [induced voltage](#) of a coil:

$$U_{ind}(t) = -N \cdot \frac{d\Phi}{dt}$$

$$\Phi(t) = B(t) \cdot A$$

$$\Phi(t) = \hat{B}(t) \cdot A \cdot \sin(2\pi ft)$$

$$\frac{d\Phi(t)}{dt} = \hat{B} \cdot A \cdot \frac{d}{dt} \sin(2\pi ft)$$

$$\frac{d}{dt} \sin(2\pi ft) = 2\pi f \cos(2\pi ft)$$

$$\frac{d\Phi}{dt} = A \cdot \hat{B} \cdot 2\pi \cdot f \cdot \cos(2\pi ft)$$

$$U_{ind}(t) = -N \cdot A \cdot \hat{B} \cdot 2\pi \cdot f \cdot \cos(2\pi ft)$$

$$\hat{U}_{ind} = -N \cdot A \cdot \hat{B} \cdot 2\pi \cdot f$$

$$\hat{B} = \frac{\hat{U}_{ind}}{N \cdot A \cdot 2\pi \cdot f}$$

$$\hat{B} = \frac{U_{ind} \cdot \sqrt{2}}{N \cdot 2\pi \cdot f \cdot A}$$

Approach 2) Derivation via the inductance of the coil

$$L = \frac{N \cdot \Phi}{I} \quad \Phi = \vec{B} \cdot \vec{A}$$

$$L = \frac{N \cdot \vec{B} \cdot \vec{A}}{I}$$

$$\vec{B} = \frac{I \cdot L}{N \cdot \vec{A}}$$

$$\hat{B} = \frac{I \cdot L \cdot \sqrt{2}}{N \cdot A}$$

Approach 3) Derivation via the magnetic circuit

$$H = \frac{N \cdot I}{l} \quad B = \mu \cdot H$$

$$\rightarrow B = \mu \cdot \frac{N \cdot I}{l}$$

$$B = \frac{\mu_0 \cdot \mu_r \cdot N \cdot I}{l}$$

$$\hat{B} = \frac{\mu_0 \cdot \mu_r \cdot N \cdot I \cdot \sqrt{2}}{l}$$

It is expected that all equations will produce approximately the same result. Simulated measured values are provided as an example. Due to the fact that the voltages and currents are not always ideally sinusoidal, peak values (nonsinepeakvalue) from the simulation were used in addition to the RMS values for the calculations. It should be shown that the maximum flux density differs for both values and therefore leads to different peak flux densities.

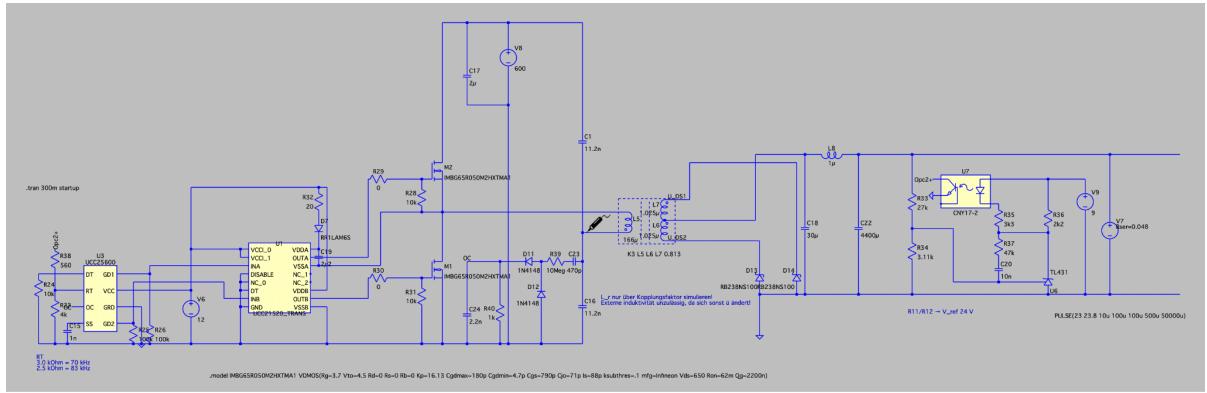


Fig. 28: Configuration of the simulation

$$U_{trafo} = 426.3V / 513V p(simulation/nonsine)$$

$$N = 28$$

$$f = 159.4kHz$$

$$A = 125mm^2$$

$$I = 3.476A / 5.1Ap(simulation/nonsine)$$

$$L = 166\mu H$$

$$\mu_r = 122.9$$

$$l = 91.2mm$$

1)

$$\begin{aligned}\hat{B} &= \frac{U_{ind} \cdot \sqrt{2}}{N \cdot 2\pi \cdot f \cdot A} \\ &= 0.172T \\ &= 0.146T(nonsinepeakvalue)\end{aligned}$$

2)

$$\begin{aligned}\hat{B} &= \frac{I \cdot L \cdot \sqrt{2}}{N \cdot A} \\ &= 0.233T \\ &= 0.242T(nonsinepeakvalue)\end{aligned}$$

3)

$$\begin{aligned}\hat{B} &= \frac{\mu_0 \cdot \mu_r \cdot N \cdot I \cdot \sqrt{2}}{l} \\ &= 0.233T \\ &= 0.242T(nonsinepeakvalue)\end{aligned}$$

Approach 1) results in the smallest flux density and has no variables that describe the magnetic circuit in more detail. Approaches 2) and 3) produce almost identical results (deviation in the fifth decimal place, probably rounding errors in the source data) and use information about the magnetic circuit. When looking at the calculated peak values, which do not follow the sine curve, it is noticeable that the flux density decreases with 1), as the voltage approximately follows a rectangular curve, which is why the approximation with $\sqrt{2}$

leads to a larger value. For approaches 2) and 3), the approximation with $\sqrt{2}$ seems quite useful for this specific example.

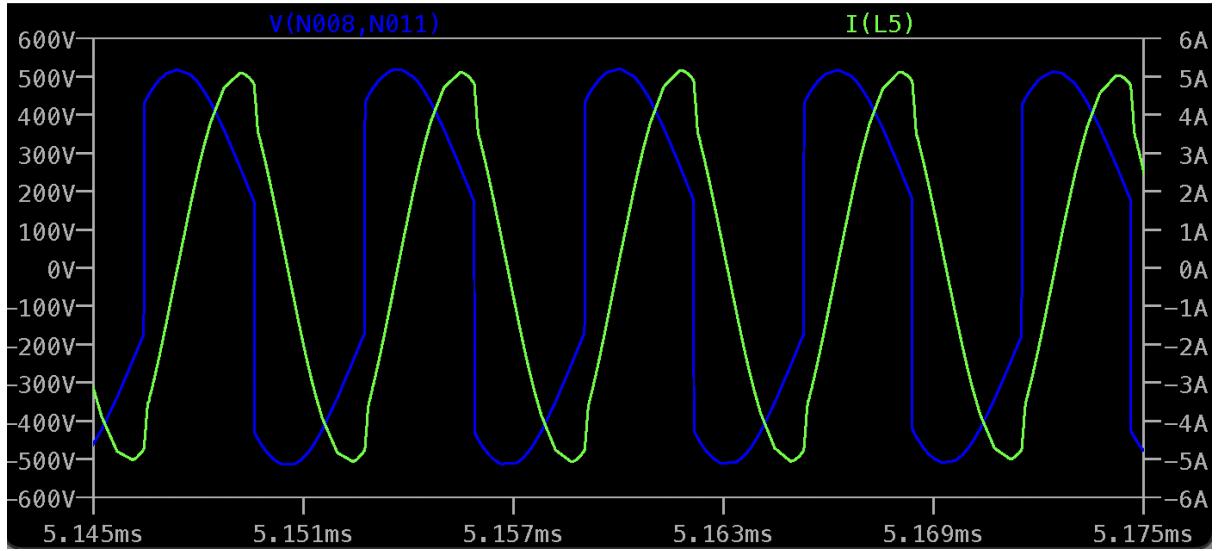


Fig. 29: Green: voltage across the transformer, blue: current through the transformer

The flux density from the Onsemi [calc-Sheet](#) is used as a further reference. Here, the maximum flux density is 0.139 T with a similar current. However, the flux density does not change when the current is changed, which contradicts equations 2) and 3). It therefore remains unclear for the time being which equation can be used.

(Comments in the [discussion area](#) are welcome!)

One aim of transformer design is to remain below the maximum flux density B_{max} of the core material in order to keep the core losses (heat dissipation) low. Some data sheets contain a diagram showing the power loss as a function of flux density and frequency:

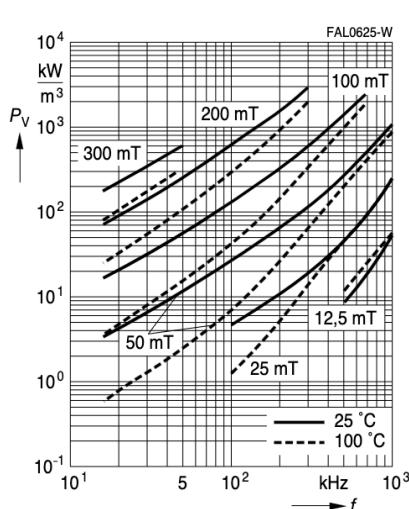


Fig. 30: Relative core losses, frequency-dependent, data sheet for the material [N97](#) from TDK page 5

The somewhat cumbersome unit kW/m³ can also be replaced by mW/cm³ without a conversion factor, which is easier to imagine in the application.

The diagram shows that a flux density of 300 mT at 5 kHz leads to losses of 600 mW/cm³ (at 25°C). The same power loss at 200 mT is achieved at 100 kHz.

What is interesting now is the theoretically possible power of a transformer, which can be calculated as follows (neglecting any losses):

$$S = \sqrt{2} \cdot \pi \cdot f \cdot B \cdot J \cdot A \cdot A_{Cu}$$

Elektrische Maschinen, Rolf Fischer, p. 119, ISBN 978-3-446-45218-3

Whereby A = Cross section of the core
and A_{Cu} = Cross-section of all turns of a winding

The relationships in the equation now show that the power at 200 mT is 13.3 times greater at 100 kHz than at 5 kHz and 300 mT. For 100 mT and 300 kHz the power increases by a factor of 20, and for 50 mT and 750 kHz by a factor of 25. All this with constant core losses.

Great, so go higher and higher with the frequency, perhaps make the core a little smaller and still get more power? - No, unfortunately not.

There are numerous loss factors (more on this later), which scale not only linearly with the frequency, but exponentially. Here you can take the saying of a colleague to heart: "Not as fast as possible, but only as fast as necessary" (in relation to the switching frequency).

Let us now look at the number of turns and the inductance as well as the permeability of a coil.

$$L = A_L \cdot N^2 \quad A_L [nH]$$

is an inductance constant which can be obtained from the data sheet of the core and is used for simplified calculation of the inductance.

Doubling the number of windings quadruples the inductance of a coil.
However, a transformer consists of two coils that are coupled together by a magnetic core (this is referred to as a magnetic circuit). The coupling k indicates the ratio of magnetization inductance and leakage inductance. In other words, how many magnetic field lines pass from one coil to the other and how many of them pass by the other coil.

$$k = \sqrt{1 - \frac{L_{leak}}{L_{prim}}}$$

The term hard/rigid coupling is used when the coupling is very high (ideally 1). The opposite is a soft or loose coupling (< 1).

Okay, cool. And what do I need this for?

- *The coupling factor is not used for the design itself, but is used in the transformer model in LTSpice. It is important to at least know that an LLC transformer has a relatively low coupling factor.*

The magnetizing inductance depends on the number of turns and the air gap. The leakage inductance, in contrast, depends on the geometric distance and arrangement of the coils as well as the number of turns. As a rule, the minimum number of turns is determined by the maximum flux density and the maximum number of turns by the desired magnetization inductance.

By grinding the middle leg of the transformer, any air gap can be set, and thus also the magnetization inductance.

6.3.12.2 Core shape

The ETD (double E-core) form factor was selected for the ferrite core transformer, as windings with a large cross-section can be easily applied. Other form factors such as PQ offer a large magnetic cross-section, but the space and distance between the windings is very limited, which is of great importance for the leakage inductance.

The ETD series is supplemented by a number that indicates the width of a core pair in millimeters. Typical values are 29, 34, 39, 44 etc.. ETD 39 and 44 are particularly relevant for the DCDC. This form factor is manufactured in many variants by TDK (formerly EPCOS), among others.

Depending on the application, the materials N27, N87 and N97 are available, whereby the data sheets indicate that the material N97 has the lowest power dissipation in the intended frequency range between 80 and 350 kHz. A special design from the company with a "distributed air gap" specializes in reducing stray losses at the air gap. In this case, a material with lower permeability is used in the middle leg in discs, which distributes the stray field of the air gap over several small gaps. A study on [air gap losses](#) comes to the conclusion that the air gap losses are approximately indirectly proportional to the number, therefore doubling the air gaps leads to halving the air gap losses.

However, the core type with a distributed air gap could not be tested as it is not available in the ETD form factor (Note: There are now available variants, see [improvements](#)). However, a low-cost variant is to take an ordinary ETD core without an air gap and increase the distance between the two core halves. This not only creates two air gaps in the magnetic circuit, but also eliminates the need to grind the core to the appropriate air gap length. This principle was fundamentally tested, but there were no meaningful comparative measurements. There is a much greater risk that the air gap on the outer legs will cause stray fields to affect nearby current paths and components and that magnetic field lines will take an unwanted shortcut from the outer legs to the inner leg. A direct comparison between different core shapes, core materials and air gap designs could be a future project. For the DCDCv9-3, an already machined core with a 1.0 mm air gap was purchased for testing. However, this is only available from the distributor with the core material N27, which is recommended for a frequency range of 25 kHz to 150 kHz. It was expected that a combination of an N27 core (with air gap) and an N97 core (without air gap) would result in the N27 core exhibiting greater heating due to higher losses in the upper frequency range.

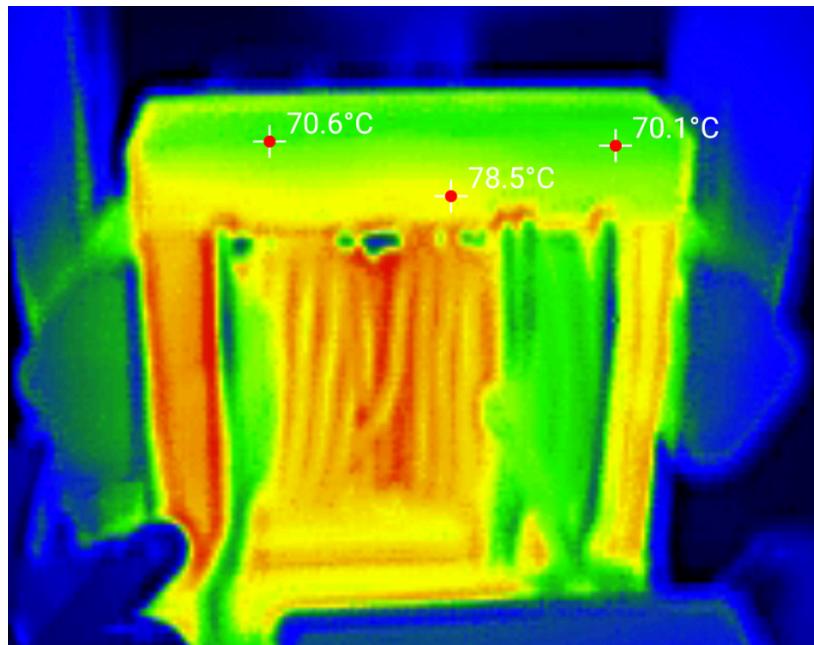


Fig. 31: Thermal image of the transformer with N27 and N97 core halves

Observations with a thermal imaging camera show, however, that the core halves become almost equally hot. Rather, the local effect of the magnetic field of the primary coil on the core material can be observed (measuring point 78.5°C). A direct comparison with only N97 core halves was not undertaken due to time constraints. However, it cannot be ruled out that two N97 cores, each with a 0.5 mm air gap, lead to lower losses. As further performance tests with the unusual N27 + N97 combination were successful, it was retained for the release. This saves the time-consuming manual grinding of the cores.

6.3.12.3 Winding design

To understand how the design of the transformer used in version 9 was developed, it is first explained how the original design was constructed and why this was not suitable.

The original design was based on a recommendation in which the secondary winding is wound on the inner primary winding. Windings are avoided in the middle (where the air gap is) in order to reduce the heating of the windings due to the stray field of the air gap. However, a modular design is difficult to realize due to the necessary gluing and isolation.

From an electrical point of view, this design works well for classic push-pull converters, but not for LLC converters, as the coupling of the windings is very high (= low leakage inductance). Experimentally, couplings of $\geq 99\%$ have been achieved in some cases. The leakage inductance serves as energy storage in the LLC resonant circuit and is also referred to in the following as resonant inductance (L_r). It is essential for the operation of this topology and has a major influence on the properties of the resonant circuit. Transformers without L_r (high coupling) are therefore not suitable and require an external resonant inductance connected in series. Up to DCDC version 8, an external resonant inductor was used, which not only required more space but also reduced efficiency.

In new winding designs, the distance between the primary and secondary windings was increased so that the coupling became smaller and L_r was available in a usable size. Although the integrated resonance inductor has proven itself in the newer designs, it is not certain whether an external resonance inductor could lead to an overall higher efficiency

when using a single-layer primary winding or even a bifilar winding (low proximity losses). Particularly at high power, the external resonance inductance would provide more space in the winding window for larger conductor cross-sections, which could reduce power losses.

6.3.12.4 Design eines LLC-Transformators

A [Calc-Sheet](#) from Onsemi for the NCP4390 LLC controller is used to calculate the transformer parameters. The controller has no relevance here, but the visualization of the gain curves is very well done (of course, the NCP4390 can also be used instead of the UCC25600, but it makes no difference for the magnetic circuit).

In the sheet, we specify the desired parameters (input and output voltage, power, etc.) up to point 6 “Design the transformer”. Particularly relevant are the input power, min. and max. input voltage, Cr, Lr and Lp for “Actual resonant network design”.

It is necessary to clarify in advance what core size should be used. The following are our own empirical values:

Core size	Continuous power (passive)	Continuous power (with fan)	Core cross-section
ETD39	300 W	500 W	125 mm ²
ETD44	500 W	750 W	172 mm ²

ETD39 is recommended for the DCDCv9 versions, even if there is theoretically enough space for the ETD44 transformer from v9-2 onwards (Y-cap soldered on the underside), which offers approx. 1% better efficiency (compared to ETD39) and more continuous power without a fan.

The procedure for designing a transformer with the Calc-Sheet is roughly as follows:

- Specify the power and voltage ranges
- Select “m = 5” (this value is only for the first iteration)
- Min. gain for max input voltage = Gain at the resonant frequency (line 21)
- Specify the diode flux voltage (e.g. 0.05 V as active rectification with FETs)
- Specify the desired resonant frequency (e.g. 120 kHz)
- Read the Q-factor from the diagram at the intersection axis with the graph of the previously specified m-value
- Transfer the “Designed Cr, Lr, Lp” values to the cells on the right for Actual resonant network Design.
- Specify the magnetic core cross-sectional area (for ETD39 it is 125 mm²) and the maximum flux density (we take 0.2 T for less losses, even if the core with the N97 material is capable of 0.41 T)
- Select the “Secondary side turns” so that “Primary side turns” is slightly larger than “Minimum primary side turns”.
- Read off the selected “Secondary side turns”, “Primary side turns” as well as Cr, Lr and Lp
→ These values can now be used for transformer construction.

6.3.12.5 Achieving the desired transformer parameters

Air gap

Compared to the core material (ferrite N97) with a conductance (μ_r) of 1650, air only has a conductance of 1. For the magnetic field, 1650 mm core length therefore has the same magnetic resistance as 1 mm air.

Why should the magnetic resistance be increased by using an air gap?

A current-carrying coil generates a magnetic field with a magnetic field strength of H (also called H-field). The magnetic field strength flows through a medium (e.g. ferrite or air), which is referred to as the magnetic flux density or B-field. The H-field is, so to speak, the external influence and the B-field the internal stress. The flux depends on the material and is related as follows:

$$H = \frac{B}{\mu} \quad \text{bzw.} \quad B = H \cdot \mu \quad \text{wobei} \quad \mu = \mu_r \cdot \mu_0 \quad \text{mit} \quad \mu_0 = 4\pi \cdot 10^{-7} \frac{N}{A^2}$$

Erzeugt man ein H-Feld mit einer Spule, ist ersichtlich, dass ein größeres μ auch ein größeres B-Feld im Material hervorruft. Ferrite haben eine maximale Flussdichte B_{sat} von z.B. 0,3 Tesla [$\frac{V \cdot s}{m^2}$]. Wird eine größere Feldstärke angelegt, führt dies zu keiner weiteren Steigerung der Flussdichte, was man auch als Sättigung bezeichnet. Um Leistungsverluste zu vermeiden, sollte eine Auslegung immer unterhalb der Sättigungsgrenze erfolgen.

Schauen wir uns ein Beispiel an einem Ferritkern ohne Luftspalt mit einer Zylinderspule an:

If an H-field is generated with a coil, it can be seen that a larger μ also produces a larger B-field in the material. Ferrites have a maximum flux density B_{max} of e.g. 0.3 Tesla [$\frac{V \cdot s}{m^2}$]. If a higher field strength is applied, this does not lead to any further increase in flux density, which is also known as saturation. To avoid power losses, the design should always be below the saturation limit.

Let's take a look at an example of a ferrite core without an air gap with a cylindrical coil:

$$H = \frac{I \cdot N}{\sqrt{l^2 + D^2}}$$

I	...	Coil current [A]
N	...	Number of windings
l	...	Length of the coil [m]
D	...	Diameter of the coil [m]

For an example we choose

$$\begin{aligned} I &= 1A \\ N &= 20 \\ l &= 0.02m \\ D &= 0.015m \end{aligned}$$

and receive

$$H = 800 \frac{A}{m}$$

By converting according to the flux density, we obtain for ferrite with $\mu_r = 1650$

$$B = H \cdot \mu_r \cdot \mu_0$$

$$B = 800 \cdot 1650 \cdot 4\pi \cdot 10^{-7} \frac{N}{A^2} = 1,659 T$$

We can see that this flux density is far above the permissible flux density of 0,3 T.

Now we repeat the calculation on a ferrite core with a 1 mm air gap.

$$H = 800 \frac{A}{m} \text{ (remains the same)}$$

From the data sheet we take a μ_r of 115 for 1 mm air gap

$$B = H \cdot \mu_r \cdot \mu_0$$

$$B = 800 \cdot 115 \cdot 4\pi \cdot 10^{-7} \frac{N}{A^2} = 0,116 T$$

We can see that the flux density is now below the permissible flux density of 0.3 T.

An air gap therefore reduces the magnetic conductivity and thus allows higher field strengths before the core material saturates. In practical terms, the primary inductance can be adjusted as required.

6.3.12.6 Primary inductance (L_p)

The air gap for the desired primary inductance can be roughly determined below using the factors given in the data sheet:

Material	Relationship between air gap – A_L value		Calculation of saturation current			
	K1 (25 °C)	K2 (25 °C)	K3 (25 °C)	K4 (25 °C)	K3 (100 °C)	K4 (100 °C)
N27	196	-0.734	308	-0.847	287	-0.865
N87	196	-0.734	300	-0.796	280	-0.873

Validity range: K1, K2: 0.10 mm < s < 3.00 mm
K3, K4: 90 nH < A_L < 850 nH

Fig. 32: [Data sheet](#) for TDK ETD39 core

Unfortunately, no factors are given for the material N97. However, as N87 and N97 have a certain similarity, the parameters of N87 are used.

For the calculation, the formula from "[E cores: general information](#)" is used for the air gap to set L_p .

$$s = \left(\frac{A_L}{K_1}\right)^{\frac{1}{K^2}} \quad A_L = [nH], s = [mm]$$

$$A_L = \frac{L_p}{N^2}$$

Substituting A_L

$$\rightarrow s = \left(\frac{\frac{L_p}{N^2}}{196}\right)^{\frac{1}{-0,734}} \quad L_p = [nH]$$

By inserting the number of primary windings determined with Onsemi's [Calc-Sheet](#) and the Lp you get

$$s = \left(\frac{\frac{166000 \text{ nH}}{28^2}}{196}\right)^{\frac{1}{-0,734}} = 0,90 \text{ mm}$$

The actual air gap for the desired Lp was 1.0 mm. However, experience has shown that the required air gap is always slightly larger than calculated. This could be due to the properties of the coil.

The calculated air gap can, however, be used as a rough guide. It is recommended that the coil is first wound onto a coil holder and, after grinding a little, Lp is measured with an LCR meter. This process should be repeated until the desired Lp has been reached. Important: Lp also depends on the position of the coil on the core. If the primary coil is later used on the right-hand half of the core, for example, it should also be measured there. Ideally, the two secondary windings are already mounted on a coil holder during the measurement.

6.3.12.7 Leakage inductance (Lr)

The leakage inductance describes the proportion of the magnetic field between two coils that does not flow through the other coil. The leakage inductance is therefore independent of the core material or air gap and depends solely on the position of the coils in relation to each other as well as the number of windings and geometry. Calculating the leakage inductance using simple distance formulas is only roughly possible. Exact values can be determined by complex FEM simulation or experimentally. In this project, a leakage inductance of a suitable size was achieved by testing various arrangements and geometries.

In principle, the leakage inductance increases quadratically with the number of windings and a greater distance between the windings increases the leakage inductance.

6.3.12.8 Coil formers

The coil formers for ETD39 or ETD44 are manufactured using an SLA printer. The resin must be heat-resistant, as temperatures of up to 120°C can occur inside the winding. As the models for SLA printing are generally made of duroplastics, melting due to high temperatures is not to be expected. However, cracks can occur in unsuitable materials due to brittleness and render the isolation ineffective. Otherwise, the models are very tight and

do not have any holes if manufactured correctly. This is extremely important as the holders are used as primary isolation (observe rule EV 4.5.3). Even if models appear to be in perfect condition, an isolation test with high voltage is **always** necessary to confirm the isolation strength. There is another chapter on [isolation testing](#) later on.

Notes on SLA printing

- Visually check that all pixels are functional during LCD or DLP SLA printing
- The models should be aligned so that the center cylinder (around which the coil is wound) has no external support structure in order to obtain a smooth surface and not to damage the isolation of the conductors.
- Holders must under no circumstances have holes, cracks, contamination or delamination.
- Models can break with sharp edges under mechanical stress, so care must be taken when handling them. Even small drops can lead to breakage.
- The necessary safety regulations for handling SLA printers and the UV resin must be observed as well as the proper disposal of consumables and material residues.

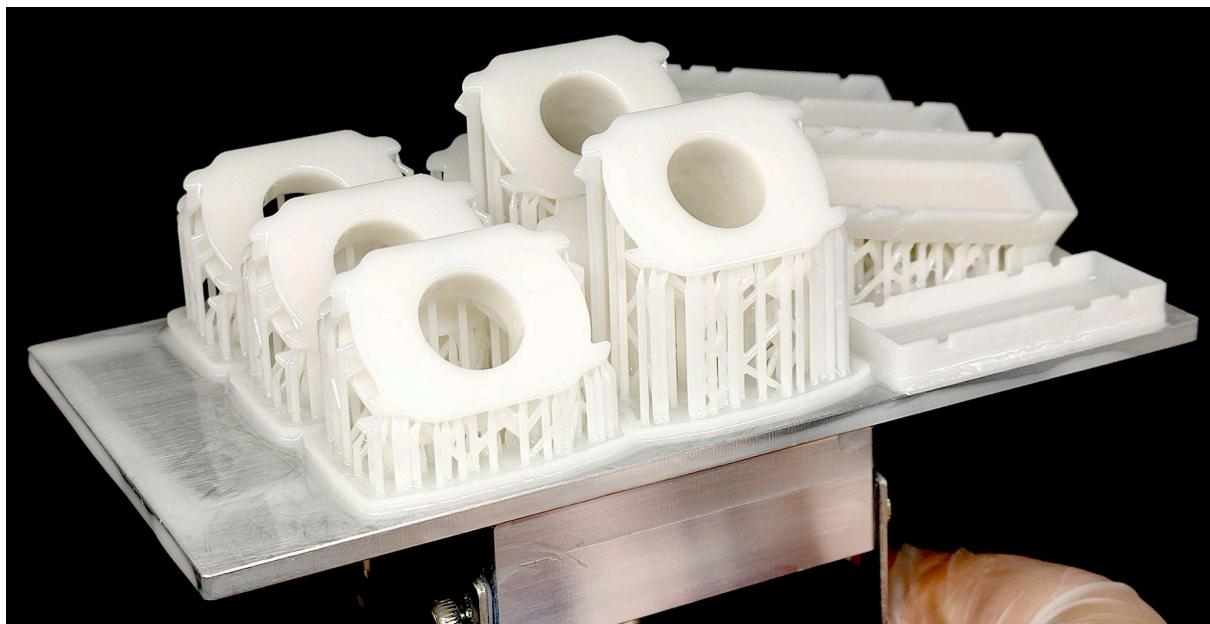


Fig. 33: SLA print of the ETD39 coil formers with support structure

6.3.12.9 Choice of coil wire

An enameled copper wire can be used for initial tests and low power/efficiency levels. Due to the many loss factors (especially skin and proximity effect), a high-frequency stranded wire (HF litz wire) is recommended. However, this can hardly be obtained from well-known distributors. To date, no official data sheet for an HF litz wire has ever been seen.

Two distributors from which orders have been placed so far:

- <https://www.spulen.com/> (no recommendation)
Although the delivery time is stated as 3-5 days, experience has shown that it can be 4 weeks or more. Many HF litz wires are currently not available and there is no response to e-mails. "GEHAIM" (*secret*) is stated as the manufacturer. Ah yes...
- [Sabenne Modellbau \(ebay\)](#) (highly recommended!)

Super-fast shipping by letter post (often 1-2 days), reasonable prices and a large selection. Products in the store can be purchased by the meter or on rolls, with different cross-sections offered on rolls.

Only cross-sections from the Sabenne Modellbau range are used below.

For the **ETD39** transformer is required:

- 1800 mm 120 x 0.1 mm HF litz wire for 28 windings (primary)
- 165 mm 600 x 0.071 mm for 2 windings (secondary winding 1 inside)
- 185 mm 600 x 0.071 mm for 2 windings (secondary winding 2 outside)
- SLA-printed coil holders (primary, secondary, isolator)
- Ferrite core halves (size ETD39):
 - 1x N27 with 1.0 mm air gap Prod. no.: B66363G1000X127
 - 1x N97 without air gap Prod. no.: B66363G0000X197



Fig. 34: Core halves with air gap, coil holder and isolator (bottom)

6.3.12.10 How to wind

The winding direction (clockwise or counterclockwise) of the primary coil does not matter as long as it always remains the same on the coil. The coil former of the primary coil has a separator in the middle to stabilize the three layers and to gain additional isolation distance. The arrangement shown was chosen to achieve a compromise between winding capacity, isolation voltage between the windings and complexity of the winding. It is a mixture of U-winding and sectional winding.

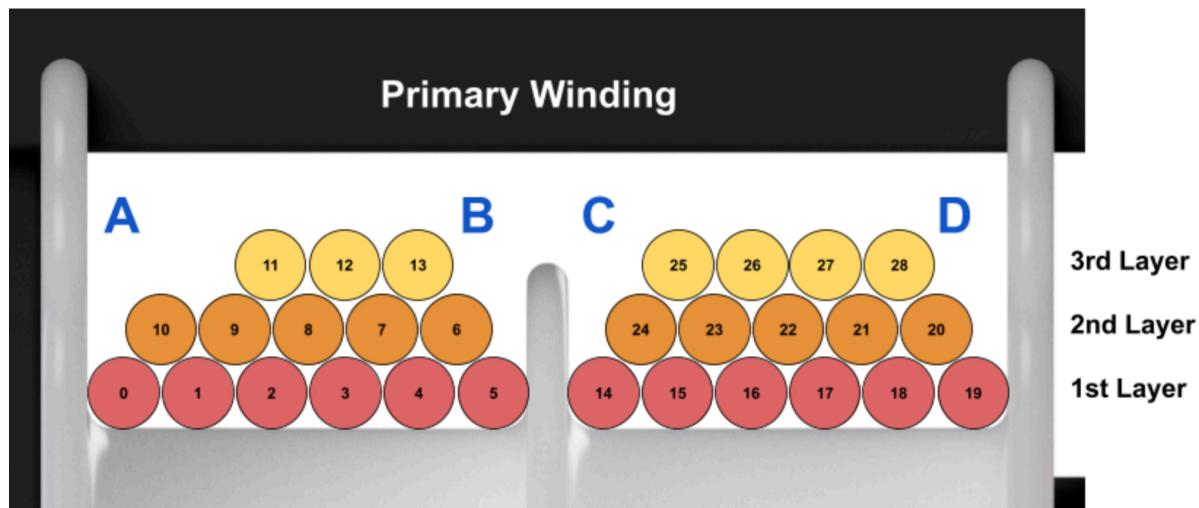


Fig. 35: Winding structure primary winding

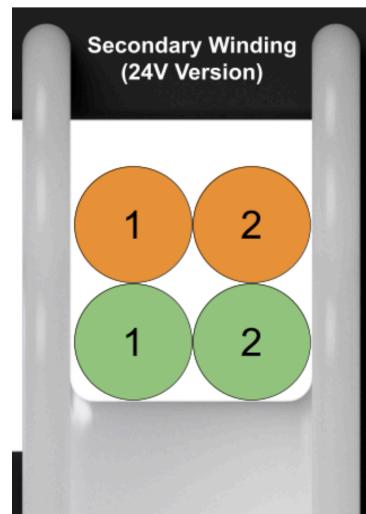


Fig. 36: Winding structure secondary winding

An almost optimal solution would be the so-called “bank winding”, which leads to a very low winding capacity. However, this winding technique is very complex and difficult to wind by hand without the use of a relatively large amount of adhesive. More about different winding schemes [here](#).



Fig. 37: Comparison of the frequency-dependent resistance of the bank winding (violet) vs. U-winding (blue) with 30 turns each on ETD39 holder (without core). The resonant frequency of the U-winding is 11.3 MHz, with an inductance of 11.6 μ H this results in a winding capacitance of 17.1 pF. The resonant frequency of the bank winding is too high for the measuring device. With the help of an additional capacitor (approx. 9 pF (+ 0.5)), a resonant frequency of 15.6 MHz could be determined, which at 10.87 μ H (minus the 9 pF) results in a winding capacitance of 0.55 pF and corresponds to a resonant frequency of 65 MHz. The measurement error may be large, but the result certainly shows the potential of this winding technique. Assuming that the input voltage is applied over the entire capacitance, this results in a 31-fold reduction in capacitive winding losses. However, this winding scheme requires more space (poorer isolation to the ferrite cores).

6.3.12.11 Reduction of transformer losses

The main losses of the windings are made up of the direct current resistance (R_{DC}) of the winding and the frequency-dependent alternating current resistance (R_{AC}), whereby the proximity effect and skin effect have the greatest influence on R_{AC} . The losses can be calculated via the resistance using the well-known formula $P_{loss} = (R_{DC} + R_{AC}) \cdot I^2$.

While the direct current resistance should be familiar from school physics, the frequency-dependent alternating current resistance should not be confused with the impedance! The Real part of the impedance is considered here.

So this actually the normal resistance? This is not frequency-dependent, is it?

In fact, the proximity effect and skin effect cause charge displacement in ordinary conductors and at high frequencies. The skin effect causes the charge carriers to no longer flow through the entire conductor, but only in the outer ring, which reduces the effective cross-section and increases the resistance.

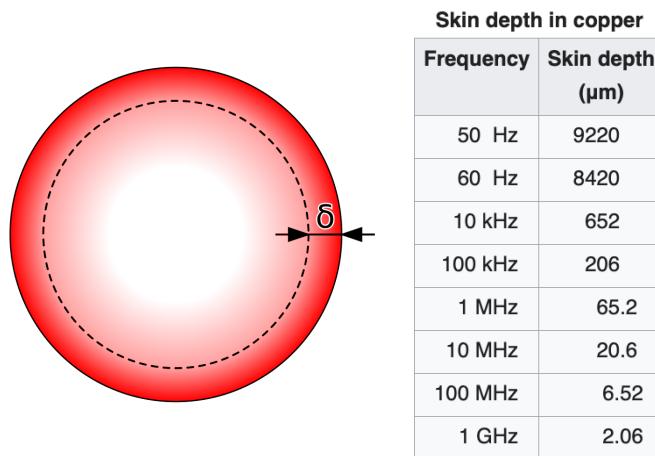


Fig. 38: Frequency-dependent penetration depth, https://en.wikipedia.org/wiki/Skin_effect

To reduce the skin effect, it is possible to use a conductor bundle with many isolated individual conductors (so-called high-frequency litz wire) instead of one conductor. The individual wires are thin enough to be penetrated as much as possible.

In the case of the transformer in this project, for example, a stranded wire with 600 individual conductors and a diameter of 71 μm is used on the secondary side. As can be seen from the table, even at 1 MHz, almost 63 % of the charge carriers would flow through the core area of the conductor.

The proximity effect is similar to the skin effect, except that the charge carriers are displaced by surrounding conductors. This effect scales exponentially with the number of layers of superimposed conductors.

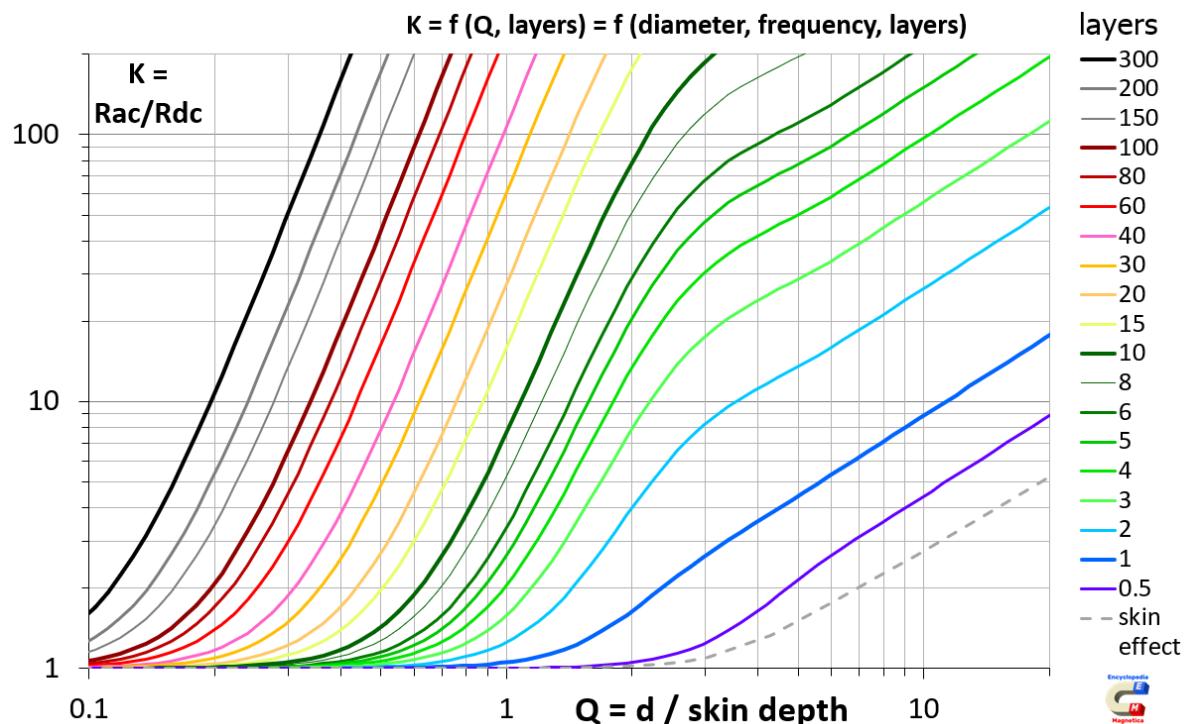


Fig. 39: Dowell's curves for copper at 20°C and a porosity factor of 0.785

S. Zurek, [Encyclopedia Magnetica](#), CC-BY-4.0

In order to reduce the proximity effect, as few conductors of a winding with the same current direction as possible should therefore lie on top of each other. In practice, the winding window of the transformer limits the width of the winding. Therefore, depending on the conductor cross-section and number of windings, it may be necessary to place several conductors on top of each other. At first glance, the transformer in this project has 3 layers on top of each other. On closer inspection, however, each individual conductor of the high-frequency litz wire must be taken into account! Assuming a rectangular conductor distribution, the number of layers can be approximated:

$$N_{Layers} = \sqrt{N_{conductors}}$$

$$N_{Layers} = \sqrt{600} = 24.5$$

There are therefore no longer 3 layers, but a total of approx. 74.

For this problem, the author has created a table based on the script for proximity effects by [Stan Zurek, Proximity effect, Encyclopedia Magnatica, CC Attribution-Share Alike 4.0 International](#). The script is executed in a Google sheet via the Apps Script extension for each cell. The result is the power loss in watts for the specified wire length, number of layers, temperature, current, fill factor, switching frequency and number of conductors.

Layer je Leiter	Layer Total	Durchmesser [mm]	HF-Litz Querschnitt [mm ²]	150 kHz für Kupfer @			20 °C und			2 Layer Wicklungen mit Porosity =			0,785 Drahtläng			150 cm			Strom			4 A _{rms}					
				0,36	0,50	0,56	0,62	0,71	0,80	0,98	1,13	1,26	1,38	1,60	1,78	1,95	2,11	2,26	2,39	2,52	2,76	3,09	3,57	3,99	4,37	5,05	5,64
Durchmesser	Litzen [mm ²]	0,1	0,2	0,25	0,3	0,4	0,5	0,75	1	1,25	1,5	2	2,5	3	3,5	4	4,5	5	6	7,5	10	12,5	15	20	25		
1	2	0,36	17,897	16,417	15,041	13,773	11,759	10,342	8,424	7,092	6,344	5,796	5,026	4,496	4,104	3,799	3,554	3,351	3,179	2,902	2,596	2,248	2,010	1,835	1,589	1,422	
1	3	0,50	14,554	17,973	18,525	18,485	17,498	16,093	13,032	10,998	9,649	8,712	7,485	6,692	6,115	5,667	5,304	5,002	4,746	4,332	3,875	3,355	3,001	2,738	2,372	2,122	
2	4	0,56	5	7,350	8,304	9,169	10,004	11,367	12,259	12,823	12,194	11,237	10,296	8,757	7,861	6,874	6,293	5,845	5,490	5,198	4,743	4,248	3,685	3,292	3,010	2,609	2,331
3	6	0,62	10	5,930	5,779	6,264	6,860	8,132	9,367	11,861	13,382	14,047	14,165	13,621	12,478	11,433	10,506	9,716	9,048	8,489	7,611	6,701	5,751	5,139	4,699	4,076	3,647
4	9	0,71	20	5,111	4,168	4,294	4,556	5,259	6,061	8,140	10,064	11,708	13,043	14,824	15,642	15,800	15,568	15,112	14,552	13,998	12,786	11,287	9,498	8,302	7,480	6,417	5,738
7	14	0,75	50	4,446	2,853	2,660	2,800	2,881	2,895	3,652	4,523	5,416	6,304	7,994	9,525	10,963	12,001	12,927	13,675	14,248	14,961	15,231	14,582	13,470	12,342	10,483	9,195
9	17	0,78	75	4,301	2,563	2,298	2,168	2,106	2,179	2,591	3,132	3,718	4,317	5,523	6,699	7,798	8,830	9,778	10,641	11,405	12,696	14,099	14,852	14,328	12,855	11,452	
10	20	0,80	100	4,241	2,442	2,147	1,985	1,864	1,876	2,140	2,536	2,981	3,450	4,406	5,361	6,296	7,196	8,057	8,873	9,641	11,021	12,694	14,506	15,345	15,523	14,864	13,730
11	22	0,85	120	4,208	2,374	2,060	1,882	1,727	1,705	1,885	2,198	2,562	2,951	3,755	4,572	5,379	6,170	6,937	7,678	8,385	9,706	11,416	13,531	14,823	15,470	15,537	14,809
12	24	0,88	150	4,164	2,287	1,954	1,755	1,558	1,491	1,565	1,772	2,031	2,316	2,922	3,546	4,172	4,794	5,406	6,008	6,589	7,705	9,230	11,333	12,877	13,918	14,840	14,789
14	28	0,92	200	4,132	2,223	1,873	1,658	1,427	1,331	1,324	1,452	1,833	2,291	2,767	3,251	3,738	4,223	4,703	5,178	6,107	7,432	9,412	11,076	12,417	14,209	15,028	
16	32	0,95	250	4,116	2,184	1,830	1,608	1,358	1,244	1,195	1,280	1,419	1,583	1,952	2,345	2,751	3,160	3,570	3,980	4,388	5,193	6,363	8,191	9,823	11,247	13,437	14,835
17	35	0,98	300	4,100	2,159	1,793	1,561	1,298	1,170	1,084	1,132	1,237	1,361	1,657	1,978	2,313	2,652	2,994	3,337	3,680	4,381	5,364	6,963	8,444	9,789	12,031	13,678
20	40	0,99	400	4,080	2,120	1,745	1,503	1,221	1,074	0,936	0,938	0,992	1,072	1,272	1,499	1,738	1,984	2,234	2,487	2,740	3,249	4,006	5,243	6,431	7,555	8,583	11,287
22	45	0,99	500	4,071	2,100	1,719	1,473	1,180	1,023	0,862	0,837	0,865	0,920	1,069	1,245	1,435	1,632	1,832	2,036	2,241	2,654	3,275	4,301	5,302	6,265	8,076	9,699
24	49	0,99	600	4,063	2,086	1,694	1,450	1,150	0,984	0,805	0,760	0,769	0,805	0,916	1,054	1,205	1,365	1,527	1,694	1,862	2,202	2,715	3,568	4,407	5,233	6,806	8,261
27	55	0,99	750	4,055	2,072	1,683	1,428	1,123	0,950	0,753	0,691	0,682	0,701	0,778	0,881	0,998	1,123	1,252	1,384	1,519	1,791	2,205	2,859	3,589	4,263	5,594	8,854
32	63	0,99	1000	4,047	2,056	1,664	1,407	1,092	0,912	0,696	0,615	0,588	0,682	0,627	0,893	0,772	0,859	0,951	1,046	1,143	1,342	1,645	2,158	2,672	3,184	4,194	5,179
35	71	0,99	1250	4,043	2,048	1,654	1,395	0,798	0,892	0,667	0,575	0,538	0,528	0,547	0,593	0,653	0,720	0,792	0,867	0,945	1,103	1,348	1,764	2,184	2,603	3,437	4,258
39	77	0,99	1500	4,043	2,042	1,646	1,385	0,683	0,786	0,643	0,544	0,499	0,480	0,514	0,558	0,609	0,685	0,725	0,786	0,943	1,112	1,450	1,792	2,135	2,821	3,500	
45	89	0,99	2000	4,039	2,036	1,637	1,375	0,649	0,859	0,616	0,509	0,455	0,428	0,414	0,426	0,453	0,487	0,525	0,567	0,611	0,704	0,849	1,101	1,367	1,615	2,132	2,650
55	110	0,99	3000	4,035	2,028	1,629	1,364	0,608	0,842	0,591	0,478	0,412	0,377	0,346	0,341	0,351	0,367	0,389	0,414	0,441	0,499	0,594	0,761	0,932	1,107	1,458	1,812
71	141	0,99	5000	4,031	2,022	1,622	1,356	1,024	0,620	0,569	0,445	0,375	0,332	0,287	0,288	0,262	0,284	0,271	0,281	0,294	0,323	0,373	0,466	0,565	0,666	0,872	1,081

Fig. 40: Visual representation of the power loss for a given number of conductors and cross-sections

The insight gained from the illustration is that a litz wire consisting of 300 individual conductors with a total cross-section of 0.75 mm² has the same power loss as a significantly larger litz wire consisting of 600 individual conductors with a total cross-section of 2.5 mm². This allows more strands next to each other, thus reducing the number of layers and therefore further reducing losses.

This principle was taken to the extreme in a transformer design with a 105 x 0.05 mm (0.21 mm²) litz wire. However, it was not taken into account that the surface area for heat dissipation is greatly reduced with such a thin litz wire, so that without a fan this winding would quickly overheat.

At this point, there would also be a need for a project that only focuses on optimizing the winding.

The transformer and its windings are measured using impedance analysis. The frequency-dependent resistance can be read directly from this.

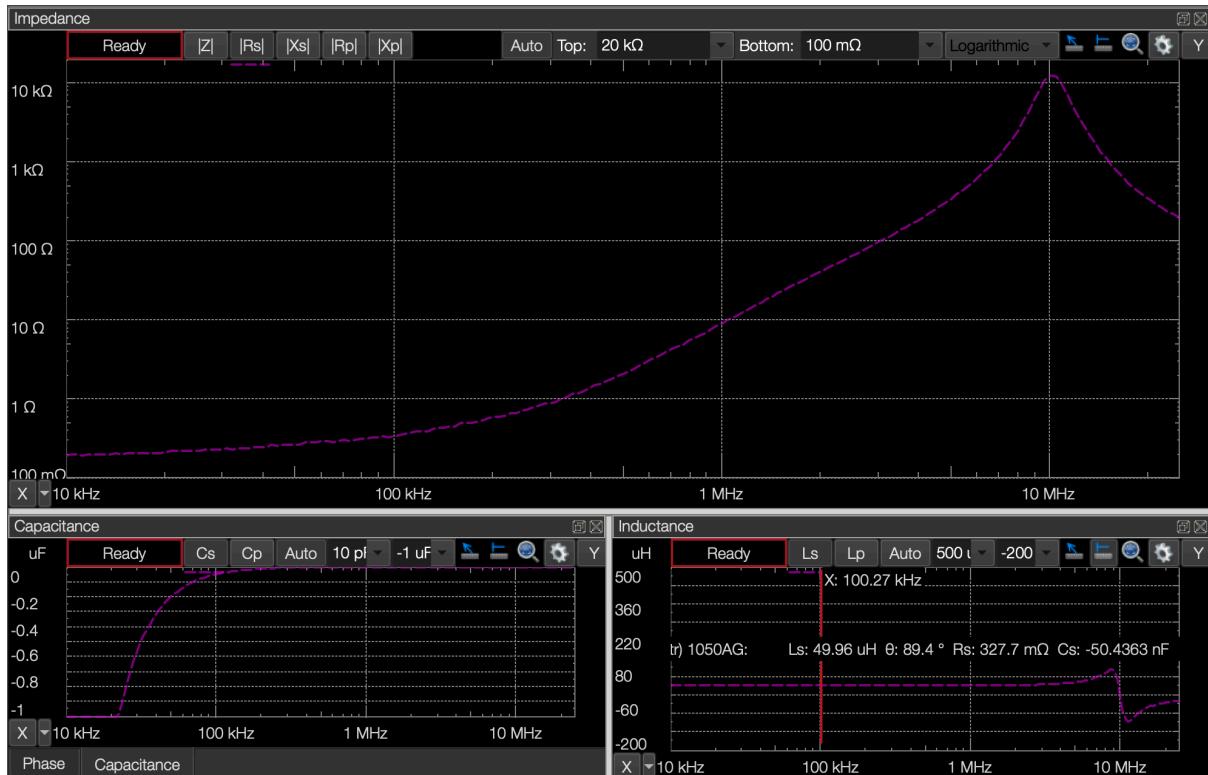


Fig. 41: Frequency-dependent resistance of the primary winding with short-circuited secondary winding, measured with Analog Discovery 2 and Impedance Analyzer extension.

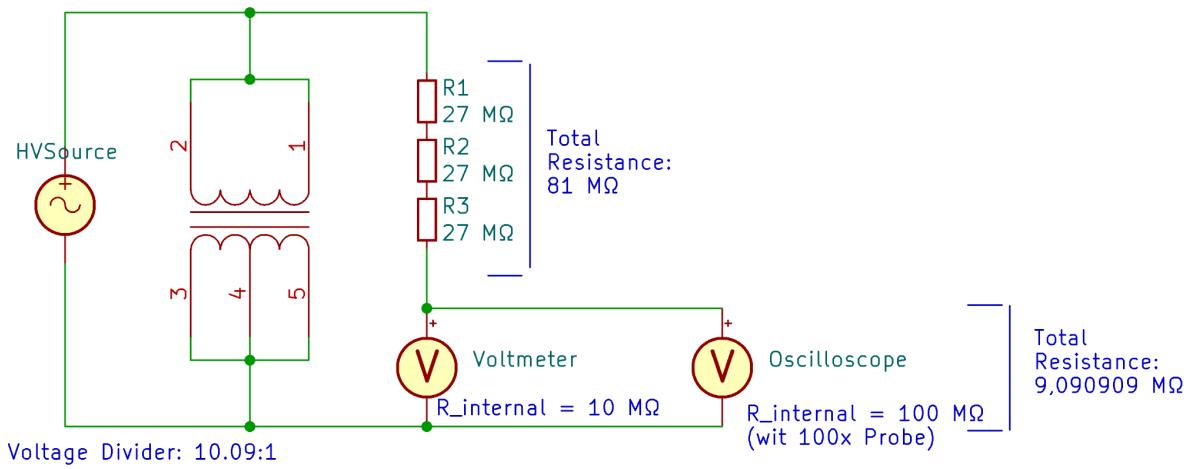
When analyzing the impedance, make sure that the core halves are pressed together with a clamp (no screw clamps due to brittle ferrite and magnetic field). Only one secondary winding must be short-circuited for the short-circuit measurement.

In addition to the resistance, the current is a key factor for the power loss. With a half-bridge topology, the current is twice as high as with a full-bridge topology, as the voltage swing is only half as large for the same power. However, the implementation would require significantly more space and complexity on the circuit board, which is why only a half-bridge is used in this project.

6.3.13 Isolation test

The Formula Student rules stipulate an isolation voltage of three times the maximum battery voltage as an AC RMS value for one minute. In this case, the battery voltage has a maximum of 600 V, so the isolation voltage must be at least 1800 V AC RMS. Although the rules do not specify a test frequency, 50 Hz is common.

Test Setup for Isolation Test (with Oscilloscope)



$$U_{Measured} = U_{in} \cdot \frac{9.090909 \text{ M}\Omega}{81 \text{ M}\Omega + 9.090909 \text{ M}\Omega}$$

$$U_{in} = U_{Measured} \cdot \frac{81 \text{ M}\Omega + 9.090909 \text{ M}\Omega}{9.090909 \text{ M}\Omega}$$

Fig. 42: Circuit of the measuring setup

The breakdown detection was recorded both with an oscilloscope by triggering on short voltage dips and acoustically or by electromagnetic interference on the microphone for the video recording. In addition to the isolation test, a further recording was made to verify the functionality of the measuring equipment used. The video recordings serve as proof that the isolation test was passed and can be found in the [Scrutineering Support presentation](#).

6.3.14 Y-Cap

The Y capacitor is used to dissipate capacitively transmitted currents, which are mainly caused by parasitic capacitances of the transformer, as it is switched between the HV supply voltage and 0 V at the half bridge. A Y-cap between the grounds of the otherwise isolated HV and LV sides allows the unintentionally transmitted currents to flow back.



Fig. 43: Voltage between GND of HV and LV side without Y capacitor



Fig. 44: Voltage between GND of HV and LV side with 3.3 nF Y capacitor

Together with the parasitic capacitance of the transformer, the Y-cap forms a capacitive voltage divider whose center tap is on the LV ground. Increasing the Y-cap reduces the voltage between the grounds. In the oscilloscopes above, the voltage could be reduced from 25 Vpp to 0.5 Vpp. The voltage level depends on the input voltage and the size of the winding capacitance between the primary and secondary/tertiary windings, but is hardly dependent on the load or frequency. Values for the Y-cap between 1 and 4.7 nF can be used without problems. Operation without a Y-cap is technically possible, but the GND

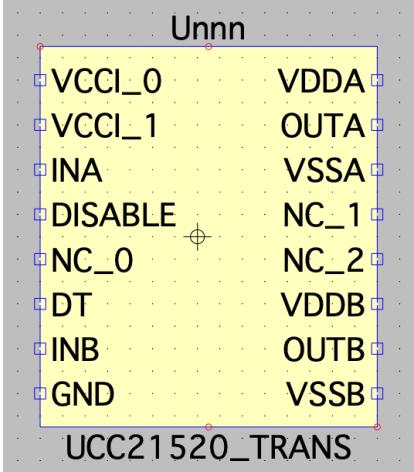
potential is shifted by the transmitted currents, so that LV consumers no longer have a zero potential in relation to the HV GND and are exposed to constant galvanic/capacitive coupled interference. However, Y capacitors can also couple interference from the HV system into the LV system, so they should not be too large.

Y capacitors must **always** be designed as safety capacitors, as they become highly resistive in the event of a fault. Normal capacitors can become permanently conductive in the event of a fault and would render the galvanic isolation ineffective.

6.4 Simulation

Simulation: [ltspice/DCDCv9-3.asc](#)

With the parameters obtained from the previous sections, a complete circuit structure was implemented in LTspice. The files used for the UCC25600, UCC21520 and TL431 must unfortunately be obtained from the sources themselves, as they cannot be included for license reasons.

Modell	URL
UCC25600 (and others)	https://web.archive.org/web/20220309044647/http://valvol.xyz/soft/ValVol.zip
TL431 (standard model) <i>The following files are displayed as plain text and must be saved as a file with the corresponding extension.</i> TL431.sub - Place in \lib\sub TL431.asy - Place in \lib\sym\Voltage Regulators	https://web.archive.org/web/20200805015613/http://ltwiki.org/images/e/e4/TL431.sub https://web.archive.org/web/20240224235540/https://ltwiki.org/images/f/fb/TL431.asy
UCC21520 1.) Download unencrypted PSpice model 2.) Open file with LTSPice 3.) Find the place that begins with the blue text ".SUBCKT". 4.) The "+" in the red line below must be removed and the following text moved to the previous (blue) line. 5.) Select the entire blue text, then right-click → Create symbol. The new symbol must have 16 connections (3 of them with NC) 6.) Arrange the pins according to the data sheet or your own requirements. 7.) Save the symbol in \lib\sym Save the model (.lib) in \lib\sub	https://www.ti.com/de/lit/zip/slum543 

After inserting the models into the local LTSPice library, the circuit of the LLC converter can be opened.

With the following settings, a good simulation speed with sufficient accuracy could be achieved.

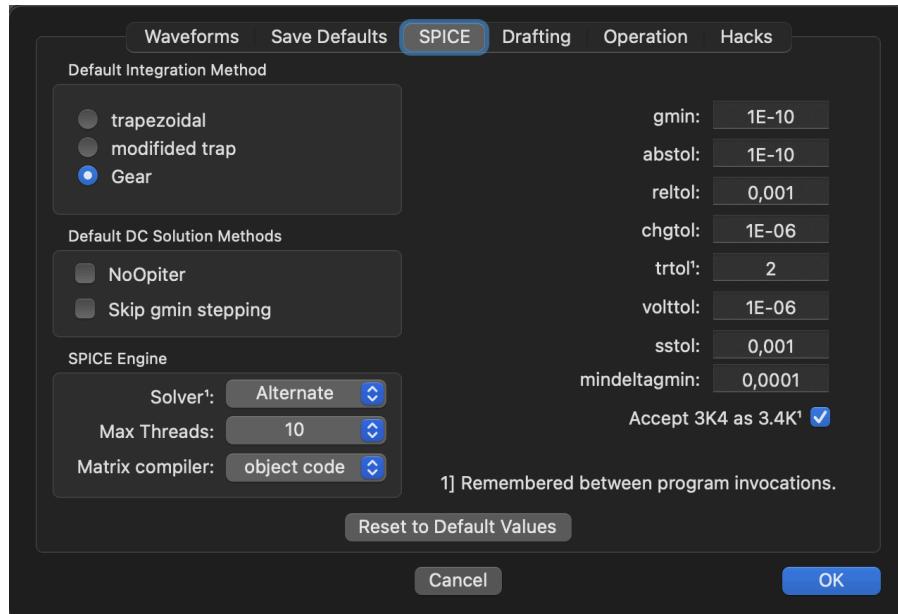


Fig. 45: Spice settings in LTSpice

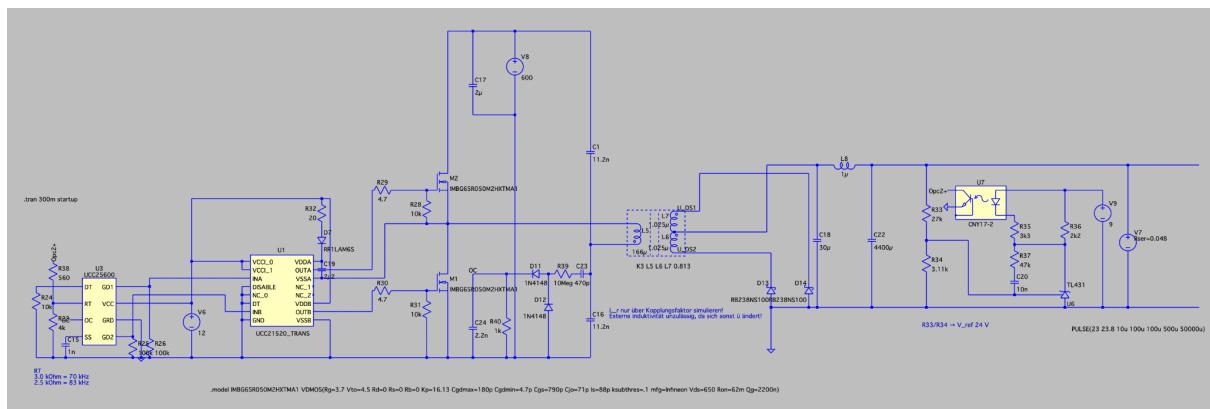


Fig. 46: Overall structure of the simulation

Notes on the simulation:

- The load is set to a power of approx. 500 W via a voltage source (bidirectional). The voltage source is also used at the beginning to pre-charge the output capacitors, which speeds up the simulation until settling.
 - The soft-start capacitor is smaller than it actually is in order to speed up the simulation until settling.
 - The resistor for the overcurrent setting (R40) is smaller in the simulation than it actually is in order to achieve a similar response behavior.
 - All components are subject to model-related deviations. In case of doubt, real measured values are preferable.

7 Calculations

(Incomplete)

Bootstrap resistor

Diode used: VS-E7FX0212-M3

V_DD = 12 V

V_Diode = 1,6 V @ 2 A

$$R_{boot} = \frac{12V - U_{diode}}{I_{diode}} = \frac{12V - 1.6V}{2A} = 5.2\Omega$$

R_Boot should be at least 5.2 Ω. 20Ω was selected for safety. The diode current is therefore 520 mA.

$$I_{boot} = \frac{12V - U_{diode}}{R_{boot}} = \frac{12V - 1.6V}{20\Omega} = 0.52A$$

When selecting the diode resistance, it should be noted that a higher value slows down the charging process and can lead to a significant voltage drop at high switching frequencies.

MOSFET Schaltverluste

$$P_{gate} = 2 \cdot V_{DD} \cdot Q_G \cdot f_{sw}$$

$$Q_{IMBG65R050} = 22nC$$

$$P_{gate} = 2 \cdot 12V \cdot 22nC \cdot 140kHz = 73,9mW$$

8 Discussion of the measurement methods

- The output voltage is measured before the fuse between the measuring point 24V_TP and GND, as otherwise the voltage drop across the fuse would influence the measurement. In terms of CV control, it would otherwise be load-dependent and dependent on the selected fuse. If necessary, a correction factor can be used to calculate the output voltage/power including the fuse.
- The temperature is measured using a thermal imaging camera. Depending on the surface, measurement errors due to reflections or low emissivity cannot be ruled out. Such influences were not observed during the measurements, but the measurement of objects with a known room temperature was elevated by approx. 1 K to 4 K. For this reason, an additional reference measurement is taken after each series of measurements.
- Ideally, the temperatures are measured after thermal equilibrium has been reached. However, as the time required is between one minute (e.g. SR MOSFETS) and 10 minutes (transformer) depending on the component, the time between load change and temperature measurement is noted in order to achieve a certain comparability of the temperature measurements.
- For some temperature measurements, the converter was operated upside down in order to reach certain measuring points. In this case, some component temperatures

increase more due to the heat dissipation of the transformer, which has a stronger heat convection to the PCB on the underside of the PCB.

- The measuring devices used to measure efficiency are almost entirely TrueRMS measuring devices (except for the output voltage). However, since current and voltage are measured separately, a small measurement error could occur even with a predominantly DC voltage/current by recording the apparent power.
- The measuring devices were referenced against a calibrated SDM3065X in order to determine the statistical measurement error. For the current measurement at the output, the shunt was referenced against the UT61+, as it can be briefly loaded with up to 20 A and only has a deviation of approx. +/- 3 mA in the measuring range up to 10 A compared to the SDM3065X. The SDM3065X itself was used for the current measurement. The measurement error was assumed to be negligible.

Reference U_in	U_in
SDM3065X [V]	UT61+ [V]
0,996242	-0,03%
1,992525	-0,04%
4,00625	-0,03%
7,00766	-0,02%
10,01391	-0,03%
15,01586	-0,03%
20,01871	-0,02%
30,0098	-0,03%
40,0220	-0,03%
50,0123	0,00%

Reference I_in	[IS REFERENCE]
SDM3065X [A]	SDM3065X [A]
0,000001	0%
0,2083	0%
1,0084	0%
2,0109	0%
4,0116	0%
6,0116	0%
8,0138	0%
10,01	0%

Reference U_out	U_out
SDM3065X [V]	VC-330 [V]
0,996242	0,28%
1,992525	0,27%
4,00625	-0,16%
7,00766	0,03%
10,01391	0,06%
15,01586	0,03%
20,01871	0,06%
30,0098	-0,03%
40,0220	-0,05%
50,0123	-0,02%

Reference I_out	I_out	
UT139C mV	UT139C mA	
1,26	1.008	0,159%
2,53	2.007	-0,114%
6,35	5.011	0,012%
12,72	10.017	0,004%
19,10	15.033	-0,003%
25,27	19.887	0,001%

The total error of the efficiency in the value range used ($U_{out} \approx 24V$) with a low load at the output is 0.175%. With a high load at the output, the measurement error can even be below 0.07%. However, it can be assumed that these low measurement errors are not achieved in practice with dynamic loads, EMI and non-uniform voltages/currents. A professional measurement of the converter with suitable measuring equipment would therefore be a welcome thing. 😊

9 PCB design

Not so important for the release, incomplete.

After completing the circuit diagram and dimensioning the transformer, the circuit board is designed. As with the circuit diagram, the open source program KiCAD was used for this.

A particular difficulty when designing with high voltage is the necessary isolation distances. These can be calculated using the Calculator Tools. Distances between nets can be defined using custom design rules in the [DCDCv9-3.kicad_dru](#) file. These prevent the traces from coming too close to each other when they are laid out. However, the rules were only implemented for particularly large voltage differences, as otherwise several hundred rules would be necessary. They were chosen restrictively so that more errors occur during the DRC check than would actually be problematic. These errors must be checked manually and excluded afterwards.

Potential between two conductors	Necessary distance outside/inside layer	Used distance outside/inside layer	Fillet radius	Usage
≤ 100 V	0.050 / 0.1 mm	0.2 / 0.2 mm	0.5 mm	24 V and signals
≤ 150 V	0.400 / 0.2 mm	0.4 / 0.2 mm	1.0 mm	Secondary rectification
≤ 630 V	1.197 / 0.575 mm	1.2 / 0.6 mm	1.0 mm	HV input
everything to the outer edge	-	0.3 / 0.3 mm	-	-
HV to LV	4.0	4.5	-	Galvanic isolation

Unfortunately, it is not possible to define voltage levels so that KiCAD itself calculates the distances based on the voltage differences (feature request?).

9.1 Basic design rules

- Function before (optical) design
- Pay attention to power losses:
 - Select components and topology as efficiently as possible
 - Current-carrying tracks/planes as wide as possible to achieve low resistance
 - Pay attention to the physical structure of the PCB:
 - How many oz of copper are on which layer?
 - How thick are the prepreg and core materials?
 - Observe the parasitics (inductive/capacitive) of conductors/planes
 - Create good heat sinks for components that generate heat
- Find out which component values are important and add a certain safety margin
- Choose the cheapest product that meets these requirements, from an established manufacturer
- Do not cheap out on components that are important for safety, reliability, efficiency or performance.
- If in doubt, leave out do simulations.

- If the simulations are inaccurate or too time-consuming, try to measure it in real life.
But always remember: „Wer misst, misst Mist“. ("Who measures measures crap!")
- RTFM (exclamation mark)

9.2 PCB requirements (for best performance)

- 4-layer printed circuit board
- 1.6 mm (standard) thickness
- 2 OZ outer copper, min. 0.5 OZ inner copper (2 OZ for inner layers would be best, but are expensive, so inner layers are less used here for high currents)
- TG 130 or higher
- The matte back of the PCB mask offers the best emissivity
- Filled and covered vias would be best, but plugged vias have not caused any problems so far (also not with PCBA)
- Vias size used: 0.4 mm hole diameter, 0.8 mm ring
- HASL lead-free or leaded? Both work well, but for the EU it is better to use the lead-free one.

9.3 KiCAD Notes

- If the “Fabrication Toolkit” plugin is used, the PCB must be updated from the circuit diagram to generate an up-to-date parts list.
- Special characters such as “ μ ” and “ Ω ” are not supported by JLC's BOM reader. This must be taken into account, otherwise no matching components will be found.

10 Measurement data analysis

Not so important → Later

10.1 Thermische Analyse

Use thermal images to show what gets warm where and how. Not so important → Later
(Alternatively, see data sheet and measurement tables Temps)

11 Conclusion

The converter has achieved what was originally required: a powerful, (so far) reliable and cost-effective low-voltage source. The small size, which became possible in the course of development, required a high level of efficiency due to the limited heat dissipation. For the author personally, this was a goal worth striving for, especially in times of energy saving. Unfortunately, size also has its downsides. For example, small changes to the circuit diagram sometimes lead to time-consuming layout shifts, which result in new distance checks for isolation. Some features, such as reverse polarity protection, could not be implemented due to space constraints. Although the idea of using only the circuit board as a heat sink reduces costs and complexity during assembly, it does have its performance limits. Although it was possible to design closer to the limits of the component specifications in the course of development, it cannot be denied that some components have to operate with a lower safety factor (thermal) for reasons of space.

On the other hand, there has been a great increase in knowledge in the field of power electronics, transformer design and circuit board layout. Particularly noteworthy in these areas are the findings on reducing switching and conduction losses, optimizing proximity losses and conductor design and minimizing parasitic conductor properties.

The result of this time-consuming and cost-intensive development can definitely compete with modules available on the market in terms of efficiency, costs and features.

12 Lessons Learned

- Do idiot tests. For example, give the Enable switch to someone to play with the task of trying to destroy the DCDC (with HV connected to the input, of course). This was already difficult with the v8, but nobody has yet managed it with the v9.
- Test the limits until they are destroyed - don't just think what it can handle, but actually know it. New designs have not yet passed long-term tests and are often tested under rather optimal conditions. By pushing various parameters (input voltage, power, ambient temperature, etc.) to the limit, worst-case conditions can be created and the limits of reliability determined.
- Measuring with measuring tips during operation. No. Simply no. I know it's damn tempting to quickly measure something somewhere on the circuit board during operation with a measuring tip. The risk of slipping, short-circuiting something or potentially harming yourself is extremely high. Here's my tip: Solder a few nice cables to the measuring point. This not only allows you to measure without contact difficulties, but also over a long period of time without having to use your hands. Measuring with Ground-Spring also works without hands: there are soldering aids with flexible arms that adhere magnetically to a plate. The clamps on the arms are also suitable for holding ground springs.
- Isolate clamps and cables! Everything that can somehow make contact should be covered with tape, even if only with masking tape. Anything is better than two cables touching each other unintentionally.
- **OTP and EMI → OVP input close to triggering at higher temps, and common mode interference (OPV ceramic capacitors), not so important → Later**
- **Output EMI → ceramic capacitors, not so important → Later**
- **Gate transformer**

13 Facts & Funnys

Here are some interesting facts and *things that happened.*

- Due to uncertainties from the regulations, the transformer of the v9-1 (48 V) was completely redesigned about two weeks before a Formula Student event in order to make it fire-resistant using FDM printing (Edit: According to the new interpretation, the components on the DCDC do not have to be fire-resistant). As the coils had to be arranged on top of each other to achieve the necessary isolation distance, the leakage inductance was reduced from approx. 40 μH to just 9 μH . This was not a problem in purely mathematical terms, as the increased resonant frequency could be compensated by using a larger resonant capacitor. During the final tests before installation in the vehicle, a primary-side inrush current of up to 34 A at 600 V was measured for approx. 700 μs . However, as the half-bridge FETs were specified for up to 99 A peak current, this measured value was classified as high but not critical. After around 3 months of use in the vehicle, with an estimated 100 power-cycles, the internal rectifier FET failed. As this had previously failed due to a short circuit at the LV output, the question arose as to whether there might be a systematic problem. As it is difficult to measure the current via the rectifier FETs, the current was roughly determined via the voltage rise of the output capacitors with known capacitance. The capacitors with 2350 μF were charged to 25 V in just under 600 μs , which resulted in a calculated peak charging current of approx. 500 A. The rectifier FETs were specified with a peak current of 488 A. This probably led to gradual destruction.

The solution to this problem was to increase the leakage inductance of the transformer. As the capacitors act like a short circuit at the moment of power-up, there is no magnetizing inductance on the primary side. Accordingly, the inrush current is only limited by the leakage inductance. However, it is important to note that the inrush current became even greater when the value was increased to 21 μH . Only in a test with 66 μH the current dropped to 16 A (peak primary). The suspected theory behind this lies in the resonant circuit: there is no magnetizing inductance at the switch-on moment, so there is only an LC resonant circuit instead of an LLC. The resonant frequency of this was approx. 206.5 kHz, while the switch-on frequency was 204 kHz. *Tacoma Bridge sends its greetings.*

At 66 μH , the resonant frequency was 119 kHz, far enough away from the switch-on frequency.

This finding is extremely important for future designs of LLC converters. Other options for limiting the inrush current (higher inrush frequency, PWM control) were investigated experimentally. Satisfactory results could be achieved with the UCC25600 although it does not have direct PWM control* and the maximum switching frequency is 350 kHz**. (See [Control IC UCC25600](#))

- *The dead time can be increased up to approx. 200 $\text{k}\Omega$ so that it acts like a PWM control. Values above this are problematic, as the switching frequency is halved abruptly.
- **The switching frequency can be more than doubled by overvoltage on the SS pin of the UCC25600 to approx. 9 V. In practice, however, this undocumented mode is not usable, as the current in the pin can exceed 100 mA and the IC heats up unacceptably.
- The v5 still had proper reverse polarity protection. However, all successors no longer did (only the intrinsic body diodes). Since the space requirement and (depending on

the implementation) loss of power could not be combined with the goals and the installation was not intended for technical laymen anyway, it was omitted. Both the v8 and the v9-1 were connected with reversed polarity due to a series of errors. In both cases, the HV fuse tripped via the body diode. In the v8, the precharge IGBT was also destroyed, but worked again after it was replaced. In the v9-1, the low-side FET was permanently conductive, but even after replacing it, no problems occurred in this context in the following months. For the release of the v9-3, consideration was given to implementing a simple reverse polarity protection by using a diode in the forward direction, as the benefit in the event of a fault outweighed the loss of efficiency. However, there was no diode that would have been small enough with the necessary characteristics.

14 Improvements

Version 9-3r is the first version to be approved for release. This means that it has been sufficiently tested and meets the requirements. However, there may still be improvements that have not been considered further. Below is a list (incomplete) of which components can still be improved and for what reason.

General: Some components are oversized for their task and are not cost-efficient.

Reference designator	Improvement
TH2	Higher resistance for better SNR or better EMI immunity at OPV and less power consumption
C46	smaller capacitance for better bypass effect? Long Vcc traces must be taken into account. UCC21520 data sheet: <i>"A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 50-V MLCC with over 100 nF is recommended for this application."</i>
C40, C41	Smaller capacitance for better bypass effect and startup behavior (time and bootstrap diode load), but must remain at 0805 footprint by design.
UVP/OPV	It may be possible to perform both measurements with a single high voltage divider by changing the reference voltage for each operational amplifier. This will free up some space (R71 and R1 are large 2512 for HV reasons). However, implementing hysteresis might be difficult. OVP is a nice-to-have anyway, which may not be needed at all with the given max f_sw.
U13	Optimizing with voltage dividers? Less precise? But may need buffer capacitor (new problems :/)
T1	Mechanical fastening currently only through cable terminals. Perhaps HF PCB transformer in the future? The losses in IDLE operation are relatively high. It is assumed that the small M-ratio ensures a high current flow. Cores with distributed air-gap could be used to reduce power loss due to stray fields: B66363Q0100K187 or B66363Q0150K187

U11 / UCC21520DW	Use a modern gate driver with separate source/sink pins, if necessary switch to 5 V or 3.3 V architecture.
R56/R58	Higher optimum values for ringing/switching losses possible, fast turn-off diode (never used in previous versions, DNP), possibly gate driver with separate source/sink pins.
R30 / R40	Pulldowns may not be necessary.
C25, C31	Smaller capacity for better bypass effect and startup behavior?
R32/R42	More optimal values for ringing/switching losses possible
U3 / MP4541	Step-down causes a lot of EMI, efficiency at best 78 % (24 V), approx. 1 mA in idle mode. Real switching behavior is strange. Looking for better options? Also has no real CC, which would be useful for charging the start cap.
U4 / TLV61048DBVR	Undervoltage cut-off does not work optimally, start cap is discharged below 2.5 V over many hours. Possibly also via D9 without the influence of U4.
C_start1	Supercap is a lithium hybrid. Advantage: High energy density, disadvantage: UVP required. Normal supercaps can be discharged to 0 V, but may not hold a charge as well.
U6A/U6B	Feed Vcc from 9 V (U2)? Although this is more stable and possibly also less noisy (be careful with the control loop!), the input SNR is lower with 9 V instead of 12 V.
D2	Possibly unnecessary after the change from 470 nF to 22 nF
R46	Current limiting resistor for bootstrap. Reduced 240619 from 47 Ohm to 20 Ohm -> 0.6 A inrush. but not optimal. Value unique / non standard.
OCP	The UCC25600 has a capacitive overcurrent/overvoltage measurement. If the limit value is exceeded, the signals to the half-bridge are switched off. However, the soft start continues immediately after the value falls below the limit, so that unwanted oscillation of the half-bridge in the single-digit Hz range can occur if the load for the overcurrent is still present.
Control loop	For a better interpretation of C26, C29, R37 see section Control loop.

15 Further links and resources

Topic	Link
PCB Design	<ul style="list-style-type: none"> ➡ What Every PCB Designer Should Know - Return Current Path (with Errata) ➡ PCB Layout & Decoupling - Explained why it's so complicated (Part 1) ➡ What Every PCB Designer Should Know - Crosstalk Explained (with Errata) ➡ What is The Best VIA Placement for Decoupling Capacitors?
LLC Converter Design (Infineon)	Resonant LLC Converter: Operation and Design
LLC Converter Design (Onsemi)	Design considerations for a Half-Bridge LLC resonant converter

DC/DC Knowledge	DC/DC BOOK OF KNOWLEDGE
AC/DC Knowledge	AC/DC BOOK OF KNOWLEDGE
TL431 Voltage Regulator	The TL431 in the Control of Switching Power Supplies
<i>optimal L_m/L_r (M)</i>	Why is an LLC converter's optimal L_m L_r ratio around 10? - Electrical Engineering Stack Exchange
Switching Losses (dmcinfo)	MOSFET Power Loss Calculator DMC, Inc.
Switching Losses (ROHM)	Calculation of Power Loss (Synchronous)
MLCC Capacitance Change vs Voltage	VCC: Capacitance Change vs Voltage in Ceramic Capacitors
Cracks in MLCCs (NASA)	Cracking Problems in Low-Voltage Chip Ceramic Capacitors
a lot about MLCC (effects you've might never heard of)	<ul style="list-style-type: none"> <input checked="" type="checkbox"/> PCIM 2019_Ceramic Capacitor Seminar_Part 1_1080 <input checked="" type="checkbox"/> PCIM 2019_Ceramic Capacitors Seminar_Part 2_1080 <input checked="" type="checkbox"/> PCIM 2019_Ceramic Capacitors Seminar_Part_3_1080
Proximity Losses and Dowell curves	Calculator of proximity effect from Dowell curves [Encyclopedia Magnetica™]
Winding Schemes	Investigation of Transformer Winding Architectures for High Voltage (2.5 kV) Capacitor Charging and Discharging Applications
LLC Converters (Bo Yang)	Chapter 4 LLC Resonant Converter (The other chapters can be easily found online)
Fringing Fields	Fringing effects
Ferrites (TDK)	Ferrites and accessories - General – Definitions

Thank you for reading! If you have any questions, criticism or ideas for improving the documentation, the author is happy to receive [feedback](#) :)