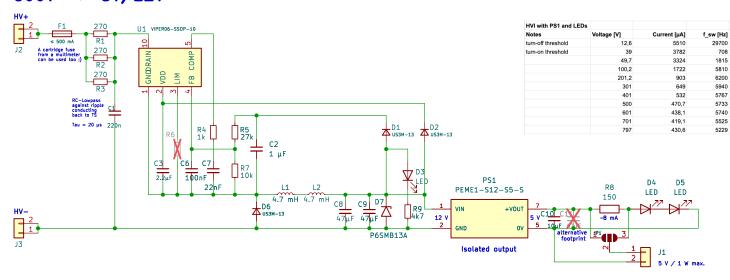
## **Buck converter using VIPER06** 800V -> 5V/12V



The HVI (High Voltage Indicator) is used to indicate voltages above 60 V for installation in the TSAC. The design shown here should comply with FS-Rules, but I'm only sure after it has passed FSG scrutineering:D Edit it bassed scruft.

Layout.

In deep uses the VIPERO6 as self-oscillating and self-regulating highlide-switch, which corresponds to the overall topology of a buck converter, the deep uses the design compact, the 60 V detection was smitted. This compiles with FS-holies, as the indicator light must light up at low rottages. In this case, this is already the case from approx. 40 V. Galvanic isolation can theoretically be dispensed when mounted with an isolating housing and viewing window. Galvanic isolation suseful in many cases, it was implemented by using a manual isolation BO/DC converter (3xV isolation rating). The back of the circuit board is designed so that the LEDs do not require touch protection, as no dangerous voitage is present (isolated by PCB). Alternatively, the circuit board can be placed anywhere in the TSAC and an LED can be attached to the housing with external view the circuit board can be placed anywhere in the TSAC and an LED can be attached to the housing with external view (1 W max.). If the included 1 W DC/DC is not used, approx. 3 W can be drawn directly (unisolated) at 12 V.

Important: Do not forget to isolate the board with Plastik70 after soldering (necessary due to isolation distances (EV 4.3.6 Table 5 Conformal Coating).

FS-Rules 2024 v1.1 / Source: https://www.formulastudent.de/fsq/rules/

Direct Connection – two devices or circuits are directly connected if the connection is not routed through any common PCB and does not include any devices or functionality other than overcurrent protection or connectors.

Galvanic Isolation — we stectic circuits are defined as galvanically isolated if all of the following conditions are true:

- The resistance between both Circuits is 500 CV/, related to the maximum TS voitage of the vehicle, at a test voitage of maximum TS voitage or 250 V, whichever is higher.

- The isolation test voitage RNS. AC for 1 min, between both circuits is higher than three times the maximum TS voitage or 750 V.

whichever is higher.

The working voltage of the isolation barrier, if specified in the datasheet, is higher than the maximum TS voltage.

Each TSAC must have a prominent indicator, a voltmeter, or a red LED visible even in bright sunlight that will illuminate whenever a voltage greater than 60 V DC or half the maximum TS voltage, whicheve is lower, is present at the vehicle side of the AIRs. EV 5.4.8

The indicator must be clearly visible while disconnecting the TSAC from the vehicles. The indicator must be clearly marked with "Voltage indicator"

EV 5.4.10

The indicator must be hard-wired electronics without software control, directly and only supplied by from the LVS or removed from the vehicle. the TS from the vehicle side of the AIRs, and always working, even if the accumulator is disconnected

If TS and LVS are on the same PCB, they must be on separate well-defined areas of the board, meeting the spacing requirements in table 5, each area clearly marked with "TS" or "LV". The outline of the area required for spacing must be marked. "Conformal coating," refers to a coating Insulator, solder resist is not a coating. Table 5: Spacing required between TS and LV  $\rightarrow$  300 V DC to 600 V DC: 4.0 mm with conformal coating. EV 4.3.6

EV 4.3.7 Teams must be prepared to demonstrate spacing on team-built equipment. For inaccessible circuitry, fully assembled spare boards must be available. Important note: The minimum switch—on time for most VIPER ICs is 400 ns.

If the Inductance (1.1+1.2) is too small, the current rise in these 400 ns will be too high and damage the IC.

L400ns = (U\_in \* 400 ns) / L

-> L400ns = 25.5 mA

The drain current limit for the VIPERO6 is 350 mA -> 9.4 mH is OK.

The VIPER06 IC comes in three different switching frequency versions: VIPER06Xx = 30 kHz VIPER06Lx = 60 kHz VIPER06Hx = 115 kHz

I recommend using the 30 kHz version, since it uses the fewest power and increases overall efficiency. This certain was hardly shiftable in this sale, but seem to be a to own (2029). The other versions can be used too, but may cause audible noise in burst mode. Burst operation also occurs with the 30 kHz version, depending on the load.

Note on capacitors:
Some values appear quite large, but bear in mind that the capacitance of MLCCs is strongly influenced by the applied voltage.
Depending on the manufacturer and series, the capacitance can drop by up to -90%. Check their resources!
(Google the part number of the MLCC manufacturer and go to their website. It often contains nice diagrams:)

Note on the 1150ec Seniution:

See "Dec 'Index' ne WPER11. Is used because I could not find a Viper06 model.

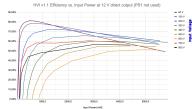
See "Dec 'Index' ne WPER11. Is used because I could not find a Viper06 model.

Important The freedback reference voitage (U.fs) for the VIPER06 is 3.3 V instead of 1.2 V (VIPER11). Adjust accordingly! Important The freedback reference voitage (U.fs) for the VIPER01 also viellocates a 1 second restart cycle on low input voitages not VIPER05 in VIPER06 is 1.5 v in VIPER06. The VIPER06 is 1.5 v in VIPER06 i

Set output Voltage:  $U_out = U_fb *(1 + R5 / R7) - U_D1_forward_voltage$ 



400 500



I'm unsure why 700 V and 800 V look so different from the others.

FAO:

263,3

293,8

343 2

708

1815

- Q: Why are 2x 4.7 mH inductors used instead of a 10 mH inductor? A: You will rarely find maximum voltage values for SMD inductors, so just an extra precaution.

- I need [Insert voilage herd], can I do blet?
  You can either change PSL (12V to 3.3 V to 24 V converters available)
  or (when used directly without PSL) the feedback voilage divider can be altered. I do not recommed going above 2.5 V because the ICs VDD voitage will be clamped, will use the internal high-voilage generator as IC's VDD supply (higher losses).
  So Ideality, stay between 12 V and 23 V.
- where do I get a cheap high voltage source for testing?
  I have been using one for 106 from amount for many years, which can generate up to
  800 V (when both 400 V rails are used) from a 8 to 32 V source (15 V delivers most power).
  If you want to support me, you can use my willfulled link where I get a amail commission
  in the docs there is an additional folder "IV Source" for a 30-printed case which also
  uses a rotany posteriometer instead of the trimp of the proportion of th
- I need more Power! A smaller inductor value could help, but be aware that the minimum on—time is 400 ns. At high input voltages this could lead to overcurrent when using small inductro values.
- Why is the text "Voltage Indicator", "Designed by XXX" and "HVI vX.X" not editable? I like to use a font (Futured) for visuals which is not pre-installed on most systems. Importing it as a logo is easier to retain it.
- This is open source. Can I modify It? Can I sell It?

  Surel But please use your own version numbering and change "Designed by Rootthecause"

  As this is licensed under CeRN ONL 22 Weekly Reciprocial, you must disclose the source, state changes and use the same license if used for non private projects.

  Learn more about this here: https://choosealicense.com/licenses/cern-onl-w-2.0/
- Q: I've got a question not listed here, can I contact you?
  A: Please use the issues form on GitHub for techical related questions.
- Q: Is there a way to support your projects?

|                    | Sheet: / File: HVI.kicad_sch |                             |      |    |
|--------------------|------------------------------|-----------------------------|------|----|
|                    | Title: HVI v1                | .1 Designed by Rootthecause |      |    |
|                    | Size: A4 Date: 2024-10-05    |                             | Rev: |    |
| KiCad E.D.A. 8.0.5 |                              | ld: 1/1                     |      |    |
|                    | - h                          |                             |      | _۲ |